SPANSION™ MCP

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50222-1E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

64M (×16) FLASH MEMORY & 8M (×16) SRAM

MB84SD23280FA/MB84SD23280FE-70

■ FEATURES

- **Power supply voltage of 1.65 V to 1.95 V**
- **High performance**
  70 ns maximum access time (Flash)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –30 °C to +85 °C
- **Package 73-ball FBGA**

(Continued)

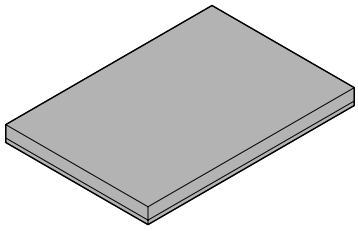
■ PRODUCT LINEUP

	Flash Memory	SRAM
Supply Voltage (V)	$V_{CC}f^*$ = 1.8 V $^{+0.15V}_{-0.15\ V}$	$V_{CC}s^*$ = 1.8 V $^{+0.15V}_{-0.15\ V}$
Max Address Access Time (ns)	70	70
Max $\overline{CE}$ Access Time (ns)	70	70
Max $\overline{OE}$ Access Time (ns)	20	35

*: Both $V_{CC}f$ and $V_{CC}s$ must be in recommended operation range when either part is being accessed.

■ PACKAGE

73-ball plastic FBGA



(BGA-73P-M03)

FUJITSU

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● **FLASH MEMORY**

- **0.17 µm process technology**
- **Simultaneous Read/Write operation (Dual Bank)**
- **FlexBank™ *1**
  Bank A: 16M bit (16KB × 4 and 64KB × 31)
  Bank B: 16M bit (64KB × 32)
  Bank C: 16M bit (64KB × 32)
  Bank D: 16M bit (16KB × 4 and 64KB × 31)
- **Minimum 100,000 program/erase cycles**
- **Sector Erase Architecture**
  Four 8K words, a hundred twenty-eight 32K words sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **$\overline{\text{WP}}$ Input Pin**
  At V_{IL}, allows protection of all sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of sector protection
- **Embedded Erase™ *2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Automatic sleep mode**
  When address remain stable, the device automatically switches itself to low power mode
- **Low V_{CC} write inhibit**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device resumes the erase operation
- **Sector Protection**
  Software command sector locking
- **Please Refer to “MBM29BS64LF” Datasheet in Detailed Function**

●**SRAM**

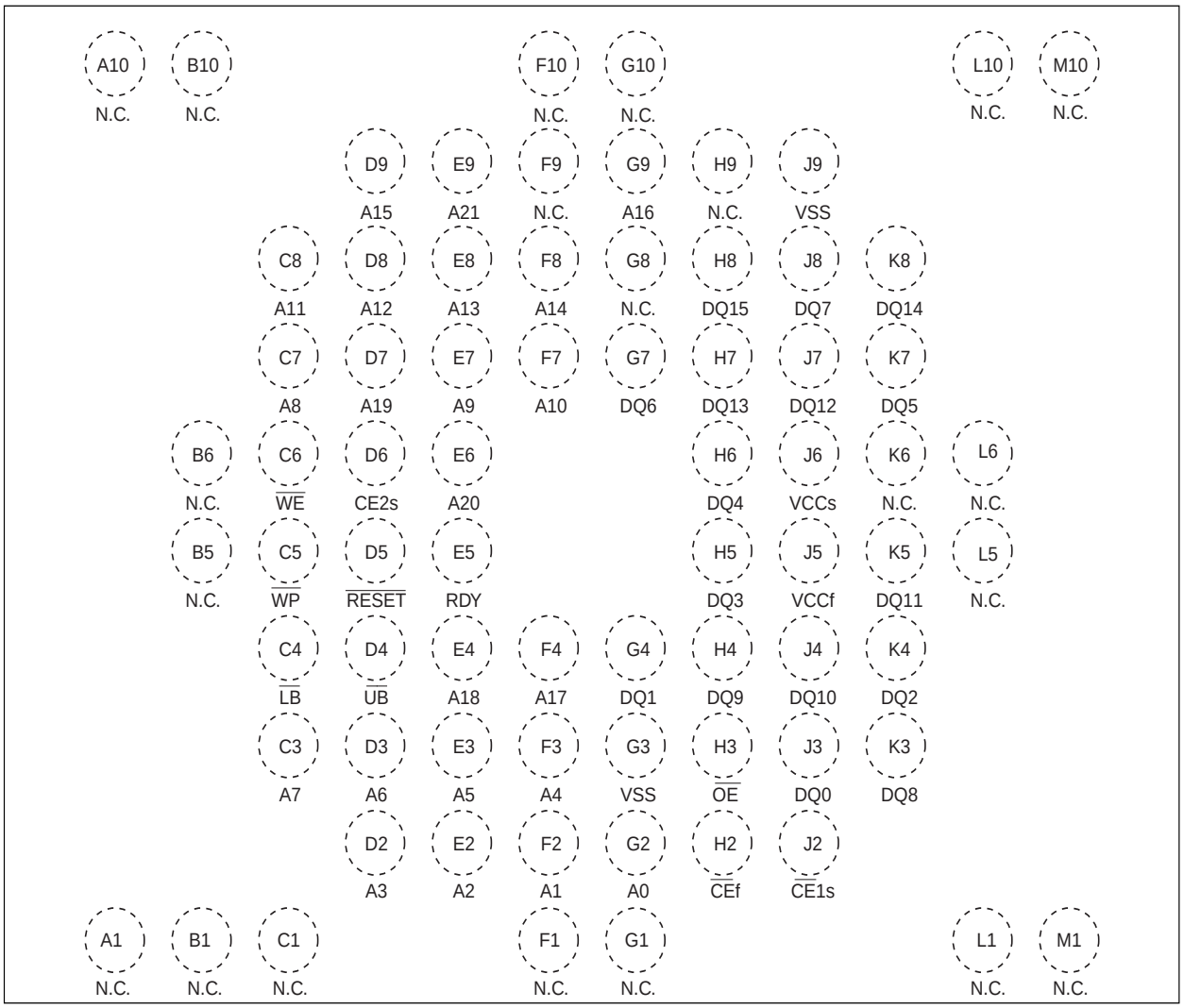
- **Power Dissipation**
  Operating : 50 mA Max
  Standby :15 µA Max
- **Power Down Features using $\overline{\text{CE}}$1s and CE2s**
- **Data Retention Supply Voltage: 1.0 V to 1.95 V**
- **$\overline{\text{CE}}$1s and CE2s Chip Select**
- **Byte Data Control: $\overline{\text{LB}}$ (DQ_7 to DQ_0), $\overline{\text{UB}}$ (DQ_{15} to DQ_8)**

*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENT

FBGA
(TOP VIEW)
Marking Side



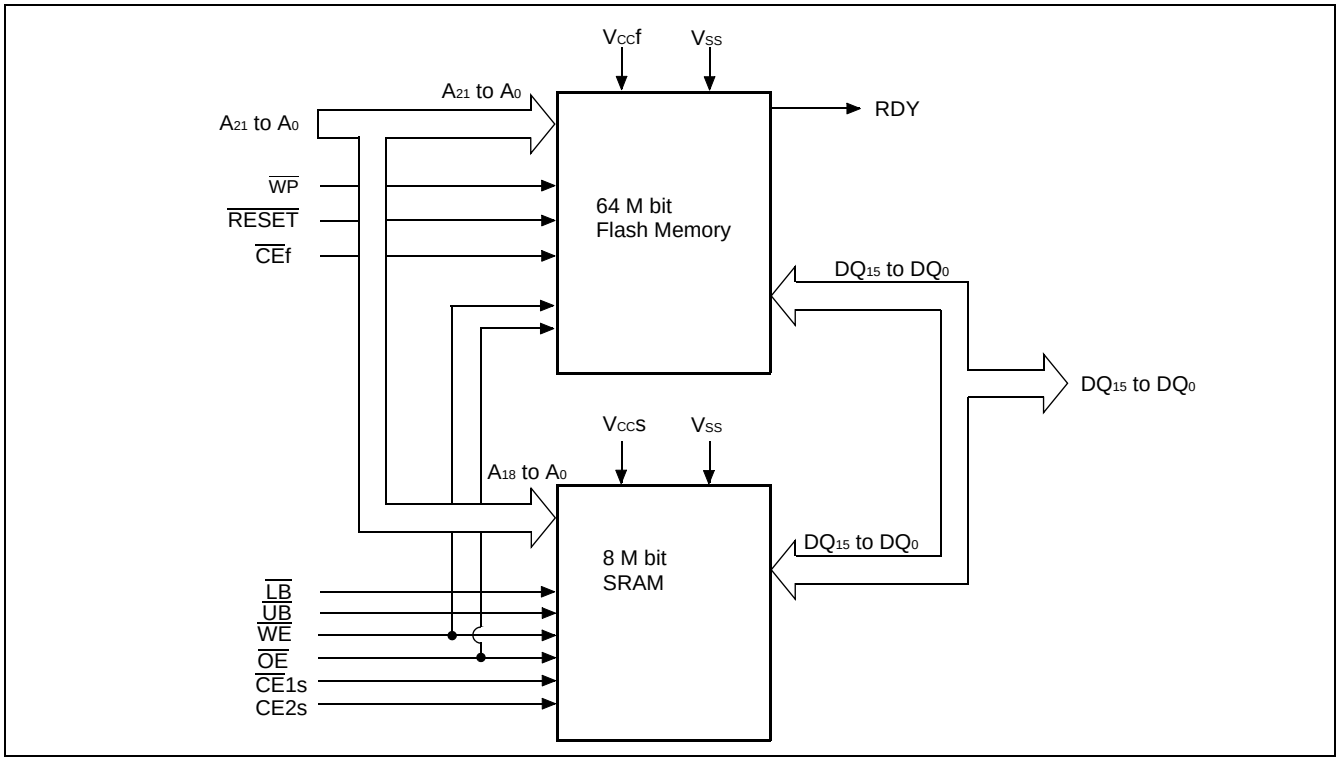
(BGA-73P-M03)

■ PIN DESCRIPTION

Pin Configuration

Pin Name	Function	Input/Output
A_{18} to A_0	Address Inputs (Common)	I
A_{21}, A_{20}, A_{19}	Address Inputs (Flash)	I
DQ_{15} to DQ_0	Data Inputs/Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE}$1s	Chip Enable (SRAM)	I
CE2s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RDY	Ready Outputs (Flash) Open Drain Output	O
$\overline{UB}$	Upper Byte Control (SRAM)	I
$\overline{LB}$	Lower Byte Control (SRAM)	I
$\overline{RESET}$	Hardware Reset Pin (Flash)	I
$\overline{WP}$	Write Protect (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (SRAM)	Power

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

User Bus Operations

Operation*1, *3	$\overline{CEf}$	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$*4
Full Standby	H	H	X	X	X	X	X	High-Z	High-Z	H	X
		X	L								
Output Disable	H	L	H	H	H	X	X	High-Z	High-Z	H	X
				X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	High-Z	High-Z		
		X	L								
Read from Flash*2	L	H	X	L	H	X	X	D_{OUT}	D_{OUT}	H	X
		X	L								
Write to Flash	L	H	X	H	L	X	X	D_{IN}	D_{IN}	H	H
		X	L								
Read from SRAM	H	L	H	L	H	L	L	D_{OUT}	D_{OUT}	H	X
						H	L	High-Z	D_{OUT}		
						L	H	D_{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	L	L	D_{IN}	D_{IN}	H	X
						H	L	High-Z	D_{IN}		
						L	H	D_{IN}	High-Z		
Flash All Sector Write Protection*4	X	X	X	X	X	X	X	X	X	H	L
Flash Hardware Reset	X	H	X	X	X	X	X	High-Z	High-Z	L	X
		X	L								

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See "■DC CHARACTERISTICS" for voltage levels.

*1: Other operations except for this indicated table are prohibited.

*2: Do not apply $\overline{CEf}$ = V_{IL}, $\overline{CE1s}$ = V_{IL} and CE2s = V_{IH} all at once.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: At $\overline{WP}$=V_{IL}, all sectors are protected.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–40	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins *	V_{IN}	–0.3	$V_{CC}f$ + 0.1	V
	V_{OUT}	–0.3	$V_{CC}s$ + 0.1	V
$V_{CC}f$ Supply *	$V_{CC}f$	–0.2	+2.5	V
$V_{CC}s$ Supply *	$V_{CC}s$	–0.5	+2.5	V

* : Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	–30	+85	°C
$V_{CC}f$ Supply Voltages	$V_{CC}f$	+1.65	+1.95	V
$V_{CC}s$ Supply Voltages	$V_{CC}s$	+1.65	+1.95	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ DC CHARACTERISTICS*1, *2

Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CCf}, V_{CCs}		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CCf}, V_{CCs}		–1.0	—	+1.0	µA
Flash V_{CC} Active Read Current *3	I_{CC1f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{WE}f$ = V_{IH}	5 MHz	—	12	16	mA
			1 MHz		3.3	5	
Flash V_{CC} Active Write Current *4	I_{CC2f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} = V_{IH}		—	15	40	mA
Flash V_{CC} Active Current (Read-While-Program)*5	I_{CC3f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	25	60	mA
Flash V_{CC} Active Current (Read-While-Erase)*5	I_{CC4f}	$\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	25	60	mA
SRAM V_{CC} Active Current	I_{CC1s}	V_{CCs} = V_{CCs} Max, $\overline{CE}1s$ = V_{IL}, CE2s = V_{IH}	t_{CYCLE} =10 MHz	—	—	50	mA
SRAM V_{CC} Active Current	I_{CC2s}	$\overline{CE}1s$ = 0.2 V, CE2s = V_{CCs} – 0.2 V	t_{CYCLE} = 10 MHz	—	—	50	mA
			t_{CYCLE} = 1 MHz	—	—	10	mA
Flash V_{CC} Standby Current	I_{SB1f}	V_{CCf} = V_{CCf} Max, $\overline{CE}f$ = $\overline{RESET}$ = V_{cc} ± 0.2 V, V_{IN} ≤ 0.2 V		—	0.2	10	µA
Flash V_{CC} Standby Current (Standby, $\overline{RESET}$) *6	I_{SB2f}	V_{CCf} = V_{CCf} Max, $\overline{RESET}$ = V_{IL}		—	0.2	10	µA
SRAM V_{CC} Standby Current	I_{SB1s}	$\overline{CE}1s$ ≥ V_{CCs} – 0.2 V, CE2s ≥ V_{CCs} – 0.2 V		—	—	14	µA
SRAM V_{CC} Standby Current	I_{SB2s}	CE2s ≤ 0.2 V		—	—	14	µA
Input Low Level	V_{IL}	—		–0.2	—	0.2	V
Input High Level	V_{IH}	—	Flash	V_{CCf}–0.2	—	V_{CCf}+0.2	V
			SRAM	1.6	—	V_{CCs}+0.2	
Flash Output Low Level	V_{OL}	Flash	V_{CCf} = V_{CCf} Min, I_{OL} = 1.0 mA	—	—	0.1	V
SRAM Output Low Level		SRAM	V_{CCs} = V_{CCs} Min, I_{OL} = 2.1 mA	—	—	0.4	V
Flash Output High Level	V_{OH}	Flash	V_{CCf} = V_{CCf} Min, I_{OH} = –0.1 mA	V_{CCf}–0.1	—	—	V
SRAM Output High Level		SRAM	V_{CCs} = V_{CCs} Min, I_{OH} = –0.5 mA	V_{CCs}–0.5	—	—	V
Flash Low V_{CC} Lock-Out Voltage	V_{LKO}	—		1.0	—	1.4	V

*1 : All voltage are referenced to V_{SS}.

*2 : I_{OUT} depends on the output load conditions.

*3 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*4 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*5 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

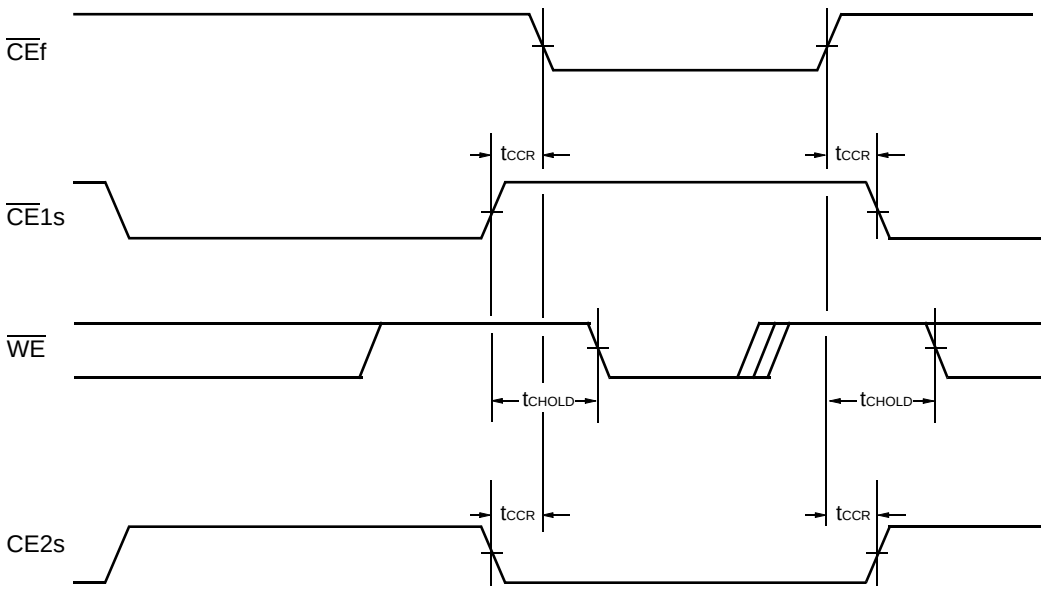
*6 : Automatic sleep mode enables the low power mode when address remain stable for t_{ACC} + 60 ns.

■ AC CHARACTERISTICS

• $\overline{CE}$ Timing

Parameter	Symbol		Condition	Value	Unit
	JEDEC	Standard		Min	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	—
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	—

• Timing Diagram for alternating SRAM to Flash



■ SECTOR LOCK/UNLOCK COMMAND

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don't care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A_6 whether that sector should be locked ($A_6 = V_{IL}$) or unlocked ($A_6 = V_{IH}$). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

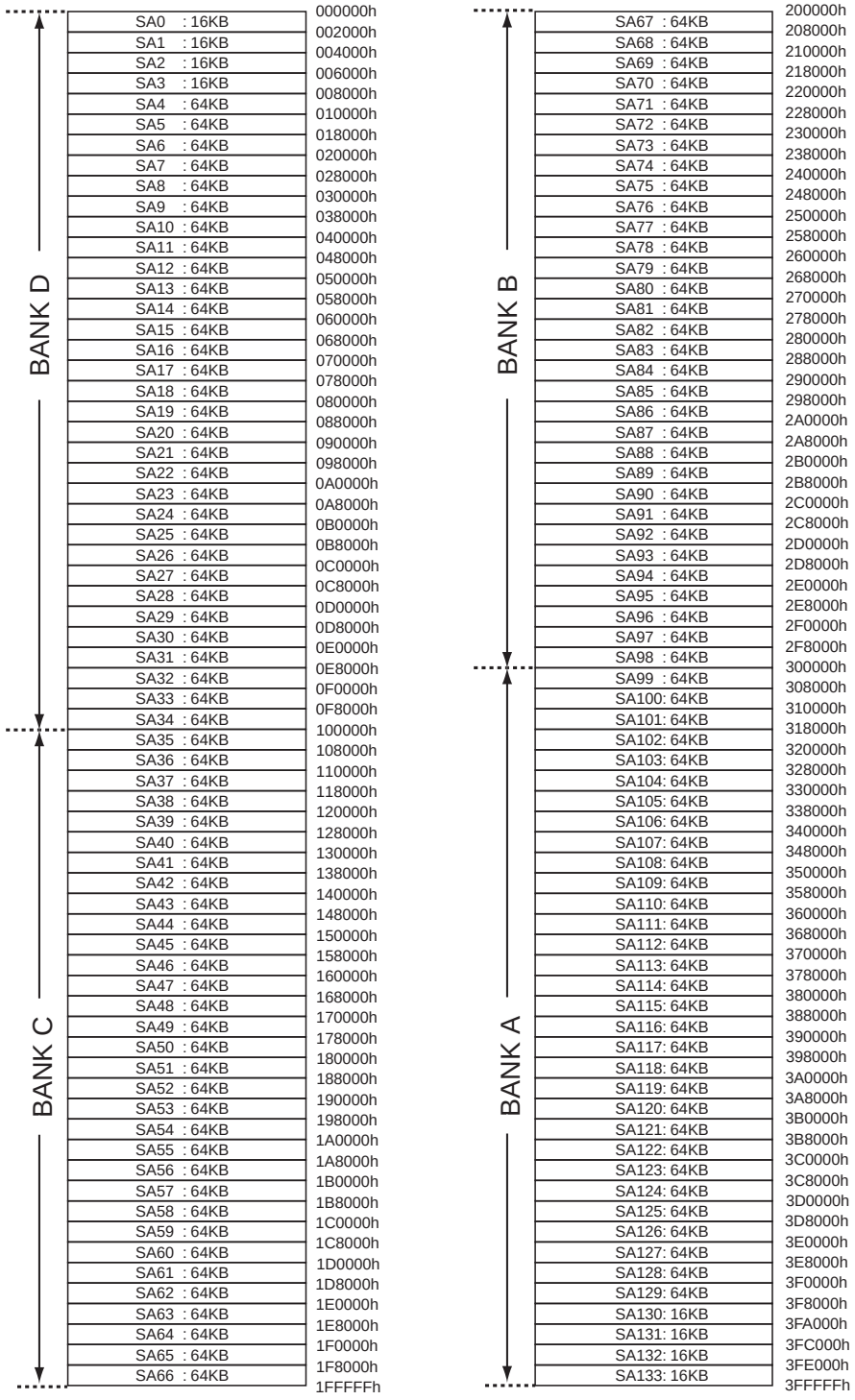
- **Flash Characteristics**
  Please refer to "■ 64M FLASH MEMORY for MCP 1.8 V".

- **SRAM Characteristics**
  Please refer to "■ 8M SRAM for MCP 1.8 V".

■ 64M FLASH MEMORY for MCP 1.8 V

1. Flexible Sector-erase Architecture on FLASH MEMORY

- Sixteen 4K words, and one hundred twenty-six 32K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



Sector Architecture

- **FlexBank™ Architecture**

Bank	Quantity	Size
A	4	8K words
	31	32K words
B	32	32K words
C	32	32K words
D	31	32K words
	4	8K words

- **Simultaneous Operation**

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

- **Sector Address Table**

Bank	Sector	Sector Size	(×16) Address Range
Bank D	SA0	8 Kwords	000000h to 001FFFh
	SA1	8 Kwords	002000h to 003FFFh
	SA2	8 Kwords	004000h to 005FFFh
	SA3	8 Kwords	006000h to 007FFFh
	SA4	32 Kwords	008000h to 00FFFFh
	SA5	32 Kwords	010000h to 017FFFh
	SA6	32 Kwords	018000h to 01FFFFh
	SA7	32 Kwords	020000h to 027FFFh
	SA8	32 Kwords	028000h to 02FFFFh
	SA9	32 Kwords	030000h to 037FFFh
	SA10	32 Kwords	038000h to 03FFFFh
	SA11	32 Kwords	040000h to 047FFFh
	SA12	32 Kwords	048000h to 04FFFFh
	SA13	32 Kwords	050000h to 057FFFh
	SA14	32 Kwords	058000h to 05FFFFh
	SA15	32 Kwords	060000h to 067FFFh
	SA16	32 Kwords	068000h to 06FFFFh
	SA17	32 Kwords	070000h to 077FFFh
	SA18	32 Kwords	078000h to 07FFFFh
	SA19	32 Kwords	080000h to 087FFFh
	SA20	32 Kwords	088000h to 08FFFFh
	SA21	32 Kwords	090000h to 097FFFh
	SA22	32 Kwords	098000h to 09FFFFh
	SA23	32 Kwords	0A0000h to 0A7FFFh
	SA24	32 Kwords	0A8000h to 0AFFFFh
	SA25	32 Kwords	0B0000h to 0B7FFFh
	SA26	32 Kwords	0B8000h to 0BFFFFh
	SA27	32 Kwords	0C0000h to 0C7FFFh
	SA28	32 Kwords	0C8000h to 0CFFFFh
	SA29	32 Kwords	0D0000h to 0D7FFFh
	SA30	32 Kwords	0D8000h to 0DFFFFh
	SA31	32 Kwords	0E0000h to 0E7FFFh
	SA32	32 Kwords	0E8000h to 0EFFFFh
	SA33	32 Kwords	0F0000h to 0F7FFFh
	SA34	32 Kwords	0F8000h to 0FFFFFh

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Bank	Sector	Sector Size	(×16) Address Range
Bank C	SA35	32 Kwords	100000h to 107FFFh
	SA36	32 Kwords	108000h to 10FFFFh
	SA37	32 Kwords	110000h to 117FFFh
	SA38	32 Kwords	118000h to 11FFFFh
	SA39	32 Kwords	120000h to 127FFFh
	SA40	32 Kwords	128000h to 12FFFFh
	SA41	32 Kwords	130000h to 137FFFh
	SA42	32 Kwords	138000h to 13FFFFh
	SA43	32 Kwords	140000h to 147FFFh
	SA44	32 Kwords	148000h to 14FFFFh
	SA45	32 Kwords	150000h to 157FFFh
	SA46	32 Kwords	158000h to 15FFFFh
	SA47	32 Kwords	160000h to 167FFFh
	SA48	32 Kwords	168000h to 16FFFFh
	SA49	32 Kwords	170000h to 177FFFh
	SA50	32 Kwords	178000h to 17FFFFh
	SA51	32 Kwords	180000h to 187FFFh
	SA52	32 Kwords	188000h to 18FFFFh
	SA53	32 Kwords	190000h to 197FFFh
	SA54	32 Kwords	198000h to 19FFFFh
	SA55	32 Kwords	1A0000h to 1A7FFFh
	SA56	32 Kwords	1A8000h to 1AFFFFh
	SA57	32 Kwords	1B0000h to 1B7FFFh
	SA58	32 Kwords	1B8000h to 1BFFFFh
	SA59	32 Kwords	1C0000h to 1C7FFFh
	SA60	32 Kwords	1C8000h to 1CFFFFh
	SA61	32 Kwords	1D0000h to 1D7FFFh
	SA62	32 Kwords	1D8000h to 1DFFFFh
	SA63	32 Kwords	1E0000h to 1E7FFFh
	SA64	32 Kwords	1E8000h to 1EFFFFh
	SA65	32 Kwords	1F0000h to 1F7FFFh
	SA66	32 Kwords	1F8000h to 1FFFFFh

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Bank	Sector	Sector Size	(×16) Address Range
Bank B	SA67	32 Kwords	200000h to 207FFFh
	SA68	32 Kwords	208000h to 20FFFFh
	SA69	32 Kwords	210000h to 217FFFh
	SA70	32 Kwords	218000h to 21FFFFh
	SA71	32 Kwords	220000h to 227FFFh
	SA72	32 Kwords	228000h to 22FFFFh
	SA73	32 Kwords	230000h to 237FFFh
	SA74	32 Kwords	238000h to 23FFFFh
	SA75	32 Kwords	240000h to 247FFFh
	SA76	32 Kwords	248000h to 24FFFFh
	SA77	32 Kwords	250000h to 257FFFh
	SA78	32 Kwords	258000h to 25FFFFh
	SA79	32 Kwords	260000h to 267FFFh
	SA80	32 Kwords	268000h to 26FFFFh
	SA81	32 Kwords	270000h to 277FFFh
	SA82	32 Kwords	278000h to 27FFFFh
	SA83	32 Kwords	280000h to 287FFFh
	SA84	32 Kwords	288000h to 28FFFFh
	SA85	32 Kwords	290000h to 297FFFh
	SA86	32 Kwords	298000h to 29FFFFh
	SA87	32 Kwords	2A0000h to 2A7FFFh
	SA88	32 Kwords	2A8000h to 2AFFFFh
	SA89	32 Kwords	2B0000h to 2B7FFFh
	SA90	32 Kwords	2B8000h to 2BFFFFh
	SA91	32 Kwords	2C0000h to 2C7FFFh
	SA92	32 Kwords	2C8000h to 2CFFFFh
	SA93	32 Kwords	2D0000h to 2D7FFFh
	SA94	32 Kwords	2D8000h to 2DFFFFh
	SA95	32 Kwords	2E0000h to 2E7FFFh
	SA96	32 Kwords	2E8000h to 2EFFFFh
	SA97	32 Kwords	2F0000h to 2F7FFFh
	SA98	32 Kwords	2F8000h to 2FFFFFh

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Bank	Sector	Sector Size	(×16) Address Range
Bank A	SA99	32 Kwords	300000h to 307FFFh
	SA100	32 Kwords	308000h to 30FFFFh
	SA101	32 Kwords	310000h to 317FFFh
	SA102	32 Kwords	318000h to 31FFFFh
	SA103	32 Kwords	320000h to 327FFFh
	SA104	32 Kwords	328000h to 32FFFFh
	SA105	32 Kwords	330000h to 337FFFh
	SA106	32 Kwords	338000h to 33FFFFh
	SA107	32 Kwords	340000h to 347FFFh
	SA108	32 Kwords	348000h to 34FFFFh
	SA109	32 Kwords	350000h to 357FFFh
	SA110	32 Kwords	358000h to 35FFFFh
	SA111	32 Kwords	360000h to 367FFFh
	SA112	32 Kwords	368000h to 36FFFFh
	SA113	32 Kwords	370000h to 377FFFh
	SA114	32 Kwords	378000h to 37FFFFh
	SA115	32 Kwords	380000h to 387FFFh
	SA116	32 Kwords	388000h to 38FFFFh
	SA117	32 Kwords	390000h to 397FFFh
	SA118	32 Kwords	398000h to 39FFFFh
	SA119	32 Kwords	3A0000h to 3A7FFFh
	SA120	32 Kwords	3A8000h to 3AFFFFh
	SA121	32 Kwords	3B0000h to 3B7FFFh
	SA122	32 Kwords	3B8000h to 3BFFFFh
	SA123	32 Kwords	3C0000h to 3C7FFFh
	SA124	32 Kwords	3C8000h to 3CFFFFh
	SA125	32 Kwords	3D0000h to 3D7FFFh
	SA126	32 Kwords	3D8000h to 3DFFFFh
	SA127	32 Kwords	3E0000h to 3E7FFFh
	SA128	32 Kwords	3E8000h to 3EFFFFh
	SA129	32 Kwords	3F0000h to 3F7FFFh
	SA130	8 Kwords	3F8000h to 3F9FFFh
	SA131	8 Kwords	3FA000h to 3FBFFFh
	SA132	8 Kwords	3FC000h to 3FDFFFh
	SA133	8 Kwords	3FE000h to 3FFFFFh

- **Sector Protection Verify Autoselect Codes Table**

Type	A_{21} to A_{13}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA*2	L	L	L	L	L	L	L	L	04h
Device Code	BA*2	L	L	L	L	L	L	L	H	227Eh
Extended Device Code*1	BA	L	L	L	L	H	H	H	L	2224h
	BA	L	L	L	L	H	H	H	H	2201h
Sector lock/ unlock	Sector Addresses	L	L	L	L	L	L	H	L	01h*2

Legend: L = V_{IL}, H = V_{IH}. See "■DC CHARACTERISTICS" for voltage levels.

*1: A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh

*2: Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

- **Flash Memory Command Definitions**

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Write Cycle		Third Write Cycle		Fourth Write Cycle		Fifth Write Cycle		Sixth Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—
Read / Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0	PA	PD								
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	F0h*2	—	—	—	—	—	—	—	—
Sector Lock/Unlock	3	XXXh	60h	XXXh	60h	SLA	60h	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—

Legend:

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, and A_{14} will uniquely select any sector.

BA = Bank Address. Address setted by A_{22}, A_{21} will select Bank A, Bank B, Bank C and Bank D.

SLA = Address of the sector to be locked. Set sector address (SA) and either A_6 = 1 for unlocked or A_6 = 0 for locked.

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data latches on the rising edge of write pulse.

CR = Configuration Register address bits A_{19} to A_{12}.

*1: This command is valid during Fast Mode.

*2: The data "00h" is also acceptable.

Notes:
- Address bits A_{21} to A_{11} = X = "H" or "L" for all address commands except for PA, SA, BA.
- Bus operations are defined in "■ DEVICE BUS OPERATION".
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

2. AC Characteristics

- **Read Operations**

Parameter		Symbol		Value		Unit
		JEDEC	Standard	Min	Max	
Access Time from $\overline{CE}$f Low		—	t_{CE}	—	70	ns
Access Time *1		—	t_{ACC}	—	70	ns
Output Enable to Output Valid		—	t_{OE}	—	20	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	ns
Output Enable to High-Z *2		—	t_{OEZ}	—	10	ns

*1 : Access Time is from the last of either stable addresses.

*2 : Not 100% tested.

- **Hardware Reset ($\overline{RESET}$)**

Parameter	Symbol		Value		Unit
	JEDEC	Standard	Min	Max	
$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read Mode*	—	t_{READY}	—	20	µs
$\overline{RESET}$ Pin Low (NOT During Embedded Algorithms) to Read Mode*	—	t_{READY}	—	500	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	ns
Reset High Time Before Read*	—	t_{RH}	200	—	ns
$\overline{RESET}$ Low to Standby Mode	—	t_{RPD}	20	—	µs

* : Not 100% tested.

- **Erase/Program Operations**

Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min	Typ	Max	
Write Cycle Time*1	t_{AVAV}	t_{WC}	80	—	—	ns
Address Setup Time*2	t_{AVWL}	t_{AS}	0	—	—	ns
Address Hold Time*2	t_{WLAX}	t_{AH}	45	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	45	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	ns
Read Recovery Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	ns
$\overline{CE}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	ns
Write Pulse Width	t_{EHWH}	t_{WP}	50	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	30	—	—	ns
Latency Between Read and Write Operations	—	$t_{SR/W}$	0	—	—	ns
Programming Operation*3	t_{WHWH1}	t_{WHWH1}	—	8	—	µs
Sector Erase Operation*3, *4	t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
Chip Erase Operation*3, *4			—	67.0	—	
V_{CC} Setup Time	—	t_{VCS}	50	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$	t_{ELWL}	t_{CS}	0	—	—	ns

*1 : Not 100% tested.

*2 : Addresses are latched on the falling edge of $\overline{WE}$.

*3 : See the “Erase and Programming Performance” section in “BDS64xF” datasheet for more information.

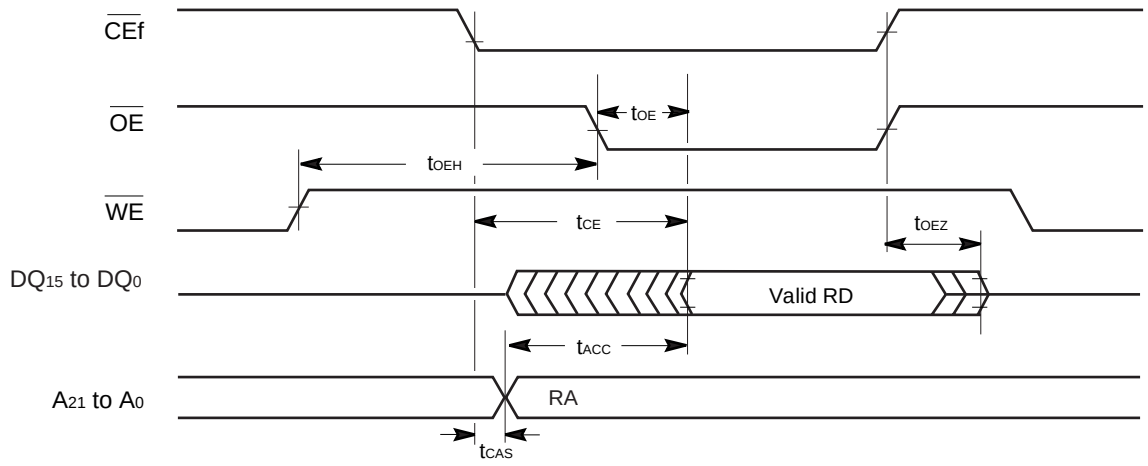
*4 : Does not include the preprogramming time.

3. Erase and Programming Performance

Parameter	Value			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2.0	s	Excludes programming prior to erasure
Word Programming Time	—	6	100	µs	Excludes system level overhead
Chip Programming Time	—	25.2	95	s	Excludes system level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

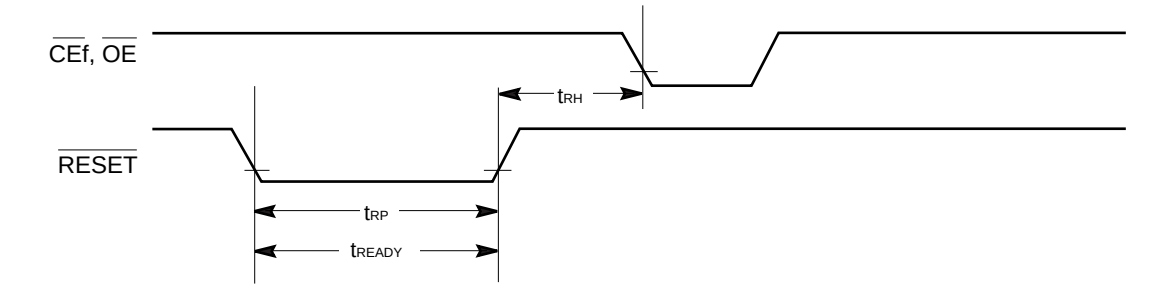
Note: Typical Erase Conditions: T_A = + 25°C, $V_{CC}f$ = 1.8 V
Typical Program Conditions: T_A = + 25°C, $V_{CC}f$ = 1.8 V, Data = checker

- **Read Mode**



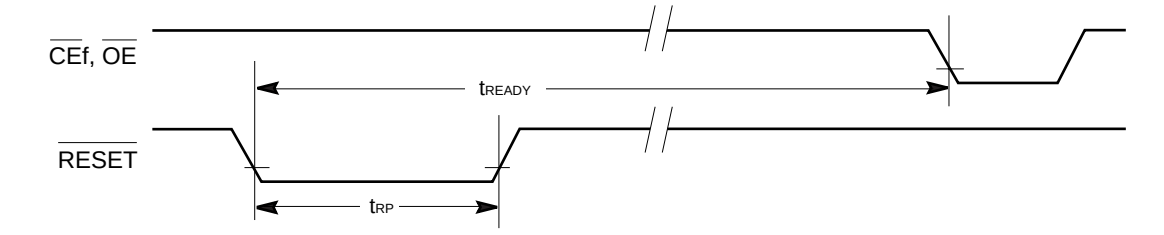
Note: RA = Read Address, RD = Read Data.

- **Reset Timings**

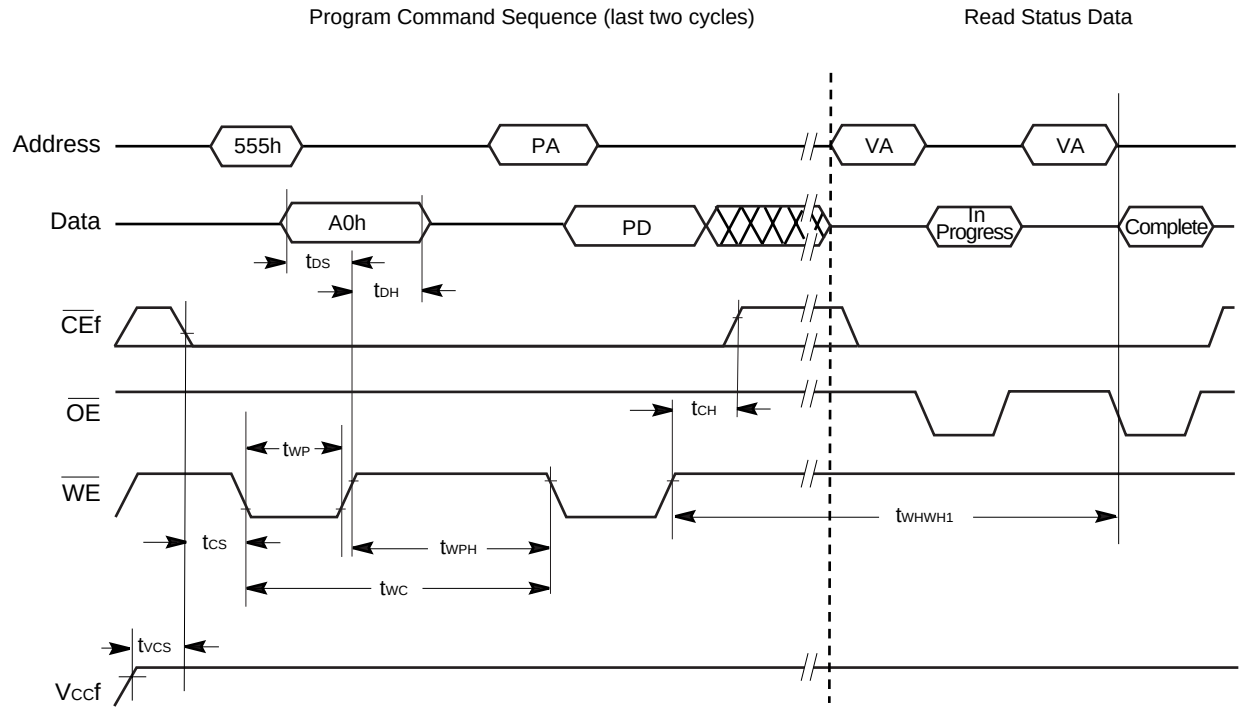


Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms

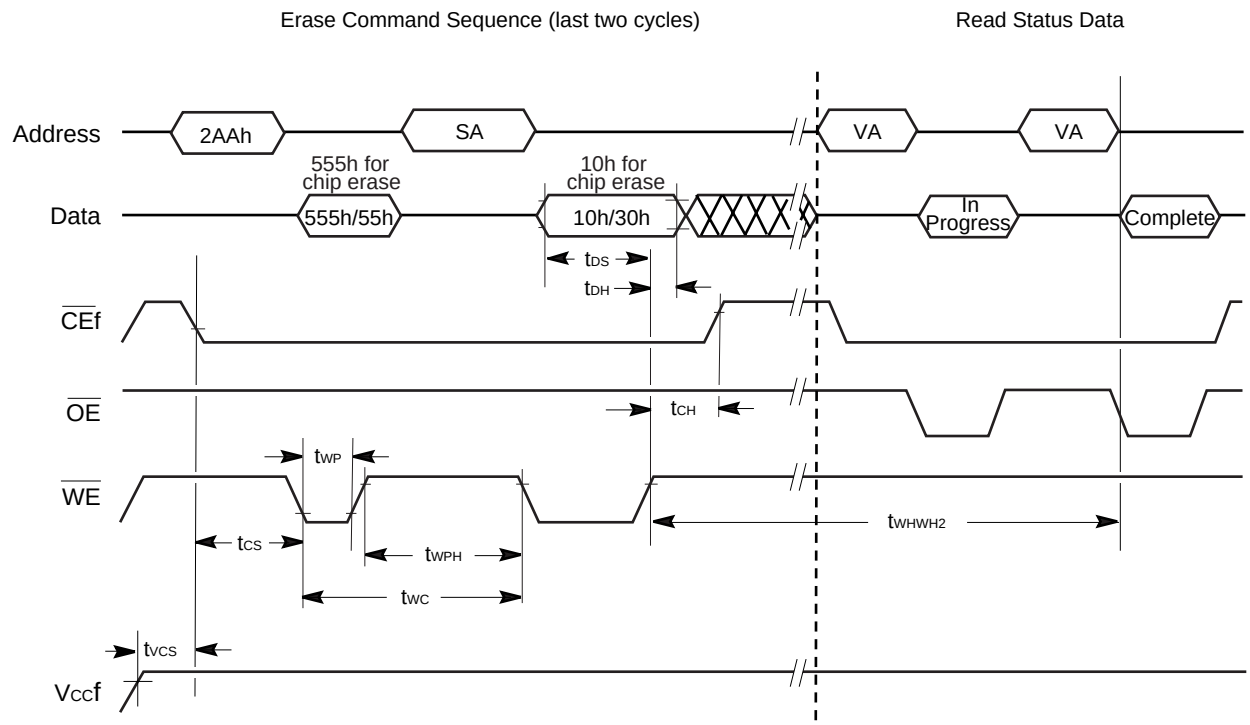


- **Program Operation Timings**



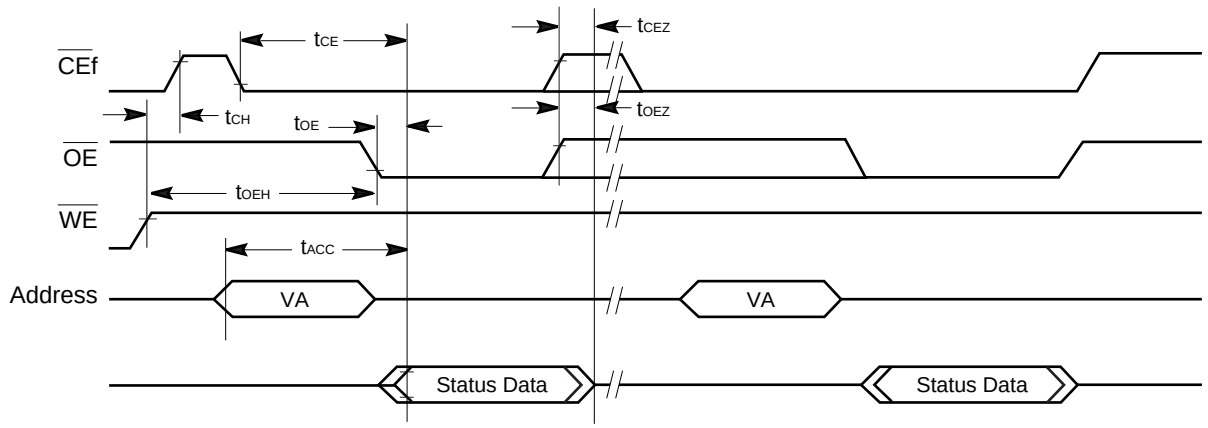
Notes :
- PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
- “In progress” and “complete” refer to status of program operation in “MBM29BS64LF” Data sheet.
- A_{21} to A_{12} are don’t care during command sequence unlock cycles.

- **Chip/Sector Erase Command Sequence**



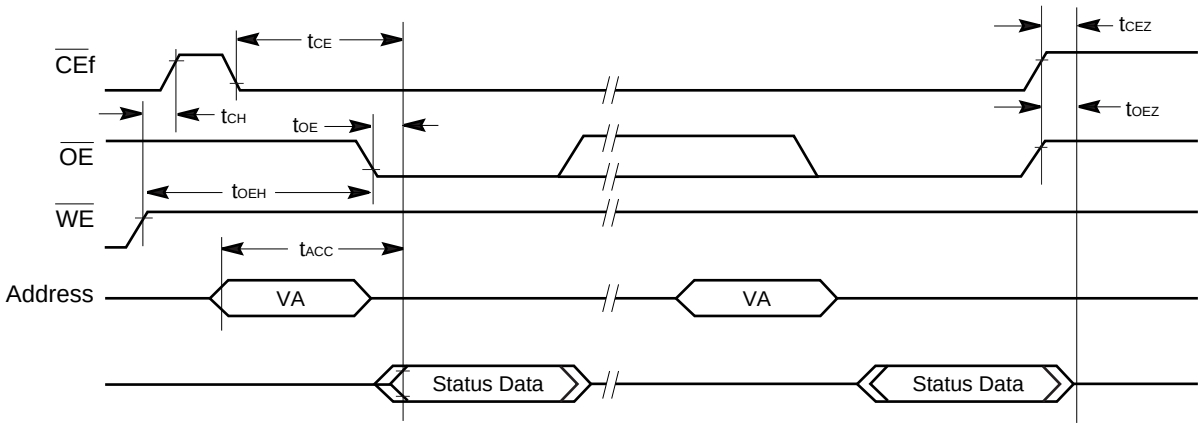
Notes : • SA is the sector address for Sector Erase.
• Address bits A_{21} to A_{12} are don't cares during unlock cycles in the command sequence.

- **$\overline{\text{Data}}$ Polling Timings (During Embedded Algorithm)**



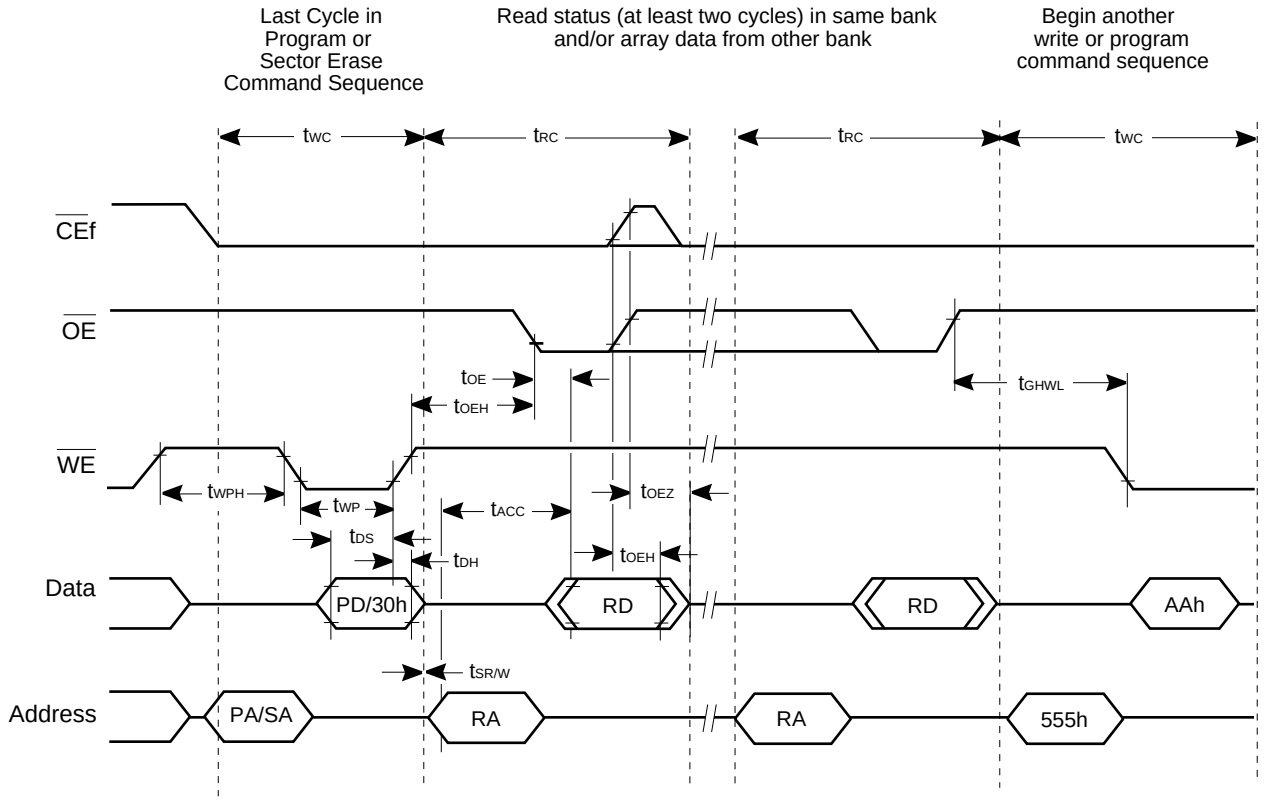
Note : VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and $\overline{\text{Data}}$ Polling will output true data.

- **Toggle Bit Timings (During Embedded Algorithm)**



Note : VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.

- **Bank-to-Bank Read/Write Cycle Timings**



Note: Break points in waveforms indicate that system may alternately read array data from the “non-busy bank” while checking the status of the program or erase operation in the “busy” bank. The system should read status twice to ensure valid information.

■ 8M SRAM for MCP 1.8 V

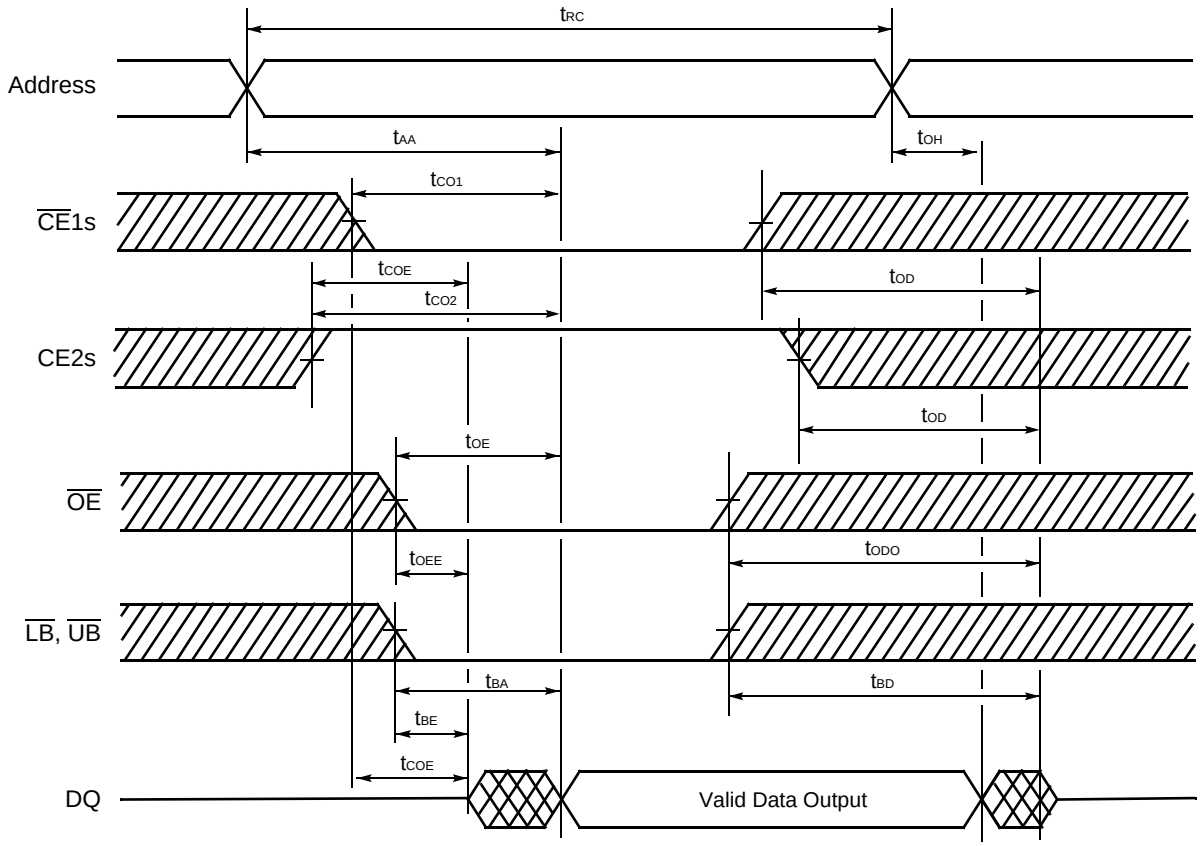
1. AC Characteristics

- **Read Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE}$1s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE}$1s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Enable Low to Output Active	t_{BE}	5	—	ns
Chip Enable ($\overline{CE}$1s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{LB}$, $\overline{UB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	5	—	ns

Note: Test Conditions–Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 1.8 V
Timing measurement reference level
Input: 0.5 × V_{CC}s
Output: 0.5 × V_{CC}s

- **Read Cycle (SRAM)**

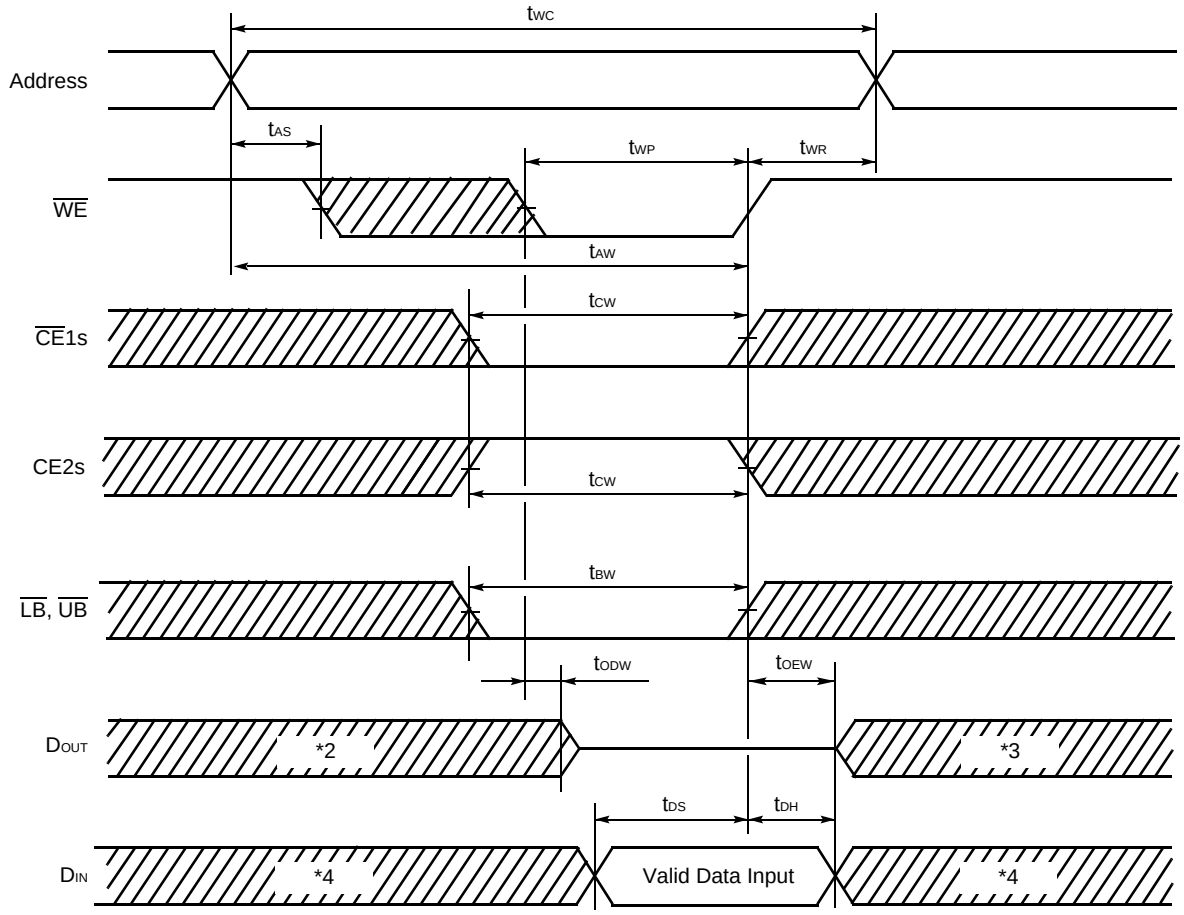


Note: $\overline{WE}$ remains High for the read cycle.

- **Write Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	55	—	ns
$\overline{CE}$1s to End of Write	t_{CW1}	55	—	ns
CE2s to End of Write	t_{CW2}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{LB}$, $\overline{UB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEW}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

- **Write Cycle*1 ($\overline{WE}$ control) (SRAM)**



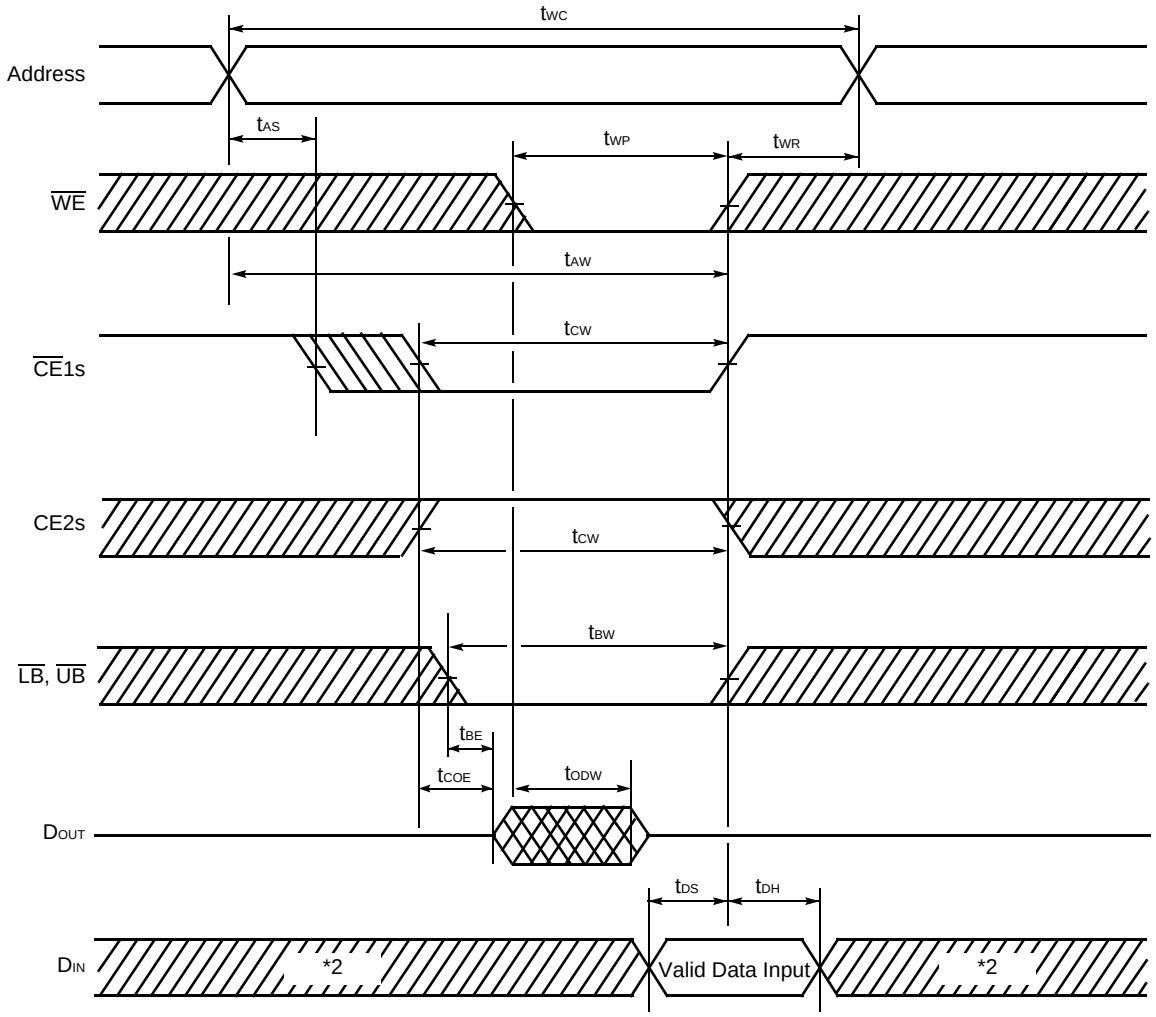
*1 : If $\overline{OE}$ is High during the write cycle, the outputs will remain at high impedance.

*2 : If $\overline{CE}$1s goes Low (or CE2s goes High) coincident with or after $\overline{WE}$ goes Low, the output will remain at high impedance.

*3 : If $\overline{CE}$1s goes High (or CE2s goes Low) coincident with or before $\overline{WE}$ goes High, the output will remain at high impedance.

*4 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

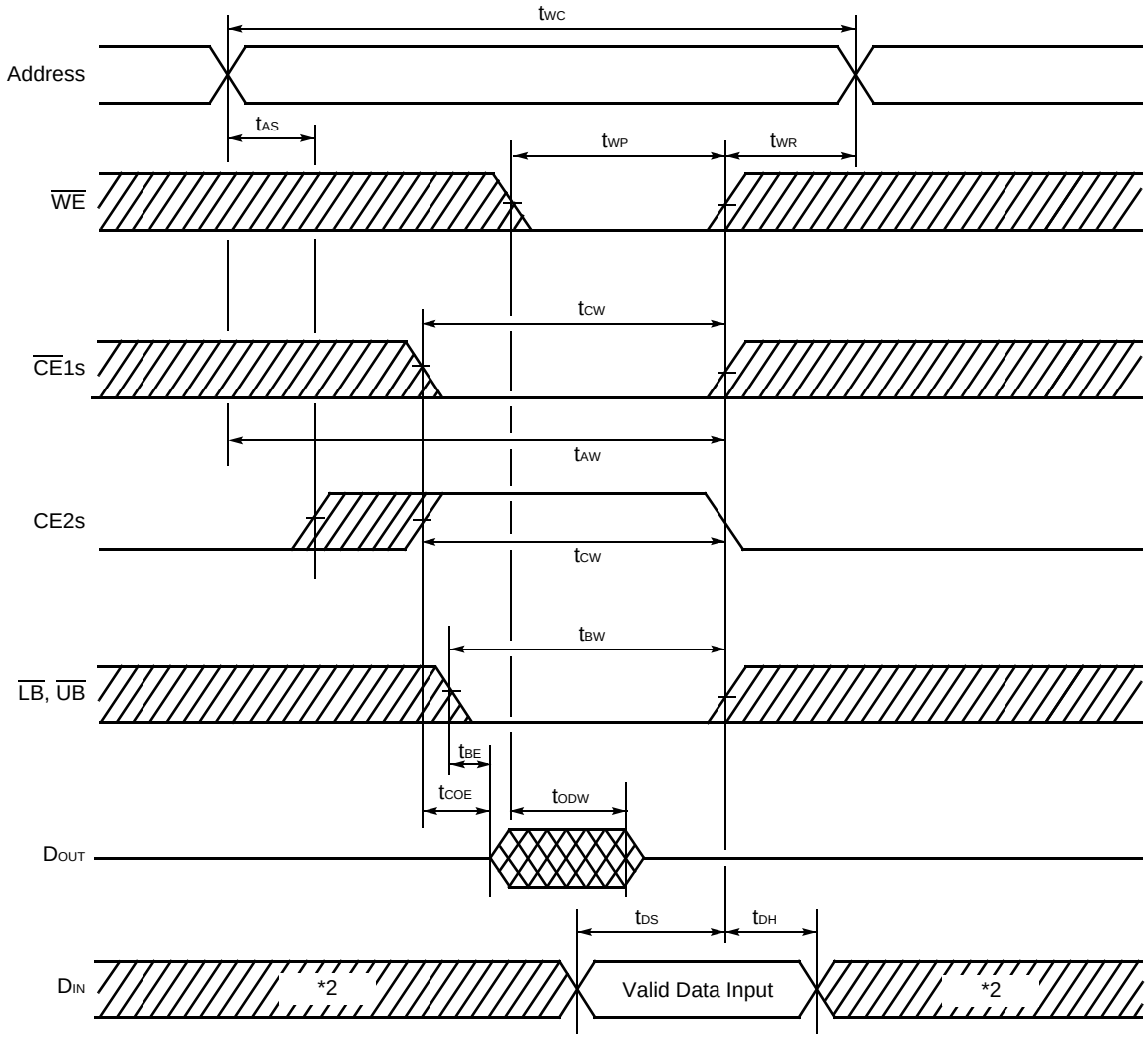
- **Write Cycle*1 ($\overline{CE}$1s control) (SRAM)**



*1: If $\overline{OE}$ is High during the write cycle, the outputs will remain at high impedance.

*2: Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

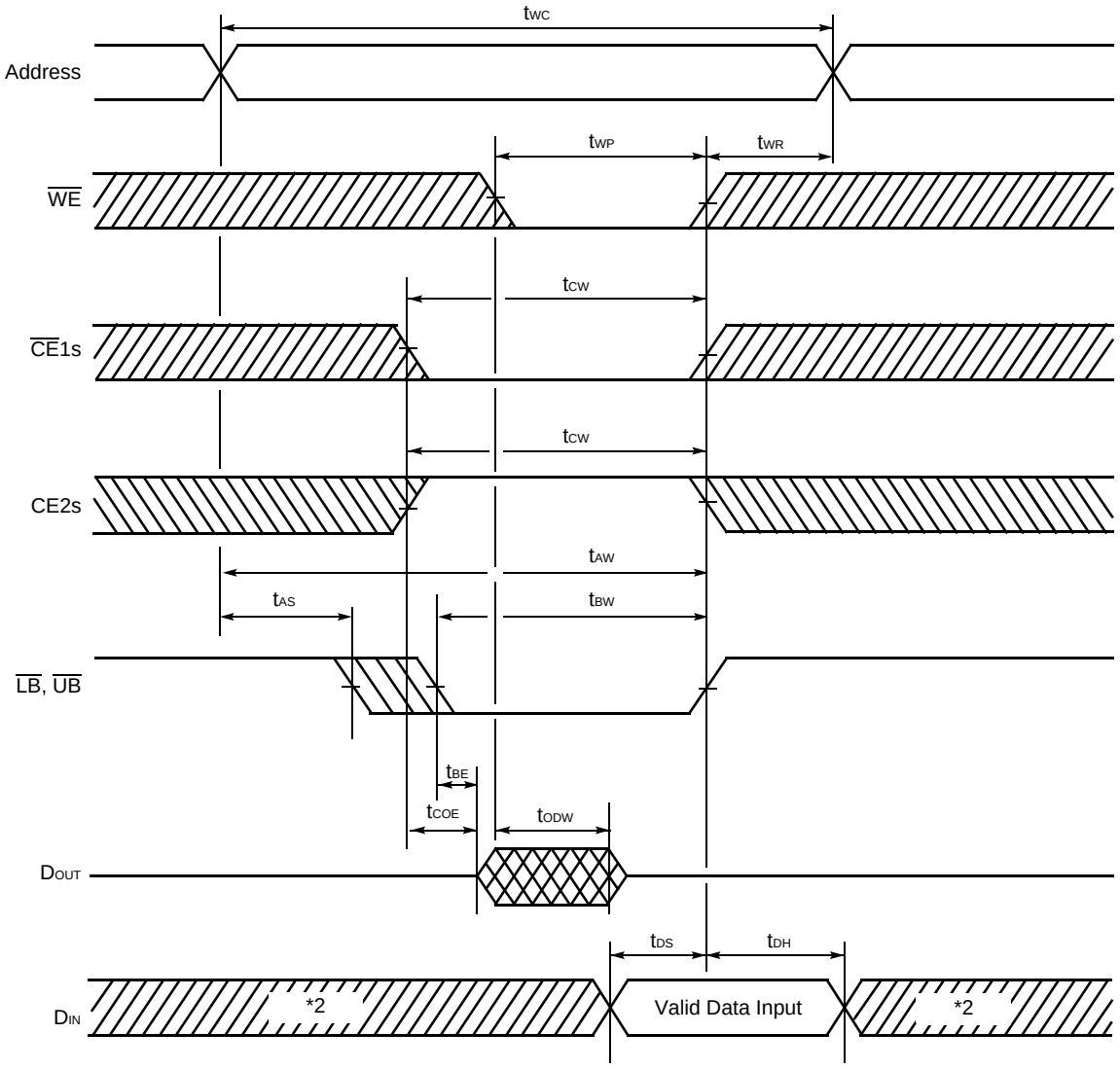
- **Write Cycle*1 (CE2s Control) (SRAM)**



*1 : If $\overline{OE}$ is High during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle*1 ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



*1 : If $\overline{OE}$ is High during the write cycle, the outputs will remain at high impedance.

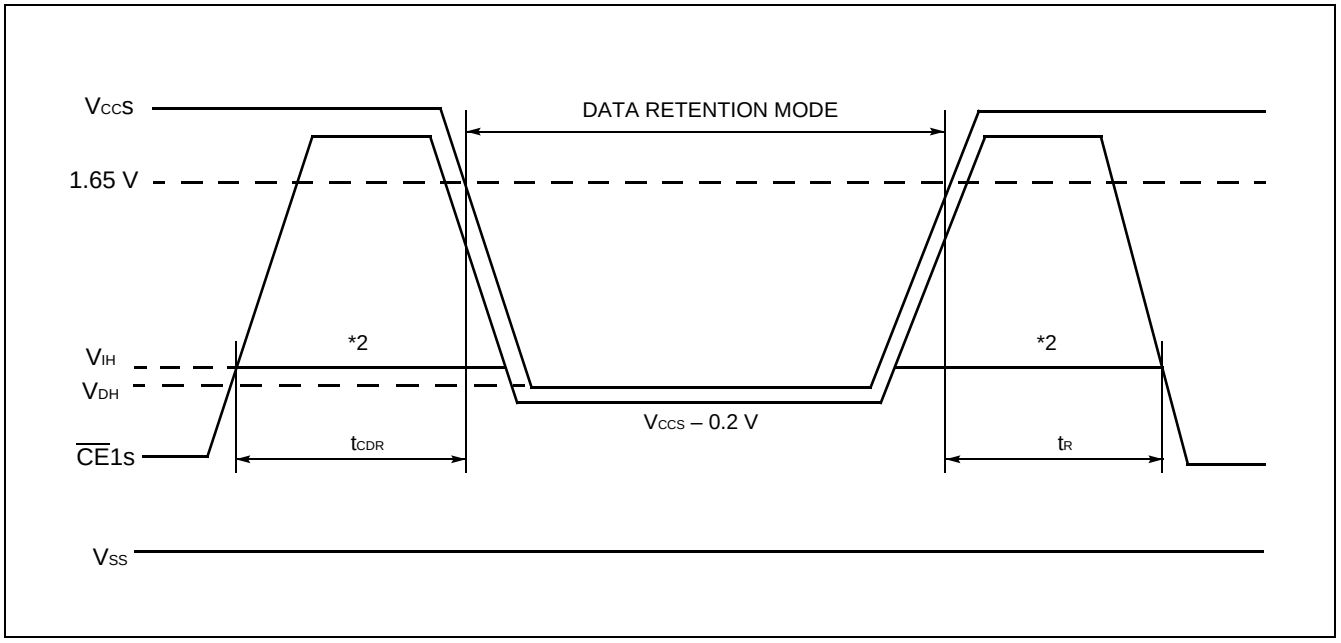
*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

2. Data Retention Characteristics (SRAM)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Data Retention Supply Voltage		V_{DH}	1.0	—	1.95	V
Standby Current	V_{DH} = 1.8 V	I_{DDS2}	—	0.3	14	µA
Chip Deselect to Data Retention Mode Time		t_{CDR}	0	—	—	ns
Recovery Time		t_R	t_{RC}	—	—	ns

Note : t_{RC}: Read cycle time

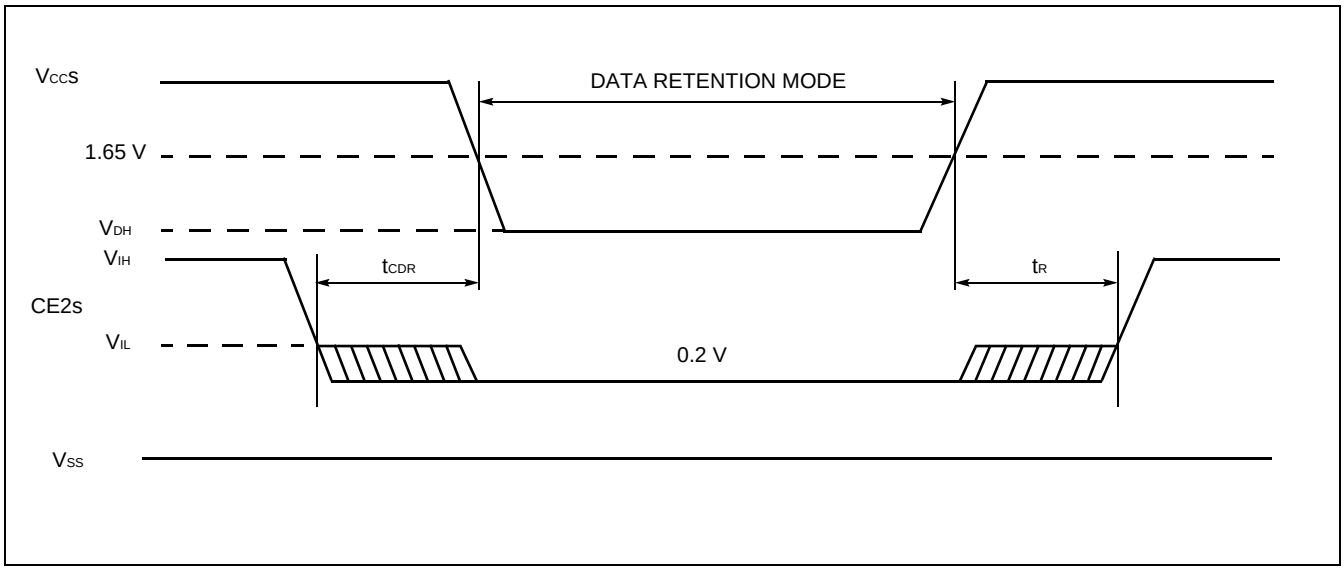
- **$\overline{CE}$1s Controlled Data Retention Mode *1**



*1 : In $\overline{CE}$1s controlled data retention mode, input level of CE2s should be fixed Vccs to V_{CC}S–0.2 V or V_{SS} to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to V_{CC}S+0.3 V.

*2 : When $\overline{CE}$1s is operating at the V_{IH} Min level, the standby current is given by I_{SB1}s during the transition of V_{CC}s from Vccs Max to V_{IH} Min level.

- **CE2s Controlled Data Retention Mode***



* : In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3 V.

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	—	—	16.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	—	22.0	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	—	—	18.0	pF

Note : Test conditions T_A = + 25 °C, f = 1.0 MHz

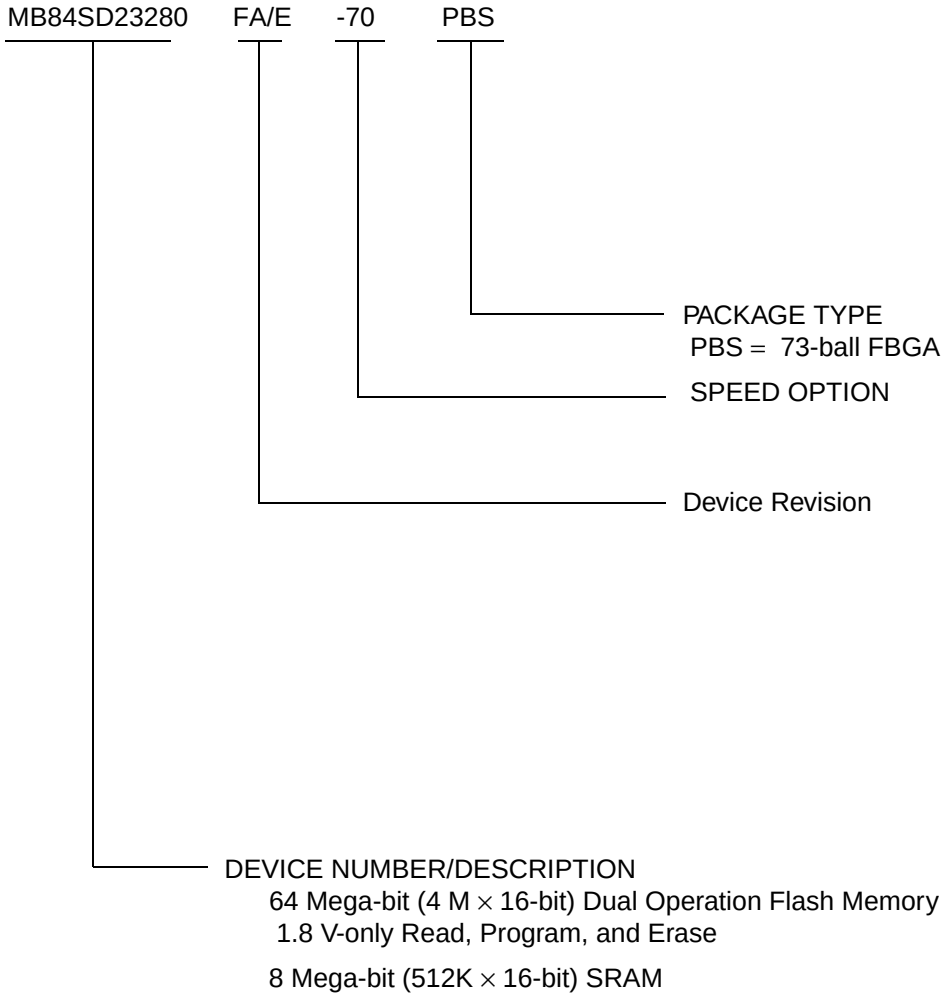
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

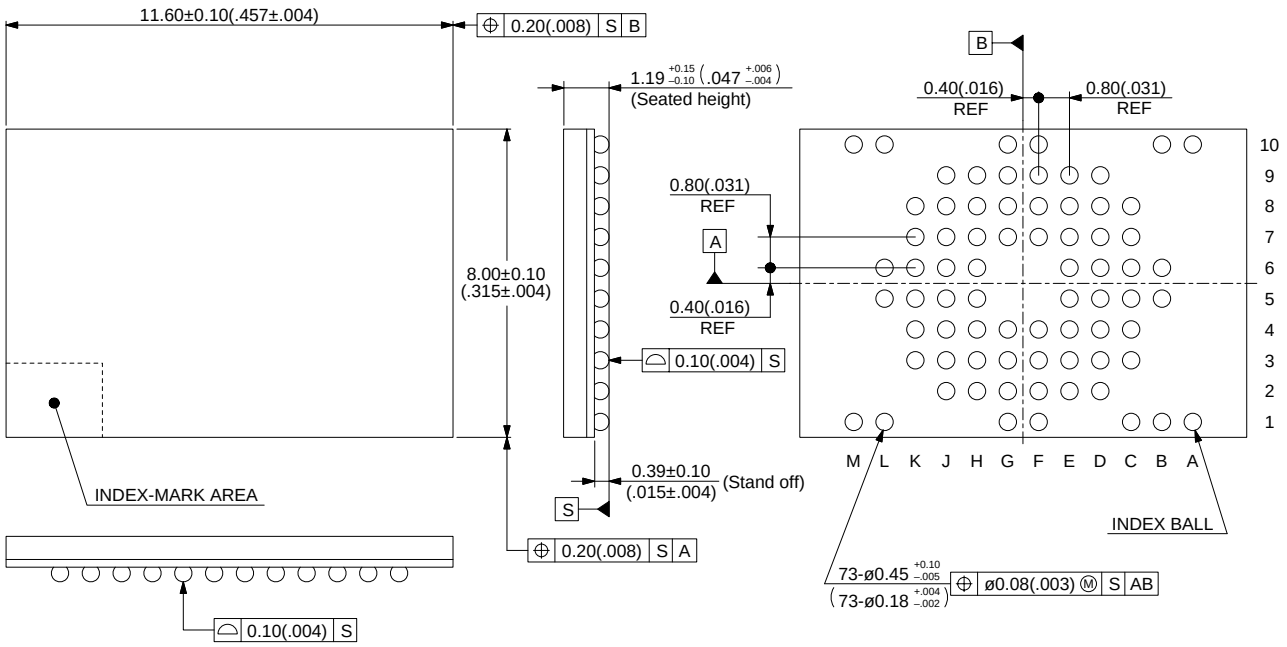
- The high voltage (V_{ID}) cannot apply to address pins and control pins.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

73-ball plastic FBGA
(BGA-73P-M03)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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