January1990
Edition 1.0

FUJITSU

DATA SHEET

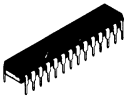
MB8464A-10-X/-10LL-X/-15-X/-15LL-X
CMOS 64K-BIT LOW-POWER SRAM

8K Words x 8 Bits CMOS Static RAM for Extended Temperature Operation

The Fujitsu MB8464A-X is an 8,192 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

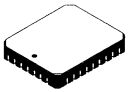
The MB8464A-X has low power dissipation, low cost and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

PLASTIC PACKAGE
DIP-28P-M02



PLASTIC PACKAGE
DIP-28P-M04

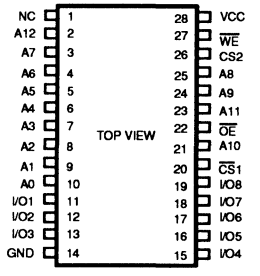
PLASTIC PACKAGE
FPT-28P-M02

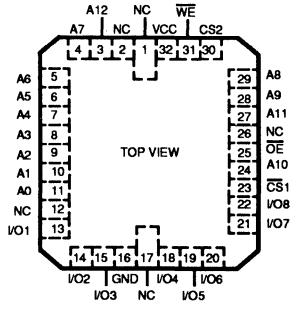


CERAMIC PACKAGE
LCC-32C-A02

- Organization: 8,192 words x 8 bits
- Access time: 100 ns max. (MB8464A-10-X/-10LL-X)
  150 ns max. (MB8465A-15-X/-15LL-X)
- Operating temperature: –40°C to +85°C
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V supply ±10% tolerance
- Low power consumption:
  1.1 mW max. (CMOS standby)
  27.5 mW max. (TTL standby)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  DIP (600 mil) MB8464A-xx(LL)P-X
  Skinny DIP (300 mil) MB8464A-xx(LL)PSK-X
  SOP (300 mil) MB8464A-xx(LL)PF-X
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB8464A-xx(LL)CV-X

PIN ASSIGNMENT





Absolute Maximum Ratings (See Note)

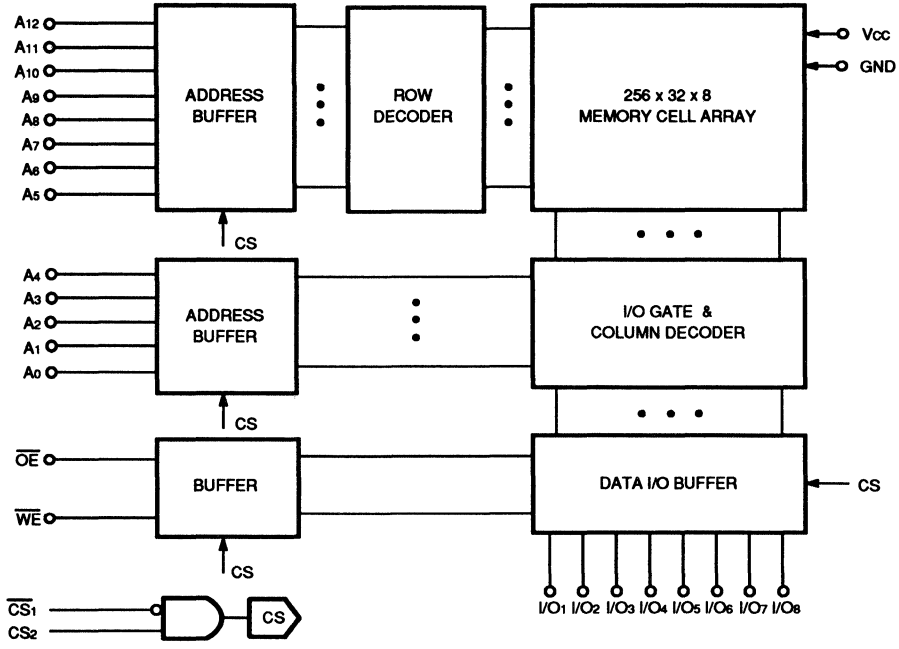
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +7.0	V
Input Voltage		V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage		$V_{I/O}$	–0.5 to V_{CC} +0.5	V
Temperature Under Bias		T_{BIAS}	–50 to +95	°C
Storage Temperature Range	Ceramic	T_{STG}	–65 to +150	°C
	Plastic		–40 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 – MB8464A-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

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CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITION (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	–40		85	°C

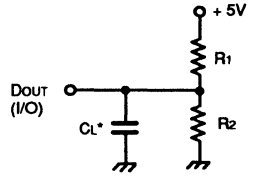
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB8464A-10-X/10LL-X MB8464A-15-X/15LL-X		Unit	Test Condition
		Min	Max		
Standby Supply Current	I_{SB1}		0.2	mA	$CS2 \le 0.2V$ or $\overline{CS1} \ge V_{CC}-0.2V$ (with $CS2 \le 0.2V$ or $CS2 \ge V_{CC}-0.2V$)
	I_{SB2}		5.0	mA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$
Active Supply Current	I_{CC1}		60	mA	$V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0mA $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$
Operating Supply Current	I_{CC2}		70	mA	Cycle = Min. Duty = 100%, I_{OUT} = 0mA
Input Leakage Current	I_{LI}	–10	10	µA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	I_{LVO}	–50	50	µA	$\overline{V_{IO}} = 0V$ to V_{CC} $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Input High Voltage	V_{IH}	2.4	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	–0.3 *	0.6	V	
Output High Voltage	V_{OH}	2.4		V	$I_{OH} = -1.0mA$
Output Low Voltage	V_{OL}		0.4	V	$I_{OL} = 2.1mA$

Note: All voltages are referenced to GND.
* : –3.0V min. for pulse width less than 20 ns. (V_{IL} min. = –0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.6V and 2.4V)
- Timing Reference Levels Input: V_{IL} = 0.6V, V_{IH} = 2.4V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

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AC CHARACTERISTICS

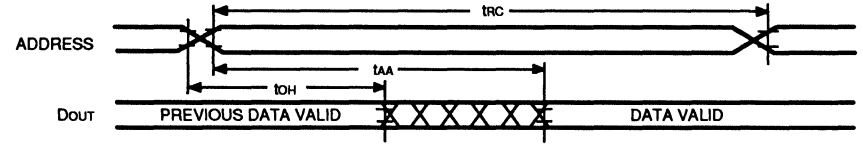
(Recommended operating conditions otherwise noted.)

READ CYCLE *1

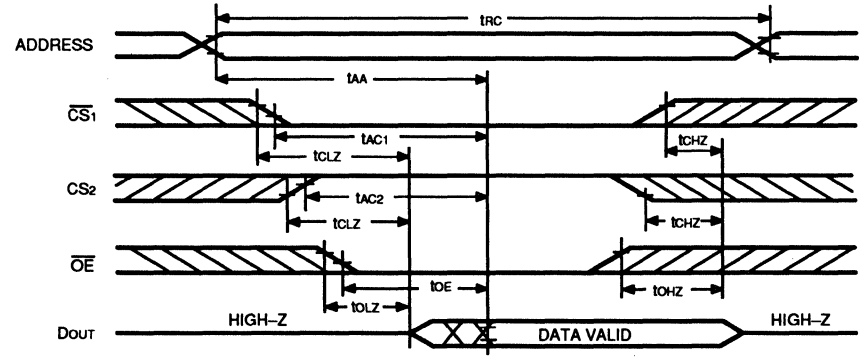
Parameter	Symbol	MB8464A-10-X/10LL-X		MB8464A-15-X/15LL-X		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		150		ns
Address Access Time	t_{AA}		100		150	ns
$\overline{CS1}$ Access Time	t_{AC1}		100		150	ns
CS2 Access Time	t_{AC2}		100		150	ns
Output Enable to Output Valid	t_{OE}		45		60	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z *4	t_{CLZ}	10		10		ns
Output Enable to Output Low-Z *4	t_{OLZ}	5		5		ns
Chip Select to Output High-Z *4	t_{CHZ}		40		50	ns
Output Enable to Output High-Z *4	t_{OHZ}		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2 : $\overline{CS1}$, CS2 CONTROLLED *3



Note: *1 $\overline{WE}$ is high for Read cycle.

*2 Device is continuously selected, $\overline{CS_1}$ = $\overline{OE}$ = V_{IL}, CS_2 = V_{IH}.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

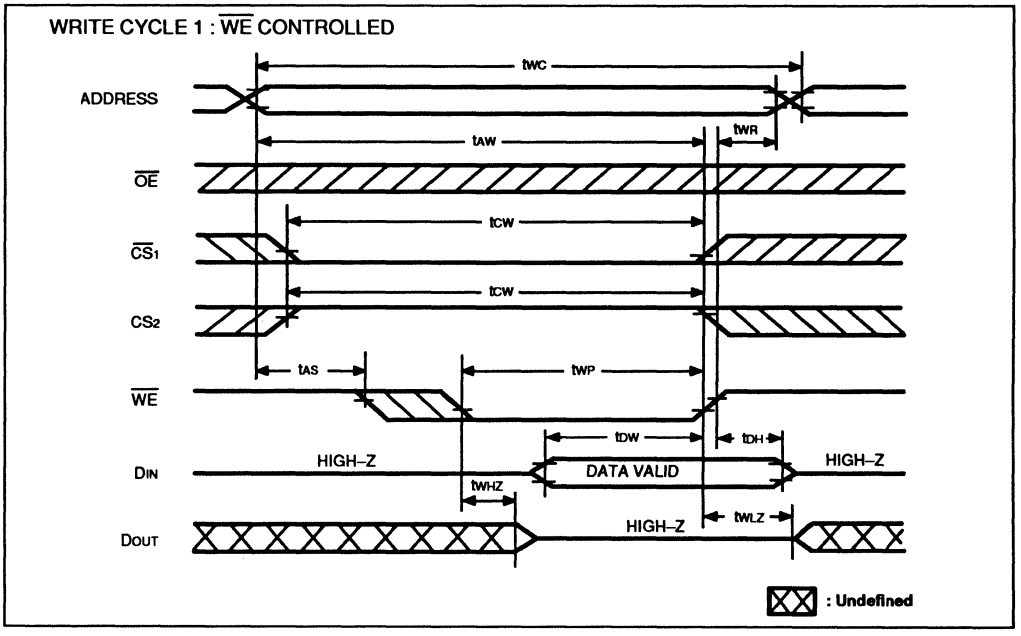
AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	MB8464A-10-X/10LL-X		MB8464A-15-X/15LL-X		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	tWC	100		150		ns
Address Valid to End of Write	tAW	80		100		ns
Chip Select to End of Write	tCW	80		100		ns
Data Valid to End of Write	tDW	40		50		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	60		90		ns
Address Setup Time	tAS	0		0		ns
Write Recovery Time *4	tWR	5		5		ns
Write Enable to Output Low-Z *5	tWLZ	5		5		ns
Write Enable to Output High-Z *5	tWHZ		40		50	ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: 1* If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

2* If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

3* All write cycle are determined from last address transition to the first address transition of the next address.

4* tWR is defined from the end point of WRITE Mode.

5* Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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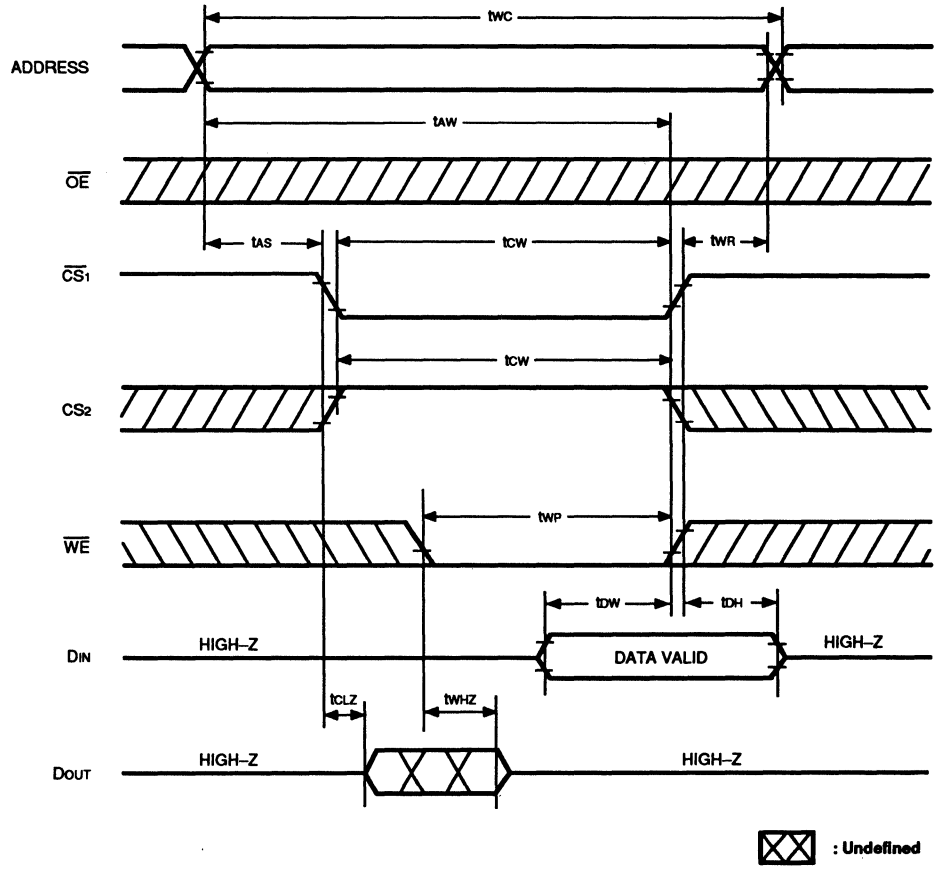
AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE 2 : $\overline{CS_1}$ CONTROLLED *1



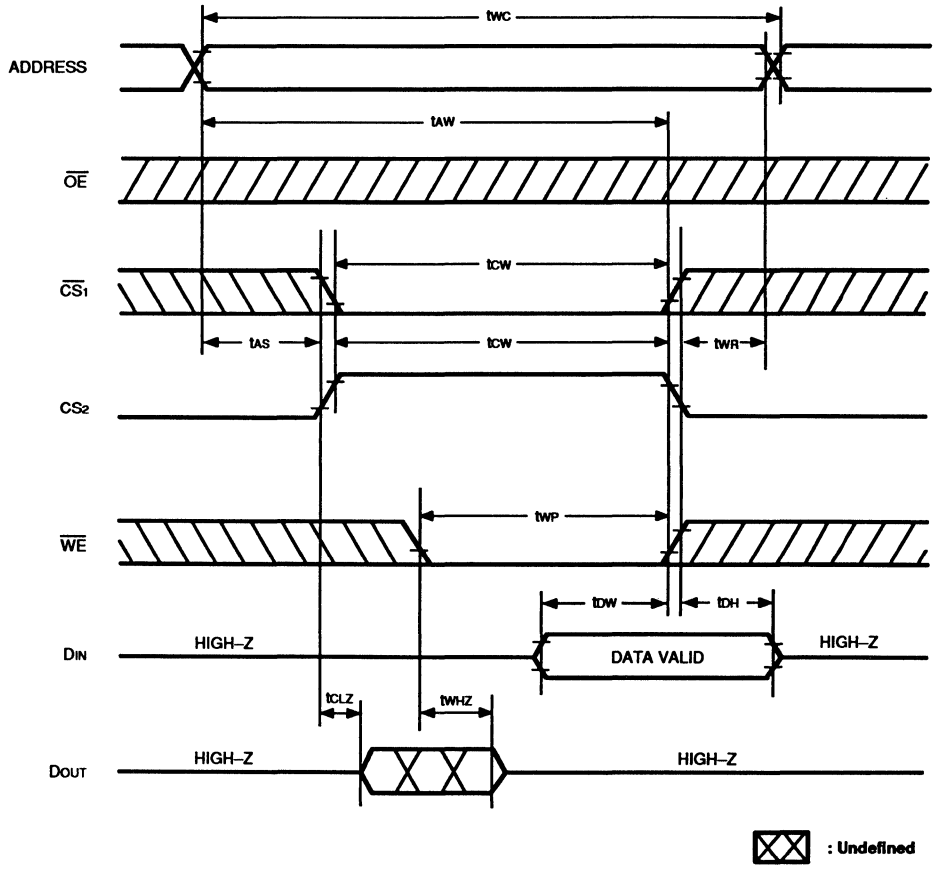
Note: *1 If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE 3 : $\overline{CS_2}$ CONTROLLED *1



Note: *1 If $\overline{OE}$, CS_1 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			50	µA
	LL-Version *2				50	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $V_{CC} = V_{DR} = 3.0V$

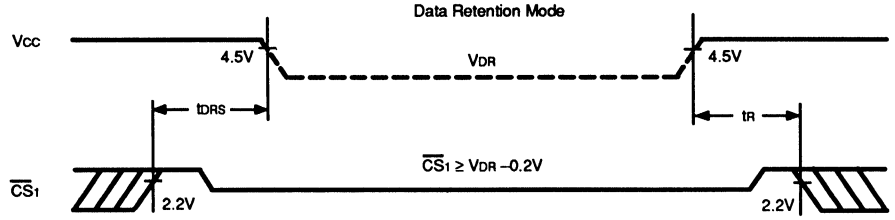
$\overline{CS_1} \geq V_{DR} - 0.2V$, $CS_2 \geq V_{DR} - 0.2V$ or $CS_2 \leq 0.2V$ (at $\overline{CS_1}$ CONTROLLED)

$CS_2 \leq 0.2V$ (at CS_2 CONTROLLED)

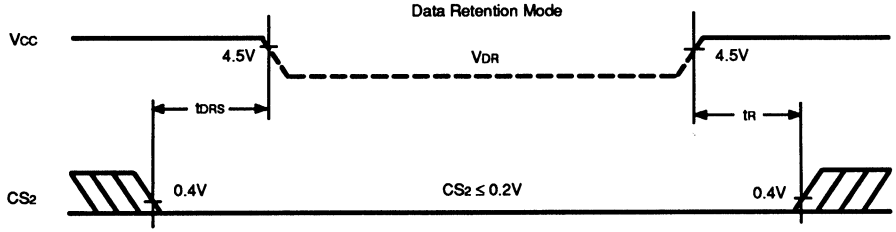
*2 I_{DR} max. = 2.0µA at $V_{DR} = 3.0V$, $T_A = -40°C$ to $+40°C$.

DATA RETENTION TIMING

$\overline{CS_1}$ CONTROLLED



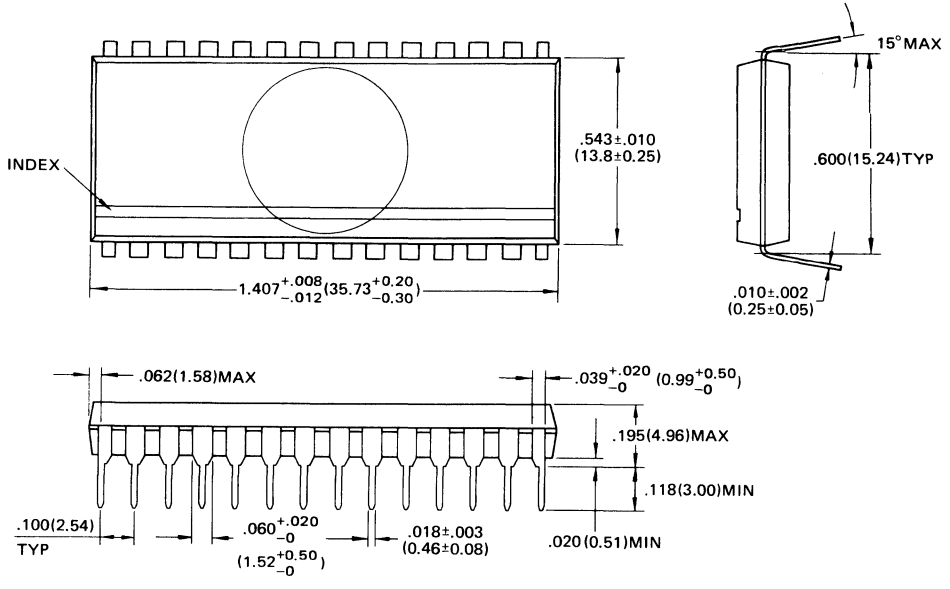
CS_2 CONTROLLED



PACKAGE DIMENSIONS

(SuffiX: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)



Dimensions in
inches (millimeters)

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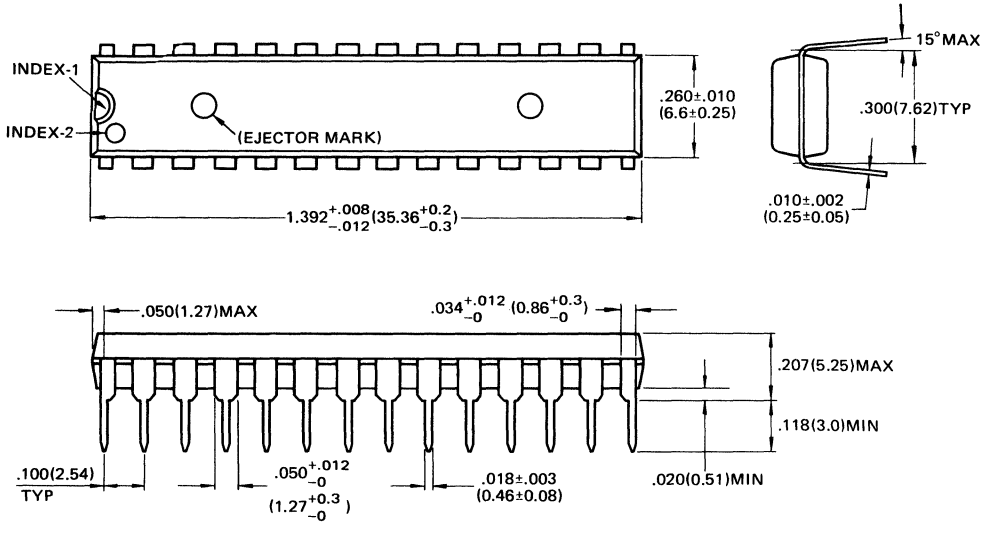
PACKAGE DIMENSIONS (Continued)

(SuffiX: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M04)



Dimensions in
inches (millimeters)

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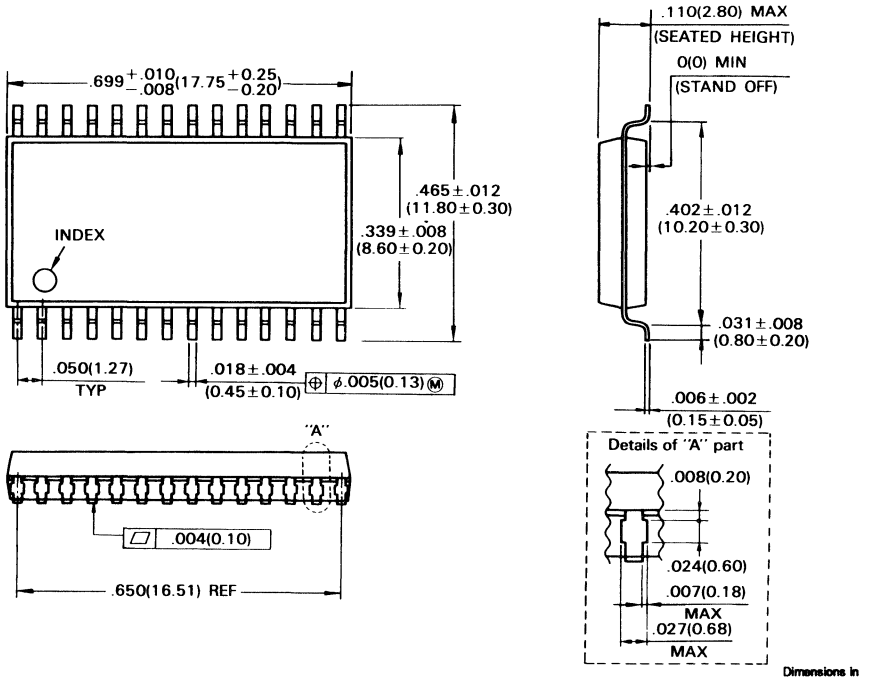
PACKAGE DIMENSIONS (Continued)

(SuffIX: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in inches (millimeters)

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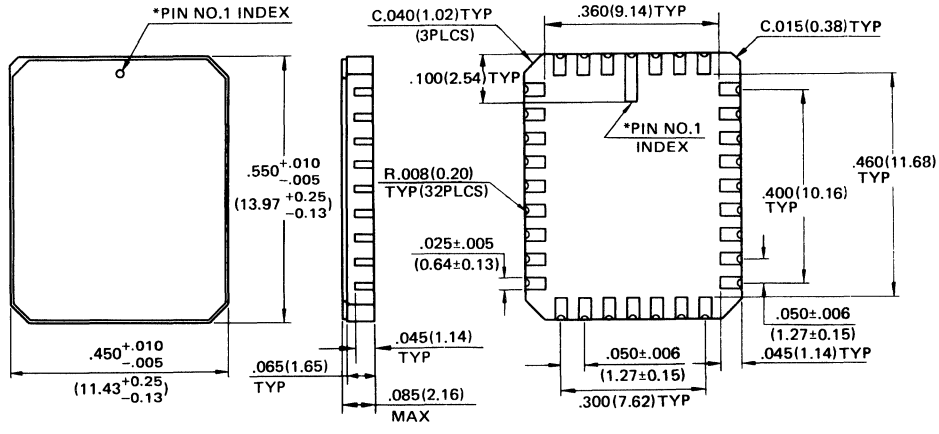
PACKAGE DIMENSIONS (Continued)

(SuffiX: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

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