CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

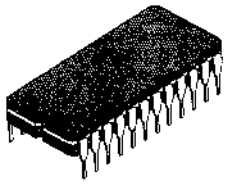
The Fujitsu MB8418/MB8418-X is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

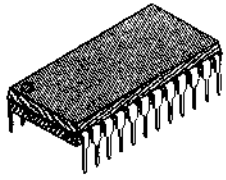
The MB8418/MB8418-X can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two chip selects ($\overline{CE}_2$ and $\overline{CE}_1$) permit the selection of an individual package when outputs are OR-tied, and the device automatically powers down. The MB8418/MB8418-X is packaged in an industry standard 24-pin dual in-line package.

FEATURES

- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200ns Max.**
- **Low Power: 55μW Max. Standby**
- **Completely Static Operation, no clocks required**
- **Extended Temperature Range (MB8418-X): −40°C to +85°C**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **MB8418 is compatible with TC5518**

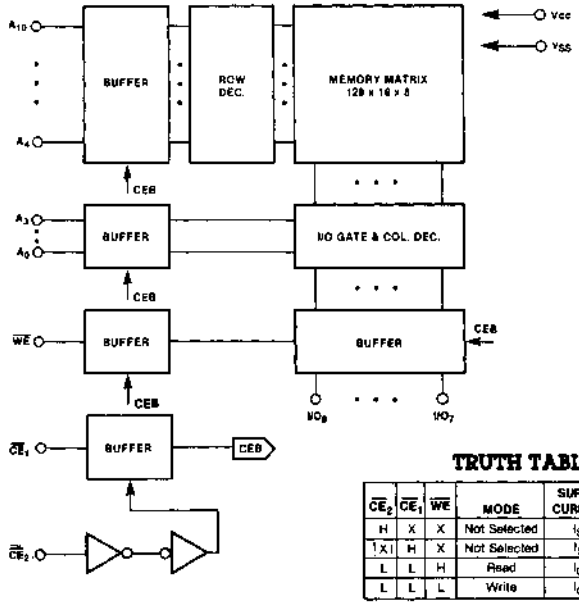


CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

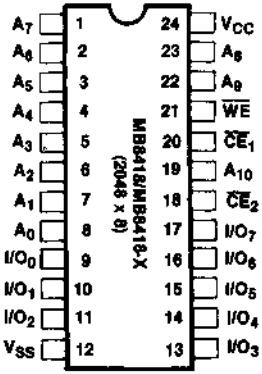
MB8418/MB8418-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}_2$	$\overline{CE}_1$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, (Referenced to V_{SS} = GND)

Parameter	Symbol	MB8418			MB8418-X			Unit
		Min	Typ	Max	Min	Typ	Max	
Ambient Temperature	T_A	0	—	+70	−40	—	+85	°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

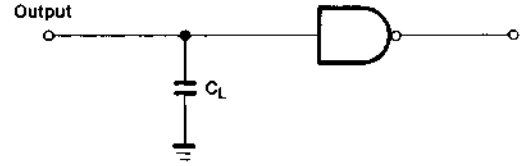
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	$\overline{CE}$ = V_{CC} − 0.2V to V_{CC} + 0.2V V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB1}	—	10	μA
Standby Supply Current	$\overline{CE}$ = V_{IH} V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB2}	—	2	mA
Active Supply Current	$\overline{CE}$ = V_{IL} V_{IN} = V_{IL} or V_{IH}; I_{OUT} = 0	I_{CC1}	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}	—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{CE_1}$ or $\overline{CE_2}$ = V_{IH}	I_{LO}	−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}	—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns (Between 0.8V to 2.2V)**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF**



DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Write Cycle Time	t_{WC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
Chip Enable Access Time	t_{ACE}	—	200	ns
Output Hold from Address Change	t_{OH}	15	—	ns
Output Low Z from $\overline{CE}_2$ or $\overline{CE}_1$	t_{CLZ}	15	—	ns
Output High Z from $\overline{CE}_2$ or $\overline{CE}_1$	t_{CHZ}	—	60	ns
Output Low Z from $\overline{WE}$	t_{WLZ}	15	—	ns
Output High Z from $\overline{WE}$	t_{WHZ}	—	60	ns
Address Set Up Time	t_{AS}	0	—	ns
Read Set Up Time	t_{RS}	0	—	ns
Read Hold Time	t_{RH}	0	—	ns
Write Set Up Time	t_{WS}	0	—	ns
Write Hold Time	t_{WH}	0	—	ns
Address Valid to End of Write	t_{AW}	160	—	ns
Chip Enable to End of Write	t_{CEW}	160	—	ns
Write Pulse Width	t_{WP}	140	—	ns
Write Recovery Time	t_{WR}	10	—	ns
Data Set Up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DH}	0	—	ns

DYNAMIC CHARACTERISTICS

Data Retention Characteristics, Notes [1,2]

Parameter	Notes	Symbol	Min	Max	Unit
Data Retention Supply Voltage	[2]	V_{DR}	2.0	5.5	V
Data Retention Supply Current	[1]	I_{DR}	—	10	μA
Data Retention Set Up Time		t_{DRS}	60	—	ns
Recovery Time		t_R	60	—	ns

NOTES:

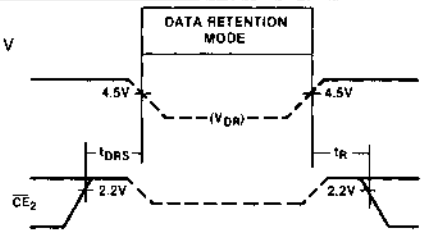
[1.] $V_{CC} = V_{DR}$, $\overline{CE}_2 = V_{DR} - 0.2$ V to $V_{DR} + 0.2$ V, $V_{IN} = -0.2$ V to $V_{DR} + 0.2$ V

[2.] When V_{DR} = 2.5V to 5.5V,

($\overline{CE}_1$) $\overline{CE}_2$ = 2.2V to V_{DR} + 0.3V

When V_{DR} = 2.0V to 2.5V

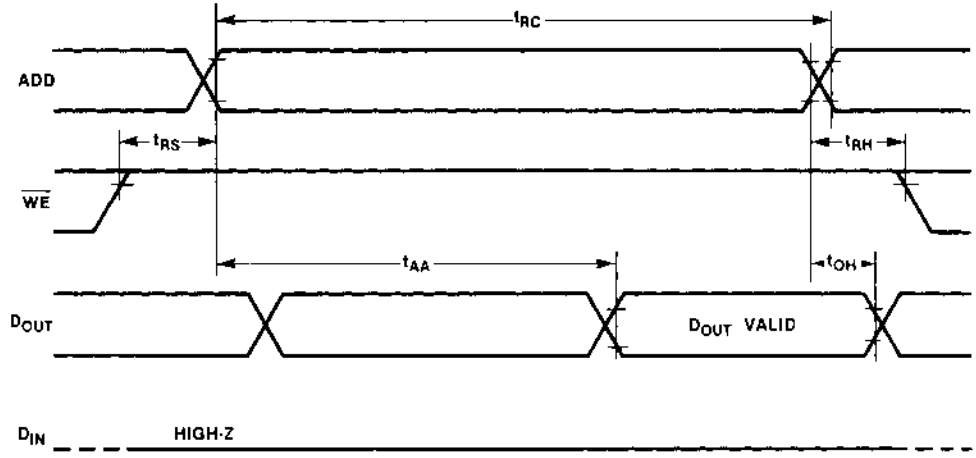
($\overline{CE}_1$) $\overline{CE}_2$ = V_{DR} − 0.3V to V_{DR} + 0.3V



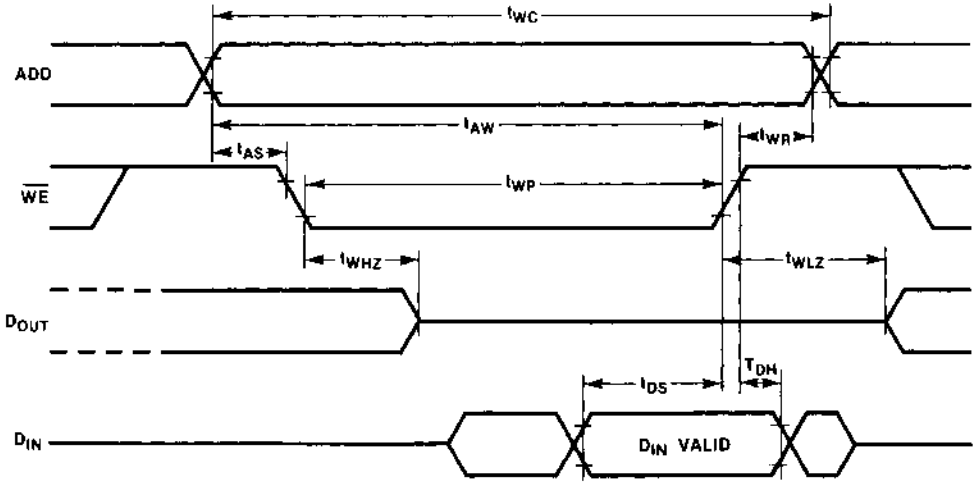
WAVEFORMS

MODE 1: $\overline{WE}$ Controlled: ($\overline{CE_2}$ = LOW, $\overline{CE_1}$ = LOW)

Read Cycle



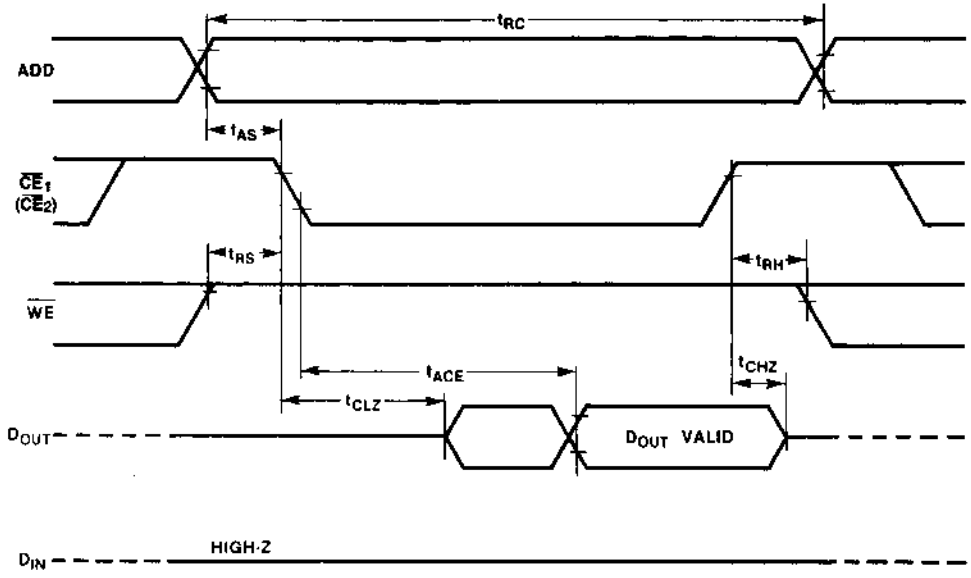
Write Cycle



WAVEFORMS (Continued)

MODE 2: $\overline{CE_1}$ or $\overline{CE_2}$ Controlled, ($\overline{CE_2}$ = LOW or $\overline{CE_1}$ = LOW)

Read Cycle



Write Cycle