April 1990
Edition 2.0

FUJITSU

DATA SHEET

MB8287-25/-35
CMOS 288K-BIT HIGH-SPEED SRAM

32K Words x 8 Bits Static Random Access Memory with Automatic Power Down

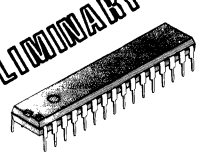
The Fujitsu MB8287 is a 32,768 words x 8 bits static random access memory with parity generator and checker, and fabricated with CMOS technology. To obtain a smaller chip size, the cell uses NMOS transistors and resistors. This device is housed in a 300 mil DIP package with low (605 mW max.) power dissipation. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

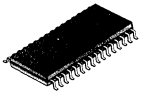
The MB8287 offers low power dissipation, low cost, and high performance.

- Organization: 32,768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 25$ ns max, $t_{ACS2} = 14$ ns max. (MB8287-25)
  $t_{AA} = t_{ACS1} = 35$ ns max, $t_{ACS2} = 15$ ns max. (MB8287-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8287-xxPSK
  SOP (450 mil) MB8287-xxPF

PRELIMINARY

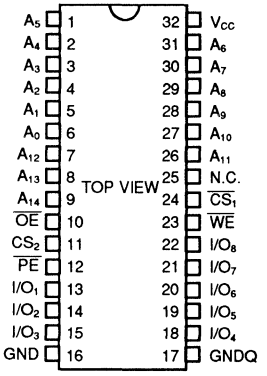


PLASTIC PACKAGE
(DIP-32P-M02)



PLASTIC PACKAGE
(FPT-32P-M02)

PIN ASSIGNMENT



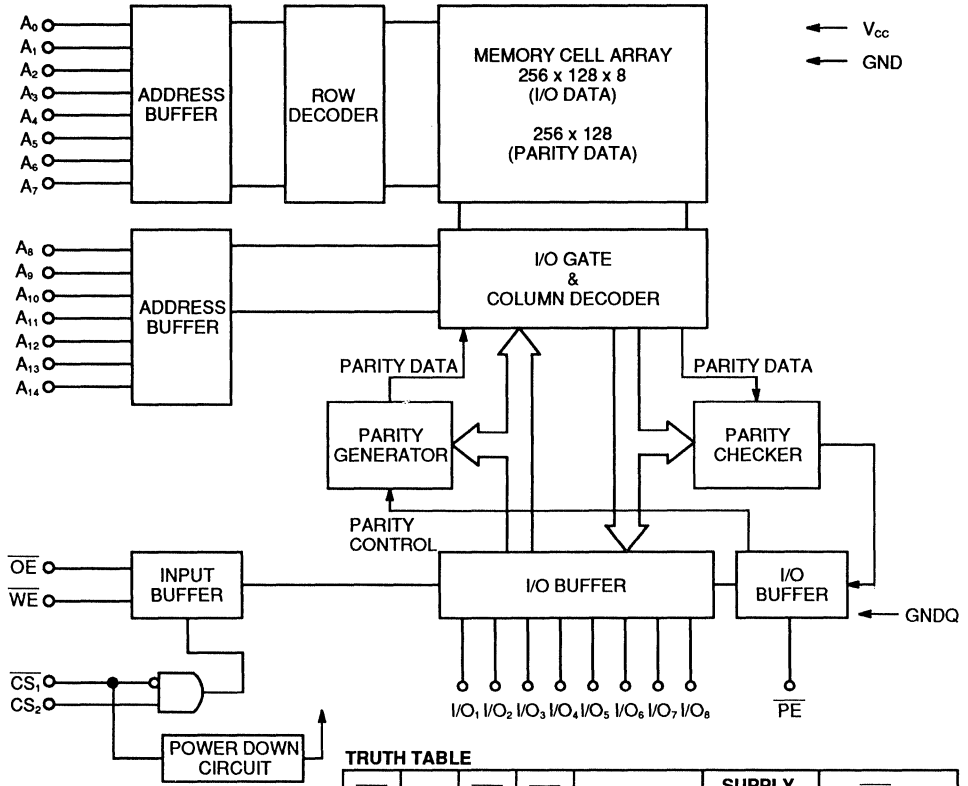
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB8287 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O, $\overline{PE}$ STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN}=0V	C_{I1}			8	pF
Input Capacitance (Other Input)	V_{IN}=0V	C_{I2}			7	pF
I/O Capacitance (with $\overline{PE}$)	$V_{I/O}$=0V	$C_{I/O}$			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

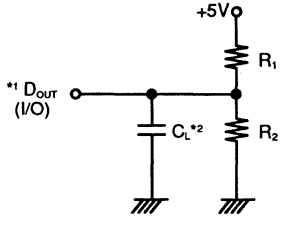
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS_1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS_1} = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	I_{OUT}=0mA, $\overline{CS_1}=V_{IL}$ Cycle=Min.		130	mA
	35ns				110	
Input Leakage Current		I_{LI}	V_{IN}=0V to V_{CC}, V_{CC}=Max.	–5	5	µA
Output Leakage Current		$I_{LI/O}$	$\overline{CS_1}=V_{IH}$ or $\overline{CS_2}=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=0V to V_{CC}	–5	5	µA
Input Low Voltage		V_{IL}		–2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	I_{OH}=–4mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL}=8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20ns. (V_{IL} min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.2V
- Output Load:



	R_1	R_2	C_L	Parameters Measured
Load I	480kΩ	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}
Load II	480kΩ	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}

*1 $\overline{PE}$ pin is included.
*2 Including Scope and Jig Capacitance

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

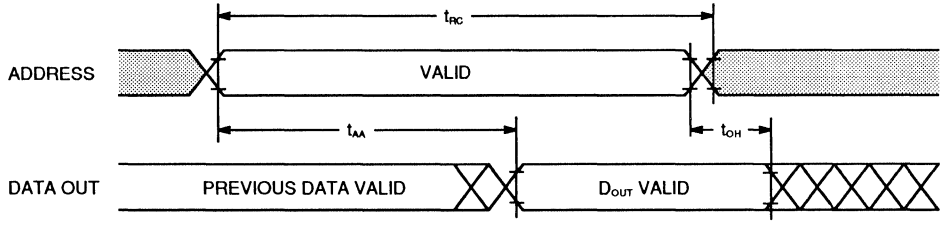
READ CYCLE*1

Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Access Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		8		ns
Output Active from CS_2*4	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2*4	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}	1	15	1	15	ns
Parity Error Access from Address*2	t_{APA}		28		40	ns
Parity Error Access from $\overline{CS_1}$*3	t_{APCS1}		28		40	ns
Parity Error Access from CS_2*3	t_{APCS2}		14		15	ns
Parity Error Access from $\overline{OE}$	t_{APOE}		12		14	ns
Parity Error Hold from Address Change	t_{POH}	3		3		ns
Parity Error Disable from Address Change*4	t_{PHZA}		20		25	ns
Parity Error Disable from $\overline{CS_1}$*4	t_{PHZ1}	1	15	1	15	ns
Parity Error Disable from CS_2*4	t_{PHZ2}	1	15	1	15	ns
Parity Error Disable from $\overline{OE}$*4	t_{POHZ}	1	15	1	15	ns

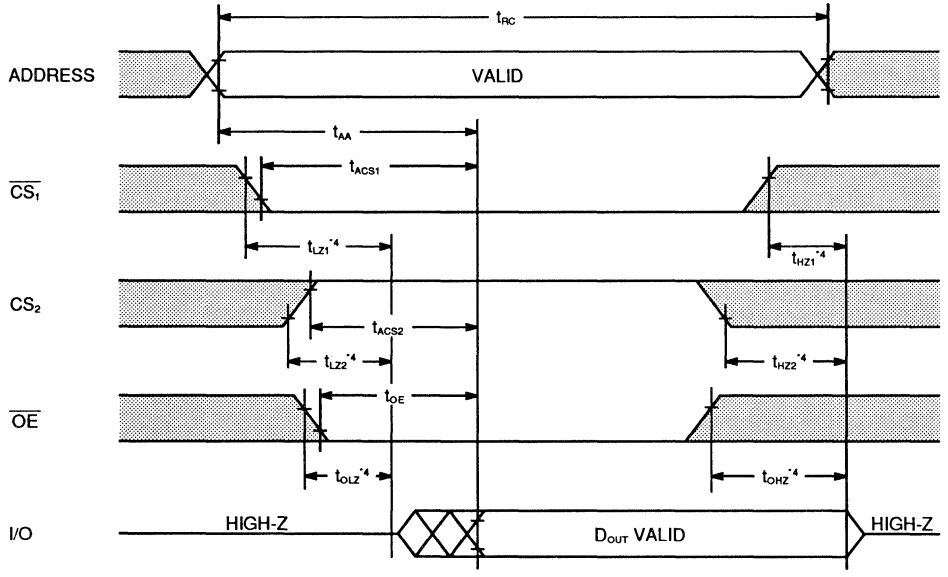
Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE : ADDRESS CONTROLLED*2



READ CYCLE : $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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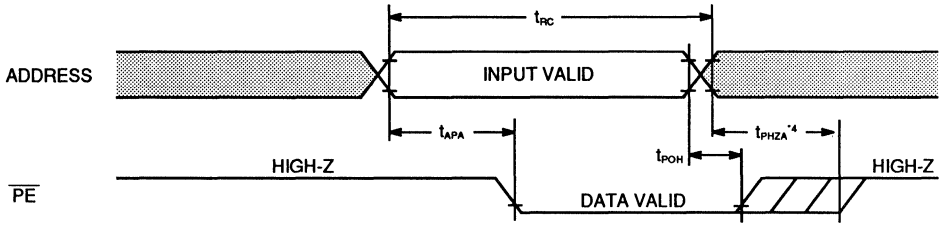
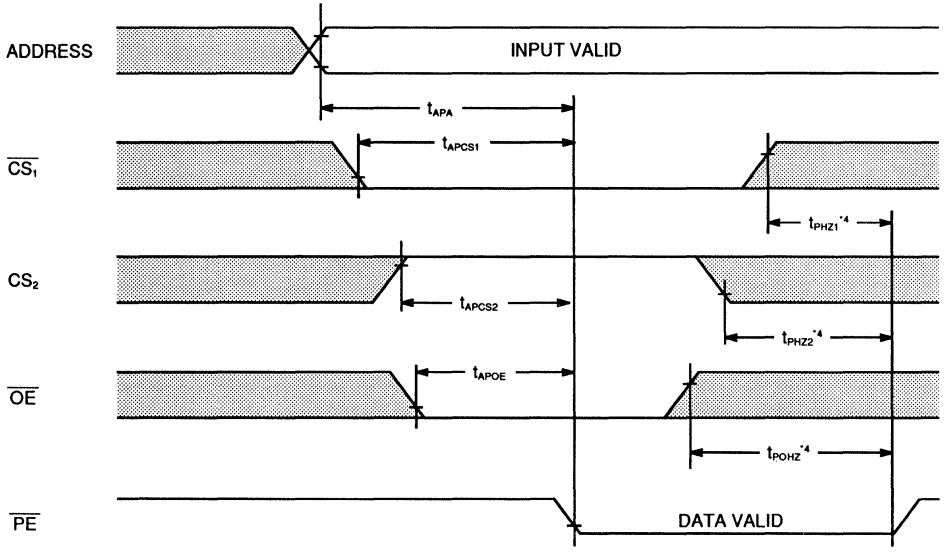
PARITY READ FUNCTION TIMING DIAGRAM*1, 5

1) ADDRESS CONTROLLED*2



2) $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}$ = "L", CS_2 = "H" and $\overline{OE}$ = "L"
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 When error occurred, $\overline{PE}$ pin outputs "L". But when no error, $\overline{PE}$ pin is in High-Z state.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1, *5, *6

Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*6 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

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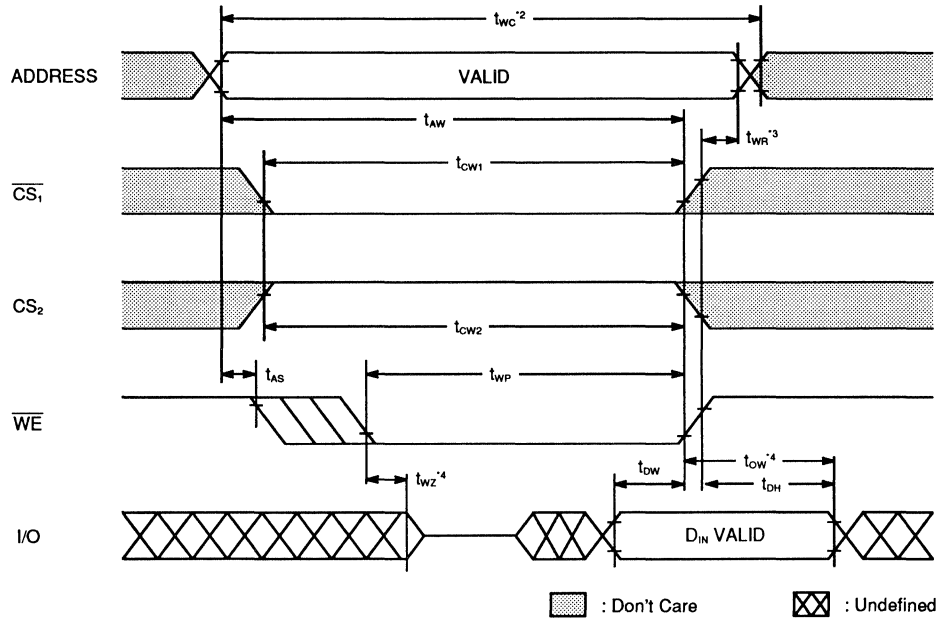
WRITE CYCLE TIMING DIAGRAM*1, *5 *6

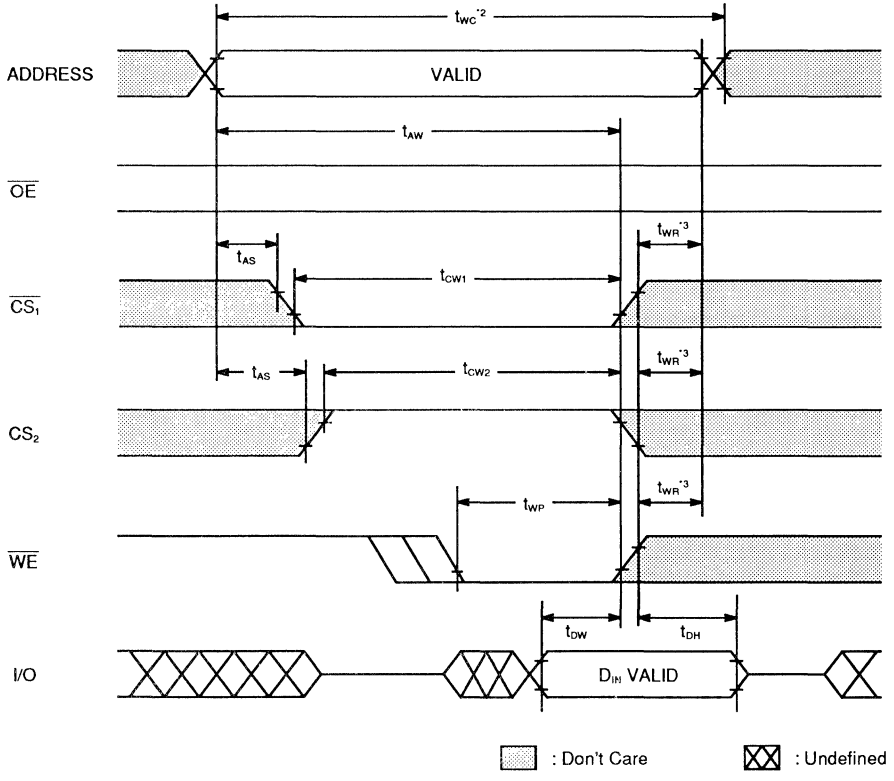
WRITE CYCLE No. 1 ($\overline{WE}$ CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*6 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

WRITE CYCLE TIMING DIAGRAM*1, *4, *5

WRITE CYCLE No. 2 ($\overline{CS_1}$, CS_2 CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*5 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

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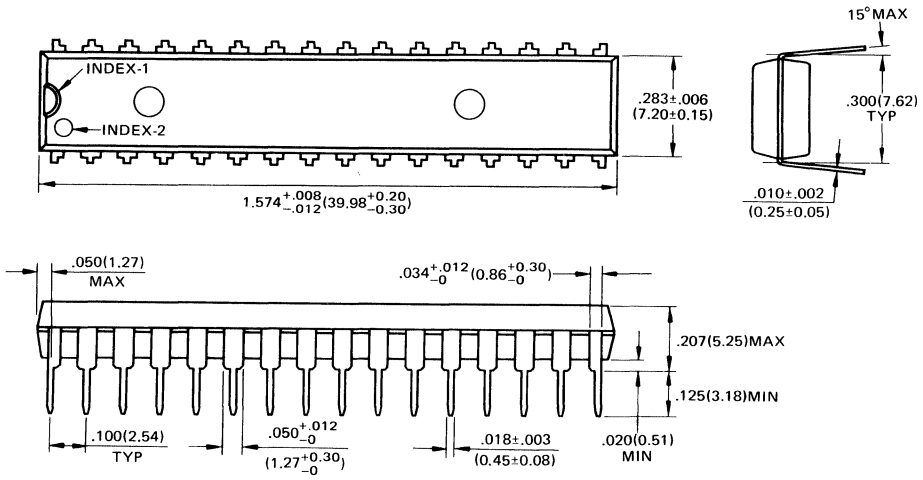
PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in
inches (millimeters)

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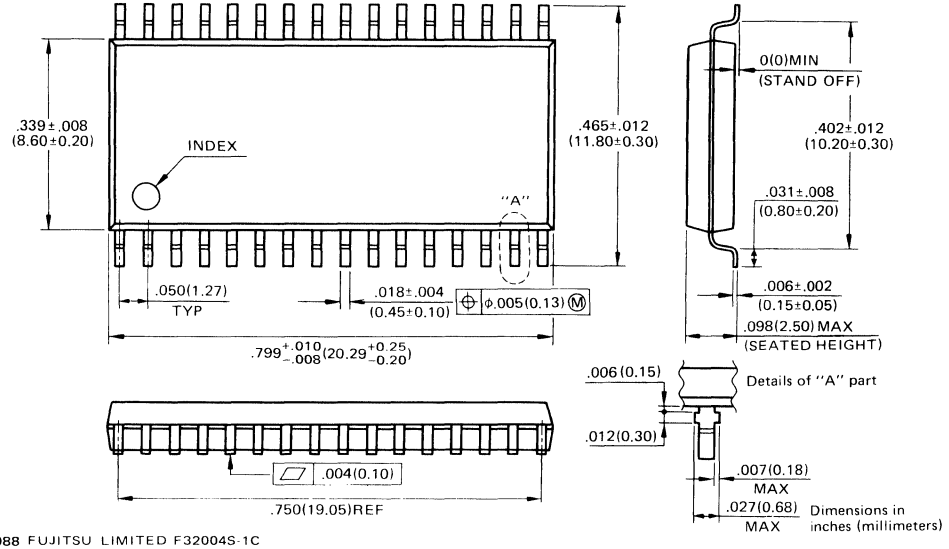
PACKAGE DIMENSIONS

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M02)



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