April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB8279RT-20/-25
CMOS 72K-BIT HIGH-SPEED SRAM

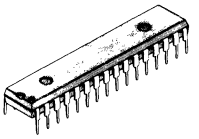
8K Words x 9 Bits Synchronous CMOS Static Random Access Memory with Automatic Power Down

The Fujitsu MB8279RT is a 8,192 words x 9 bits static random access memory fabricated with a CMOS silicon gate process.

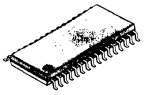
Write operation is initiated by an internal write pulse generator, which is driven by the CLK input; therefore, external control of write pulse width is not necessary. Compared to the traditional RAM, the MB8279RT provides improved system level cycle time because signal skews are not involved.

The MB8279RT is housed in 32-pin plastic skinny DIP and SOP packages. All pins are TTL compatible and a single +5 V power supply is required.

- Organization: 8,192 words x 9 bits
- Access time: t_{ACL} = 20 ns max. (MB8279RT-20)
  $t_{ACS2} = t_{PE2}$ = 10 ns max.
  t_{ACL} = 25 ns max. (MB8279RT-25)
  $t_{ACS2} = t_{PE2}$ = 12 ns max.
- Registered addresses, $\overline{CS_1}$, $\overline{WE}$ and data inputs
- Write cancel function by asynchronous CS_2 pin
- On-chip write pulse generator
- On-chip parity checker
- CMOS peripheral circuits
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. Active operation
  30 mA max. Standby operation
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Three-state data outputs and open drain parity error outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8279RT-xxPSK
  SOP MB8279RT-xxPF



PLASTIC PACKAGE
DIP-32P-M02



PLASTIC PACKAGE
FPT-32P-M02

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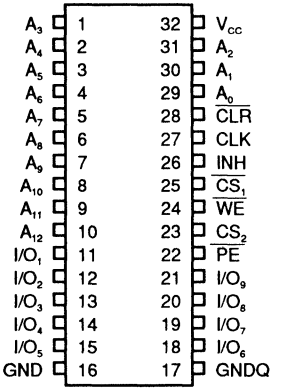
PIN ASSIGNMENT

(TOP VIEW)



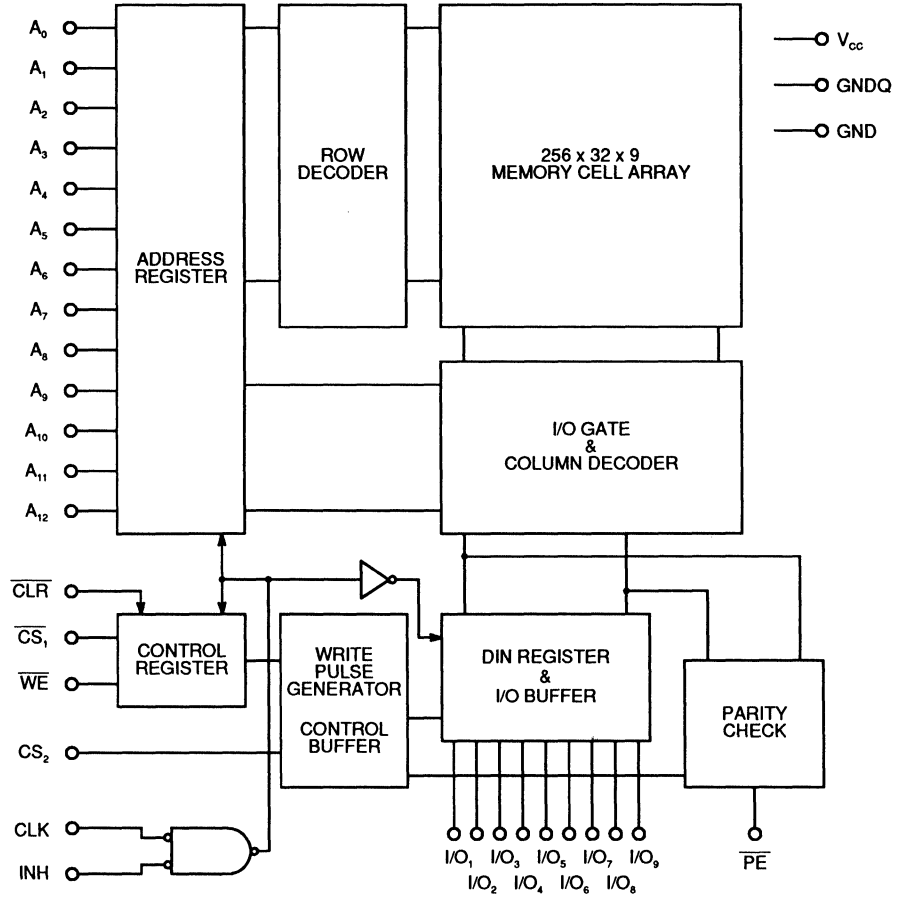
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Output Voltage	$V_{I/O}$	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB8279RT BLOCK DIAGRAM



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CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CLK	Clock	Input	Address, $\overline{CS}$, and $\overline{WE}$ are fetched at the rising edge of the CLK, and D_{IN} is fetched at falling edge of the CLK.
INH	Inhibit	Input	While INH="H", a low level of CLK is disabled.
$\overline{CLR}$	Clear	Input	When $\overline{CLR}$="L", the contents of $\overline{CS}$, and $\overline{WE}$ register are cleared to standby.
A_0 to A_{12}	Address Input	Input	Synchronous address inputs.
$\overline{CS_1}$	Chip Select 1	Input	Synchronous Chip Select 1 ($\overline{CS_1}$) input. (This pin can be used as power down.)
CS_2	Chip Select 2	Input	Asynchronous high-speed Chip Select 2 (CS_2) input. (This pin can be used as write cancel.)
$\overline{WE}$	Write Enable	Input	Synchronous Write Enable ($\overline{WE}$) input.
I/O_1 to I/O_9	Data Input/Output	Input/ Output	Data inputs/outputs. (Synchronous data input/Asynchronous data outputs)
PE	Parity Error	Output	Asynchronous parity error output: $\overline{PE}$ output remains High-Impedance state through undefined area.
V_{CC}	Power Supply	–	+5V ±10% power supply.
GNDQ	Ground for Output	–	Ground for output circuits.
GND	Ground for Others	–	Ground for other circuits.

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TRUTH TABLE

$\overline{CLR}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	MODE	I/O PIN	$\overline{PE}$ OUTPUT PIN	SUPPLY CURRENT
L	X	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	H	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	L	L	X	CHIP DISABLE	HIGH-Z	HIGH-Z	ACTIVE
H	L	H	H	READ	D_{OUT}	$\overline{PE}$ OUTPUT	ACTIVE
H	L	H	L	WRITE	D_{IN}	HIGH-Z	ACTIVE

Legend: H=High level, L=Low level, X=Don't care.
Notes: $\overline{CS_1}$, and $\overline{WE}$ are input at the rising edge of the CLK.
$\overline{PE}$ output remains High-Impedance state through undefined area.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

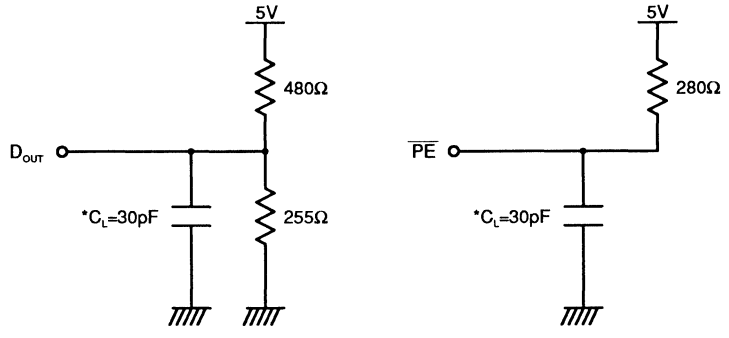
(Recommended operating conditions otherwise noted)

Parameter		Test Conditions	Symbol	Min	Max	Unit
Standby Supply Current		$\overline{CS_1}$=V_{IH}	I_{SB}		30	mA
Operating Supply Current		$\overline{CS_1}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Input Leakage Current		V_{IN}=GND to V_{CC}	I_{IL}	−10	10	µA
Output Leakage Current		$\overline{CS_1}$=V_{IH}, or CS_2=V_{IL} V_{OUT}=GND to V_{CC}	$I_{LI/O}$	−10	10	µA
Input Low Voltage			V_{IL}	−2.0*1	0.8	V
Input High Voltage			V_{IH}	2.2	6.0	V
Output High Voltage		I_{OH}=−4mA	V_{OH}	2.4		V
Output Low Voltage	D_{OUT}	I_{OL}=8mA	V_{OL}		0.4	V
	$\overline{PE}$	I_{OL}=16mA				
Peak Power-on Current*2		V_{CC}=GND to 4.5V $\overline{CLR}$=GND	I_{PO}		120	mA

Note: *1 −2.0V Min. for pulse width less than 20ns. (V_{IL}=−0.5V at DC level)
*2 The $\overline{CLR}$ input should be connected to GND to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- INPUT PULSE LEVELS: 0.6V TO 2.4V
- INPUT PULSE RISE & FALL TIMES: 5ns (Transient between 0.8V and 2.2V)
- TIMING REFERENCE LEVELS: INPUT: V_{IL}=0.8V, V_{IH}=2.2V
  OUTPUT: V_{OL}=0.8V, V_{OH}=2.2V
- OUTPUT LOAD



*INCLUDING JIG AND STRAY CAPACITANCE.
(C_L=5pF for t_{LZ}, t_{HZ}, t_{LZ2}, t_{HZ2} and t_{CRHZ}) (C_L=5pF for t_{PLZ}, t_{PHZ}, t_{PLZ2}, t_{PHZ2} and t_{CRHZ})

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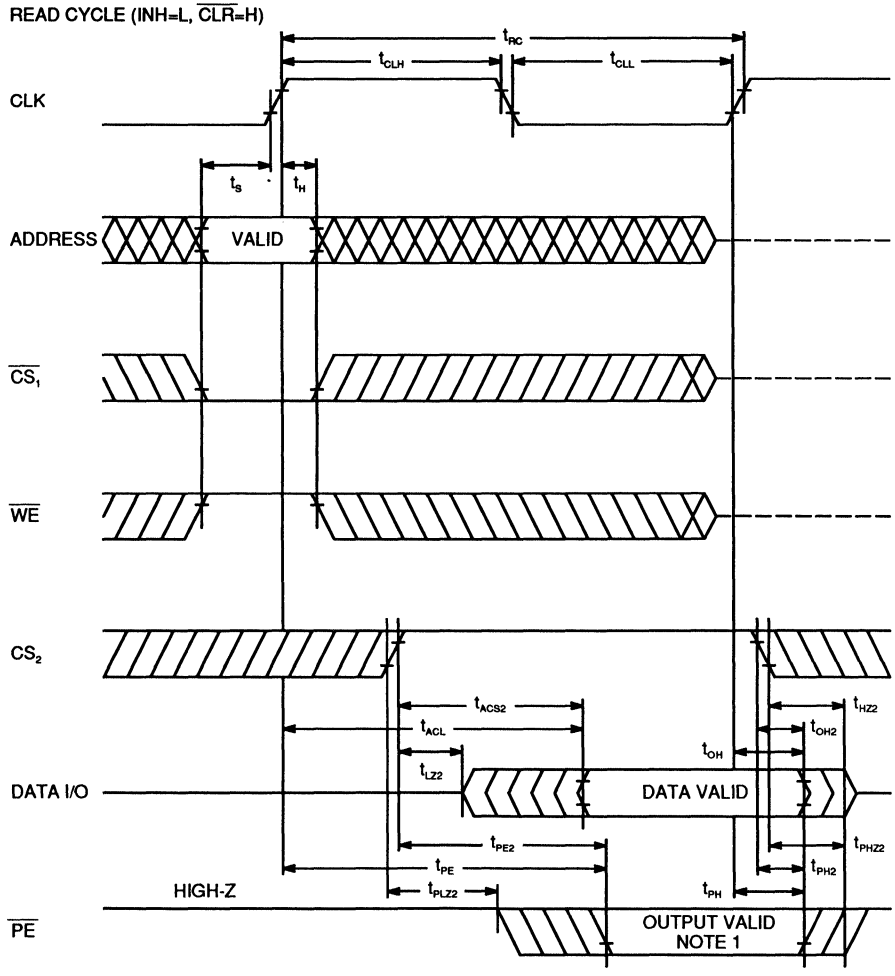
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Read Cycle Time	When on uses $\overline{PE}$	t_{RC}	20		25		ns
	When uses $\overline{PE}$	t_{RC}	25		30		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
Clock Access Time	D_{OUT}	t_{ACL}		20		25	ns
	$\overline{PE}$	t_{PE}		25		30	ns
CS_2 Access Time	D_{OUT}	t_{ACS2}		10		12	ns
	$\overline{PE}$	t_{PE2}		10		12	ns
CS_2 to Output Low-Z	D_{OUT}	t_{LZ2}	2		2		ns
	$\overline{PE}$	t_{PLZ2}	2		2		ns
CS_2 to Output High-Z	D_{OUT}	t_{HZ2}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ2}	2	8	2	10	ns
Output Hold from Clock	D_{OUT}	t_{OH}	2		2		ns
	$\overline{PE}$	t_{PH}	2		2		ns
Output Hold from CS_2	D_{OUT}	t_{OH2}	2		2		ns
	$\overline{PE}$	t_{PH2}	2		2		ns

READ CYCLE TIMING DIAGRAM



Note 1: $\overline{PE}$ output remains High-Impedance state through undefined area.

WRITE CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	20		25		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
CS_2 Setup Time		t_{CS}	2		2		ns
CS_2 Hold Time		t_{CH}	8		10		ns
Data Setup Time		t_{DS}	0		0		ns
Data Hold Time		t_{DH}	6		6		ns
CLK to Output High-Z	D_{OUT}	t_{HZ}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ}	2	8	2	10	ns
CLK to Output Low-Z	D_{OUT}	t_{LZ}	2		2		ns
	$\overline{PE}$	t_{PLZ}	2		2		ns

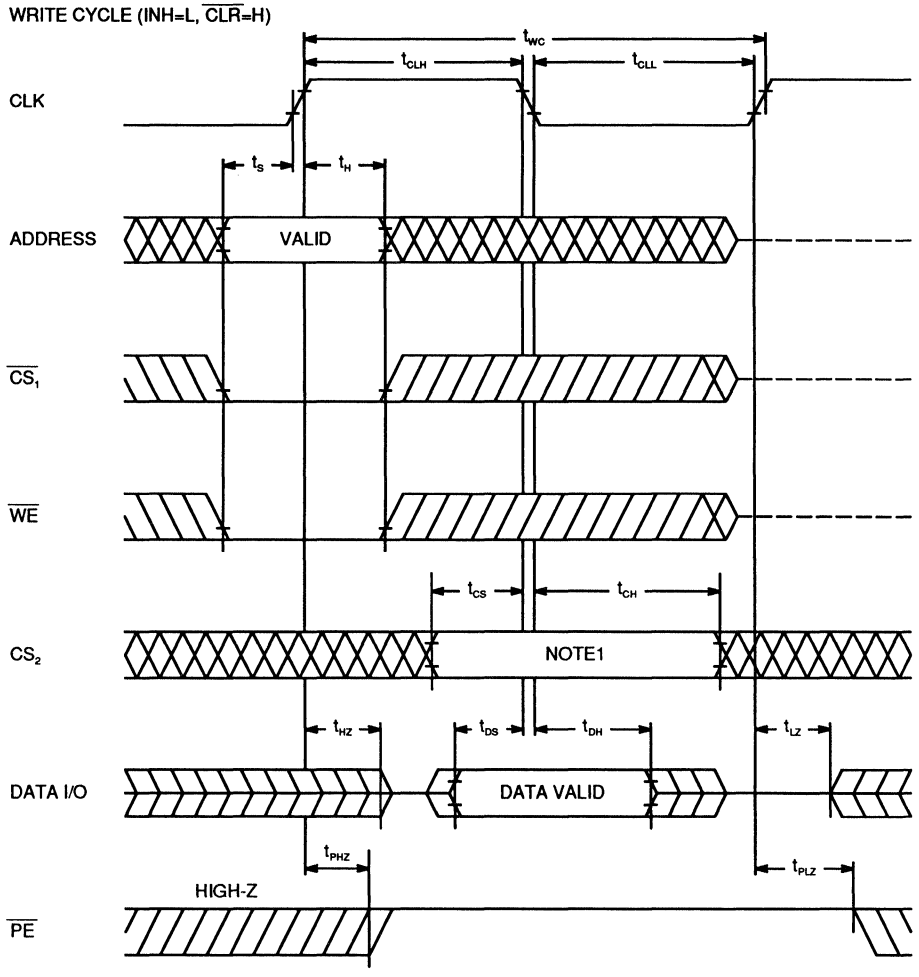
CLOCK INHIBIT TIMING

Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clock Inhibit Setup Time	t_{CLIS}	2		2		ns
Clock Inhibit Hold Time	t_{CLIH}	2		2		ns
Clock Enable Setup Time	t_{CLES}	2		2		ns
Clock Enable Hold Time	t_{CLEH}	0		0		ns

REGISTER CLEAR TIMING

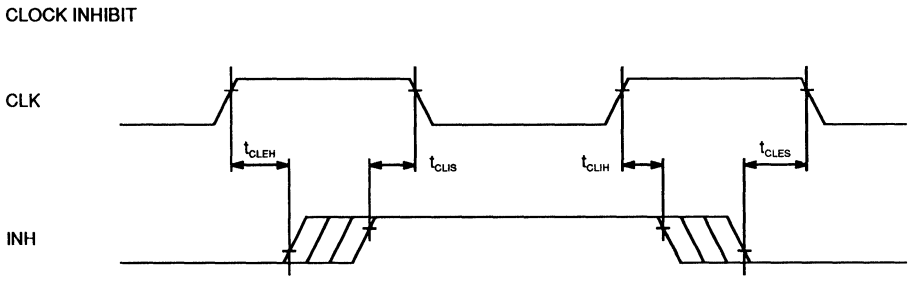
Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clear Pulse Width	t_{CRW}	7		7		ns
Clear Hold Time	t_{CRH}	10		10		ns
Clear Recovery Time	t_{CRR}	10		10		ns
Clear to Output High-Z	t_{CRHZ}	2	8	2	10	ns

WRITE CYCLE TIMING DIAGRAM

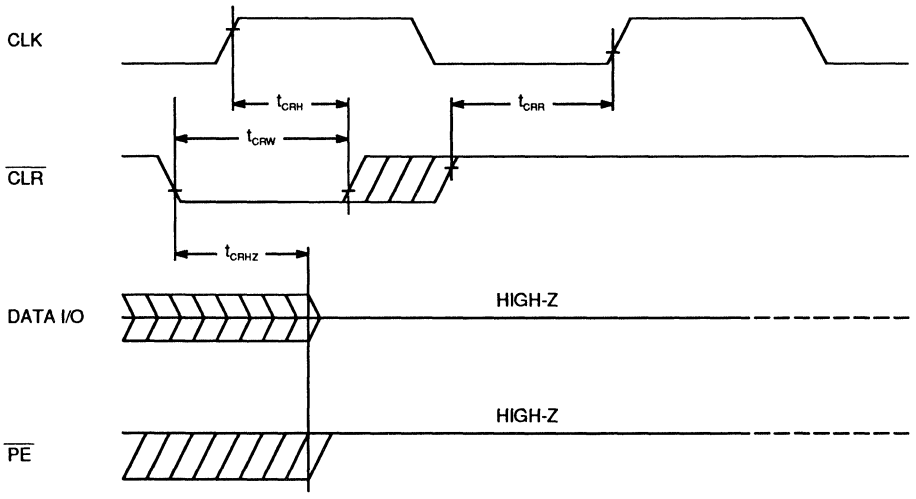


Note 1: When CS_2 = "H" level, write operation is excuted and when CS_2 = "L" level, write operation is cancelled.

CLOCK INHIBIT TIMING DIAGRAM



REGISTER CLEAR TIMING



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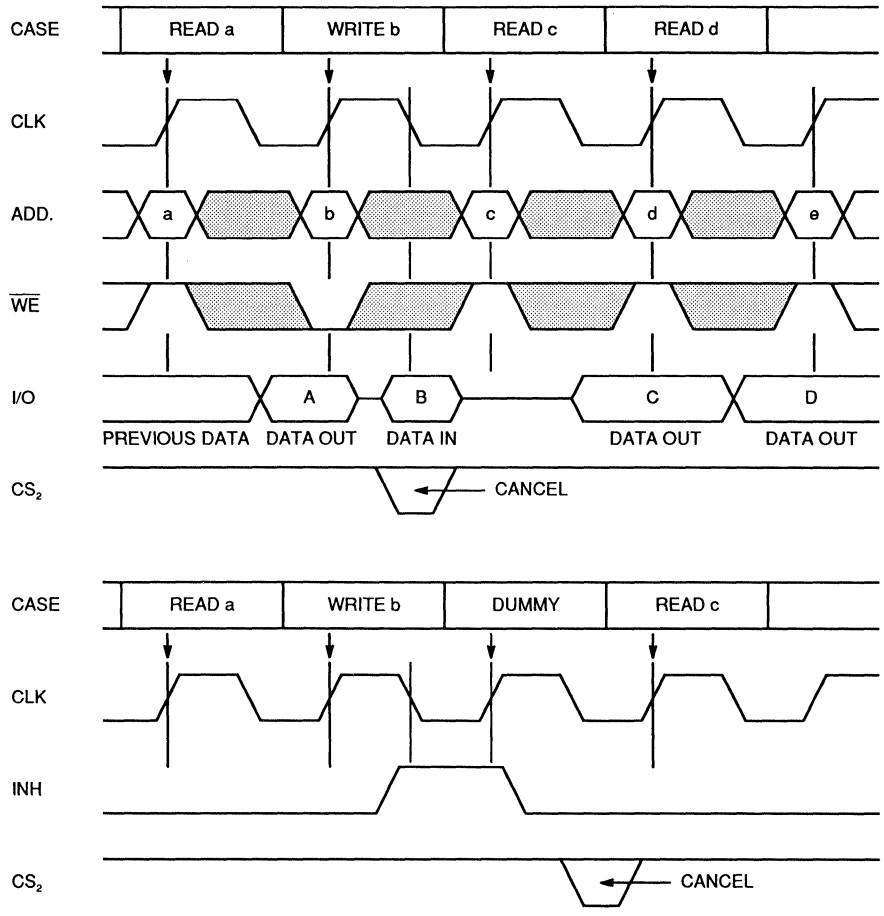
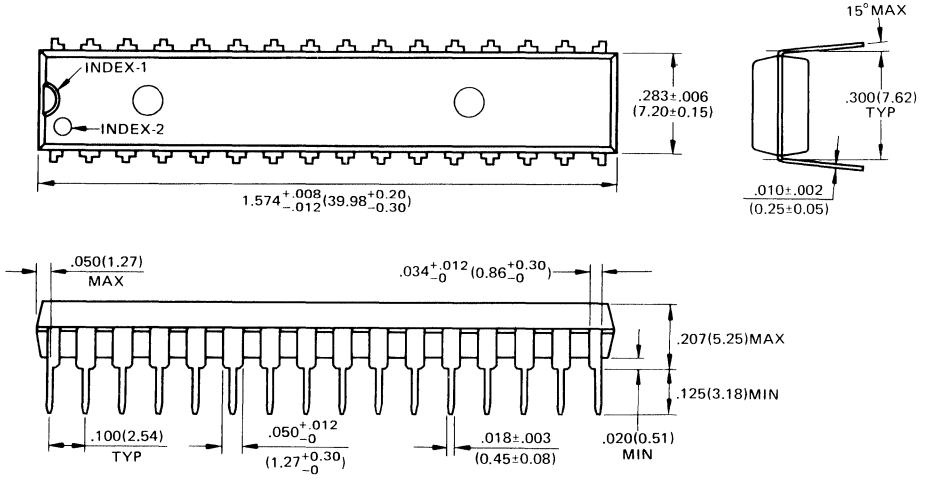
EXAMPLE OF MB8279RT BASIC FUNCTION



PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in
inches (millimeters)

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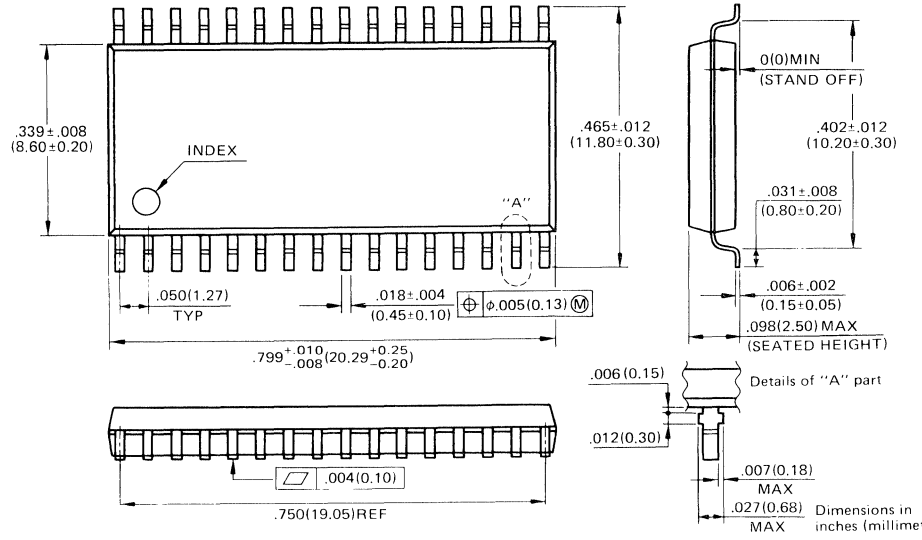
PACKAGE DIMENSIONS (Continued)

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M02)



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