FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10193-2E

*MEMORY*
**CMOS**
# 1 M × 16 BITS HYPER PAGE MODE DYNAMIC RAM

# MB81V18165A-60/60L/-70/70L

**CMOS 1,048,576 × 16 BITS Hyper Page Mode Dynamic RAM**



## ■ DESCRIPTION

The Fujitsu MB81V18165A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB81V18165A features a "hyper page" mode of operation whereby high-speed random access of up to 1,024 × 16 bits of data within the same row can be selected. The MB81V18165A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V18165A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V18165A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V18165A are not critical and all inputs are LVTTL compatible.

## ■ PRODUCT LINE & FEATURES

| Parameter | | | MB81V18165A | | | |
|---|---|---|---|---|---|---|
| | | | -60 | -60L | -70 | -70L |
| $\overline{RAS}$ Access Time | | | 60 ns max. | | 70 ns max. | |
| Random Cycle Time | | | 104 ns min. | | 124 ns min. | |
| Address Access Time | | | 30 ns max. | | 35 ns max. | |
| $\overline{CAS}$ Access Time | | | 15 ns max. | | 17 ns max. | |
| Hyper Page Mode Cycle Time | | | 25 ns min. | | 30 ns min. | |
| Low Power Dissipation | Operating Current | | 648 mW max. | | 612 mW max. | |
| | Standby Current | LVTTL Level | 3.6 mW max. | 3.6 mW max. | 3.6 mW max. | 3.6 mW max. |
| | | CMOS Level | 1.8 mW max. | 0.54 mW max. | 1.8 mW max. | 0.54 mW max. |

- 1,048,576 words × 16 bits organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 1,024 refresh cycles every 16.4 ms
- Self refresh function
- Standard and low power versions
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Hyper page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

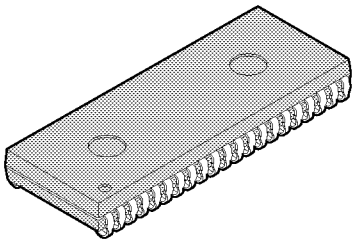
## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage at Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.5 to +4.6 | V |
| Voltage of $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +4.6 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Short Circuit Output Current | $I_{OUT}$ | –50 to +50 | mA |
| Operating Temperature | $T_{OPE}$ | 0 to +70 | °C |
| Storage Temperature | $T_{STG}$ | –55 to +125 | °C |

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

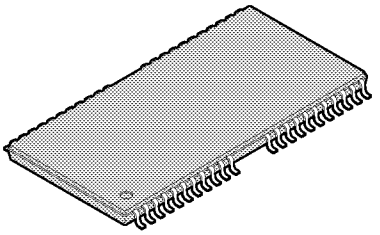
## ■ PACKAGE

Plastic SOJ Packaage



(LCC-42P-M01)

Plastic TSOP Package



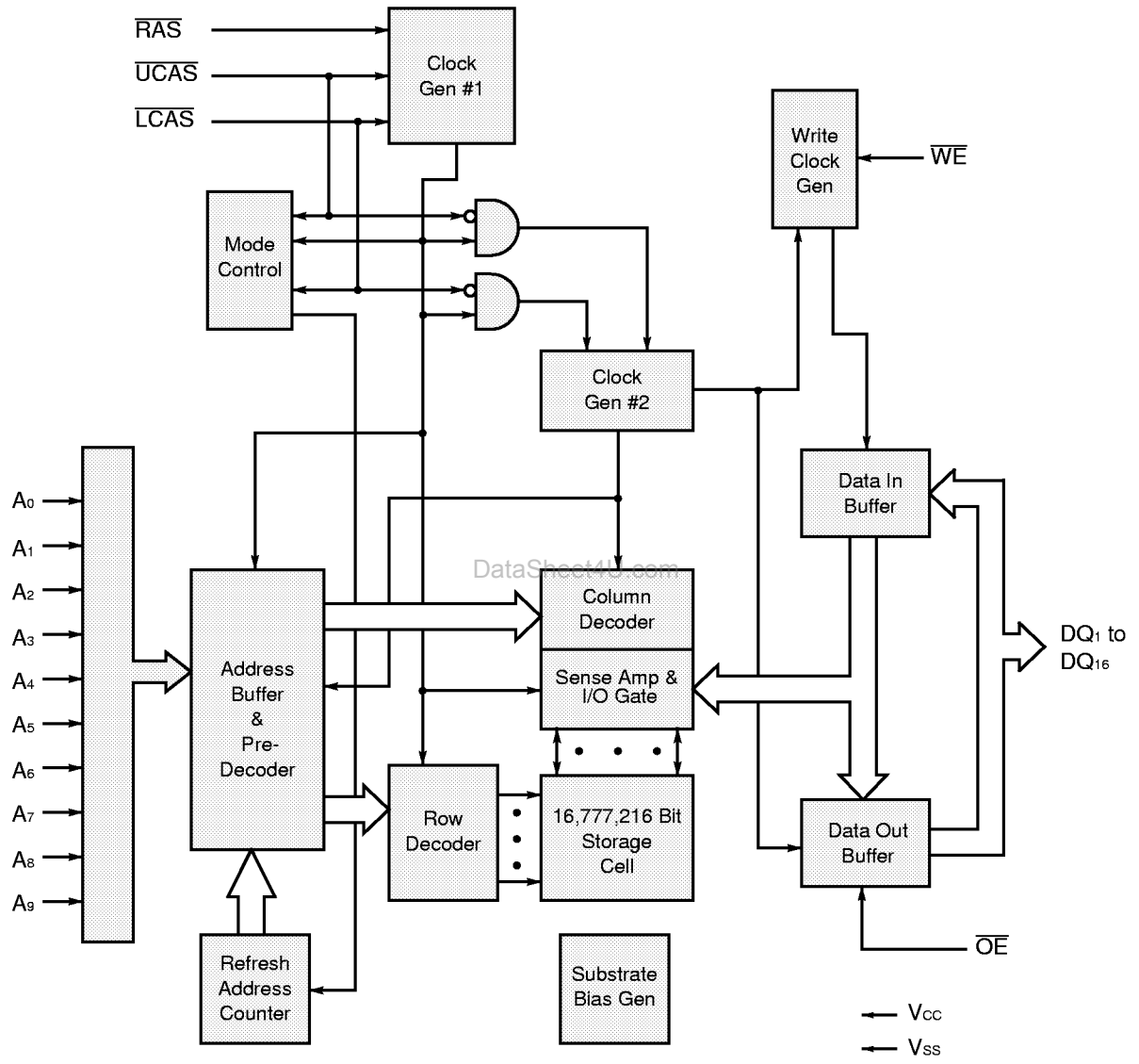
(FPT-50P-M06)
(Normal Bend)



### Package and Ordering Information

– 42-pin plastic (400 mil) SOJ,order as MB81V16165A-××PJ
– 50-pin plastic (400 mil) TSOP-II with normal bend leads,order as MB81V16165A-××PFTN and MB81V16165A-××LPFTN (Low Power)

**Fig. 1 – MB81V18165A DYNAMIC RAM - BLOCK DIAGRAM**



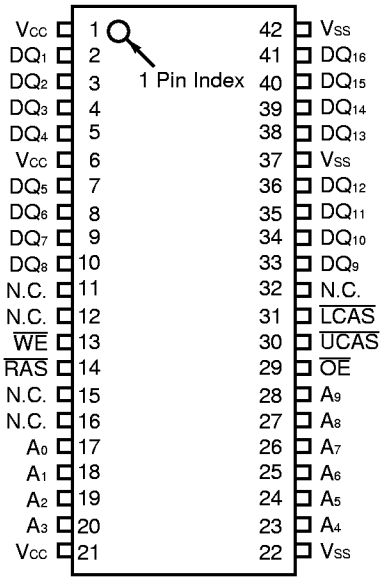

## ■ CAPACITANCE

($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Max. | Unit |
|---|---|---|---|
| Input Capacitance, $A_0$ to $A_9$ | $C_{IN1}$ | 5 | pF |
| Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$ | $C_{IN2}$ | 5 | pF |
| Input/Output Capacitance, $DQ_1$ to $DQ_{16}$ | $C_{DQ}$ | 7 | pF |

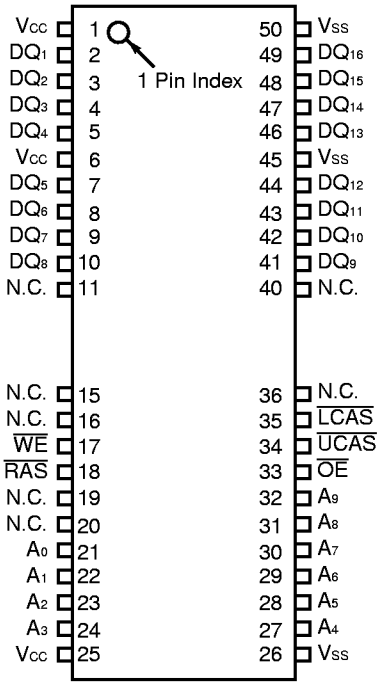
## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

42-Pin SOJ
(TOP VIEW)
<LCC-42P-M01>




| Designator | Function |
|---|---|
| $A_0$ to $A_9$ | Address inputs<br>row : $A_0$ to $A_9$<br>column : $A_0$ to $A_9$<br>refresh : $A_0$ to $A_9$ |
| $\overline{RAS}$ | Row address strobe |
| $\overline{LCAS}$ | Lower column address strobe |
| $\overline{UCAS}$ | Upper column address strobe |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $DQ_1$ to $DQ_{16}$ | Data Input/Output |
| $V_{CC}$ | +3.3 volt power supply |
| $V_{SS}$ | Circuit ground |
| N.C. | No connection |

50-Pin TSOP
(TOP VIEW)
<Normal Bend: FPT-50P-M06>



## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit | Ambient Operating Temp. |
|---|---|---|---|---|---|---|---|
| Supply Voltage | *1 | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 0°C to +70°C |
| | | $V_{SS}$ | 0 | 0 | 0 | | |
| Input High Voltage, all inputs | *1 | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | |
| Input Low Voltage, all inputs* | *1 | $V_{IL}$ | –0.3 | — | 0.8 | V | |

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only ten address bits ($A_0$ to $A_9$) are available, the column and row inputs are separately strobed by $\overline{LCAS}$ or $\overline{UCAS}$ and $\overline{RAS}$ as shown in Figure 1. First, ten row address bits are input on pins $A_0$-through-$A_9$ and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{LCAS}$ or $\overline{UCAS}$). Both row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after $t_{RAH}$ (min) + $t_T$ is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways: an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{LCAS}$/$\overline{UCAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of $DQ_1$ to $DQ_8$ is strobed by $\overline{LCAS}$ and $DQ_9$ to $DQ_{16}$ is strobed by $\overline{UCAS}$ and the setup/hold times are referenced to each $\overline{LCAS}$ and $\overline{UCAS}$ because $\overline{WE}$ goes Low before $\overline{LCAS}$/$\overline{UCAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{LCAS}$/$\overline{UCAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

- $t_{RAC}$ : from the falling edge of $\overline{RAS}$ when $t_{RCD}$ (max) is satisfied.
- $t_{CAC}$ : from the falling edge of $\overline{LCAS}$ (for $DQ_1$ to $DQ_8$) $\overline{UCAS}$ (for $DQ_9$ to $DQ_{16}$) when $t_{RCD}$ is greater than $t_{RCD}$ (max).
- $t_{AA}$ : from column address input when $t_{RAD}$ is greater than $t_{RAD}$ (max), and $t_{RCD}$ (max) is satisfied.
- $t_{OEA}$ : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$.
- $t_{OEZ}$ : from $\overline{OE}$ inactive.
- $t_{OFF}$ : from $\overline{CAS}$ inactive while $\overline{RAS}$ inactive.
- $t_{OFR}$ : from $\overline{RAS}$ inactive while $\overline{CAS}$ inactive.
- $t_{WEZ}$ : from $\overline{WE}$ active while $\overline{CAS}$ inactive.

The data remains valid after either $\overline{OE}$ is inactive, or both $\overline{RAS}$ and $\overline{LCAS}$ (and/or $\overline{UCAS}$) are inactive, or $\overline{CAS}$ is reactived. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## HYPER PAGE MODE OPERATION

The hyper page mode operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (within column address locations), any of $1,024 \times 16$-bits can be accessed and, when multiple MB81V18165As are used, $\overline{CAS}$ is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when $\overline{CAS}$ is inactive until $\overline{CAS}$ is reactivated.

## ■ DC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Note 3**

| Parameter | Notes | Symbol | Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| | | | | | | Std power | Low power | |
| Output high voltage | *1 | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | — | — | V |
| Output low voltage | *1 | $V_{OL}$ | $I_{OL}$ = +2.0 mA | — | — | 0.4 | 0.4 | V |
| Input leakage current (any input) | | $I_{I(L)}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$; 3.0 V ≤ $V_{CC}$ ≤ 3.6 V; $V_{SS}$ = 0 V; All other pins not under test = 0 V | –10 | — | 10 | 10 | µA |
| Output leakage current | | $I_{DO(L)}$ | 0 V ≤ $V_{OUT}$ ≤ $V_{CC}$; Data out disabled | –10 | — | 10 | 10 | µA |
| Operating current (Average power supply current) | *2 MB81V18165A-60/60L | $I_{CC1}$ | $\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; $t_{RC}$ = min | — | — | 180 | 180 | mA |
| | *2 MB81V18165A-70/70L | | | | | 170 | 170 | mA |
| Standby current (Power supply current) | LVTTL Level | $I_{CC2}$ | $\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = $V_{IH}$ | — | — | 1.0 | 1.0 | mA |
| | CMOS Level | | $\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ ≥ $V_{CC}$ –0.2 V | | | 0.5 | 150 | µA |
| Refresh current #1 (Average power supply current) | *2 MB81V18165A-60/60L | $I_{CC3}$ | $\overline{LCAS}$ = $\overline{UCAS}$ = $V_{IH}$, $\overline{RAS}$ cycling; $t_{RC}$ = min | — | — | 180 | 180 | mA |
| | *2 MB81V18165A-70/70L | | | | | 170 | 170 | mA |
| Hyper page mode current | *2 MB81V18165A-60/60L | $I_{CC4}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{LCAS}$ = $\overline{UCAS}$ cycling; $t_{HPC}$ = min | — | — | 110 | 110 | mA |
| | *2 MB81V18165A-70/70L | | | | | 100 | 100 | mA |
| Refresh current #2 (Average power supply current) | *2 MB81V18165A-60/60L | $I_{CC5}$ | $\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC}$ = min | — | — | 170 | 170 | mA |
| | *2 MB81V18165A-70/70L | | | | | 160 | 160 | mA |
| Battery back up current (Average power supply current) | *2 MB81V18165A-60 | $I_{CC6}$ | $\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC}$ = 16 µs; $t_{RAS}$ = min to 300 ns; $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, $V_{IL}$ ≤ 0.2 V | — | — | 2000 | — | µA |
| | *2 MB81V18165A-70 | | | | | | | |
| | *2 MB81V18165A-60L | | $\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC}$ = 128 µs; $t_{RAS}$ = min to 300 ns; $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, $V_{IL}$ ≤ 0.2 V | — | — | — | 300 | µA |
| | *2 MB81V18165A-70L | | | | | | | |
| Refresh current #3 (Average power supply current) | MB81V18165A-60/60L | $I_{CC9}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ = $V_{IL}$ Self refresh; | — | — | 1000 | 250 | µA |
| | MB81V18165A-70/70L | | | | | | | |

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB81V18165A-60/60L | | MB81V18165A-70/70L | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 1 | Time Between Refresh | Standard | $t_{REF}$ | — | 16.4 | — | 16.4 | ms |
| | | Low power | | — | 128 | — | 128 | |
| 2 | Random Read/Write Cycle Time | | $t_{RC}$ | 104 | — | 124 | — | ns |
| 3 | Read-Modify-Write Cycle Time | | $t_{RWC}$ | 138 | — | 162 | — | ns |
| 4 | Access Time from $\overline{RAS}$ | *6,9 | $t_{RAC}$ | — | 60 | — | 70 | ns |
| 5 | Access Time from $\overline{CAS}$ | *7,9 | $t_{CAC}$ | — | 15 | — | 17 | ns |
| 6 | Column Address Access Time | *8,9 | $t_{AA}$ | — | 30 | — | 35 | ns |
| 7 | Output Hold Time | | $t_{OH}$ | 3 | — | 3 | — | ns |
| 8 | Output Hold Time from $\overline{CAS}$ | | $t_{OHC}$ | 5 | — | 5 | — | ns |
| 9 | Output Buffer Turn On Delay Time | | $t_{ON}$ | 0 | — | 0 | — | ns |
| 10 | Output Buffer Turn Off Delay Time | *10 | $t_{OFF}$ | — | 15 | — | 17 | ns |
| 11 | Output Buffer Turn Off Delay Time from $\overline{RAS}$ | *10 | $t_{OFR}$ | — | 15 | — | 17 | ns |
| 12 | Output Buffer Turn Off Delay Time from $\overline{WE}$ | *10 | $t_{WEZ}$ | — | 15 | — | 17 | ns |
| 13 | Transition Time | | $t_T$ | 1 | 50 | 1 | 50 | ns |
| 14 | $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 40 | — | 50 | — | ns |
| 15 | $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 60 | 100000 | 70 | 100000 | ns |
| 16 | $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 15 | — | 17 | — | ns |
| 17 | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | *21 | $t_{CRP}$ | 5 | — | 5 | — | ns |
| 18 | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | *11,12,22 | $t_{RCD}$ | 14 | 45 | 14 | 53 | ns |
| 19 | $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 10 | — | 13 | — | ns |
| 20 | $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 40 | — | 50 | — | ns |
| 21 | $\overline{CAS}$ Precharge Time (Normal) | *19 | $t_{CPN}$ | 10 | — | 10 | — | ns |
| 22 | Row Address Set Up Time | | $t_{ASR}$ | 0 | — | 0 | — | ns |
| 23 | Row Address Hold Time | | $t_{RAH}$ | 10 | — | 10 | — | ns |
| 24 | Column Address Set Up Time | | $t_{ASC}$ | 0 | — | 0 | — | ns |
| 25 | Column Address Hold Time | | $t_{CAH}$ | 10 | — | 10 | — | ns |
| 26 | Column Address Hold Time from $\overline{RAS}$ | | $t_{AR}$ | 24 | — | 24 | — | ns |
| 27 | $\overline{RAS}$ to Column Address Delay Time | *13 | $t_{RAD}$ | 12 | 30 | 12 | 35 | ns |
| 28 | Column Address to $\overline{RAS}$ Lead Time | | $t_{RAL}$ | 30 | — | 35 | — | ns |
| 29 | Column Address to $\overline{CAS}$ Lead Time | | $t_{CAL}$ | 23 | — | 28 | — | ns |
| 30 | Read Command Set Up Time | | $t_{RCS}$ | 0 | — | 0 | — | ns |

*(Continued)*

| No. | Parameter | Notes | Symbol | MB81V18165A-60/60L | | MB81V18165A-70/70L | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 31 | Read Command Hold Time Referenced to $\overline{RAS}$ | *14 | $t_{RRH}$ | 0 | — | 0 | — | ns |
| 32 | Read Command Hold Time Referenced to $\overline{CAS}$ | *14 | $t_{RCH}$ | 0 | — | 0 | — | ns |
| 33 | Write Command Set Up Time | *15,20 | $t_{WCS}$ | 0 | — | 0 | — | ns |
| 34 | Write Command Hold Time | | $t_{WCH}$ | 10 | — | 10 | — | ns |
| 35 | Write Hold Time from $\overline{RAS}$ | | $t_{WCR}$ | 24 | — | 24 | — | ns |
| 36 | $\overline{WE}$ Pulse Width | | $t_{WP}$ | 10 | — | 10 | — | ns |
| 37 | Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 15 | — | 17 | — | ns |
| 38 | Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 10 | — | 13 | — | ns |
| 39 | DIN Set Up Time | | $t_{DS}$ | 0 | — | 0 | — | ns |
| 40 | DIN Hold Time | | $t_{DH}$ | 10 | — | 10 | — | ns |
| 41 | Data Hold Time from $\overline{RAS}$ | | $t_{DHR}$ | 24 | — | 24 | — | ns |
| 42 | $\overline{RAS}$ to $\overline{WE}$ Delay Time | *20 | $t_{RWD}$ | 77 | — | 89 | — | ns |
| 43 | $\overline{CAS}$ to $\overline{WE}$ Delay Time | *20 | $t_{CWD}$ | 32 | — | 36 | — | ns |
| 44 | Column Address to $\overline{WE}$ Delay Time | *20 | $t_{AWD}$ | 47 | — | 54 | — | ns |
| 45 | $\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles) | | $t_{RPC}$ | 5 | — | 5 | — | ns |
| 46 | $\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CSR}$ | 0 | — | 0 | — | ns |
| 47 | $\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CHR}$ | 10 | — | 12 | — | ns |
| 48 | Access Time from $\overline{OE}$ | *9 | $t_{OEA}$ | — | 15 | — | 17 | ns |
| 49 | Output Buffer Turn Off Delay from $\overline{OE}$ | *10 | $t_{OEZ}$ | — | 15 | — | 17 | ns |
| 50 | $\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data | | $t_{OEL}$ | 10 | — | 10 | — | ns |
| 51 | $\overline{OE}$ to $\overline{CAS}$ Lead Time | | $t_{COL}$ | 5 | — | 5 | — | ns |
| 52 | $\overline{OE}$ Hold Time Referenced to $\overline{WE}$ | *16 | $t_{OEH}$ | 5 | — | 5 | — | ns |
| 53 | $\overline{OE}$ to Data In Delay Time | | $t_{OED}$ | 15 | — | 17 | — | ns |
| 54 | $\overline{RAS}$ to Data In Delay Time | | $t_{RDD}$ | 15 | — | 17 | — | ns |
| 55 | $\overline{CAS}$ to Data In Delay Time | | $t_{CDD}$ | 15 | — | 17 | — | ns |
| 56 | DIN to $\overline{CAS}$ Delay Time | *17 | $t_{DZC}$ | 0 | — | 0 | — | ns |
| 57 | DIN to $\overline{OE}$ Delay Time | *17 | $t_{DZO}$ | 0 | — | 0 | — | ns |
| 58 | $\overline{OE}$ Precharge Time | | $t_{OEP}$ | 8 | — | 8 | — | ns |
| 59 | $\overline{OE}$ Hold Time Referenced to $\overline{CAS}$ | | $t_{OECH}$ | 10 | — | 10 | — | ns |
| 60 | $\overline{WE}$ Precharge Time | | $t_{WPZ}$ | 8 | — | 8 | — | ns |

(Continued)

*(Continued)*

| No. | Parameter | Notes | Symbol | MB81V18165A-60/60L | | MB81V18165A-70/70L | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 61 | $\overline{WE}$ to Data In Delay Time | | $t_{WED}$ | 15 | — | 17 | — | ns |
| 62 | Hyper Page Mode $\overline{RAS}$ Pulse Width | | $t_{RASP}$ | — | 100000 | — | 100000 | ns |
| 63 | Hyper Page Mode Read/Write Cycle Time | | $t_{HPC}$ | 25 | — | 30 | — | ns |
| 64 | Hyper Page Mode Read-Modify-Write Cycle Time | | $t_{HPRWC}$ | 69 | — | 79 | — | ns |
| 65 | Access Time from $\overline{CAS}$ Precharge | *9,18 | $t_{CPA}$ | — | 35 | — | 40 | ns |
| 66 | Hyper Page Mode $\overline{CAS}$ Precharge Time | | $t_{CP}$ | 10 | — | 10 | — | ns |
| 67 | Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | | $t_{RHCP}$ | 35 | — | 40 | — | ns |
| 68 | Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | *20 | $t_{CPWD}$ | 52 | — | 59 | — | ns |

Notes: *1. Referenced to $V_{SS}$.

*2. $I_{CC}$ depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
$I_{CC}$ depends on the number of address change as $\overline{RAS}$ = $V_{IL}$, $\overline{UCAS}$ = $V_{IH}$, $\overline{LCAS}$ = $V_{IH}$ and $V_{IL}$ > –0.3 V.
$I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC5}$ are specified at one time of address change during $\overline{RAS}$ = $V_{IL}$ and $\overline{UCAS}$ = $V_{IH}$, $\overline{LCAS}$ = $V_{IH}$.
$I_{CC2}$ is specified during $\overline{RAS}$ = $V_{IH}$ and $V_{IL}$ > –0.3 V.
$I_{CC6}$ is measured on condition that all address signals are fixed steady state.

*3. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*4. AC characteristics assume $t_T$ = 2 ns.

*5. Input voltage levels are 0 V and 3.0 V, and input reference levels are $V_{IH}$ (min) and $V_{IL}$ (max) for measuring timing of input signals. Also, the transition time ($t_T$) is measured between $V_{IH}$ (min) and $V_{IL}$ (max).
The output reference levels are $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.

*6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will be increased by the amount that $t_{RCD}$ exceeds the value shown. Refer to Fig.2 and 3.

*7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is $t_{CAC}$.

*8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is $t_{AA}$.

*9. Measured with a load equivalent to one TTL load and 100 pF.

*10. $t_{OFF}$, $t_{OFR}$, $t_{WEZ}$ and $t_{OEZ}$ are specified that output buffer change to high impedance state.

*11. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.

*12. $t_{RCD}$ (min) = $t_{RAH}$ (min) + 2$t_T$ + $t_{ASC}$ (min).

*13. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.

*14. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.

*15. $t_{WCS}$ is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*16. Assumes that $t_{WCS} < t_{WCS}$ (min).

*17. Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.

*18. $t_{CPA}$ is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$ and $\overline{LCAS}$ from "L" to "H"). Therefore, if $t_{CP}$ is long, $t_{CPA}$ is longer than $t_{CPA}$ (max).

*19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*20. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and $D_{OUT}$ pin will maintain high-impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPWD} \geq t_{CPWD}$ (min) the cycle is a read-modify-write cycle and data from the selected cell will appear at the $D_{OUT}$ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the $D_{OUT}$ pin, and write operation can be executed by satisfying $t_{RWL}$, $t_{CWL}$, and $t_{RAL}$ specifications.

*21. The last $\overline{CAS}$ rising edge.

*22. The first $\overline{CAS}$ falling edge.

Fig. 2 – $t_{RAC}$ vs. $t_{RCD}$

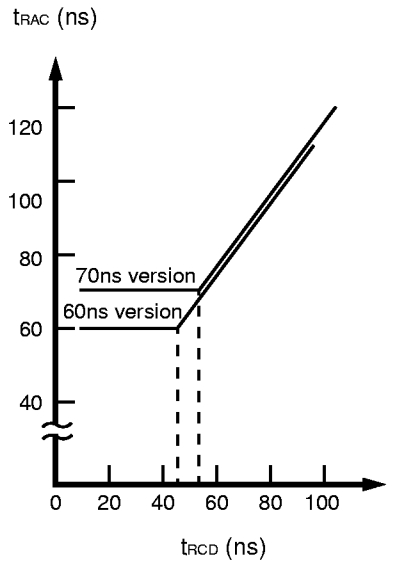



Fig. 3 – $t_{RAC}$ vs. $t_{RAD}$

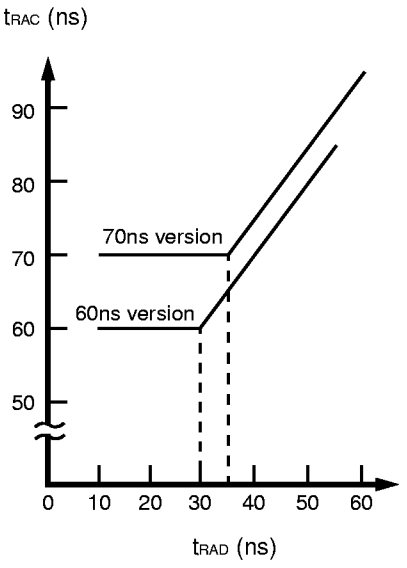
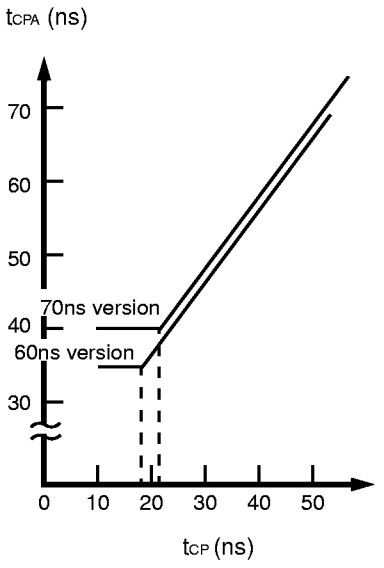



Fig. 4 – $t_{CPA}$ vs. $t_{CP}$





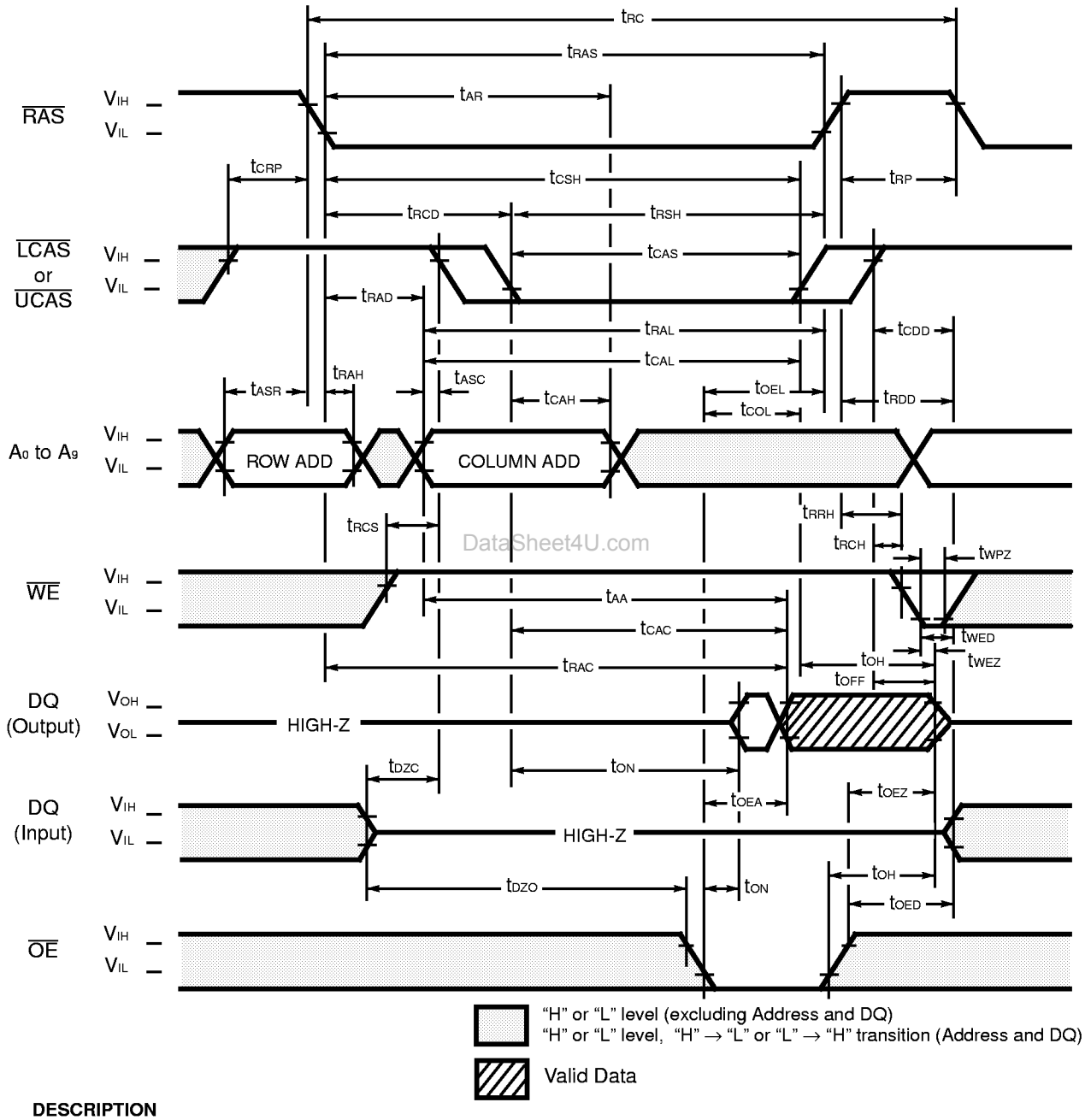

## ■ FUNCTIONAL TRUTH TABLE



| Operation Mode | Clock Input | | | | | Address Input | | Input/Output Data | | | | Refresh | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | $DQ_1$ to $DQ_8$ | | $DQ_9$ to $DQ_{16}$ | | | |
| | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Row | Column | Input | Output | Input | Output | | |
| Standby | H | H | H | X | X | — | — | — | High-Z | — | High-Z | — | |
| Read Cycle | L | L<br>H<br>L | H<br>L<br>L | H | L | Valid | Valid | — | Valid<br>High-Z<br>Valid | — | High-Z<br>Valid<br>Valid | Yes* | $t_{RCS} \geq t_{RCS}$ (min) |
| Write Cycle (Early Write) | L | L<br>H<br>L | H<br>L<br>L | L | X | Valid | Valid | Valid<br>—<br>Valid | High-Z | —<br>Valid<br>Valid | High-Z | Yes* | $t_{WCS} \geq t_{WCS}$ (min) |
| Read-Modify-Write Cycle | L | L<br>H<br>L | H<br>L<br>L | H→L | L→H | Valid | Valid | Valid<br>—<br>Valid | Valid<br>High-Z<br>Valid | —<br>Valid<br>Valid | High-Z<br>Valid<br>Valid | Yes* | |
| $\overline{RAS}$-only Refresh Cycle | L | H | H | X | X | Valid | — | — | High-Z | — | High-Z | Yes | |
| $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle | L | L | L | X | X | — | — | — | High-Z | — | High-Z | Yes | $t_{CSR} \geq t_{CSR}$ (min) |
| Hidden Refresh Cycle | H→L | L<br>H<br>L | H<br>L<br>L | H→X | L | — | — | — | Valid<br>High-Z<br>Valid | — | High-Z<br>Valid<br>Valid | Yes | Previous data is kept |

X: "H" or "L"
*: It is impossible in Hyper Page Mode.

## Fig. 5 – READ CYCLE




**DESCRIPTION**

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. DQ pins are valid when $\overline{RAS}$ and $\overline{CAS}$ are High or until $\overline{OE}$ goes High. The access time is determined by $\overline{RAS}$ ($t_{RAC}$), $\overline{LCAS}$/$\overline{UCAS}$ ($t_{CAC}$), $\overline{OE}$ ($t_{OEA}$) or column addresses ($t_{AA}$) under the following conditions:

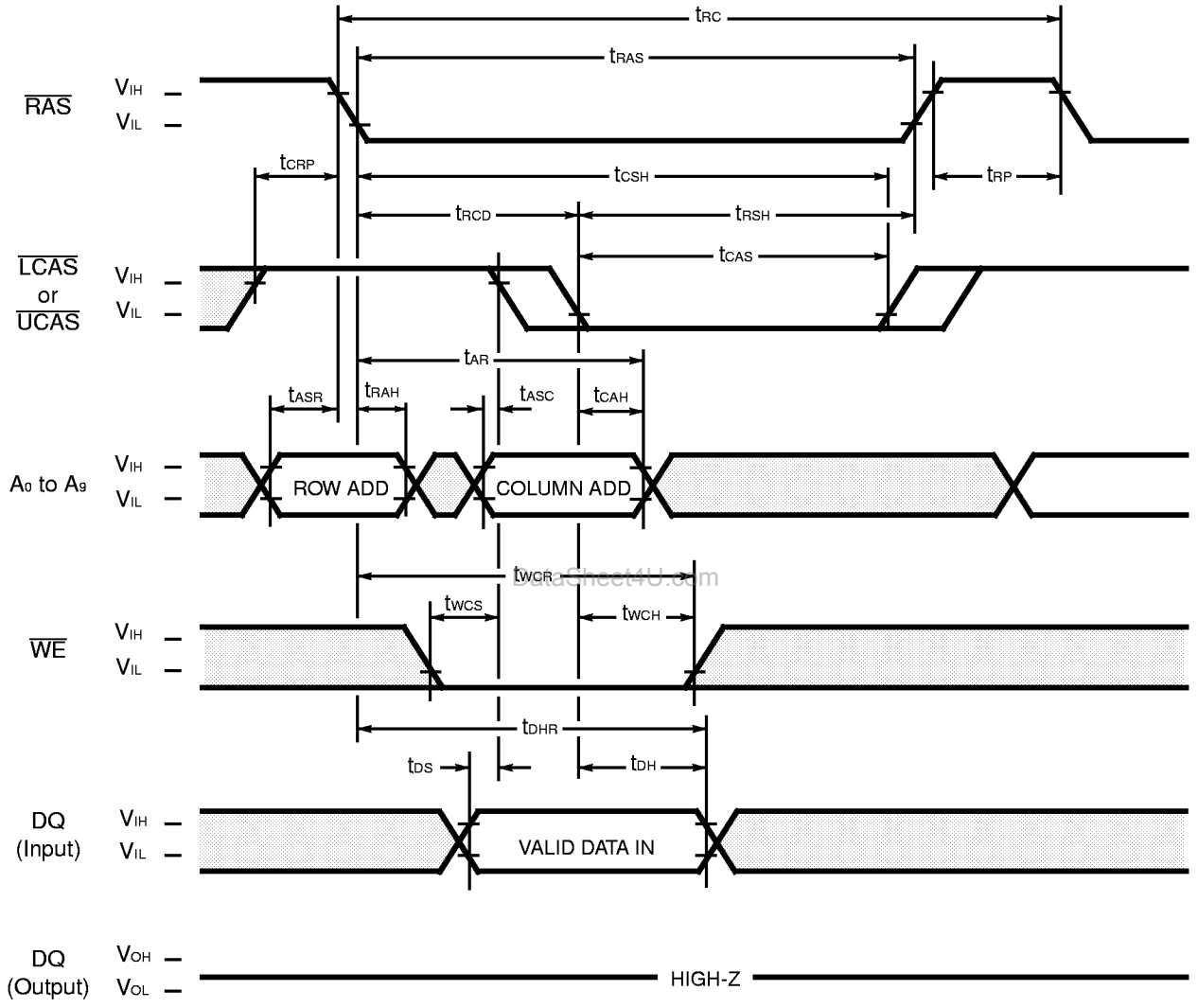
If $t_{RCD} > t_{RCD}$ (max), access time = $t_{CAC}$.

If $t_{RAD} > t_{RAD}$ (max), access time = $t_{AA}$.

If $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$ (whichever occurs later), access time = $t_{OEA}$.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after $t_{OH}$ is satisfied.

## Fig. 6 – EARLY WRITE CYCLE

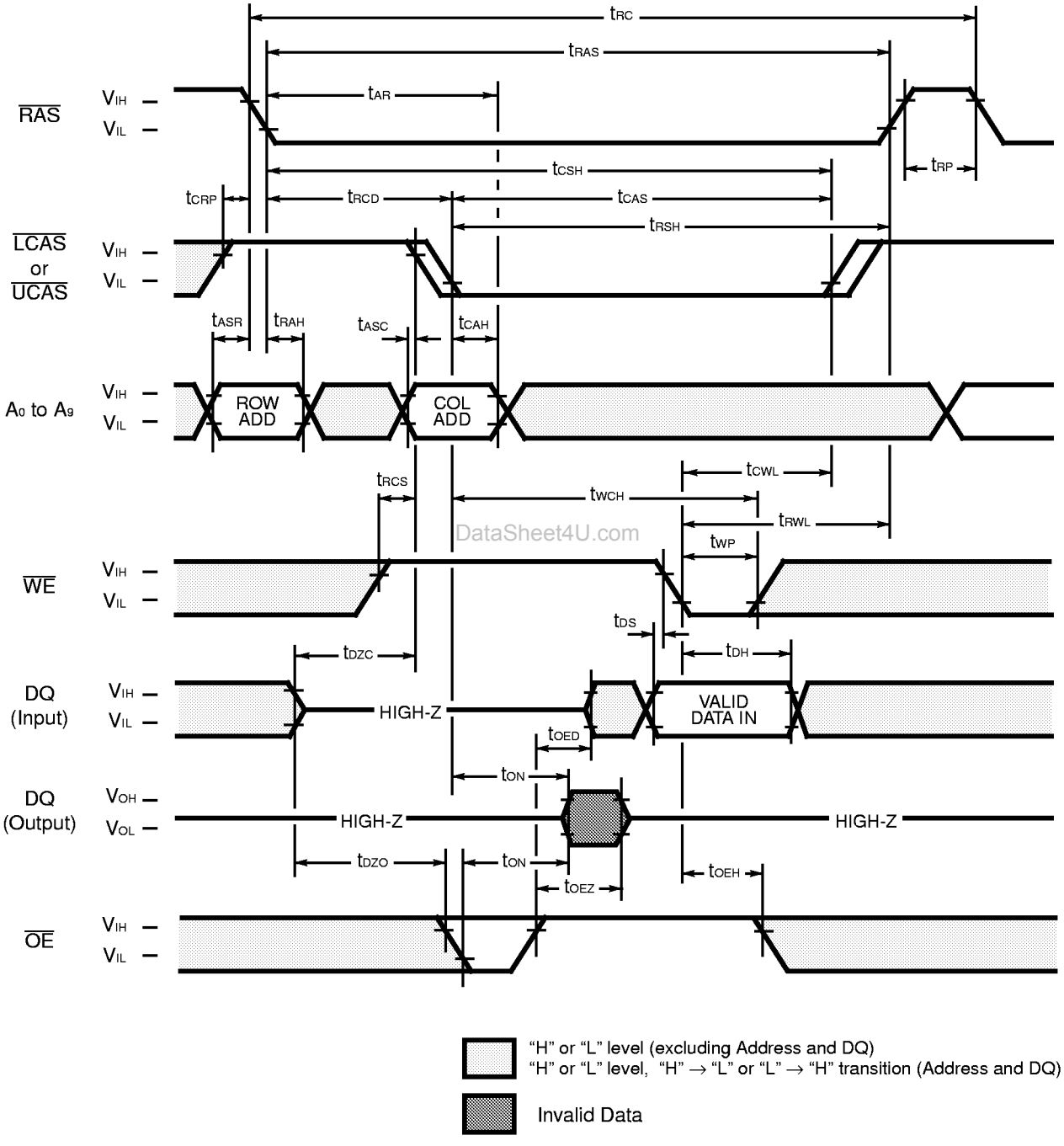



"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

**DESCRIPTION**

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters $t_{RWL}$, $t_{CWL}$, $t_{RAL}$ and $t_{CAL}$ must be satisfied. In the early write cycle shown above $t_{WCS}$ satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

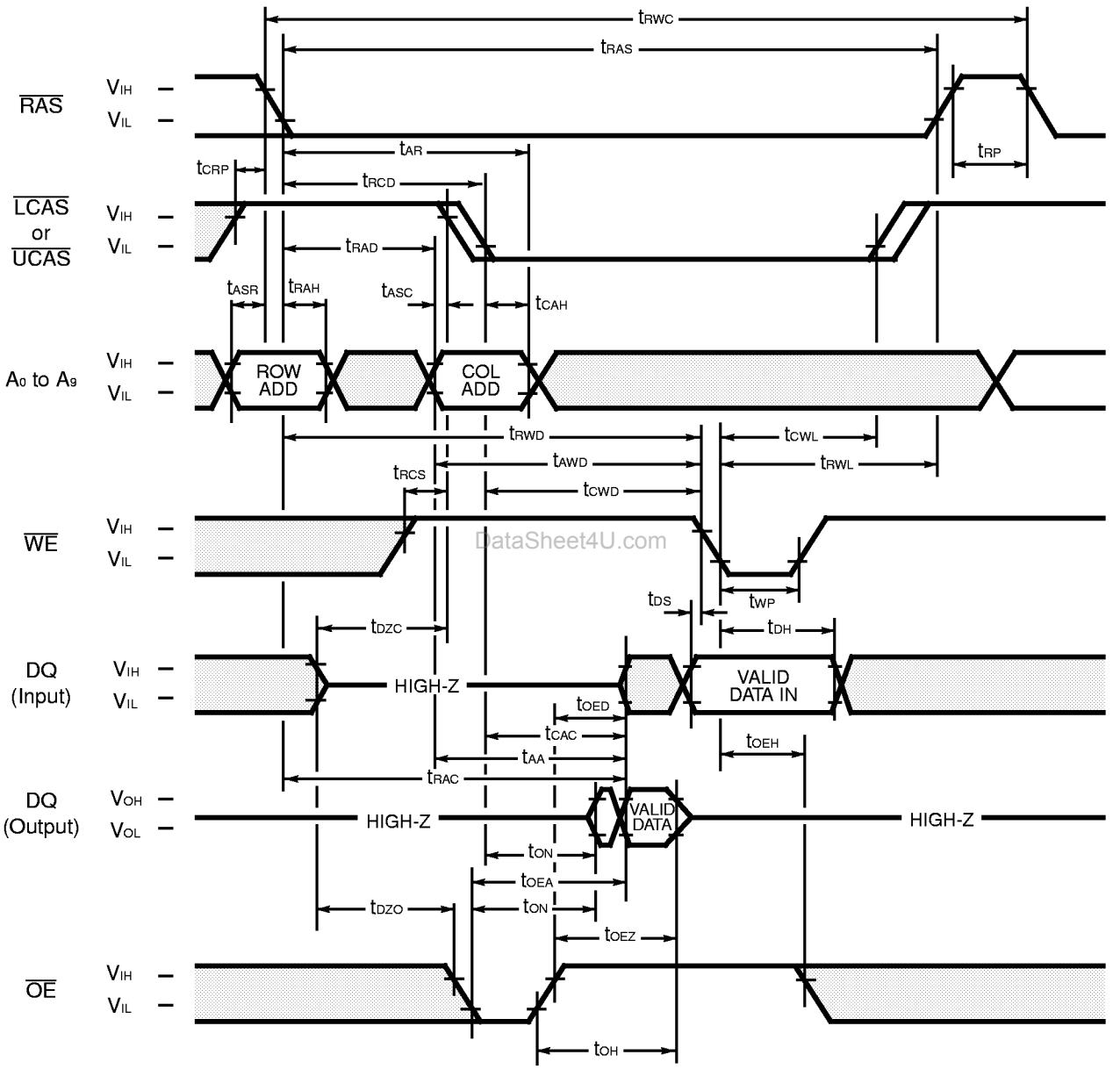
## Fig. 7 – DELAYED WRITE CYCLE ($\overline{OE}$ CONTROLLED)




**DESCRIPTION**

In the delayed write cycle, $t_{WCS}$ is not satisfied; thus, the data on the DQ pins are latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

## Fig. 8 – READ-MODIFY-WRITE CYCLE

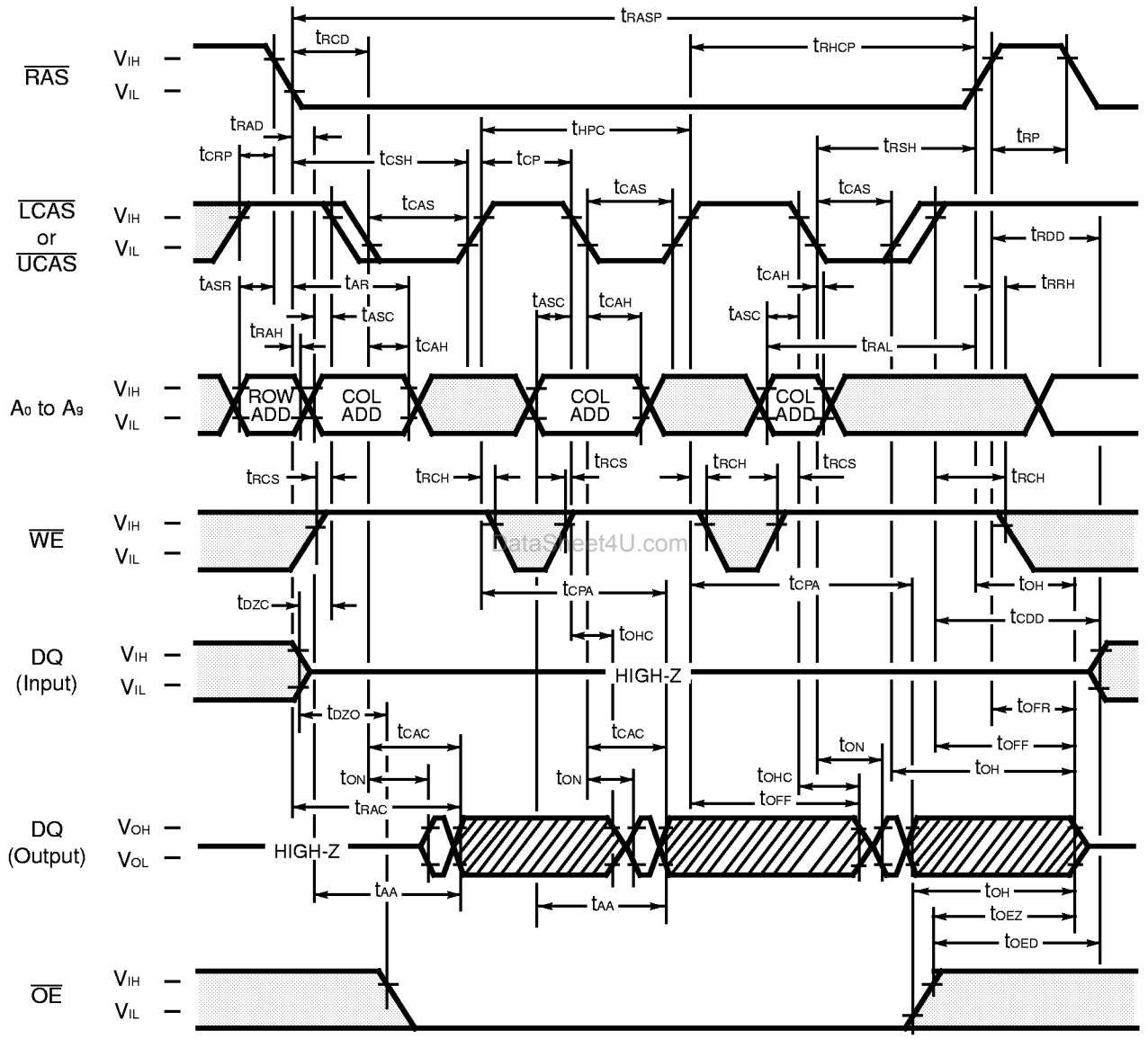



"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

**DESCRIPTION**

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

## Fig. 9 – HYPER PAGE MODE READ CYCLE




During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

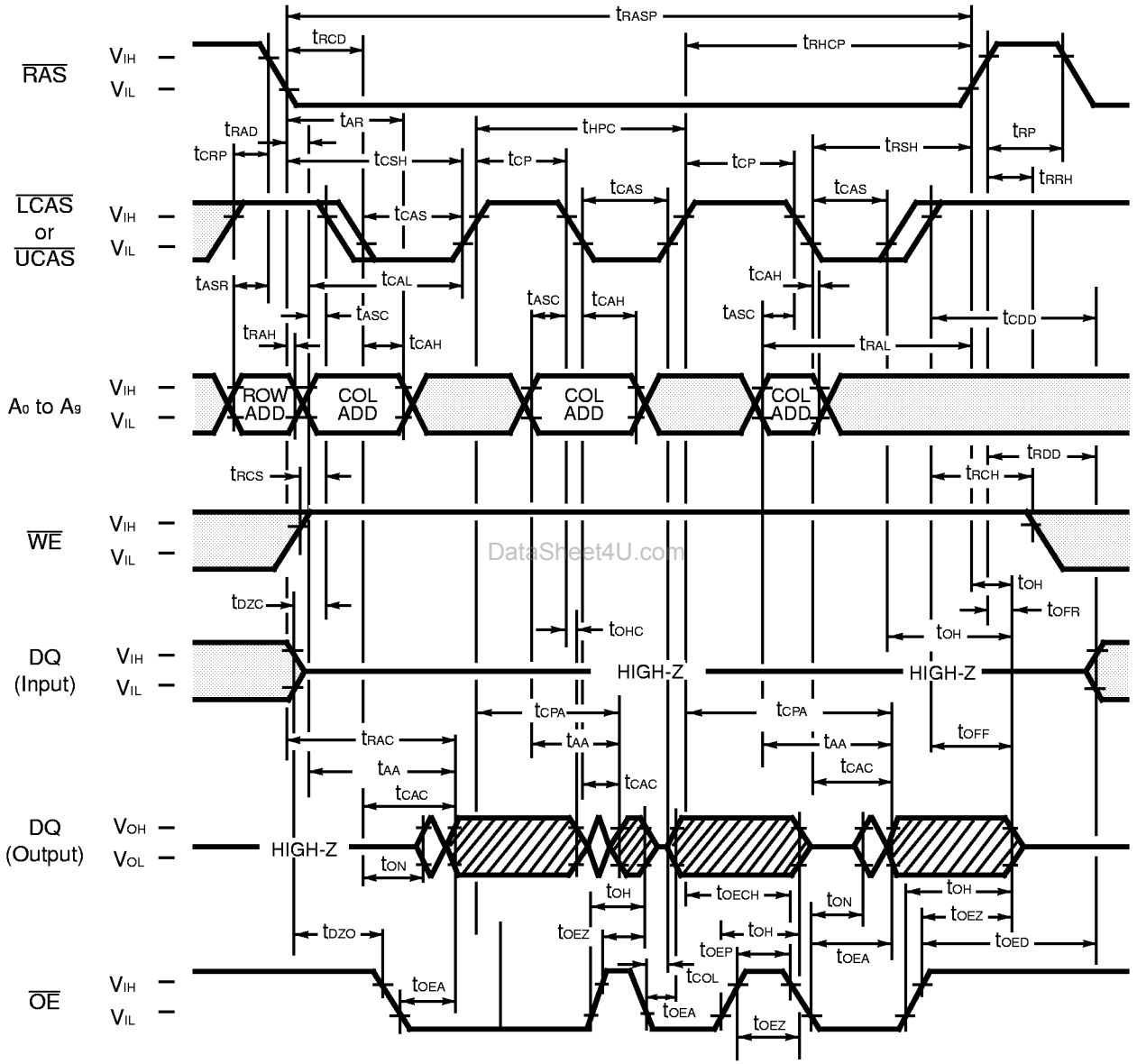
"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

Valid Data

**DESCRIPTION**

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

**Fig. 10 – HYPER PAGE MODE READ CYCLE ($\overline{OE}$ = "H" or "L")**




During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

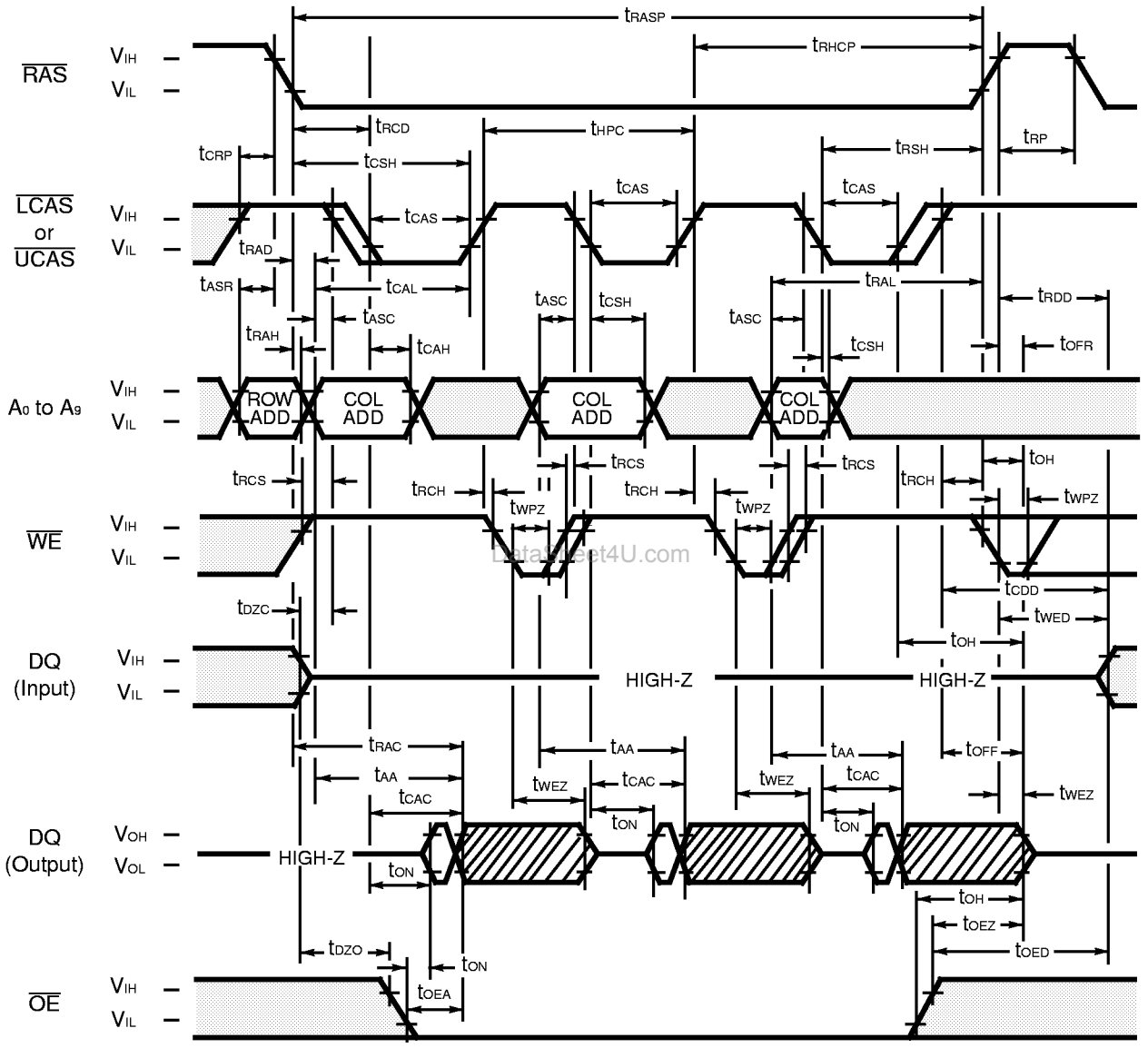
"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

Valid Data

**DESCRIPTION**

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

**Fig. 11 – HYPER PAGE MODE READ CYCLE ($\overline{WE}$ = "H" or "L")**



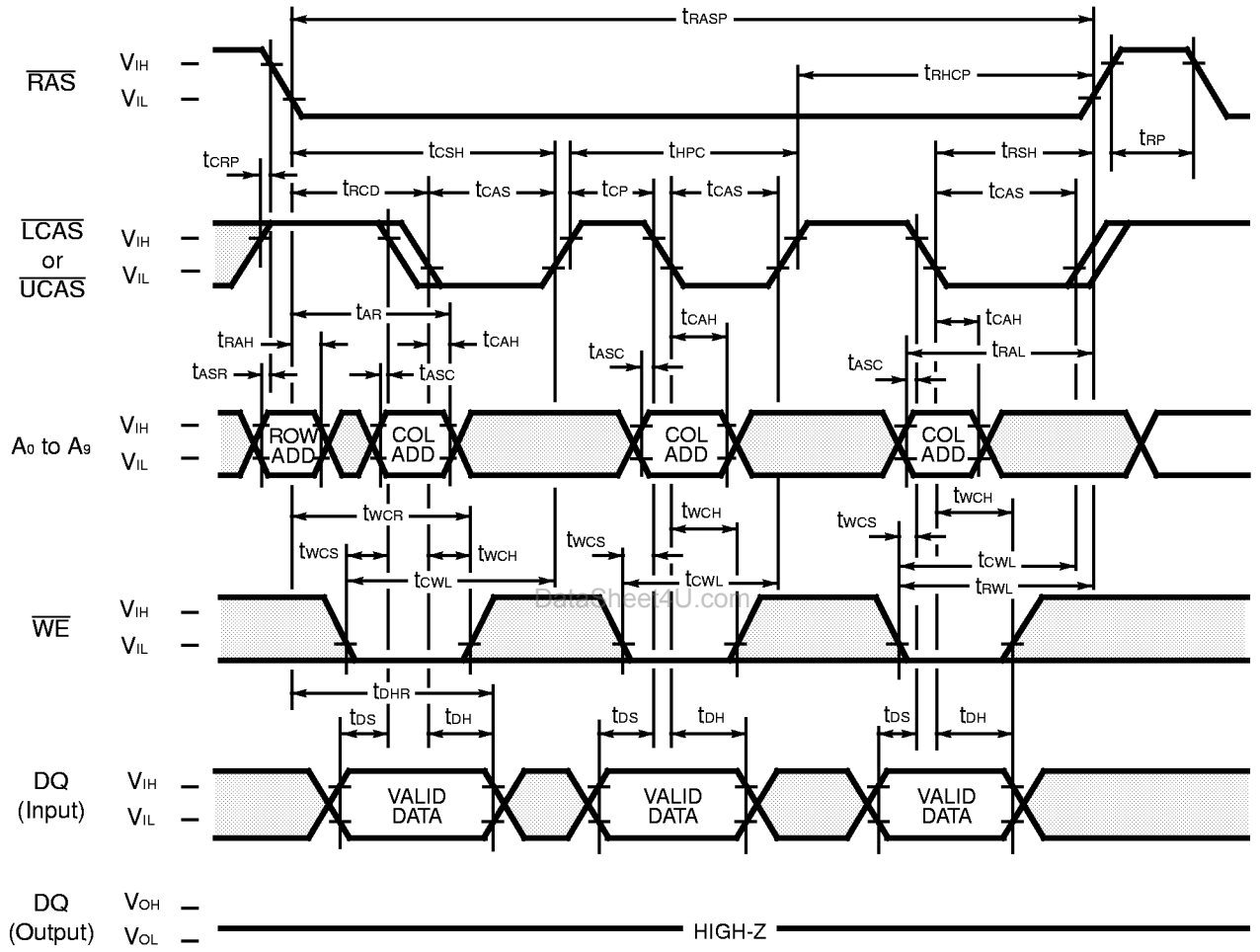

During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)
Valid Data

**DESCRIPTION**

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

**Fig. 12 – HYPER PAGE MODE EARLY WRITE CYCLE**



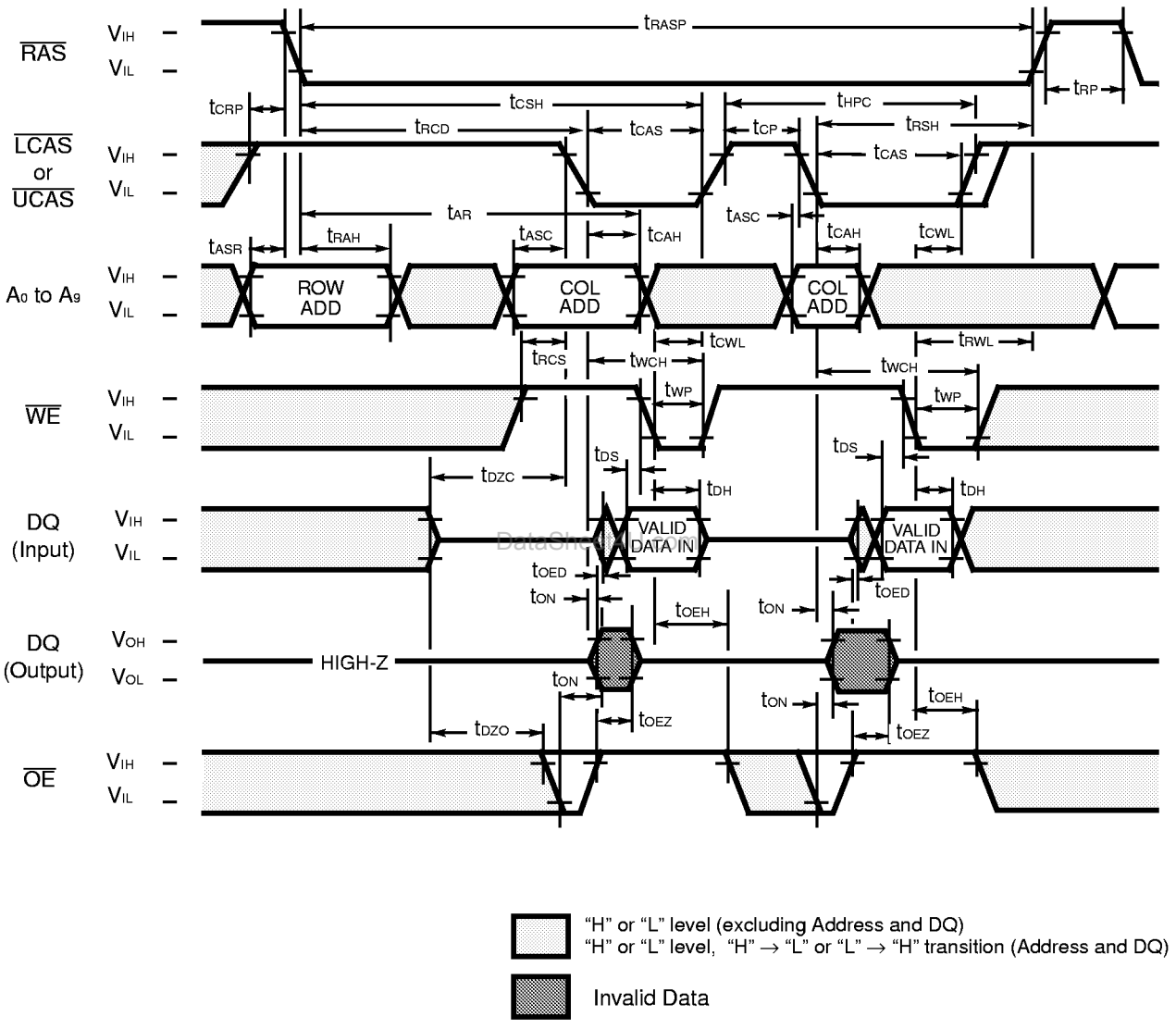

During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

**DESCRIPTION**

The hyper page mode early write cycle is executed in the same manner as the hyper page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the $DQ_1$ to $DQ_8$ is latched on the falling edge of $\overline{LCAS}$ and one appearing on the $DQ_9$ to $DQ_{16}$ is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the hyper page mode early write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, $t_{CWL}$ must be satisfied.

## Fig. 13 – HYPER PAGE MODE DELAYED WRITE CYCLE



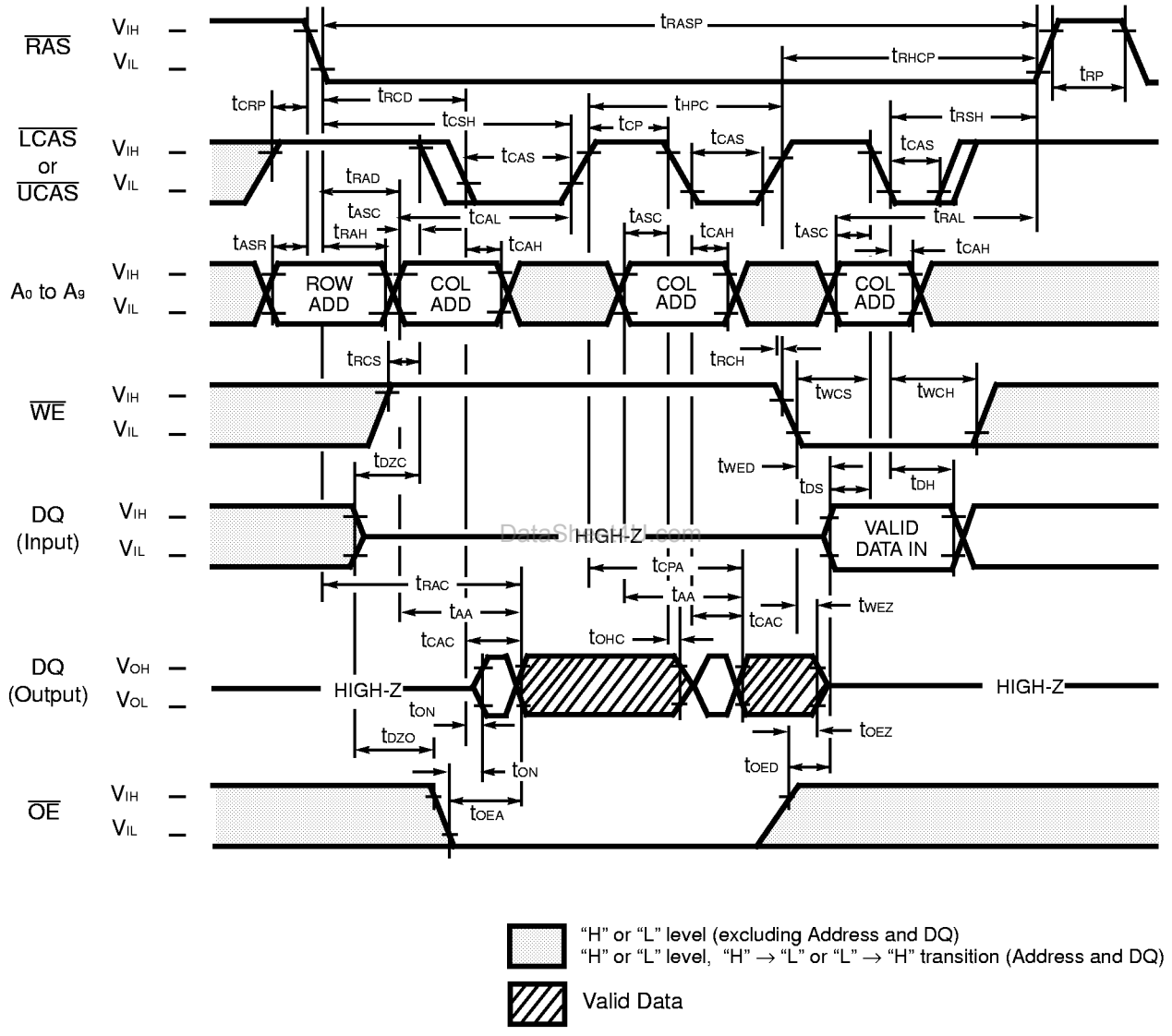

"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

Invalid Data

**DESCRIPTION**

The hyper page mode delayed write cycle is executed in the same manner as the hyper page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the hyper page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

## Fig. 14 – HYPER PAGE MODE READ/WRITE MIXED CYCLE



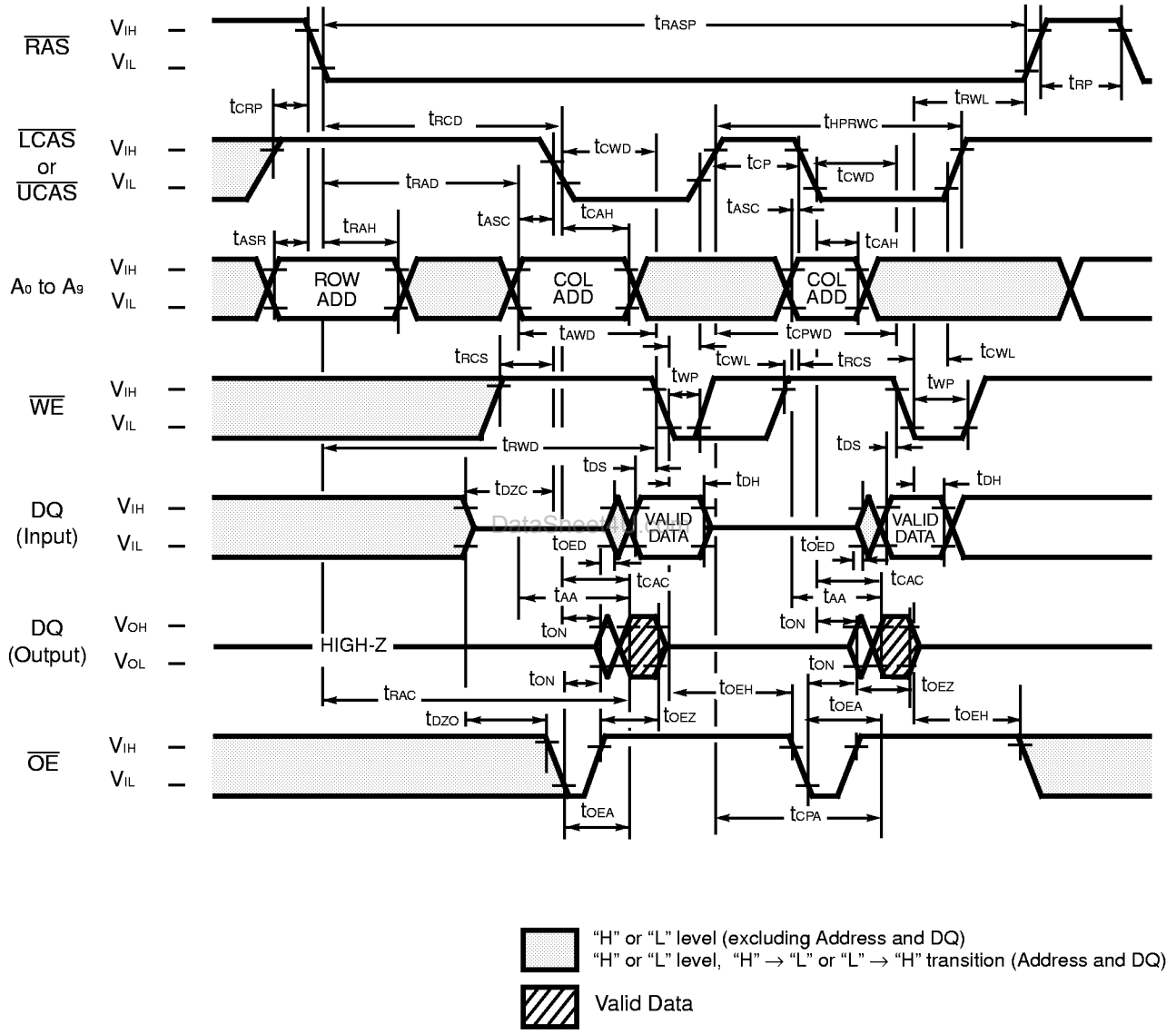

"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

Valid Data

**DESCRIPTION**

The hyper page mode performs read/write operations repetitively during one $\overline{RAS}$ cycle. At this time, $t_{HPC}$ (min) is invalid.

**Fig. 15 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE**



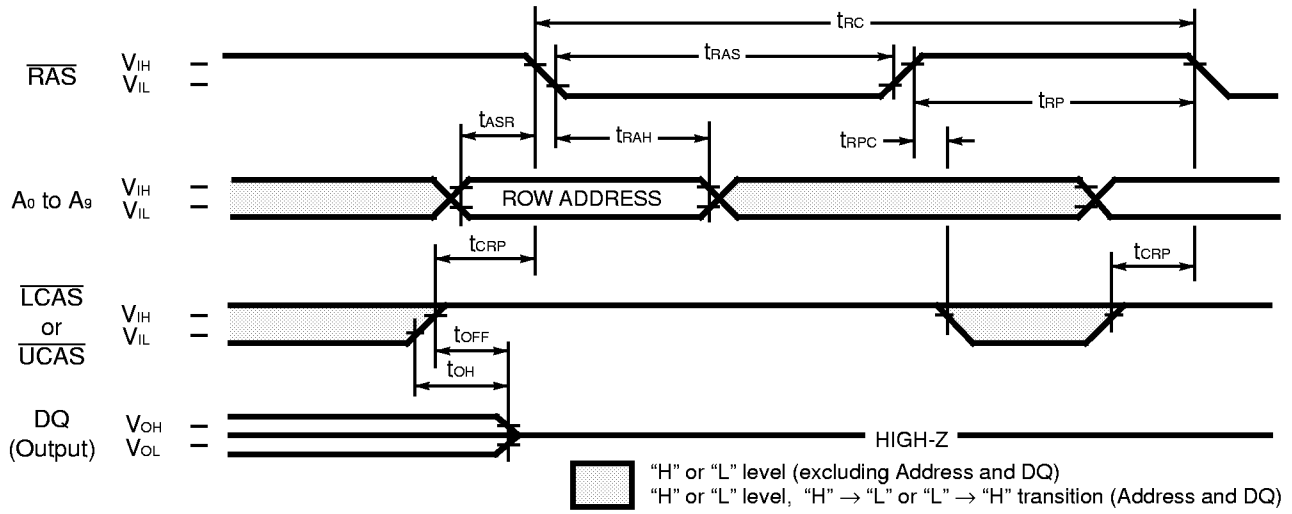

"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

Valid Data

**DESCRIPTION**

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

## Fig. 16 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

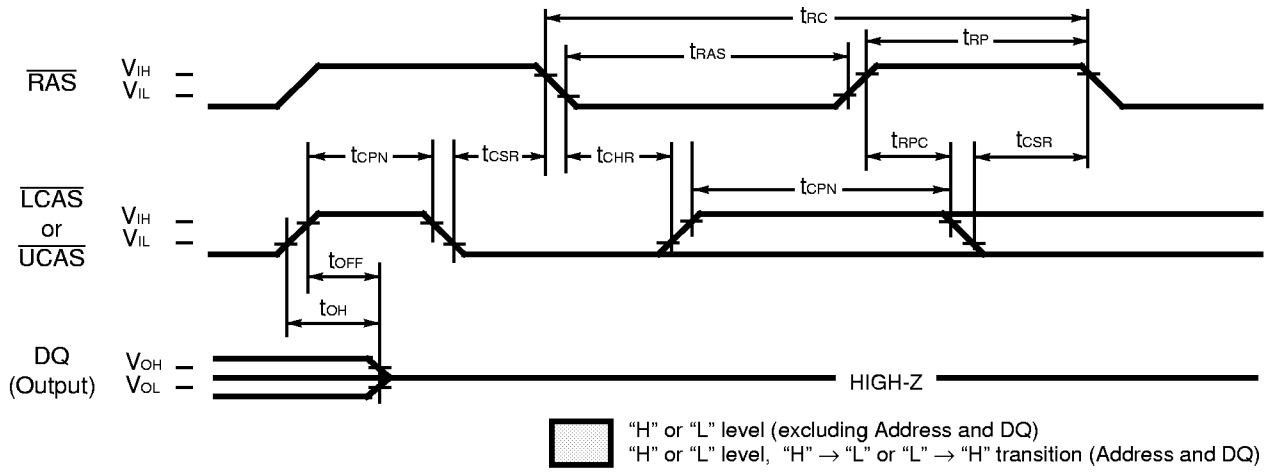



**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{LCAS}$ and $\overline{UCAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

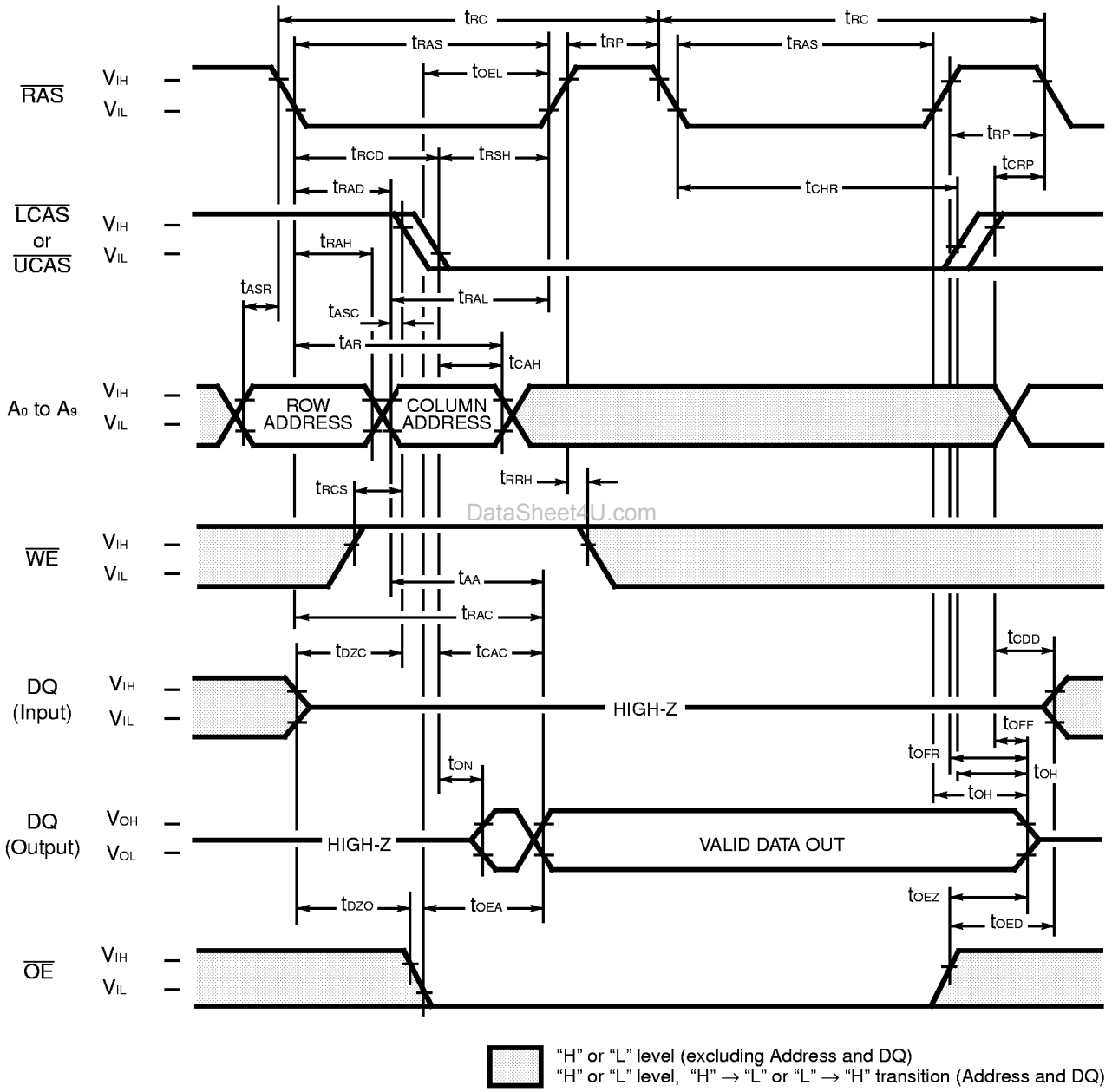
## Fig. 17 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")




**DESCRIPTION**

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ is held Low for the specified setup time ($t_{CSR}$) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

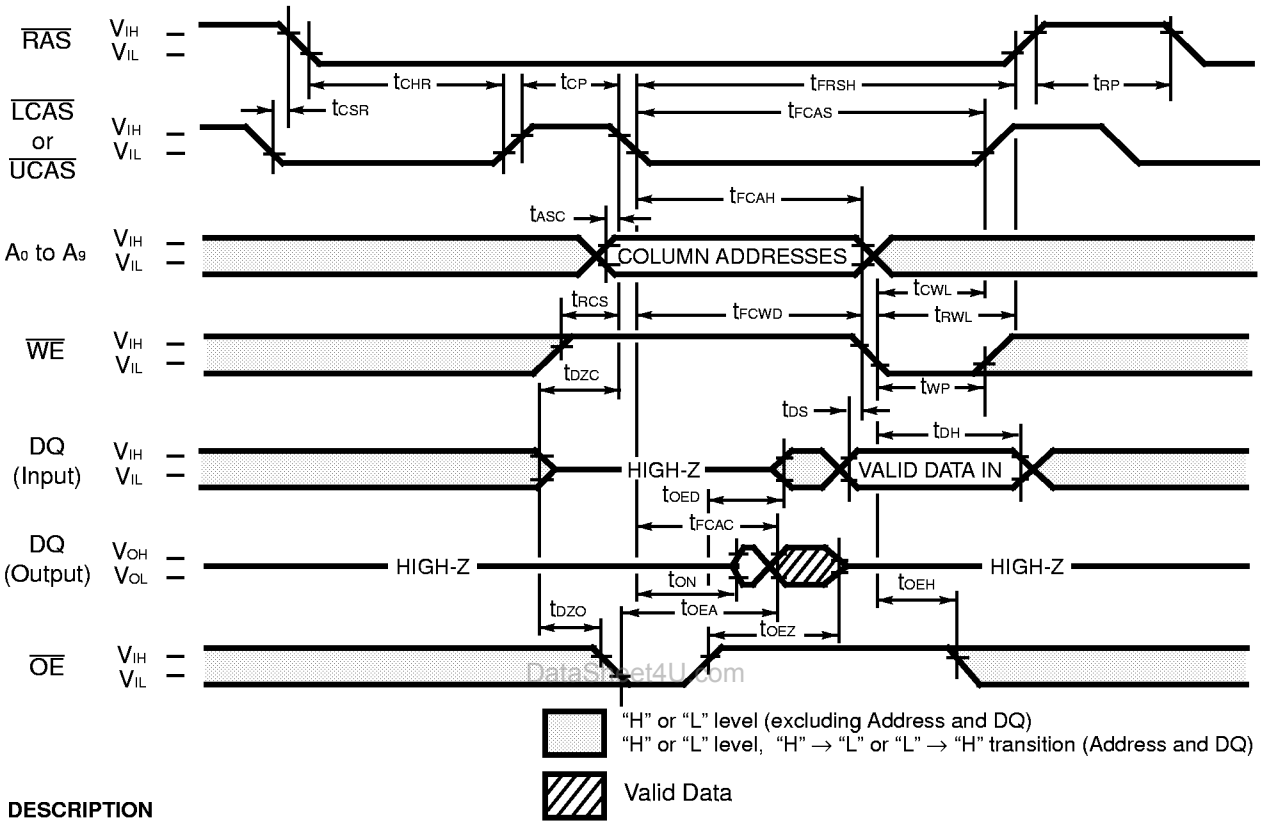
## Fig. 18 – HIDDEN REFRESH CYCLE




**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

**Fig. 19 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE**




**DESCRIPTION**

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the function of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits $A_0$ through $A_9$ are defined by the on-chip refresh counter.

Column Address: Bits $A_0$ through $A_7$ are defined by latching levels on $A_0$-$A_7$ at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows;

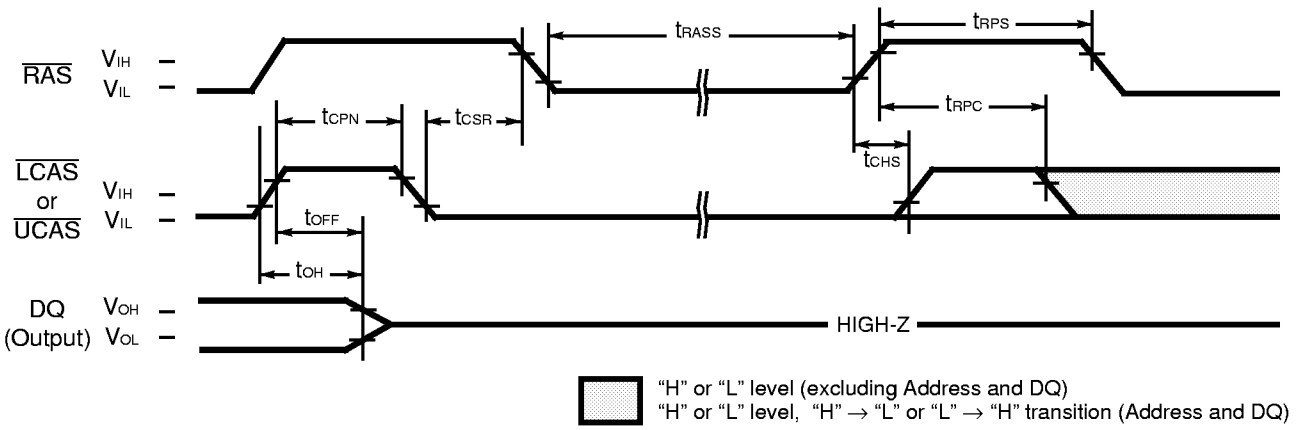
1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1,024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1,024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1,024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB81V18165A-60/60L | | MB81V18165A-70/70L | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 69 | Access Time from $\overline{CAS}$ | $t_{FCAC}$ | — | 50 | — | 55 | ns |
| 70 | Column Address Hold Time | $t_{FCAH}$ | 35 | — | 35 | — | ns |
| 71 | $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{FCWD}$ | 70 | — | 77 | — | ns |
| 72 | $\overline{CAS}$ Pulse Width | $t_{FCAS}$ | 90 | — | 99 | — | ns |
| 73 | $\overline{RAS}$ Hold Time | $t_{FRSH}$ | 90 | — | 99 | — | ns |

**Note:** Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

**Fig. 20 – SELF REFRESH CYCLE ($A_0$ - $A_9$ = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")**




**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB81V18165A-60/60L | | MB81V18165A-70/70L | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 74 | $\overline{RAS}$ Pulse Width | $t_{RASS}$ | 100 | — | 100 | — | µs |
| 75 | $\overline{RAS}$ Precharge Time | $t_{RPS}$ | 104 | — | 124 | — | ns |
| 76 | $\overline{CAS}$ Hold Time | $t_{CHS}$ | –50 | — | –50 | — | ns |

**Note:** Assumes Self Refresh cycle only.

**DESCRIPTION**

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self Refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator.

If $\overline{CAS}$ goes to "L" before $\overline{RAS}$ goes to "L" (CBR) and the condition of $\overline{CAS}$ "L" and $\overline{RAS}$ "L" is kept for term of $t_{RASS}$ (more than 100 µs), the device can enter the Self Refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during "$\overline{RAS}$ = L" and "$\overline{CAS}$ = L".

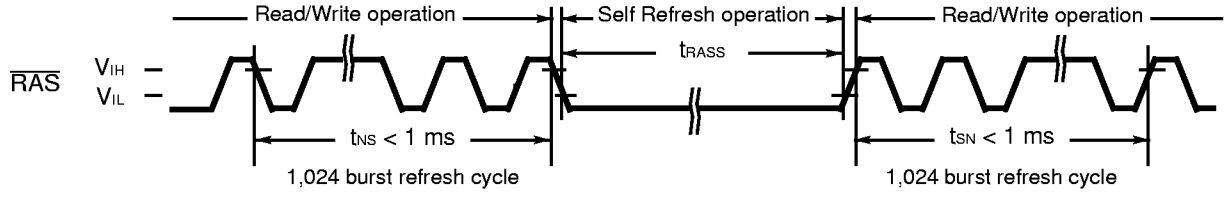
Exit from Self Refresh cycle is performed by toggling $\overline{RAS}$ and $\overline{CAS}$ to "H" with specified $t_{CHS}$ min. In this time, $\overline{RAS}$ must be kept "H" with specified $t_{RPS}$ min.

Using self refresh mode, data can be retained without external $\overline{CAS}$ signal during system is in standby.

Restriction for Self Refresh operation;

For Self Refresh operation, the notice below must be considered.

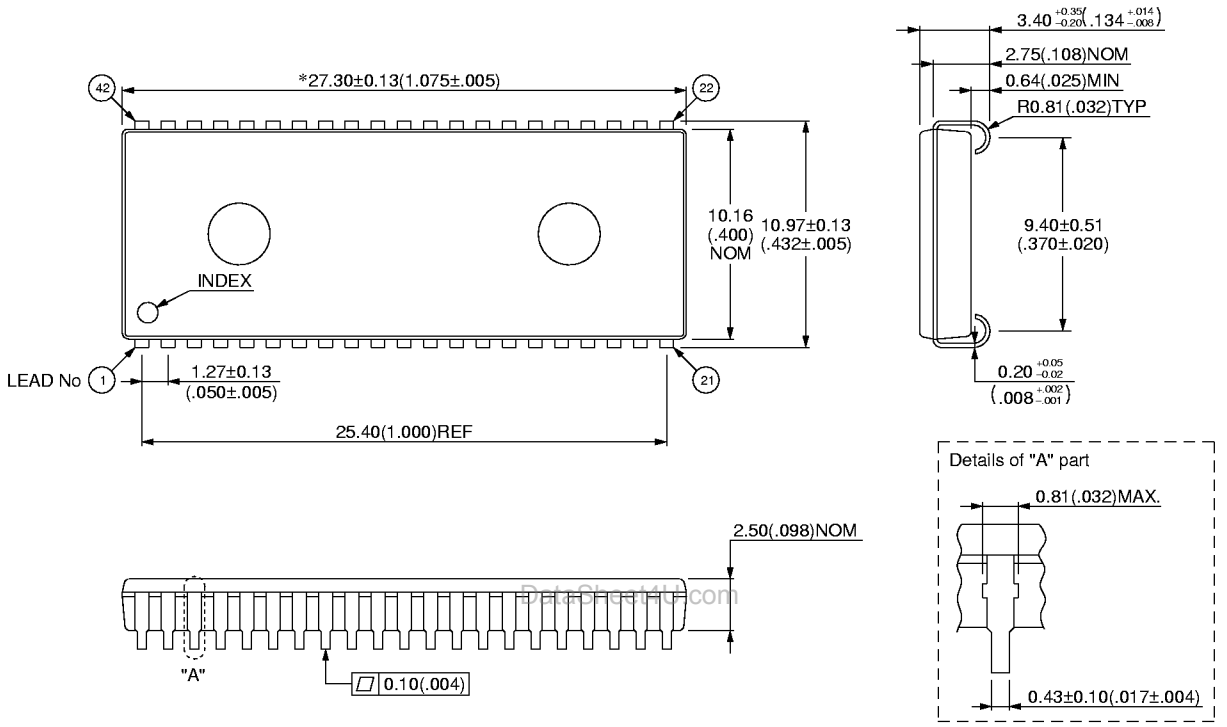
1) In the case that distributed CBR refresh are operated between read/write cycles
   Self Refresh cycles can be executed without special rule if 4,096 cycles of distributed CBR refresh are executed within $t_{REF}$ max.
2) In the case that burst CBR refresh or distributed/burst $\overline{RAS}$-only refresh are operated between read/write cycles
   1,024 times of burst CBR refresh or 1,024 times of burst $\overline{RAS}$-only refresh must be executed before and after Self Refresh cycles.




* read/write operation can be performed non refresh time within $t_{NS}$ or $t_{SN}$.

## ■ PACKAGE DIMENSIONS

**42-LEAD PLASTIC LEADED CHIP CARRIER**
**(CASE No.: LCC-42P-M01)**



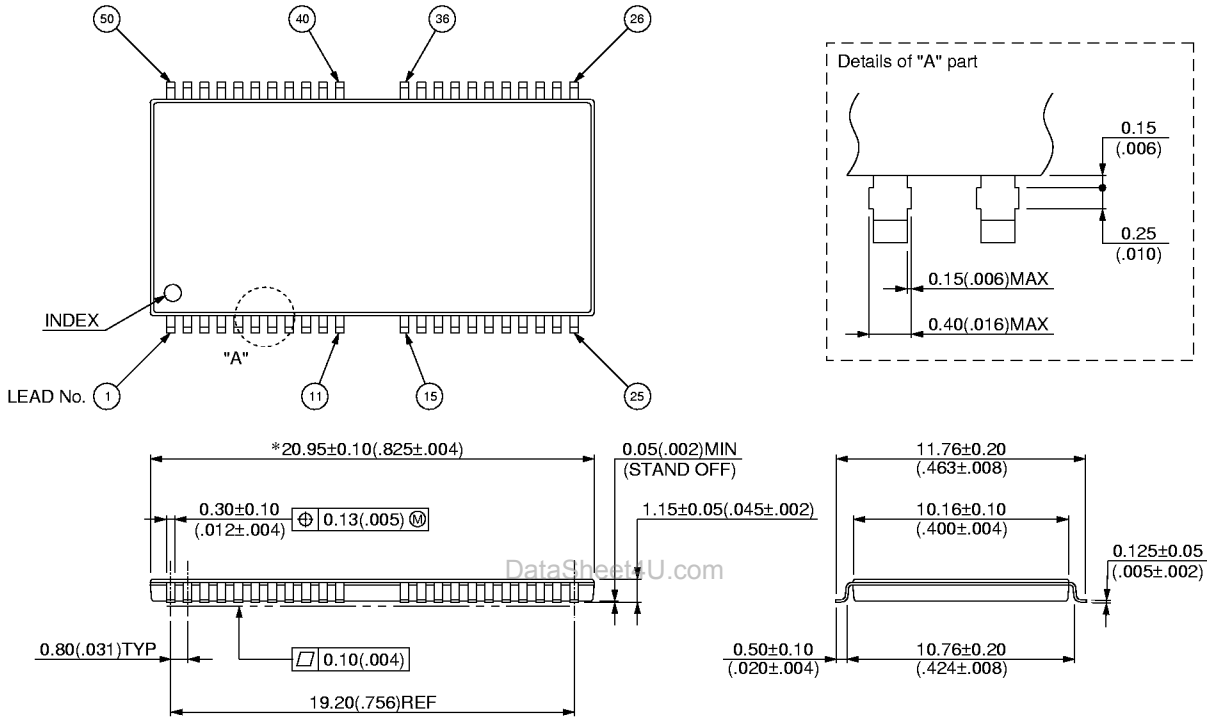

*: This dimension exclude resin protrusion. (Each side: 0.15 (.006) MAX.)



Dimensions in mm (inches)

## ■ PACKAGE DIMENSIONS

**50-LEAD PLASTIC FLAT PACKAGE**
**(CASE No.: FPT-50P-M06)**




*: This dimension exclude resin protrusion. (Each side: 0.15 (.006) MAX.)



Dimensions in mm (inches)