

## MEMORY

## CMOS

# 4 × 512 K × 32 BIT SYNCHRONOUS DYNAMIC RAM

## MB81F643242C-60/-70/-10

### CMOS 4-Bank × 524,288-Word × 32 Bit Synchronous Dynamic Random Access Memory

#### ■ DESCRIPTION

The Fujitsu MB81F643242C is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) containing 67,108,864 memory cells accessible in a 32-bit format. The MB81F643242C features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81F643242C SDRAM is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints, and may improve data bandwidth of memory as much as 5 times more than a conventional DRAM.

The MB81F643242C is ideally suited for workstations, personal computers, laser printers, high resolution graphic adapters/accelerators and other applications where an extremely large memory and bandwidth are required and where a simple interface is needed.

#### ■ PRODUCT LINE & FEATURES

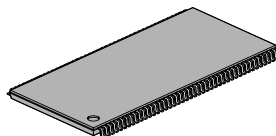
Parameter		MB81F643242C			Reference Value@ 67 MHz, CL=3
		-60	-70	-10	
CL - t <sub>RCD</sub> - t <sub>RP</sub>	CL = 2	2 - 2 - 2 clk min.	2 - 2 - 2 clk min.	2 - 2 - 2 clk min.	2 - 2 - 2 clk min.
	CL = 3	3 - 3 - 3 clk min.	3 - 3 - 3 clk min.	3 - 3 - 3 clk min.	3 - 3 - 3 clk min.
Clock Frequency		167 MHz max.	143 MHz max.	100 MHz max.	67 MHz max.
Burst Mode Cycle Time	CL = 2	10 ns min.	10 ns min.	15 ns min.	20 ns min.
	CL = 3	6 ns min.	7 ns min.	10 ns min.	15 ns min.
Access Time from Clock	CL = 2	6 ns max.	6 ns max.	7 ns max.	7 ns max.
	CL = 3	5.5 ns max.	5.5 ns max.	7 ns max.	7 ns max.
Operating Current		165 mA max.	155 mA max.	115 mA max.	100 mA max.
Power Down Mode Current (I <sub>CC2P</sub> )		2 mA max.			
Self Refresh Current (I <sub>CC6</sub> )		2 mA max.			

- Single +3.3 V Supply ±0.3 V tolerance
- LVTTTL compatible I/O interface
- 4 K refresh cycles every 64 ms
- Four bank operation
- Burst read/write operation and burst read/single write operation capability

- Programmable burst type, burst length, and CAS latency
- Auto-and Self-refresh (every 15.6 μs)
- CKE power down mode
- Output Enable and Input Data Mask

## ■ PACKAGE

86 pin Plastic TSOP(II) Package



(FPT-86P-M01)  
(Normal Bend)

### Package and Ordering Information

- 86-pin plastic (10.16 × 22.22 mm) TSOP-II without SCITT Function, order as MB81F643242C-xxFN
- 86-pin plastic (10.16 × 22.22 mm) TSOP-II with SCITT Function, order as MB81F643242C-xxFN-S

## PIN ASSIGNMENTS AND DESCRIPTIONS

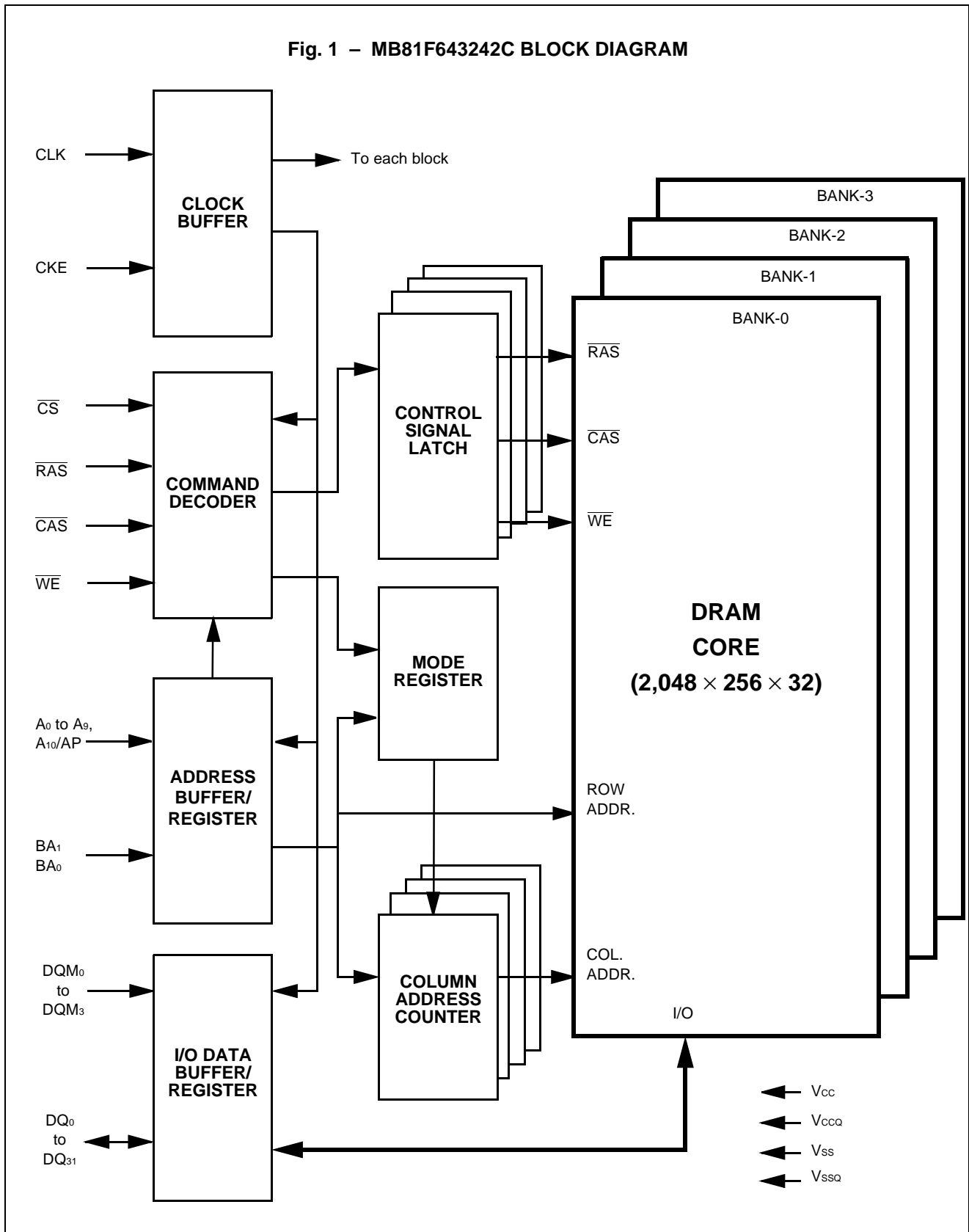
86-Pin TSOP(II)  
(TOP VIEW)  
<Normal Bend: FPT-86P-M01>

V <sub>CC</sub>	1	86	V <sub>SS</sub>
DQ <sub>0</sub>	2	85	DQ <sub>15</sub>
V <sub>CCQ</sub>	3	84	V <sub>SSQ</sub>
DQ <sub>1</sub>	4	83	DQ <sub>14</sub>
DQ <sub>2</sub>	5	82	DQ <sub>13</sub>
V <sub>SSQ</sub>	6	81	V <sub>CCQ</sub>
DQ <sub>3</sub>	7	80	DQ <sub>12</sub>
DQ <sub>4</sub>	8	79	DQ <sub>11</sub>
V <sub>CCQ</sub>	9	78	V <sub>SSQ</sub>
DQ <sub>5</sub>	10	77	DQ <sub>10</sub>
DQ <sub>6</sub>	11	76	DQ <sub>9</sub>
V <sub>SSQ</sub>	12	75	V <sub>CCQ</sub>
DQ <sub>7</sub>	13	74	DQ <sub>8</sub>
N.C.	14	73	N.C.
V <sub>CC</sub>	15	72	V <sub>SS</sub>
DQM <sub>0</sub>	16	71	DQM <sub>1</sub>
WE	17	70	N.C.
CAS	18	69	N.C.
RAS	19	68	CLK
CS	20	67	CKE
N.C.	21	66	A <sub>9</sub>
BA <sub>0</sub>	22	65	A <sub>8</sub>
BA <sub>1</sub>	23	64	A <sub>7</sub>
A <sub>10</sub> /AP	24	63	A <sub>6</sub>
A <sub>0</sub>	25	62	A <sub>5</sub>
A <sub>1</sub>	26	61	A <sub>4</sub>
A <sub>2</sub>	27	60	A <sub>3</sub>
DQM <sub>2</sub>	28	59	DQM <sub>3</sub>
V <sub>CC</sub>	29	58	V <sub>SS</sub>
N.C.	30	57	N.C.
DQ <sub>16</sub>	31	56	DQ <sub>31</sub>
V <sub>SSQ</sub>	32	55	V <sub>CCQ</sub>
DQ <sub>17</sub>	33	54	DQ <sub>30</sub>
DQ <sub>18</sub>	34	53	DQ <sub>29</sub>
V <sub>CCQ</sub>	35	52	V <sub>SSQ</sub>
DQ <sub>19</sub>	36	51	DQ <sub>28</sub>
DQ <sub>20</sub>	37	50	DQ <sub>27</sub>
V <sub>SSQ</sub>	38	49	V <sub>CCQ</sub>
DQ <sub>21</sub>	39	48	DQ <sub>26</sub>
DQ <sub>22</sub>	40	47	DQ <sub>25</sub>
V <sub>CCQ</sub>	41	46	V <sub>SSQ</sub>
DQ <sub>23</sub>	42	45	DQ <sub>24</sub>
V <sub>CC</sub>	43	44	V <sub>SS</sub>

# MB81F643242C-60/-70/-10 Advanced Info (AE0.1E)

Pin Number	Symbol	Function
1, 3, 9, 15, 29, 35, 41, 43, 49, 55, 75, 81	$V_{CC}, V_{CCQ}$	Supply Voltage
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	$DQ_0$ to $DQ_{31}$	Data I/O
6, 12, 32, 38, 44, 46, 52, 58, 72, 78, 84, 86	$V_{SS}, V_{SSQ}$	Ground
14, 21, 30, 57, 69, 70, 73	N.C.	No Connection
17	$\overline{WE}$	Write Enable
18	$\overline{CAS}$	Column Address Strobe
19	$\overline{RAS}$	Row Address Strobe
20	$\overline{CS}$	Chip Select
22, 23	$BA_1, BA_0$	Bank Select (Bank Address)
24	AP	Auto Precharge Enable
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	$A_0$ to $A_{10}$	Address Input <ul style="list-style-type: none"> <li>• Row: <math>A_0</math> to <math>A_{10}</math></li> <li>• Column: <math>A_0</math> to <math>A_7</math></li> </ul>
67	CKE	Clock Enable
68	CLK	Clock Input
16, 28, 59, 71	$DQM_0$ to $DQM_3$	Input Mask/Output Enable

## ■ BLOCK DIAGRAM



## ■ FUNCTIONAL TRUTH TABLE Note \*1

### COMMAND TRUTH TABLE Note \*2, \*3, and \*4

Function	Notes	Symbol	CKE		CS	RAS	CAS	WE	BA <sub>1</sub> , BA <sub>0</sub>	A <sub>10</sub> (AP)	A <sub>9</sub> to A <sub>8</sub>	A <sub>7</sub> to A <sub>0</sub>
			n-1	n								
Device Deselect	*5	DESL	H	X	H	X	X	X	X	X	X	X
No Operation	*5	NOP	H	X	L	H	H	H	X	X	X	X
Burst Stop		BST	H	X	L	H	H	L	X	X	X	X
Read	*6	READ	H	X	L	H	L	H	V	L	X	V
Read with Auto-precharge	*6	READA	H	X	L	H	L	H	V	H	X	V
Write	*6	WRIT	H	X	L	H	L	L	V	L	X	V
Write with Auto-precharge	*6	WRITA	H	X	L	H	L	L	V	H	X	V
Bank Active	*7	ACTV	H	X	L	L	H	H	V	V	V	V
Precharge Single Bank		PRE	H	X	L	L	H	L	V	L	X	X
Precharge All Banks		PALL	H	X	L	L	H	L	X	H	X	X
Mode Register Set	*8, *9	MRS	H	X	L	L	L	L	L	L	V	V

- Notes:**
- \*1. V = Valid, L = Logic Low, H = Logic High, X = either L or H.
  - \*2. All commands assumes no CSUS command on previous rising edge of clock.
  - \*3. All commands are assumed to be valid state transitions.
  - \*4. All inputs are latched on the rising edge of clock.
  - \*5. NOP and DESL commands have the same effect on the part. Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.
  - \*6. READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to "STATE DIAGRAM" in section "■ FUNCTIONAL DESCRIPTION".
  - \*7. ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command).
  - \*8. Required after power up.
  - \*9. MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to "STATE DIAGRAM" in section "■ FUNCTIONAL DESCRIPTION".

## DQM TRUTH TABLE

Function	Symbol	CKE		DQM <sub>i</sub> <sup>*1, *2</sup>
		n-1	n	
Data Write/Output Enable	ENB <sub>i</sub> <sup>*1</sup>	H	X	L
Data Mask/Output Disable	MASK <sub>i</sub> <sup>*1</sup>	H	X	H

**Notes:** \*1. i = 0, 1, 2, 3

\*2. DQM<sub>0</sub> for DQ<sub>0</sub> to DQ<sub>7</sub>, DQM<sub>1</sub> for DQ<sub>8</sub> to DQ<sub>15</sub>, DQM<sub>2</sub> for DQ<sub>16</sub> to DQ<sub>23</sub>, DQM<sub>3</sub> for DQ<sub>24</sub> to DQ<sub>31</sub>,

## CKE TRUTH TABLE

Current State	Function	Notes	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA <sub>1</sub> , BA <sub>0</sub>	A <sub>10</sub> (AP)	A <sub>9</sub> to A <sub>0</sub>
				n-1	n							
Bank Active	Clock Suspend Mode Entry	*1	CSUS	H	L	X	X	X	X	X	X	X
Any (Except Idle)	Clock Suspend Continue	*1		L	L	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit			L	H	X	X	X	X	X	X	X
Idle	Auto-refresh Command	*2	REF	H	H	L	L	L	H	X	X	X
Idle	Self-refresh Entry	*2, *3	SELF	H	L	L	L	L	H	X	X	X
Self Refresh	Self-refresh Exit	*4	SELF <sub>X</sub>	L	H	L	H	H	H	X	X	X
				L	H	H	X	X	X	X	X	X
Idle	Power Down Entry	*3	PD	H	L	L	H	H	H	X	X	X
				H	L	H	X	X	X	X	X	X
Power Down	Power Down Exit			L	H	L	H	H	H	X	X	X
				L	H	H	X	X	X	X	X	X

**Notes:** \*1. The CSUS command requires that at least one bank is active. Refer to "STATE DIAGRAM" in section "■ FUNCTIONAL DESCRIPTION".

NOP or DSEL commands should only be issued after CSUS and PRE(or PALL) commands asserted at the same time.

\*2. REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). Refer to "STATE DIAGRAM" in section "■ FUNCTIONAL DESCRIPTION".

\*3. SELF and PD commands should only be issued after the last read data have been appeared on DQ.

\*4. CKE should be held high within one t<sub>RC</sub> period after t<sub>CKSP</sub>.

**OPERATION COMMAND TABLE (Applicable to single bank)**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Bank Active after $t_{RCD}$	
	L	L	H	L	BA, AP	PRE/PALL	NOP	
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*3, *6
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after $t_{RSC}$ )	*3, *7
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Precharge; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

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(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP	*4
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge → Idle; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*4
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Read with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*2
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*2
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

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# MB81F643242C-60/-70/-10 Advanced Info (AE0.1E)

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Pre-charging	H	X	X	X	X	DESL	NOP (Idle after $t_{RP}$ )	
	L	H	H	H	X	NOP	NOP (Idle after $t_{RP}$ )	
	L	H	H	L	X	BST	NOP (Idle after $t_{RP}$ )	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	NOP (PALL may affect other bank)	*5
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after $t_{RCD}$ )	
	L	H	H	H	X	NOP	NOP (Bank Active after $t_{RCD}$ )	
	L	H	H	L	X	BST	NOP (Bank Active after $t_{RCD}$ )	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*2
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Refreshing	H	X	X	X	X	DESL	NOP (Idle after $t_{RC}$ )	
	L	H	H	X	X	NOP/BST	NOP (Idle after $t_{RC}$ )	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after $t_{RSC}$ )	
	L	H	H	H	X	NOP	NOP (Idle after $t_{RSC}$ )	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

## ABBREVIATIONS:

RA = Row Address      BA = Bank Address  
CA = Column Address    AP = Auto Precharge

- Notes:**
- \*1. All entries in OPERATION COMMAND TABLE assume the CKE was High during the proceeding clock cycle and the current clock cycle.  
Illegal means don't used command. If used, power up sequence be asserted after power shut down.
  - \*2. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
  - \*3. Illegal if any bank is not idle.
  - \*4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.  
Refer to "TIMING DIAGRAM -11 & -12" in section "■ TIMING DIAGRAMS".
  - \*5. NOP to bank precharging or in idle state. May precharge bank specified by BA (and AP).
  - \*6. SELF command should only be issued after the last read data have been appeared on DQ.
  - \*7. MRS command should only be issued on condition that all DQ are in Hi-Z.

**COMMAND TRUTH TABLE FOR CKE Note \*1**

Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after $t_{RC}$ )	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery → Idle after $t_{RC}$ )	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after $t_{RC}$	
	H	H	L	H	H	H	X	Idle after $t_{RC}$	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	H	X	X	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	*2

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Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle	
	L	H	L	H	H	H	X		
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	
	L	H	L	L	X	X	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
All Banks Idle	H	H	H	X	X	X	MODE	Refer to the Operation Command Table.	
	H	H	L	H	X	X	MODE	Refer to the Operation Command Table.	
	H	H	L	L	H	X	MODE	Refer to the Operation Command Table.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	MODE	Refer to the Operation Command Table.	
	H	L	H	X	X	X	X	Power Down	
	H	L	L	H	H	H	X	Power Down	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh	*3
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	

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Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
Bank Active, Bank Activating, Read/Write	H	H	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	X	X	X	X	X	X	Invalid	
Clock Suspend	H	X	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	Illegal	

- Notes:** \*1. All entries in "COMMAND TRUTH TABLE FOR CKE" are specified at CKE(n) state and CKE input from CKE(n-1) to CKE(n) state must satisfy corresponding set up and hold time for CKE.  
\*2. CKE should be held High for  $t_{RC}$  period.  
\*3. SELF command should only be issued after the last data have been appeared on DQ.

## ■ FUNCTIONAL DESCRIPTION

### SDRAM BASIC FUNCTION

Three major differences between this SDRAM and conventional DRAMs are: synchronized operation, burst mode, and mode register.

The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory although it has been using two clocks,  $\overline{RAS}$  and  $\overline{CAS}$ . Each operation of DRAM is determined by their timing phase differences while each operation of SDRAM is determined by commands and all operations are referenced to a positive clock edge. Fig. 2 shows the basic timing diagram differences between SDRAMs and DRAMs.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode register** is to justify the SDRAM operation and function into desired system conditions. MODE REGISTER TABLE shows how SDRAM can be configured for system requirement by mode register programming.

### CLOCK INPUT (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

### CHIP SELECT ( $\overline{CS}$ )

$\overline{CS}$  enables all commands inputs,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$ , and address input. When  $\overline{CS}$  is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn't needed,  $\overline{CS}$  can be tied to ground level.

### COMMAND INPUT ( $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ )

Unlike a conventional DRAM,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  do not directly imply SDRAM operation, such as Row address strobe by  $\overline{RAS}$ . Instead, each combination of  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  input in conjunction with  $\overline{CS}$  input at a rising edge of the CLK determines SDRAM operation. Refer to "■ FUNCTIONAL TRUTH TABLE".

### ADDRESS INPUT ( $A_0$ to $A_{10}$ )

Address input selects an arbitrary location of a total of 524,288 words of each memory cell matrix. A total of nineteen address input signals are required to decode such a matrix. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), eleven Row addresses are initially latched and the remainder of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

### BANK SELECT ( $BA_0$ , $BA_1$ )

This SDRAM has four banks and each bank is organized as 512 K words by 32-bit.

Bank selection by  $BA_0$ ,  $BA_1$  occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).



## DATA INPUT AND OUTPUT (DQ<sub>0</sub> to DQ<sub>31</sub>)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input:

- t<sub>RAC</sub>** ; from the bank active command when t<sub>RCD</sub> (min) is satisfied. (This parameter is reference only.)
- t<sub>CAC</sub>** ; from the read command when t<sub>RCD</sub> is greater than t<sub>RCD</sub> (min). (This parameter is reference only.)
- t<sub>AC</sub>** ; from the clock edge after t<sub>RAC</sub> and t<sub>CAC</sub>.

The polarity of the output data is identical to that of the input. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t<sub>OH</sub>).

## DATA I/O MASK (DQM)

DQM is an active high enable input and has an output disable and input mask function. During burst cycle and when DQM<sub>0</sub> to DQM<sub>3</sub> = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type. DQM<sub>0</sub>, DQM<sub>1</sub>, DQM<sub>2</sub>, DQM<sub>3</sub>, controls DQ<sub>0</sub> to DQ<sub>7</sub>, DQ<sub>8</sub> to DQ<sub>15</sub>, DQ<sub>16</sub> to DQ<sub>23</sub>, DQ<sub>24</sub> to DQ<sub>31</sub>, respectively.

## BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as t<sub>AC</sub> and t<sub>CK</sub>, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after t <sub>OWD</sub>
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0). The interleave mode is a scrambled decoding scheme for A<sub>0</sub> and A<sub>2</sub>. If the first access of column address is even (0), the next address will be odd (1), or vice-versa. When the full burst operation is executed at single write mode, Auto-precharge command is valid only at write operation.

The burst type can be selected either sequential or interleave mode. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by burst length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0).

Burst Length	Starting Column Address A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	Sequential Mode	Interleave
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

## FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps round to first column address (= 0) and continues to count until interrupted by the new read (READ) /write (WRIT), precharge (PRE), or burst stop (BST) command. The selection of Auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.

For the detail rule, please refer to “TIMING DIAGRAM - 8” in section “■ TIMING DIAGRAMS”.

When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

## BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

## PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE). With the Precharge command, SDRAM will automatically be in standby state after precharge time ( $t_{RP}$ ).

The precharged bank is selected by combination of AP and BA<sub>0</sub>, BA<sub>1</sub> when Precharge command is asserted. If AP = High, all banks are precharged regardless of BA<sub>0</sub>, BA<sub>1</sub> (PALL). If AP = Low, a bank to be selected by BA<sub>0</sub>, BA<sub>1</sub> is precharged (PRE).

The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion.

This auto precharge is entered by AP = High when a read or write command is asserted. Refer to "■ FUNCTIONAL TRUTH TABLE".

## AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 16  $\mu$ s or a total 4096 refresh commands within a 64 ms period.

## SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SDRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

**Notes:** When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

## SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum  $t_{CKSP}$  after CKE brought high, and then the No Operation command (NOP) or the Deselect command (DESL) should be asserted within one  $t_{RC}$  period. CKE should be held High within one  $t_{RC}$  period after  $t_{CKSP}$ . Refer to "TIMING DIAGRAM -16" in section "■ TIMING DIAGRAMS" for the detail.

It is recommended to assert an Auto-refresh command just after the  $t_{RC}$  period to avoid the violation of refresh period.

**Notes:** When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted after the self-refresh exit.

## MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS latency, and Operation Code. Refer to "■ MODE REGISTER TABLE".

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all DQ is in Hi-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDRAM. Refer to "POWER-UP INITIALIZATION" below.

## POWER-UP INITIALIZATION

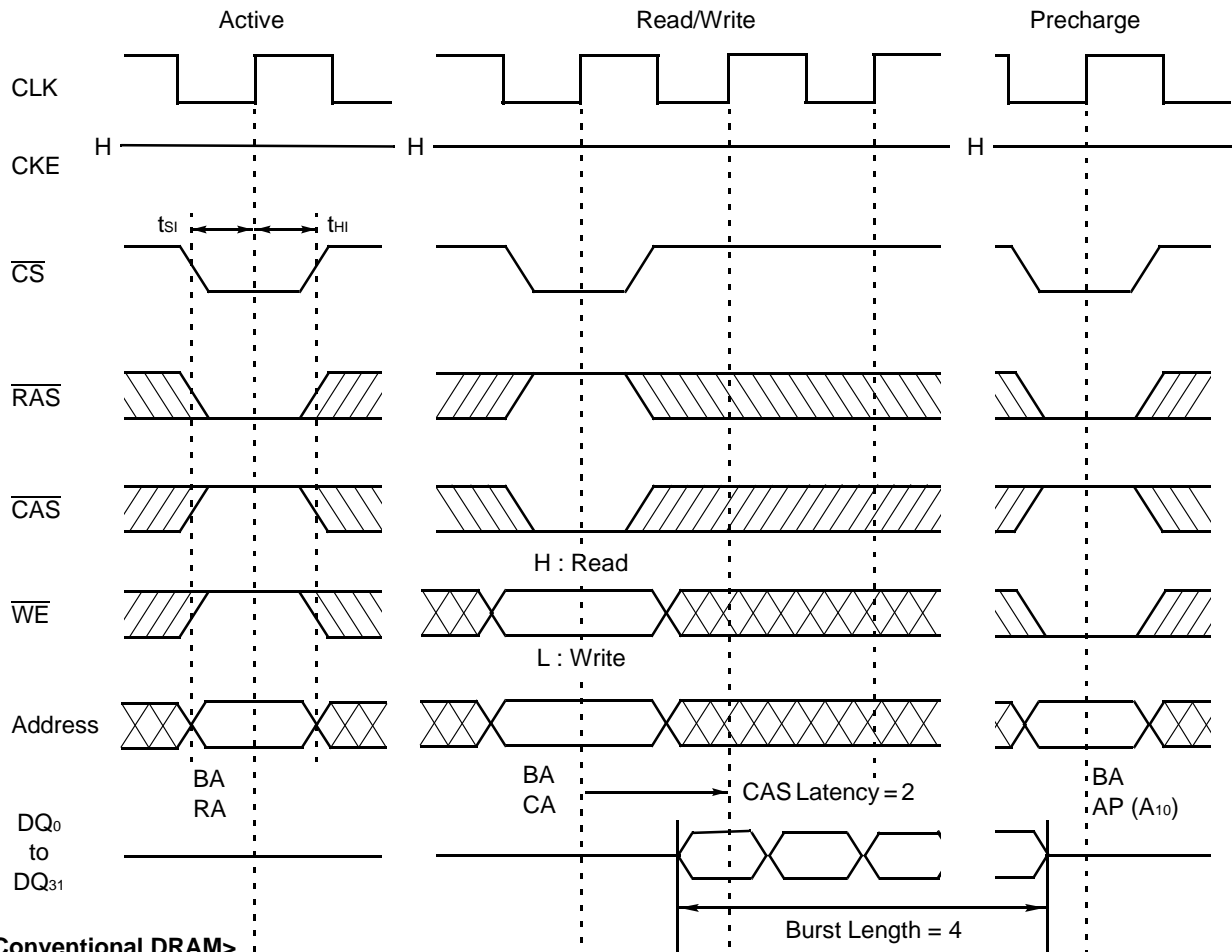
The SDRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply power and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 100  $\mu$ s.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 2 Auto-refresh command (REF).
5. Program the mode register by Mode Register Set command (MRS).

In addition, it is recommended DQM and CKE to track  $V_{CC}$  to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 2 Auto-refresh command (REF).

**Fig. 2 – BASIC TIMING FOR CONVENTIONAL DRAM VS SYNCHRONOUS DRAM**

**<SDRAM>**



**<Conventional DRAM>**

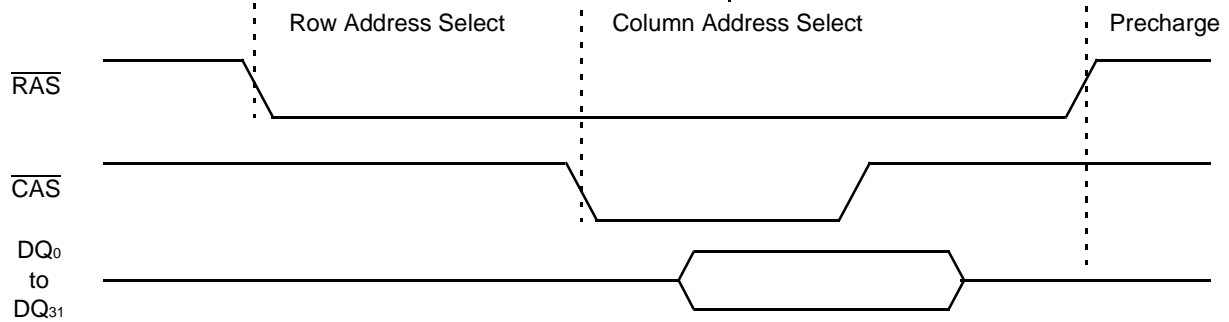
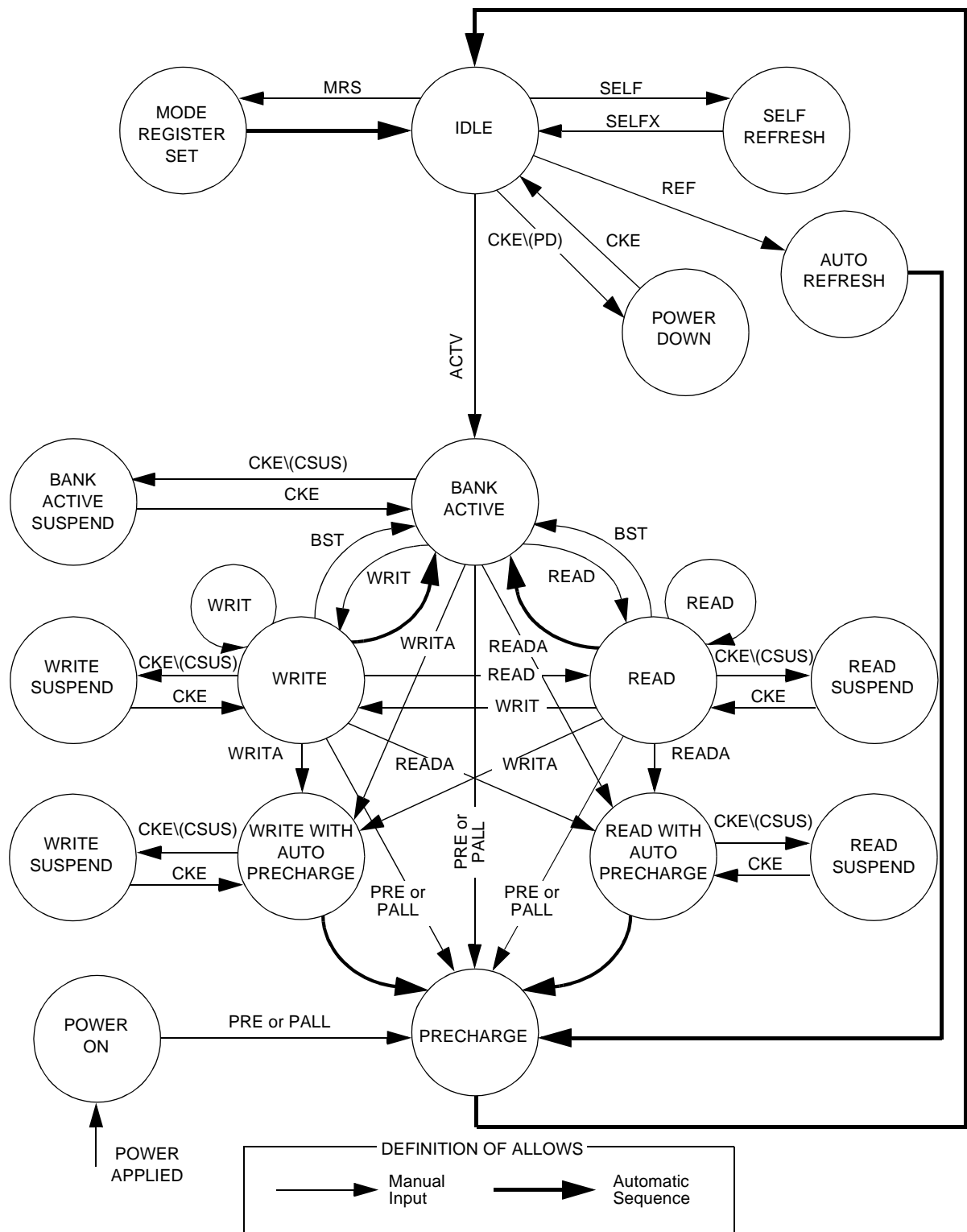


Fig. 3 – STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)



**Note:** CKE\ means CKE goes Low-level from High-level.

## ■ BANK OPERATION COMMAND TABLE

### MINIMUM CLOCK LATENCY OR DELAY TIME FOR 1 BANK OPERATION

Second command (same bank) First command	MRS	ACTV	READ	READA <sup>*4</sup>	WRIT	WRITA <sup>*4</sup>	PRE	PALL	REF	SELF	BST
MRS	t <sub>RSC</sub>	t <sub>RSC</sub>					t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>
ACTV			t <sub>RCD</sub>	t <sub>RCD</sub>	t <sub>RCD</sub>	t <sub>RCD</sub>	t <sub>RAS</sub>	t <sub>RAS</sub>			1
READ			1	1	1 <sup>*5</sup>	1 <sup>*5</sup>	1 <sup>*4</sup>	1 <sup>*4</sup>			1
READA	BL <sup>*1,2</sup> + t <sub>RP</sub>	BL + t <sub>RP</sub>					BL <sup>*4</sup> + t <sub>RP</sub>	BL <sup>*4</sup> + t <sub>RP</sub>	BL <sup>*2</sup> + t <sub>RP</sub>	BL <sup>*2,7</sup> + t <sub>RP</sub>	
WRIT			t <sub>WR</sub>	t <sub>WR</sub>	1	1	t <sub>DPL</sub> <sup>*4</sup>	t <sub>DPL</sub> <sup>*4</sup>			1
WRITA	BL-1 <sup>*2</sup> + t <sub>DAL</sub>	BL-1 + t <sub>DAL</sub>					BL-1 <sup>*4</sup> + t <sub>DAL</sub>	BL-1 <sup>*4</sup> + t <sub>DAL</sub>	BL-1 <sup>*2</sup> + t <sub>DAL</sub>	BL-1 <sup>*2</sup> + t <sub>DAL</sub>	
PRE	t <sub>RP</sub> <sup>*2,3</sup>	t <sub>RP</sub>					1	1 <sup>*4</sup>	t <sub>RP</sub> <sup>*2</sup>	t <sub>RP</sub> <sup>*2,6</sup>	1
PALL	t <sub>RP</sub> <sup>*3</sup>	t <sub>RP</sub>					1	1	t <sub>RP</sub>	t <sub>RP</sub> <sup>*6</sup>	1
REF	t <sub>RC</sub>	t <sub>RC</sub>					t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>
SELF	t <sub>RC</sub>	t <sub>RC</sub>					t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>

- Notes:**
- \*1. If  $t_{RP}(\min.) < CL \times t_{CK}$ , minimum latency is a sum of  $(BL + CL) \times t_{CK}$ .
  - \*2. Assume all banks are in Idle state.
  - \*3. Assume output is in High-Z state.
  - \*4. Assume  $t_{RAS}(\min.)$  is satisfied.
  - \*5. Assume no I/O conflict.
  - \*6. Assume after the last data have been appeared on DQ.
  - \*7. If  $t_{RP}(\min.) < (CL - 1) \times t_{CK}$ , minimum latency is a sum of  $(BL + CL - 1) \times t_{CK}$ .



Illegal Command

## ■ MULTI BANK OPERATION COMMAND TABLE

### MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

Second command (other bank) First command	MRS	ACTV	<sup>*5</sup> READ	<sup>*5,*6</sup> READA	<sup>*5</sup> WRIT	<sup>*5,*6</sup> WRITA	PRE	PALL	REF	SELF	BST
MRS	t <sub>RSC</sub>	t <sub>RSC</sub>					t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>	t <sub>RSC</sub>
ACTV		<sup>*2</sup> t <sub>RRD</sub>	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*6,*7</sup> 1	<sup>*7</sup> t <sub>RAS</sub>			1
READ		<sup>*2,*4</sup> 1	1	1	<sup>*10</sup> 1	<sup>*10</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1			1
READA	<sup>*1,*2</sup> BL+ t <sub>RP</sub>	<sup>*2,*4</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1	<sup>*6,*10</sup> 1	<sup>*6,*10</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> BL+ t <sub>RP</sub>	<sup>*2</sup> BL+ t <sub>RP</sub>	<sup>*2,*9</sup> BL+ t <sub>RP</sub>	
WRIT		<sup>*2,*4</sup> 1	1	1	1	1	<sup>*6</sup> 1	<sup>*6</sup> t <sub>DPL</sub>			1
WRITA	<sup>*2</sup> BL-1 + t <sub>DAL</sub>	<sup>*2,*4</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> 1	<sup>*6</sup> BL-1 + t <sub>DAL</sub>	<sup>*2</sup> BL-1 + t <sub>DAL</sub>	<sup>*2</sup> BL-1 + t <sub>DAL</sub>	
PRE	<sup>*2,*3</sup> t <sub>RP</sub>	<sup>*2,*4</sup> 1	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*7</sup> 1	<sup>*6,*7</sup> 1	<sup>*7</sup> 1	<sup>*2</sup> t <sub>RP</sub>	<sup>*2,*8</sup> t <sub>RP</sub>	1
PALL	<sup>*3</sup> t <sub>RP</sub>	t <sub>RP</sub>					1	1	t <sub>RP</sub>	<sup>*8</sup> t <sub>RP</sub>	1
REF	t <sub>RC</sub>	t <sub>RC</sub>					t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>
SELF	t <sub>RC</sub>	t <sub>RC</sub>					t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>	t <sub>RC</sub>

- Notes:**
- \*1. If  $t_{RP}(\min.) < CL \times t_{CK}$ , minimum latency is a sum of  $(BL+CL) \times t_{CK}$ .
  - \*2. Assume bank of the object is in Idle state.
  - \*3. Assume output is in High-Z state.
  - \*4.  $t_{RRD}(\min.)$  of other bank (second command will be asserted) is satisfied.
  - \*5. Assume other bank is in active, read or write state.
  - \*6. Assume  $t_{RAS}(\min.)$  is satisfied.
  - \*7. Assume other banks are not in READA/WRITA state.
  - \*8. Assume after the last data have been appeared on DQ.
  - \*9. If  $t_{RP}(\min.) < (CL-1) \times t_{CK}$ , minimum latency is a sum of  $(BL+CL-1) \times t_{CK}$ .
  - \*10. Assume no I/O conflict.

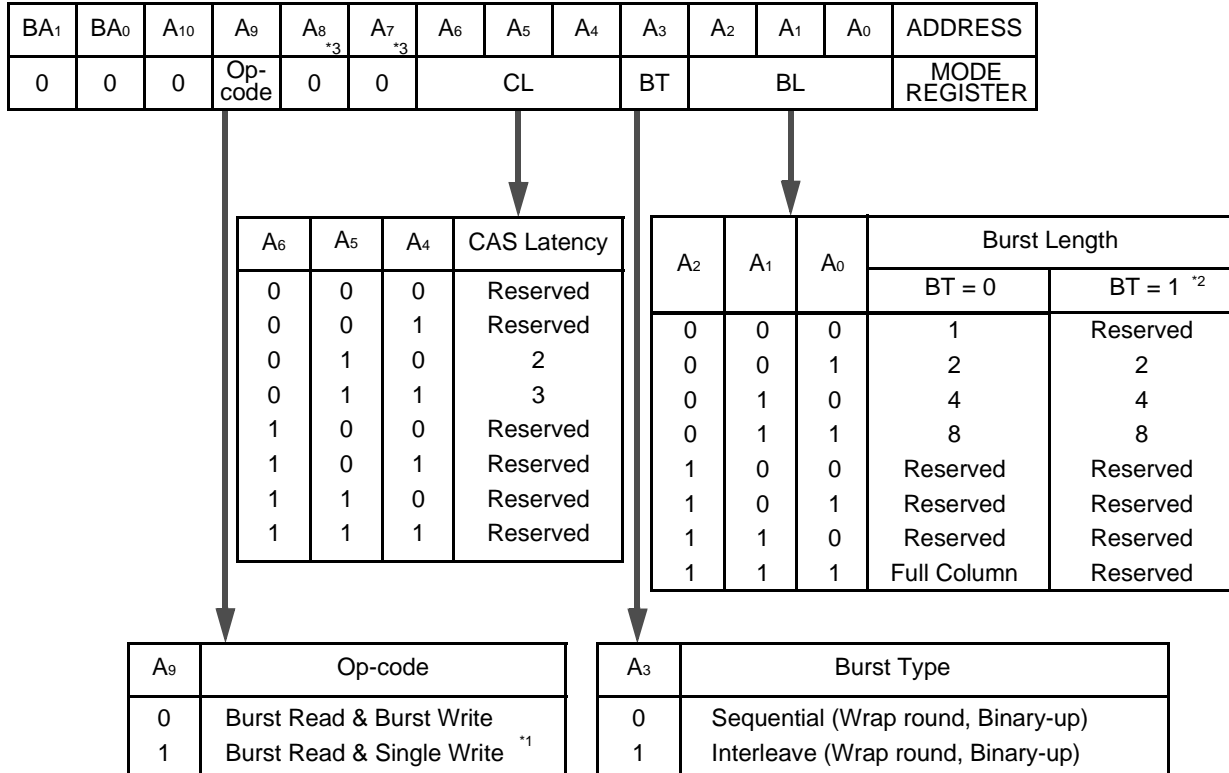


Illegal Command



## ■ MODE REGISTER TABLE

### MODE REGISTER SET



- Notes:** \*1. When A<sub>9</sub> = 1, burst length at Write is always one regardless of BL value.  
\*2. BL = 1 and Full Column are not applicable to the interleave mode.  
\*3. A<sub>7</sub> = 1 and A<sub>8</sub> = 1 are reserved for vender test.

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage of V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub> , V <sub>CCQ</sub>	−0.5 to +4.6	V
Voltage at Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	−0.5 to +4.6	V
Short Circuit Output Current	I <sub>OUT</sub>	±50	mA
Power Dissipation	P <sub>D</sub>	1.3	W
Storage Temperature	T <sub>STG</sub>	−55 to +125	°C

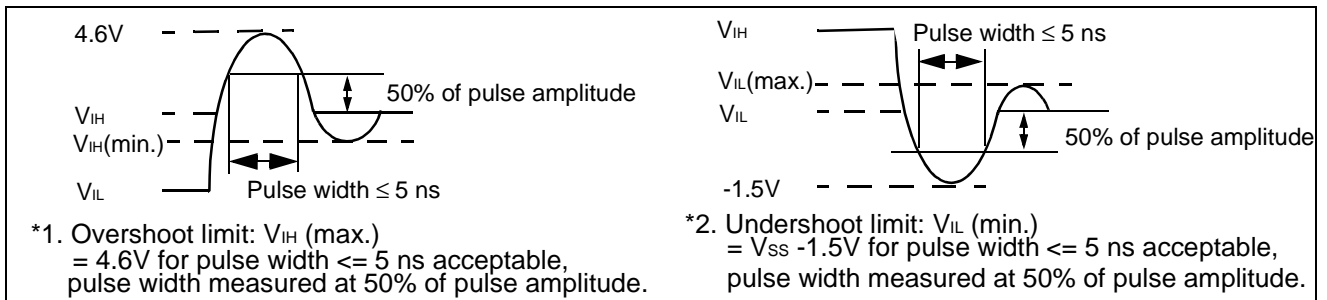
**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V<sub>SS</sub>)

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V <sub>CC</sub> , V <sub>CCQ</sub>	3.0	3.3	3.6	V
		V <sub>SS</sub> , V <sub>SSQ</sub>	0	0	0	V
Input High Voltage	*1	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.5	V
Input Low Voltage	*2	V <sub>IL</sub>	−0.5	—	0.8	V
Ambient Temperature		T <sub>A</sub>	0	—	70	°C

**Notes:**



**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Except for CLK	C <sub>IN1</sub>	2.5	—	5.0	pF
Input Capacitance for CLK	C <sub>IN2</sub>	2.5	—	4.0	pF
I/O Capacitance	C <sub>I/O</sub>	4.0	—	6.5	pF

## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note \*1, \*2, and \*3

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Output High Voltage		$V_{OH(DC)}$	$I_{OH} = -2 \text{ mA}$	2.4	—	V
Output Low Voltage		$V_{OL(DC)}$	$I_{OL} = 2 \text{ mA}$	—	0.4	V
Input Leakage Current (Any Input)		$I_{LI}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ ; All other pins not under test = 0 V	-5	5	$\mu\text{A}$
Output Leakage Current		$I_{LO}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ ; Data out disabled	-5	5	$\mu\text{A}$
Operating Current (Average Power Supply Current)	MB81F643242C-60	$I_{CC1}$	Burst: Length = 1 $t_{RC} = \text{min}$ , $t_{CK} = \text{min}$ One bank active Output pin open Addresses changed up to 1-time during $t_{RC}$ (min) $0 \text{ V} \leq V_{IN} \leq V_{IL \text{ max}}$ $V_{IH \text{ min}} \leq V_{IN} \leq V_{CC}$	—	165	mA
	MB81F643242C-70				155	
	MB81F643242C-10				115	
	Reference Value *4 @67MHz (CL=3)				100	
Precharge Standby Current (Power Supply Current)		$I_{CC2P}$	CKE = $V_{IL}$ All banks idle $t_{CK} = \text{min}$ Power down mode $0 \text{ V} \leq V_{IN} \leq V_{IL \text{ max}}$ $V_{IH \text{ min}} \leq V_{IN} \leq V_{CC}$	—	2	mA
		$I_{CC2PS}$	CKE = $V_{IL}$ All banks idle CLK = $V_{IH}$ or $V_{IL}$ Power down mode $0 \text{ V} \leq V_{IN} \leq V_{IL \text{ max}}$ $V_{IH \text{ min}} \leq V_{IN} \leq V_{CC}$	—	1	mA
		$I_{CC2N}$	CKE = $V_{IH}$ All banks idle, $t_{CK} = 15 \text{ ns}$ NOP commands only, Input signals (except to CMD) are changed 1 time during 30 ns $0 \text{ V} \leq V_{IN} \leq V_{IL \text{ max}}$ $V_{IH \text{ min}} \leq V_{IN} \leq V_{CC}$	—	12	mA
		$I_{CC2NS}$	CKE = $V_{IH}$ All banks idle CLK = $V_{IH}$ or $V_{IL}$ Input signal are stable $0 \text{ V} \leq V_{IN} \leq V_{IL \text{ max}}$ $V_{IH \text{ min}} \leq V_{IN} \leq V_{CC}$	—	2	mA

(Continued)

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Active Standby Current (Power Supply Current)		$I_{CC3P}$	CKE = $V_{IL}$ Any bank active $t_{CK} = \min$ $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \min} \leq V_{IN} \leq V_{CC}$	—	2	mA
		$I_{CC3PS}$	CKE = $V_{IL}$ Any bank active CLK = $V_{IH}$ or $V_{IL}$ $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \min} \leq V_{IN} \leq V_{CC}$	—	1	mA
		$I_{CC3N}$	CKE = $V_{IH}$ Any bank active $t_{CK} = 15 \text{ ns}$ NOP commands only, Input signals (except to CMD) are changed 1 time during 30 ns $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \min} \leq V_{IN} \leq V_{CC}$	—	25	mA
		$I_{CC3NS}$	CKE = $V_{IH}$ Any bank idle CLK = $V_{IH}$ or $V_{IL}$ Input signals are stable $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \min} \leq V_{IN} \leq V_{CC}$	—	2	mA
Burst mode Current (Average Power Supply Current)	MB81F643242C-60	$I_{CC4}$	$t_{CK} = \min$ Burst Length = 4 Output pin open All banks active Gapless data $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \max} \leq V_{IN} \leq V_{CC}$	—	305	mA
	MB81F643242C-70				260	
	MB81F643242C-10				185	
	Reference Value *4 @67MHz (CL=3)				125	
Refresh Current #1 (Average Power Supply Current)	MB81F643242C-60	$I_{CC5}$	Auto-refresh; $t_{CK} = \min$ $t_{RC} = \min$ $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \max} \leq V_{IN} \leq V_{CC}$	—	235	mA
	MB81F643242C-70				220	
	MB81F643242C-10				155	
	Reference Value *4 @67MHz (CL=3)				125	
Refresh Current #2 (Average Power Supply Current)		$I_{CC6}$	Self-refresh; $t_{CK} = \min$ CKE $\leq 0.2 V$ $0 V \leq V_{IN} \leq V_{IL \max}$ $V_{IH \max} \leq V_{IN} \leq V_{CC}$	—	2	mA

- Notes:**
- \*1. All voltage are referenced to  $V_{SS}$ .
  - \*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure in section "■ FUNCTIONAL DESCRIPTION".
  - \*3.  $I_{CC}$  depends on the output termination or load conditions, clock cycle rate, signal clocking rate. The specified values are obtained with the output open and no termination register.
  - \*4. This value is for reference only.

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note \*1, 2, and \*3

Parameter	Notes	Symbol	MB81F643242C -60		MB81F643242C -70		MB81F643242C -10		Reference Value *4 @67MHz, CL=3		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period	CL = 2	t <sub>CK2</sub>	10	—	10	—	15	—	20	—	ns
	CL = 3	t <sub>CK3</sub>	6	—	7	—	10	—	15	—	ns
Clock High Time	*5	t <sub>CH</sub>	2.5	—	2.5	—	3	—	4	—	ns
Clock Low Time	*5	t <sub>CL</sub>	2.5	—	2.5	—	3	—	4	—	ns
Input Setup Time	*5	t <sub>SI</sub>	1.5	—	2	—	2	—	3	—	ns
Input Hold Time	*5	t <sub>HI</sub>	1	—	1	—	1	—	1	—	ns
Access Time from Clock (t <sub>CK</sub> = min)	CL = 2	t <sub>AC2</sub>	—	6	—	6	—	7	—	7	ns
	CL = 3	t <sub>AC3</sub>	—	5.5	—	5.5	—	7	—	7	ns
Output in Low-Z	*5	t <sub>LZ</sub>	1	—	1	—	1	—	1	—	ns
Output in High-Z	CL = 2	t <sub>HZ2</sub>	2.5	6	2.5	6	3	7	3	7	ns
	CL = 3	t <sub>HZ3</sub>		5.5		5.5		7		7	ns
Output Hold Time	CL = 2	t <sub>OH</sub>	2.5	—	2.5	—	3	—	3	—	ns
	CL = 3										ns
Time between Auto-Refresh command interval	*4	t <sub>REFI</sub>	—	15.6	—	15.6	—	15.6	—	15.6	μs
Time between Refresh		t <sub>REF</sub>	—	64	—	64	—	64	—	64	ms
Transition Time		t <sub>T</sub>	0.5	10	0.5	10	0.5	10	0.5	10	ns
CKE Setup Time for Power Down Exit Time	*5	t <sub>CKSP</sub>	1.5	—	2	—	3	—	3	—	ns

# MB81F643242C-60/-70/-10 Advanced Info (AE0.1E)

## BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter Notes	Symbol	MB81F643242C-60		MB81F643242C-70		MB81F643242C-10		Reference Value *4 @67MHz, CL=3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{\text{RAS}}$ Cycle Time *9	$t_{\text{RC}}$	60	—	63	—	90	—	110	—	ns
$\overline{\text{RAS}}$ Precharge Time	$t_{\text{RP}}$	18	—	20	—	30	—	40	—	ns
$\overline{\text{RAS}}$ Active Time	$t_{\text{RAS}}$	42	110K	42	110K	60	110K	70	110K	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	$t_{\text{RCD}}$	18	—	20	—	30	—	30	—	ns
Write Recovery Time	$t_{\text{WR}}$	6	—	7	—	10	—	15	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ Bank Active Delay Time	$t_{\text{RRD}}$	12	—	14	—	20	—	30	—	ns
Data-in to Precharge Lead Time	$t_{\text{DPL}}$	7	—	7	—	10	—	15	—	ns
Data-in to Active/Refresh Command Period	CL=2	$t_{\text{DAL2}}$	1 cyc + $t_{\text{RP}}$	—	1 cyc + $t_{\text{RP}}$	—	1 cyc + $t_{\text{RP}}$	—	1 cyc + $t_{\text{RP}}$	ns
	CL=3	$t_{\text{DAL3}}$	2 cyc + $t_{\text{RP}}$	—	2 cyc + $t_{\text{RP}}$	—	2 cyc + $t_{\text{RP}}$	—	2 cyc + $t_{\text{RP}}$	ns
Mode Resister Set Cycle Time	$t_{\text{RSC}}$	12	—	14	—	20	—	30	—	ns

## CLOCK COUNT FORMULA Note \*10

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad (\text{Round off a whole number})$$

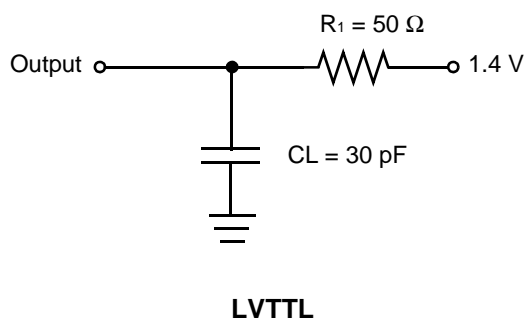
## LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	MB81F643242C -60	MB81F643242C -70	MB81F643242C -10	Unit
CKE to Clock Disable		I <sub>CKE</sub>	1	1	1	cycle
DQM to Output in High-Z		I <sub>DQZ</sub>	2	2	2	cycle
DQM to Input Data Delay		I <sub>DQD</sub>	0	0	0	cycle
Last Output to Write Command Delay		I <sub>OWD</sub>	2	2	2	cycle
Write Command to Input Data Delay		I <sub>DWD</sub>	0	0	0	cycle
Precharge to Outputting High-Z Delay	CL = 2	I <sub>ROH2</sub>	2	2	2	cycle
	CL = 3	I <sub>ROH3</sub>	3	3	3	cycle
Burst Stop Command to Output in High-Z Delay	CL = 2	I <sub>BSH2</sub>	2	2	2	cycle
	CL = 3	I <sub>BSH3</sub>	3	3	3	cycle
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay (min)		I <sub>CCD</sub>	1	1	1	cycle
$\overline{\text{CAS}}$ Bank Delay (min)		I <sub>CBD</sub>	1	1	1	cycle

- Notes:**
- \*1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure in section "■ FUNCTIONAL DESCRIPTION".
  - \*2. AC characteristics assume  $t_r = 1$  ns and 30 pF of capacitive load.
  - \*3. 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max). (See Fig. 5)
  - \*4. This value is for reference only.
  - \*5. If input signal transition time ( $t_r$ ) is longer than 1 ns;  $[(t_r/2) - 0.5]$  ns should be added to  $t_{AC}$  (max),  $t_{HZ}$  (max), and  $t_{CKSP}$  (min) spec values,  $[(t_r/2) - 0.5]$  ns should be subtracted from  $t_{LZ}$  (min),  $t_{HZ}$  (min), and  $t_{OH}$  (min) spec values, and  $(t_r - 1.0)$  ns should be added to  $t_{CH}$  (min),  $t_{CL}$  (min),  $t_{SI}$  (min), and  $t_{HI}$  (min) spec values.
  - \*6.  $t_{AC}$  also specifies the access time at burst mode.
  - \*7.  $t_{AC}$  and  $t_{OH}$  are the specs value under OUTPUT LOAD CIRCUIT shown in Fig. 4.
  - \*8. Specified where output buffer is no longer driven.
  - \*9. Actual clock count of  $t_{RC}$  ( $I_{RC}$ ) will be sum of clock count of  $t_{RAS}$  ( $I_{RAS}$ ) and  $t_{RP}$  ( $I_{RP}$ ).
  - \*10. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off to a whole number).

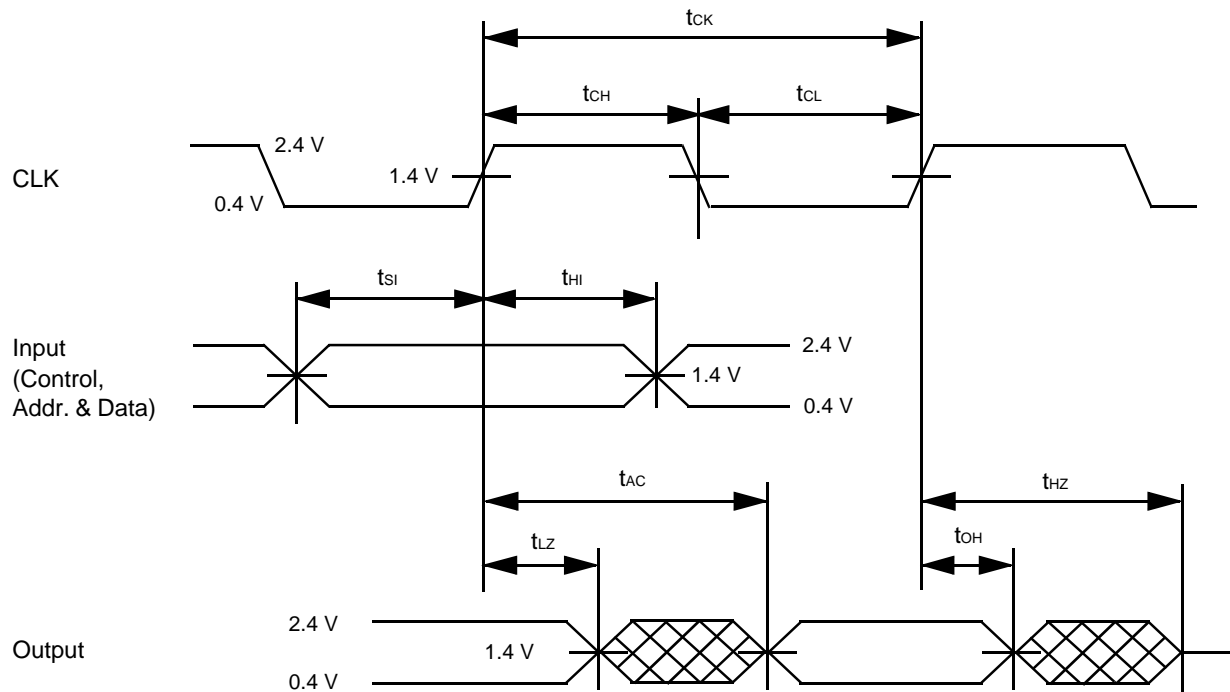
Fig. 4 – OUTPUT LOAD CIRCUIT



**Note:** By adding appropriate correlation factors to the test conditions,  $t_{AC}$  and  $t_{OH}$  measured when the Output is coupled to the Output Load Circuit are within specifications.



**Fig. 5 – TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME**



**Note:** Reference level of input signal is 1.4 V for LVTTTL.  
Access time is measured at 1.4 V for LVTTTL.

**Fig. 6 – TIMING DIAGRAM, DELAY TIME FOR POWER DOWN EXIT**

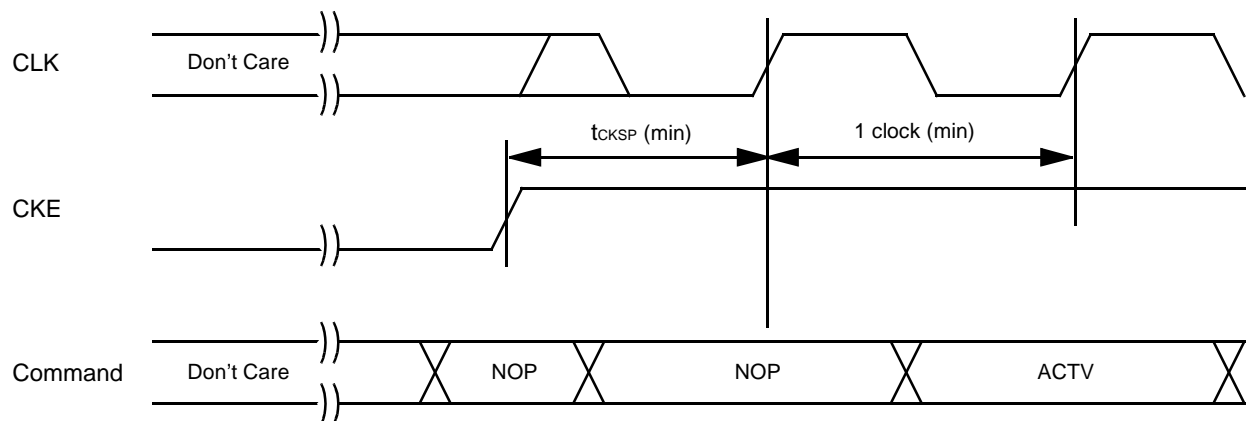
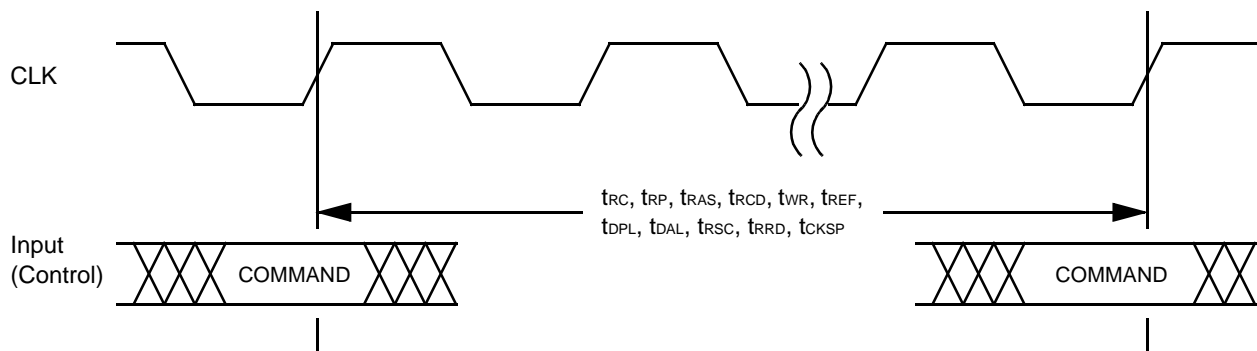
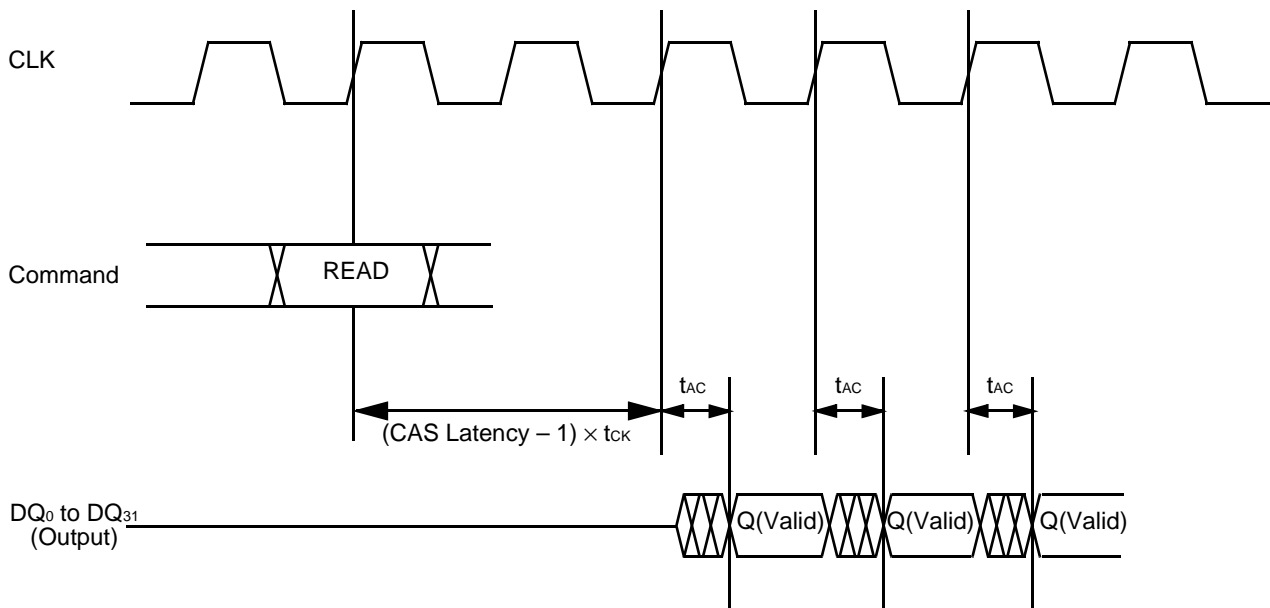


Fig. 7 – TIMING DIAGRAM, PULSE WIDTH



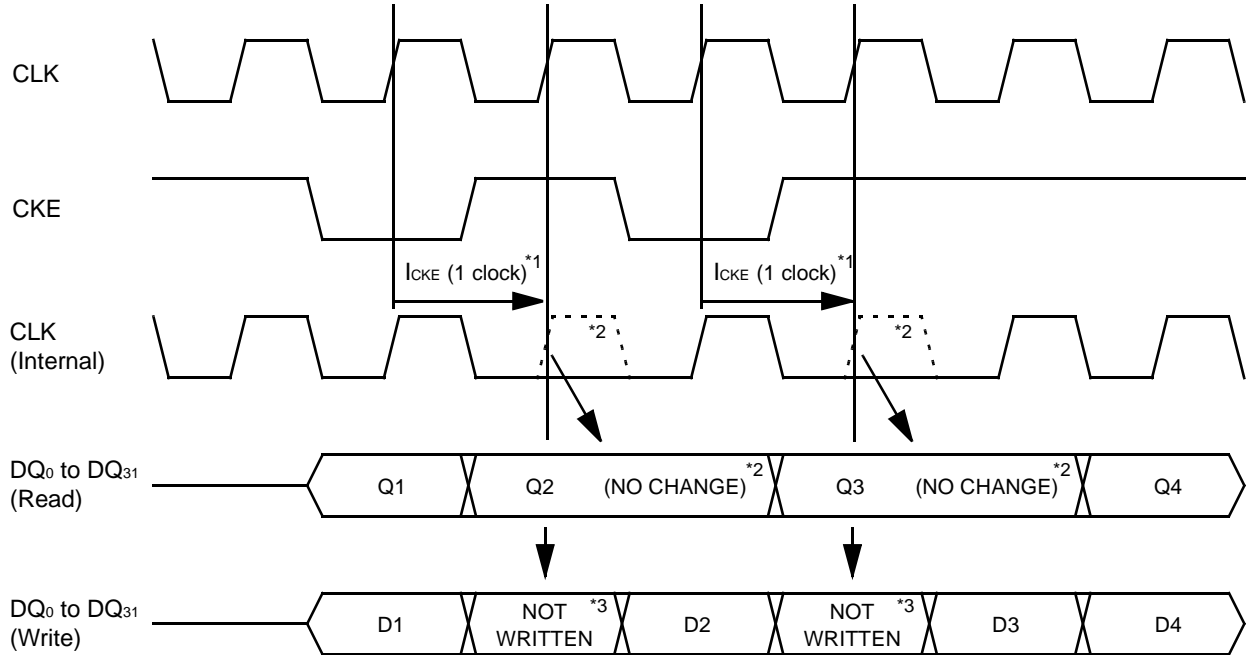
**Note:** These parameters are a limit value of the rising edge of the clock from one command input to next input.  $t_{CKSP}$  is the latency value from the rising edge of CKE.  
Measurement reference voltage is 1.4 V.

Fig. 8 – TIMING DIAGRAM, ACCESS TIME



## ■ TIMING DIAGRAMS

**TIMING DIAGRAM – 1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)**

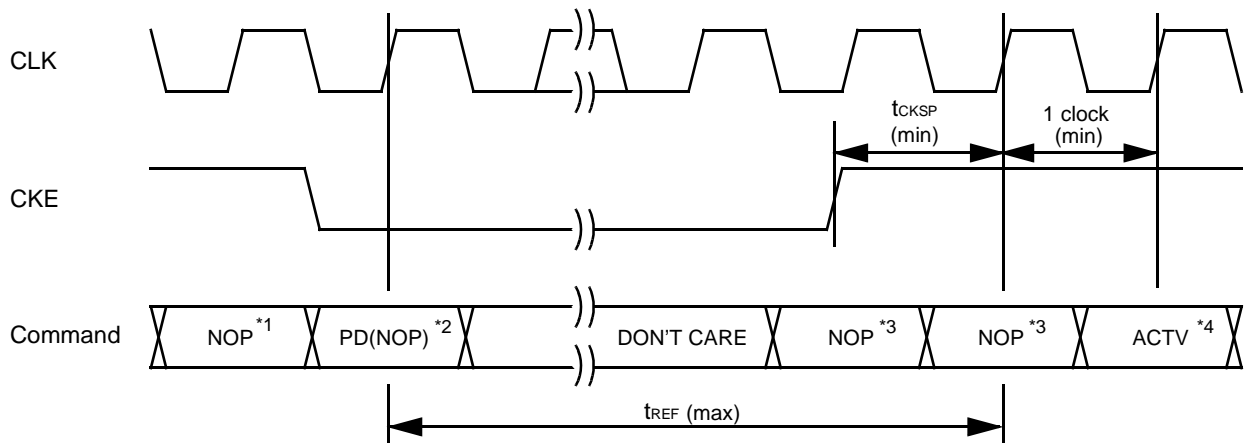


**Notes:** \*1. The latency of CKE (l<sub>CKE</sub>) is one clock.

\*2. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output data remain the same data.

\*3. During the write mode, data at the next clock of CSUS command is ignored.

**TIMING DIAGRAM – 2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT**



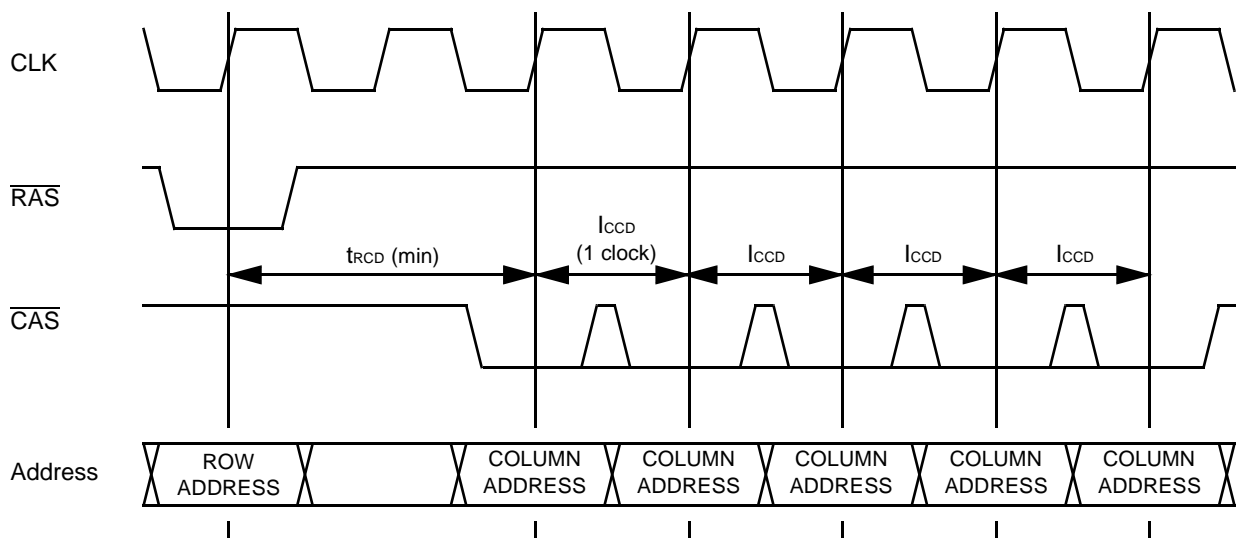
**Notes:** \*1. Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.

\*2. Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.

\*3. It is recommended to apply NOP command in conjunction with CKE.

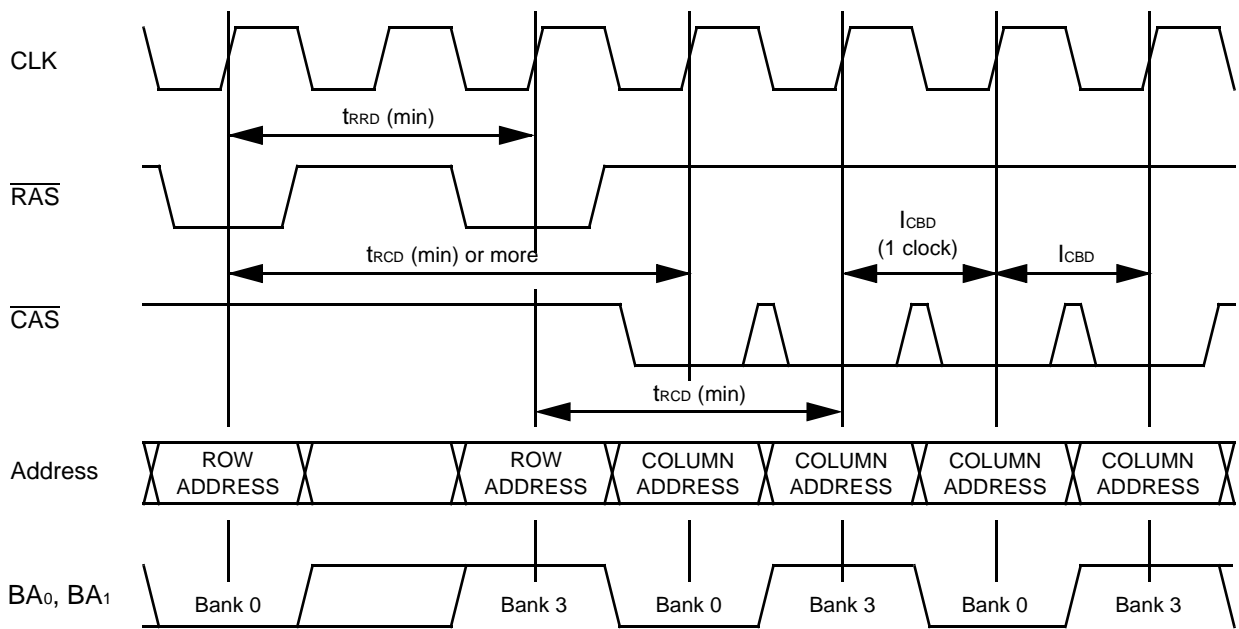
\*4. The ACTV command can be latched after t<sub>CKSP</sub> (min) + 1 clock (min).

TIMING DIAGRAM – 3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



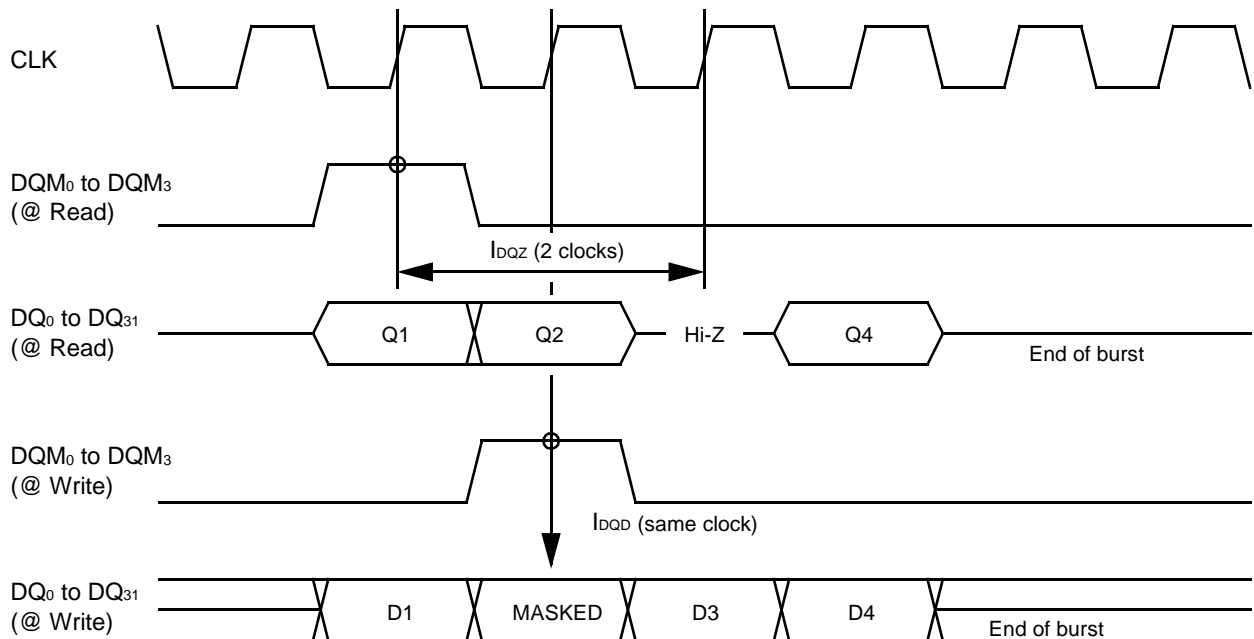
**Note:**  $\overline{CAS}$  to  $\overline{CAS}$  delay can be one or more clock period.

TIMING DIAGRAM – 4 : DIFFERENT BANK ADDRESS INPUT DELAY

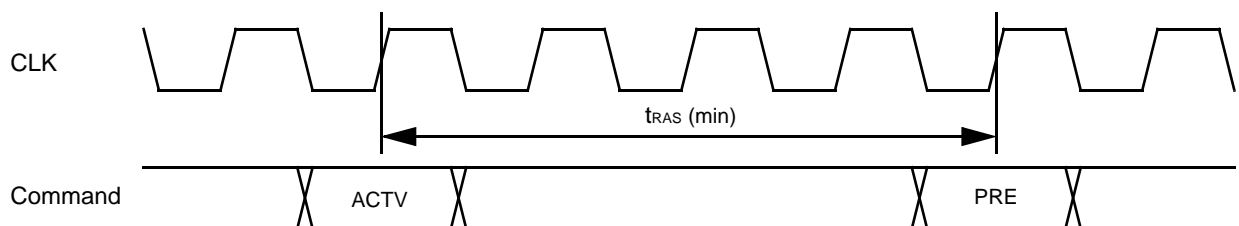


**Note:**  $\overline{CAS}$  Bank delay can be one or more clock period.

**TIMING DIAGRAM – 5 : DQM<sub>0</sub> - DQM<sub>3</sub> - INPUT MASK AND OUTPUT DISABLE (@ BL = 4)**

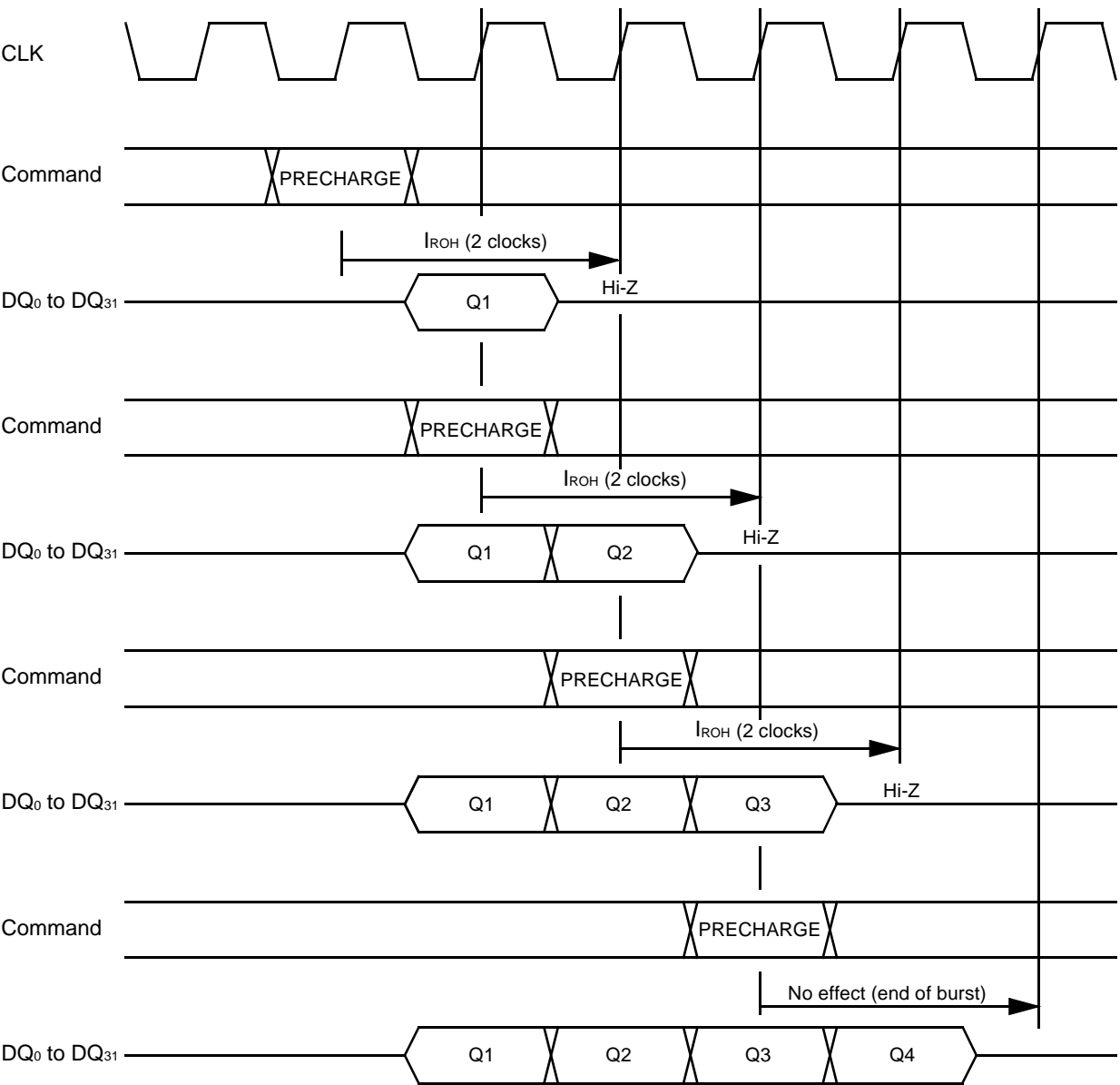


**TIMING DIAGRAM – 6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)**



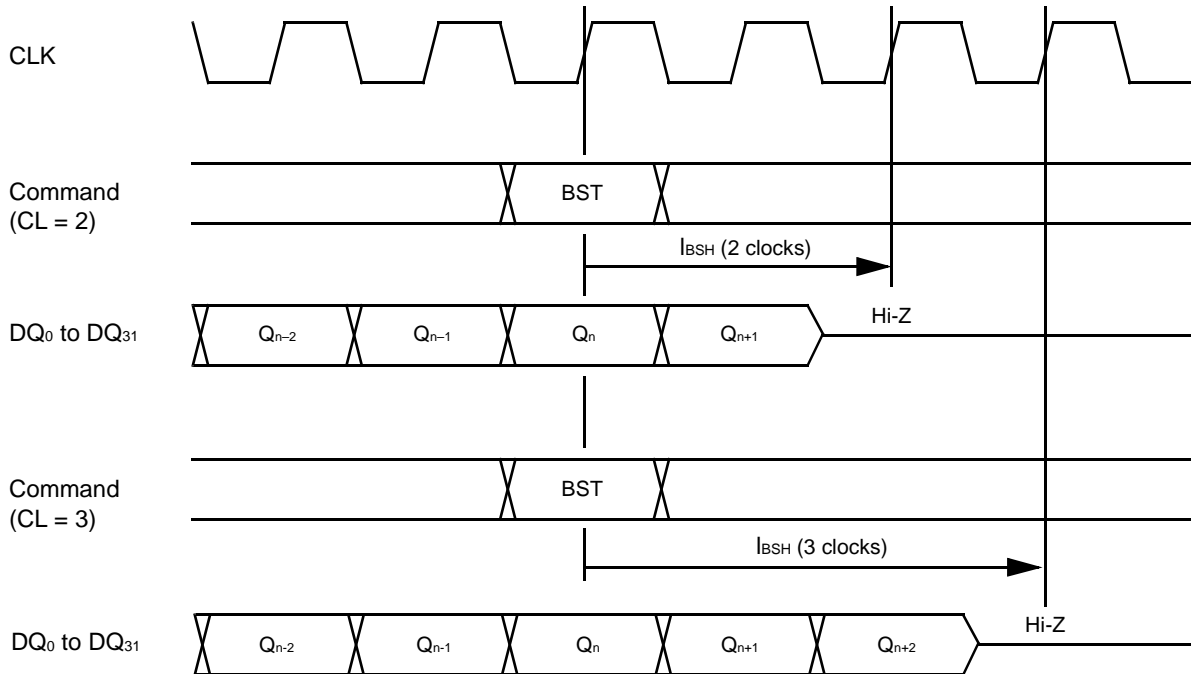
**Note:** PRECHARGE means 'PRE' or 'PALL'.

TIMING DIAGRAM – 7 : READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)

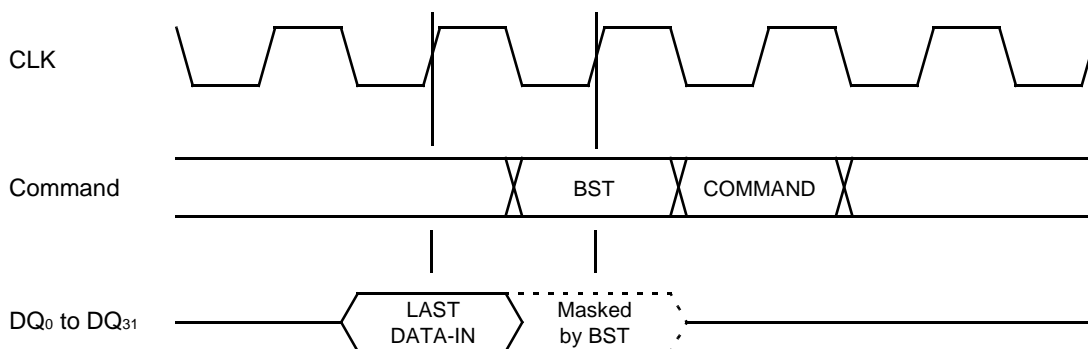


**Note:** In case of CL = 2, the I<sub>ROH</sub> is 2 clocks.  
In case of CL = 3, the I<sub>ROH</sub> is 3 clocks.  
PRECHARGE means 'PRE' or 'PALL'.

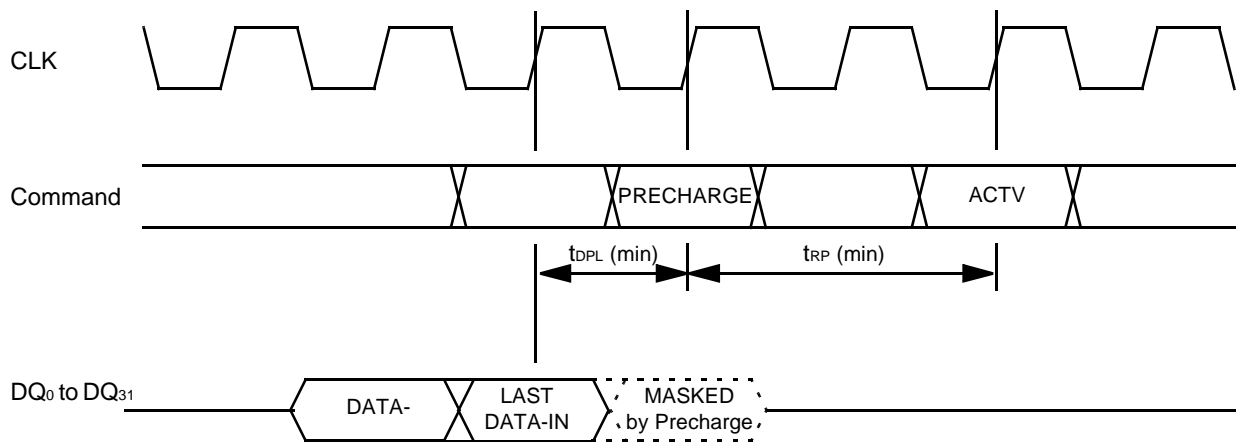
**TIMING DIAGRAM – 8 : READ INTERRUPTED BY BURST STOP (EXAMPLE @ BL = Full Column)**



**TIMING DIAGRAM – 9 : WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ BL = 2)**

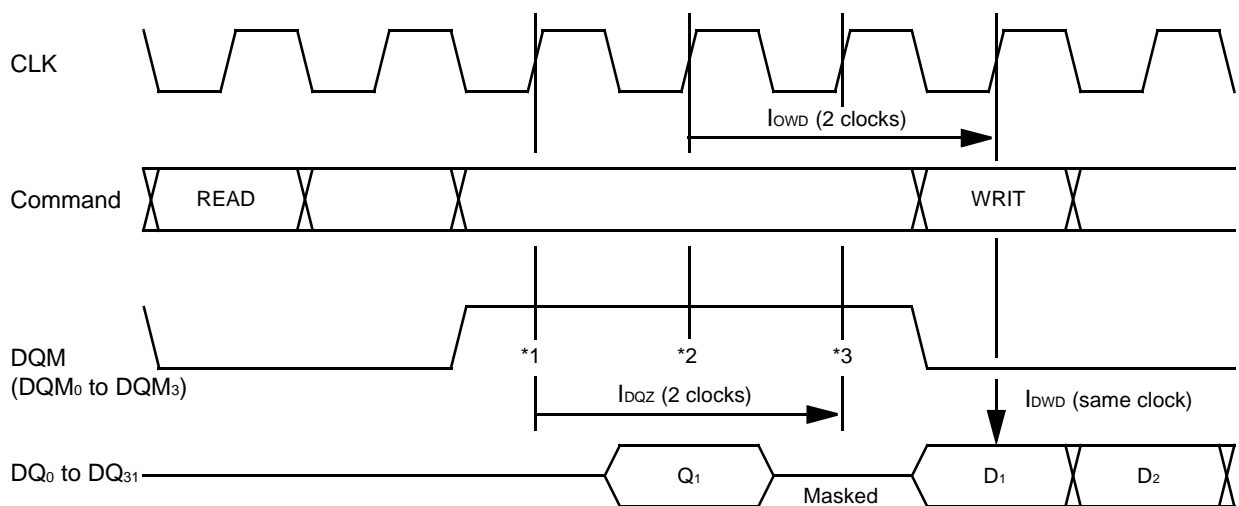


**TIMING DIAGRAM – 10 : WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 3)**



**Note:** The precharge command (PRE) should only be issued after the  $t_{DPL}$  of final data input is satisfied. PRECHARGE means 'PRE' or 'PALL'.

**TIMING DIAGRAM – 11 : READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 3, BL = 4)**

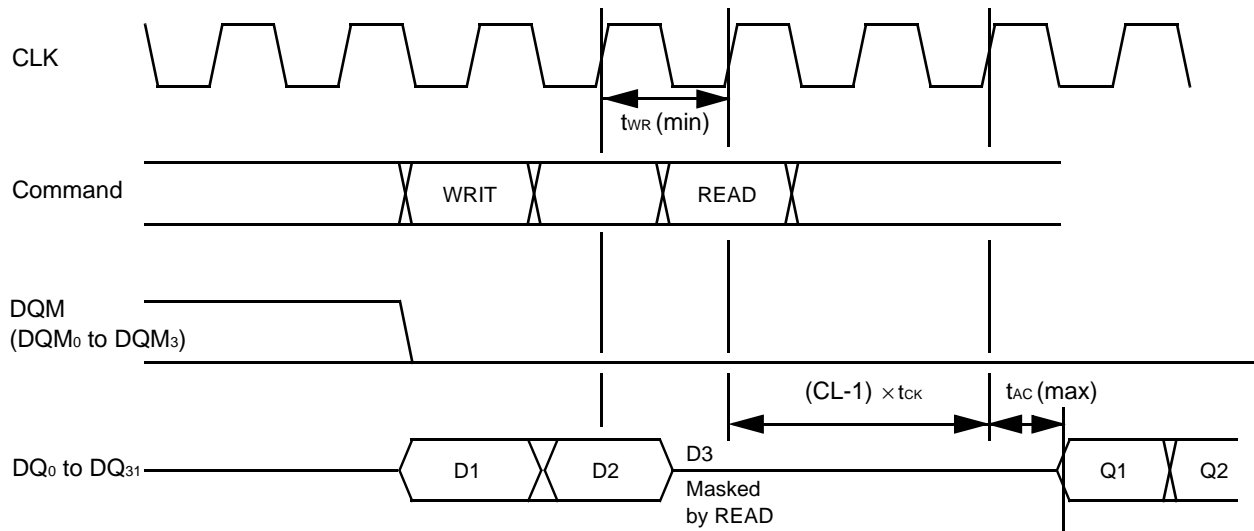


**Notes:**

- \*1. First DQM makes high-impedance state High-Z between last output and first input data.
- \*2. Second DQM makes internal output data mask to avoid bus contention.
- \*3. Third DQM in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

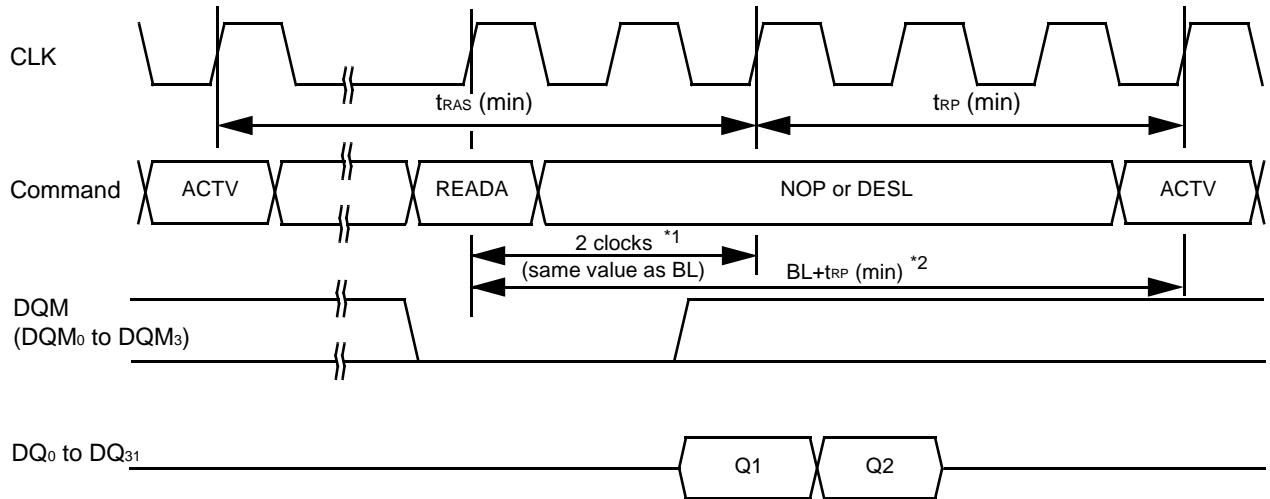


**TIMING DIAGRAM – 12 : WRITE TO READ TIMING (EXAMPLE @ CL = 3, BL = 4)**



**Note:** Read command should be issued after  $t_{WR}$  of final data input is satisfied.

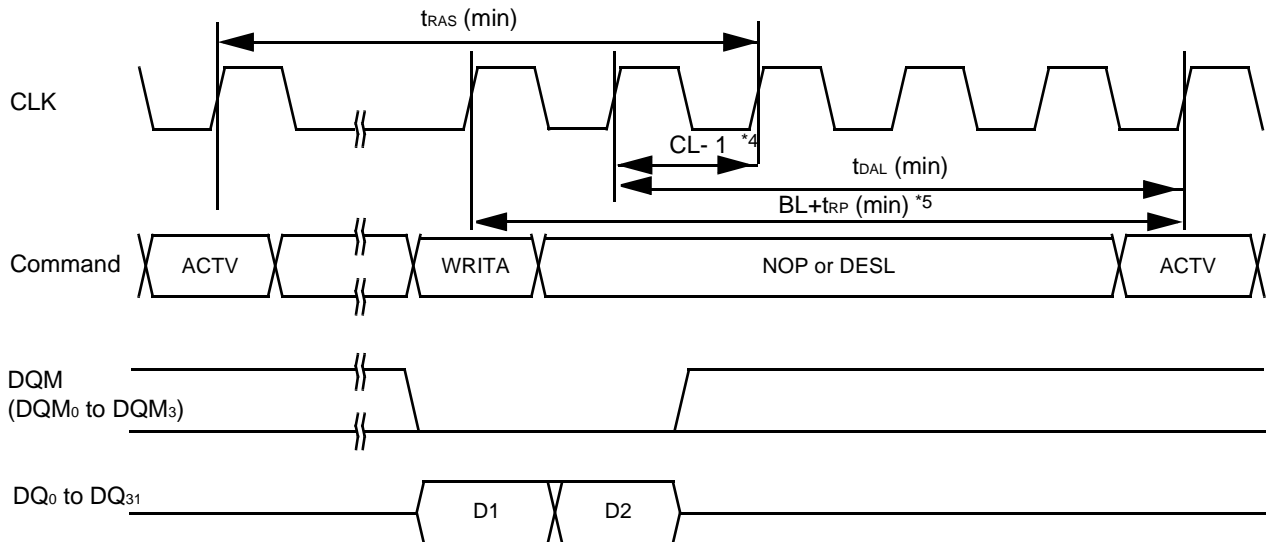
**TIMING DIAGRAM – 13 : READ WITH AUTO-PRECHARGE  
(EXAMPLE @ CL = 2, BL = 2 Applied to same bank)**



**Notes:** \*1. Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.

\*2. Next ACTV command should be issued after BL+t<sub>RP</sub> (min) from READA command.

**TIMING DIAGRAM – 14 : WRITE WITH AUTO-PRECHARGE \*1, \*2, and \*3  
(EXAMPLE @ CL = 2, BL = 2 Applied to same bank)**



**Notes:** \*1. Even if the final data is masked by DQM, the precharge does not start the clock of final data input.

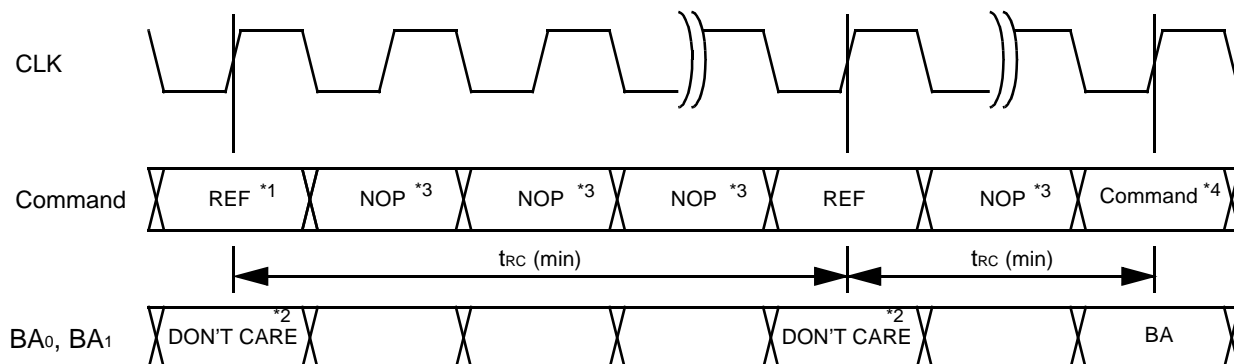
\*2. Once auto precharge command is asserted, no new command within the same bank can be issued.

\*3. Auto-precharge command doesn't affect at full column burst operation except Burst READ & Single Write.

\*4. Precharge at write with Auto-precharge is started after the CL - 1 from the end of burst.

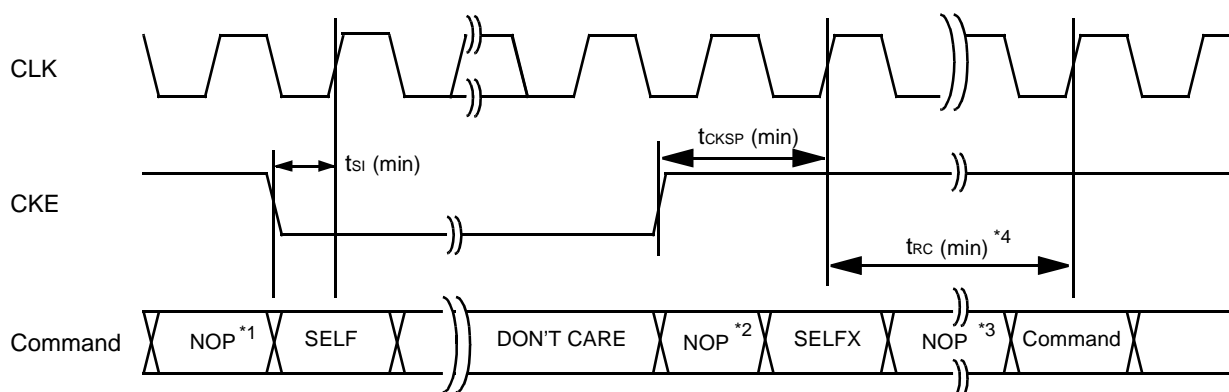
\*5. Next command should be issued after BL+ t<sub>RP</sub> (min) at CL = 2, BL+1+t<sub>RP</sub> (min) at CL = 3 from WRITA command.

**TIMING DIAGRAM – 15 : AUTO-REFRESH TIMING**



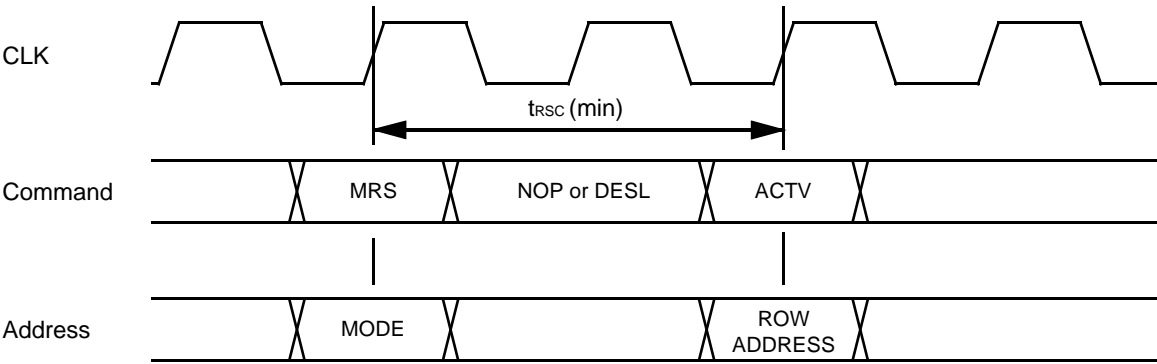
- Notes:**
- \*1. All banks should be precharged prior to the first Auto-refresh command (REF).
  - \*2. Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
  - \*3. Either NOP or DESL command should be asserted during t<sub>RC</sub> period while Auto-refresh mode.
  - \*4. Any activation command such as ACTV or MRS command other than REF command should be asserted after t<sub>RC</sub> from the last REF command.

**TIMING DIAGRAM – 16 : SELF-REFRESH ENTRY AND EXIT TIMING**



- Notes:**
- \*1. Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).
  - \*2. The Self-refresh Exit command (SELF<sub>X</sub>) is latched after t<sub>CKSP</sub> (min). It is recommended to apply NOP command in conjunction with CKE.
  - \*3. Either NOP or DESL command can be used during t<sub>RC</sub> period.
  - \*4. CKE should be held high within one t<sub>RC</sub> period after t<sub>CKSP</sub>.

TIMING DIAGRAM – 17 : MODE REGISTER SET TIMING

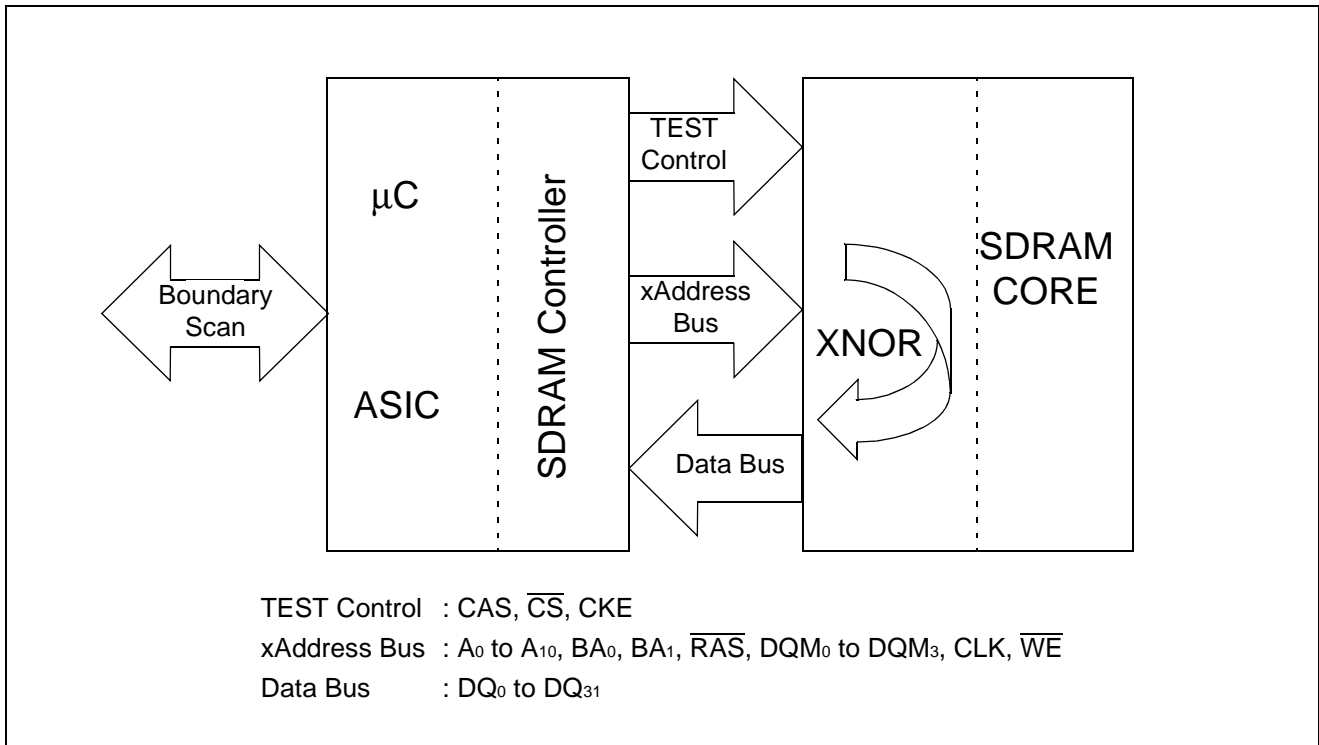


**Notes:** The Mode Register Set command (MRS) should only be asserted after all banks have been precharged.

## ■ SCITT TEST MODE

### ABOUT SCITT

SCITT (Static Component Interconnection Test Technology) is an XNOR circuit based test technology that is used for testing interconnection between SDRAM and SDRAM controller on the printed circuit boards. SCITT provides inexpensive board level test mode in combination with boundary-scan. The basic idea is simple, consider all output of SDRAM as output of XNOR circuit and each output pin has a unique mapping on the input of SDRAM. The ideal schematic block diagram is as shown below.



It is static and provides easy test pattern that result in a high diagnostic resolution for detecting all open/short faults. The MB81F643242C adopts SCITT as an optional function. See Package and "Ordering Information" in section "■ PACKAGE".

## SCITT TEST SEQUENCE

The followings are the SCITT test sequence. SCITT Test can be executed after power-on and prior to Precharge command in POWER-UP INITIALIZATION. Once Precharge command is issued to SDRAM, it never get back to SCITT Test Mode during regular operation for the purpose of a fail-safe way in get in and out of test mode.

1. Apply power. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power for a minimum of 100us.
3. Enter SCITT test mode.
4. Execute SCITT test.
5. Exit from SCITT mode.

It is required to follow Power On Sequence to execute read or write operation.

6. Start clock. Attempt to maintain either NOP or DESL command at the input.
7. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
8. Assert minimum of 2 Auto-Refresh command (REF).
9. Program the mode register by Mode Register Set command (MRS).

The 3,4,5 steps define the SCITT mode available. It is possible to skip these steps if necessary (Refer to POWER-UP INITIALIZATION).

## COMMAND TRUTH TABLE Note \*1

	Control			Input					Output
	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	A <sub>0</sub> to A <sub>10</sub> BA <sub>0</sub> , BA <sub>1</sub>	DQM <sub>0</sub> to DQM <sub>3</sub>	CLK	DQ <sub>0</sub> to DQ <sub>31</sub>
SCITT mode entry	H→L *2	L	L	X	X	X	X	X	X
SCITT mode exit	L→H *3	H *5	L *5	X	X	X	X	X	X
SCITT mode output enable *4	L	L	H	V	V	V	V	V	V

**Notes:** \*1. L = Logic Low, H = Logic High, V = Valid, X = either L or H

\*2. The SCITT mode entry command assumes the first  $\overline{\text{CAS}}$  falling edge with  $\overline{\text{CS}}$  and CKE = L after power on.

\*3. The SCITT mode exit command assumes the first  $\overline{\text{CAS}}$  rising edge after the test mode entry.

\*4. Refer the test code table.

\*5.  $\overline{\text{CS}}$  = H or CKE = L is necessary to disable outputs in SCITT mode exit.

## MB81F643242C-60/-70/-10 Advanced Info (AE0.1E)

## TEST CODE TABLE

DQ<sub>0</sub> to DQ<sub>31</sub> output data is static and is determined by following logic during the SCITT mode operation.

$DQ_0 = \overline{RAS} \text{ xnor } A_0$	$DQ_{11} = \overline{RAS} \text{ xnor } BA_1$	$DQ_{22} = A_0 \text{ xnor } A_4$
$DQ_1 = \overline{RAS} \text{ xnor } A_1$	$DQ_{12} = \overline{RAS} \text{ xnor } BA_0$	$DQ_{23} = A_0 \text{ xnor } A_5$
$DQ_2 = \overline{RAS} \text{ xnor } A_2$	$DQ_{13} = \overline{RAS} \text{ xnor } DQM_0$	$DQ_{24} = A_0 \text{ xnor } A_6$
$DQ_3 = \overline{RAS} \text{ xnor } A_3$	$DQ_{14} = \overline{RAS} \text{ xnor } DQM_1$	$DQ_{25} = A_0 \text{ xnor } A_7$
$DQ_4 = \overline{RAS} \text{ xnor } A_4$	$DQ_{15} = \overline{RAS} \text{ xnor } DQM_2$	$DQ_{26} = A_0 \text{ xnor } A_8$
$DQ_5 = \overline{RAS} \text{ xnor } A_5$	$DQ_{16} = \overline{RAS} \text{ xnor } DQM_3$	$DQ_{27} = A_0 \text{ xnor } A_9$
$DQ_6 = \overline{RAS} \text{ xnor } A_6$	$DQ_{17} = \overline{RAS} \text{ xnor } CLK$	$DQ_{28} = A_0 \text{ xnor } A_{10}$
$DQ_7 = \overline{RAS} \text{ xnor } A_7$	$DQ_{18} = \overline{RAS} \text{ xnor } \overline{WE}$	$DQ_{29} = A_0 \text{ xnor } BA_1$
$DQ_8 = \overline{RAS} \text{ xnor } A_8$	$DQ_{19} = A_0 \text{ xnor } A_1$	$DQ_{30} = A_0 \text{ xnor } BA_0$
$DQ_9 = \overline{RAS} \text{ xnor } A_9$	$DQ_{20} = A_0 \text{ xnor } A_2$	$DQ_{31} = A_0 \text{ xnor } DQM_0$
$DQ_{10} = \overline{RAS} \text{ xnor } A_{10}$	$DQ_{21} = A_0 \text{ xnor } A_3$	

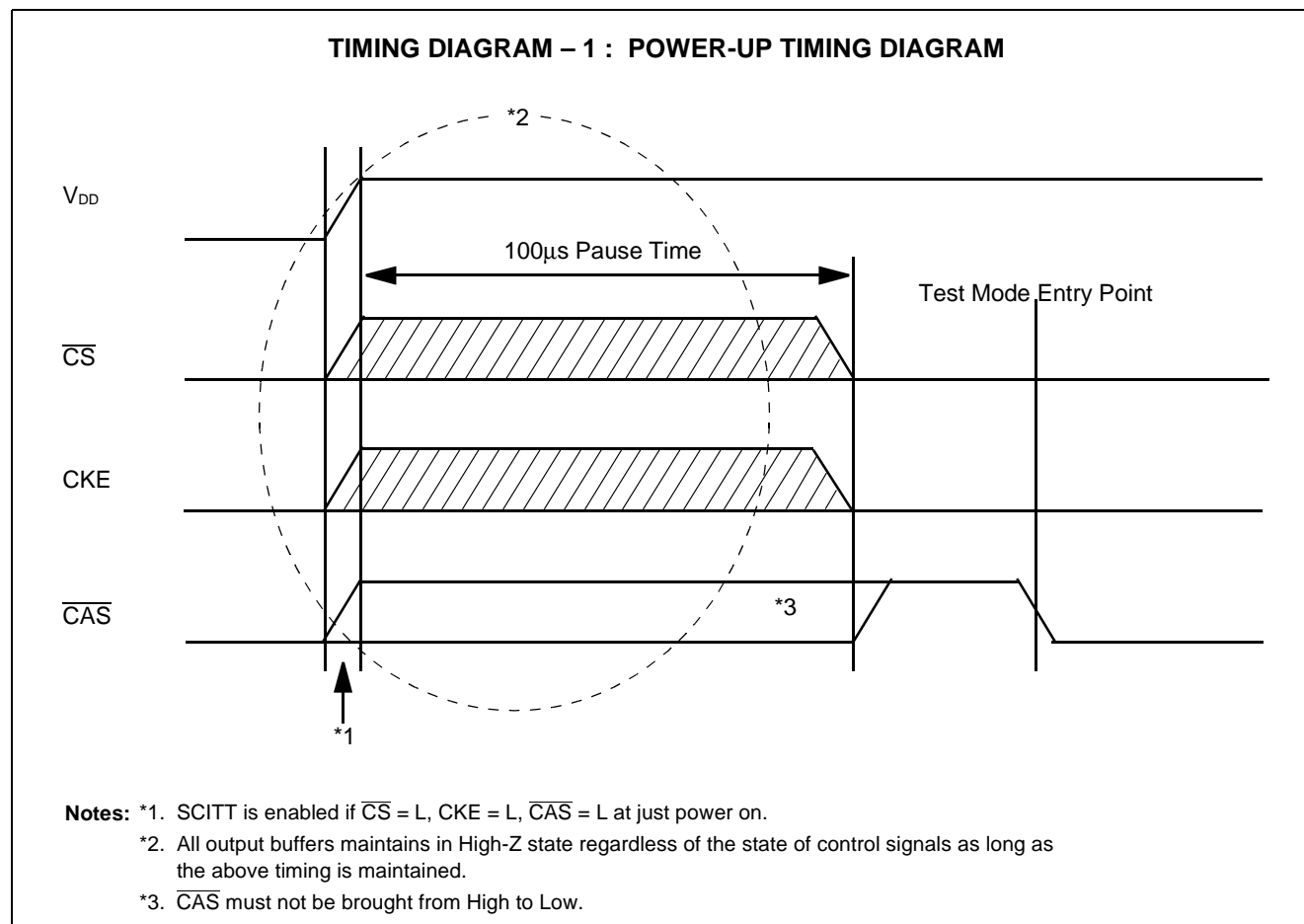
- EXAMPLE OF TEST CODE TABLE

[illegible]

## AC SPECIFICATION

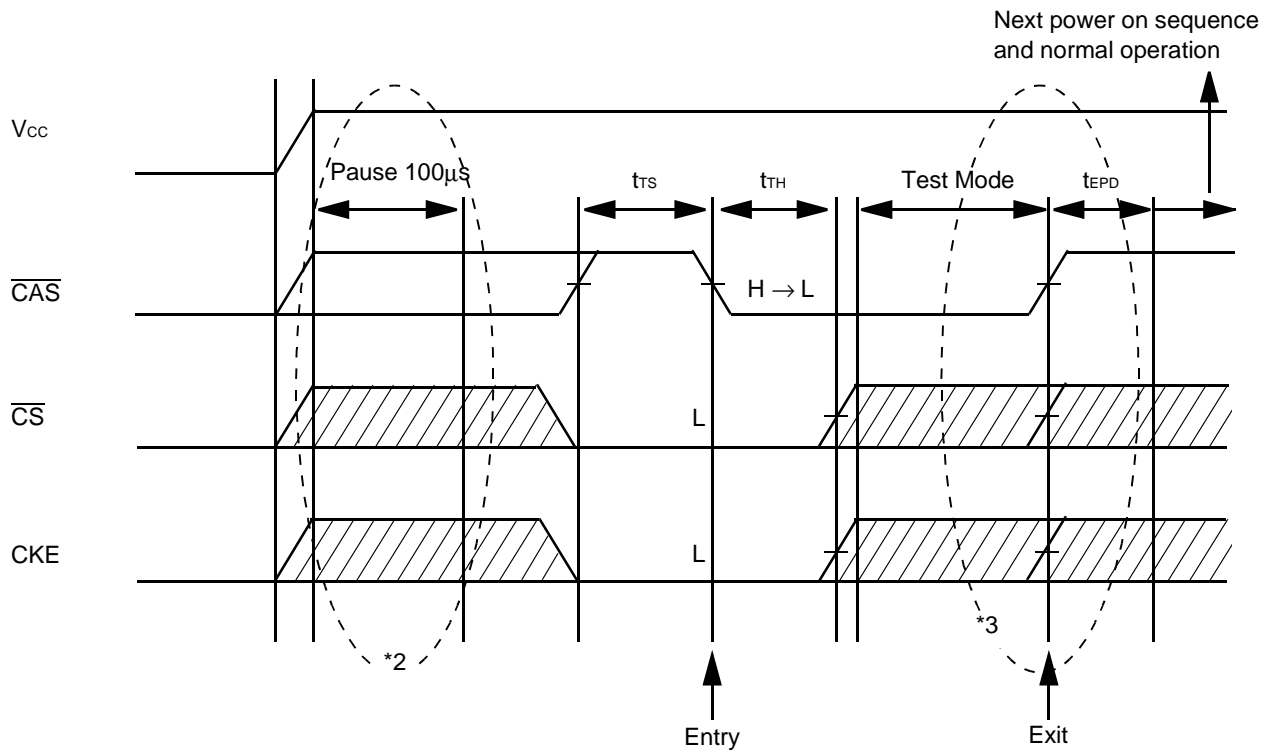
Parameter	Description	Minimum	Maximum	Units
$t_{TS}$	Test mode entry set up time	10	—	ns
$t_{TH}$	Test mode entry hold time	10	—	ns
$t_{EPD}$	Test mode exit to power on sequence delay time	10	—	ns
$t_{TLZ}$	Test mode output in Low-Z time	0	—	ns
$t_{THZ}$	Test mode output in High-Z time	0	20	ns
$t_{TCA}$	Test mode access time from control signals (output enable & chip select)	—	40	ns
$t_{TIA}$	Test mode Input access time	—	20	ns
$t_{TOH}$	Test mode Output Hold time	0	—	ns
$t_{ETD}$	Test mode entry to test delay time	10	—	ns
$t_{TIH}$	Test mode input hold time	30	—	ns

## TIMING DIAGRAMS





**TIMING DIAGRAM – 2 : SCITT TEST ENTRY AND EXIT \*1**

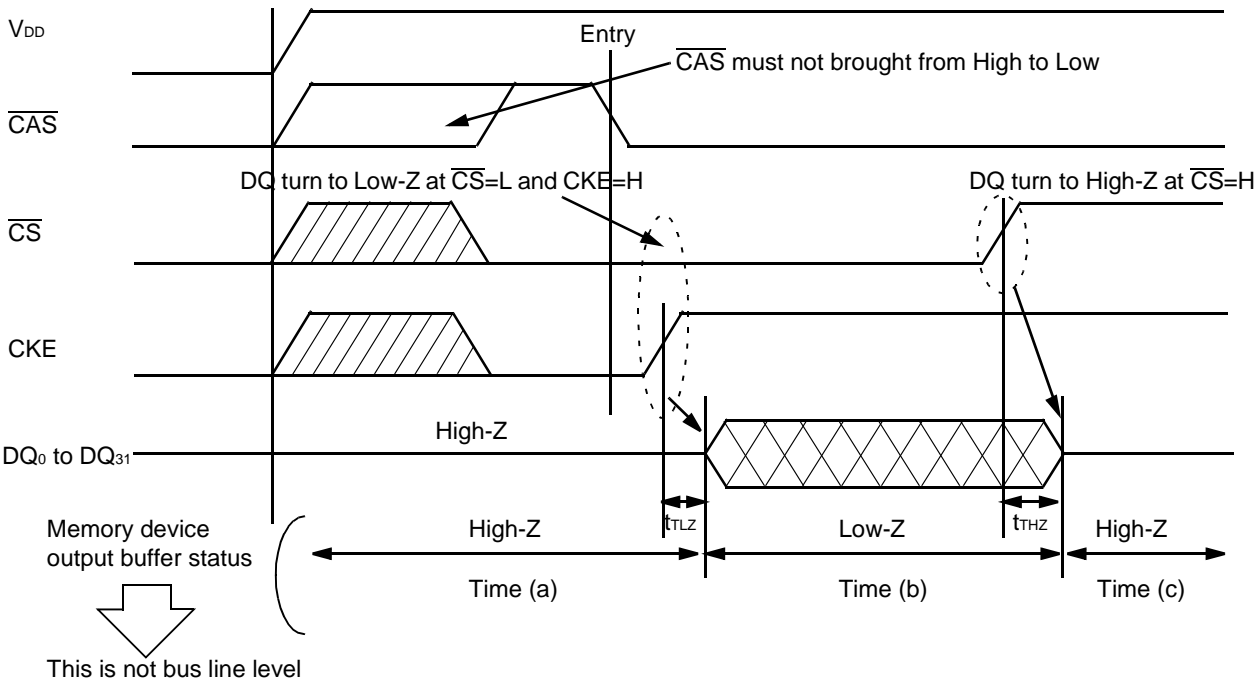


**Notes:** \*1. If entry and exit operation have not been done correctly,  $\overline{CAS}$ ,  $\overline{CS}$ ,  $CKE$  pins will have some problems.

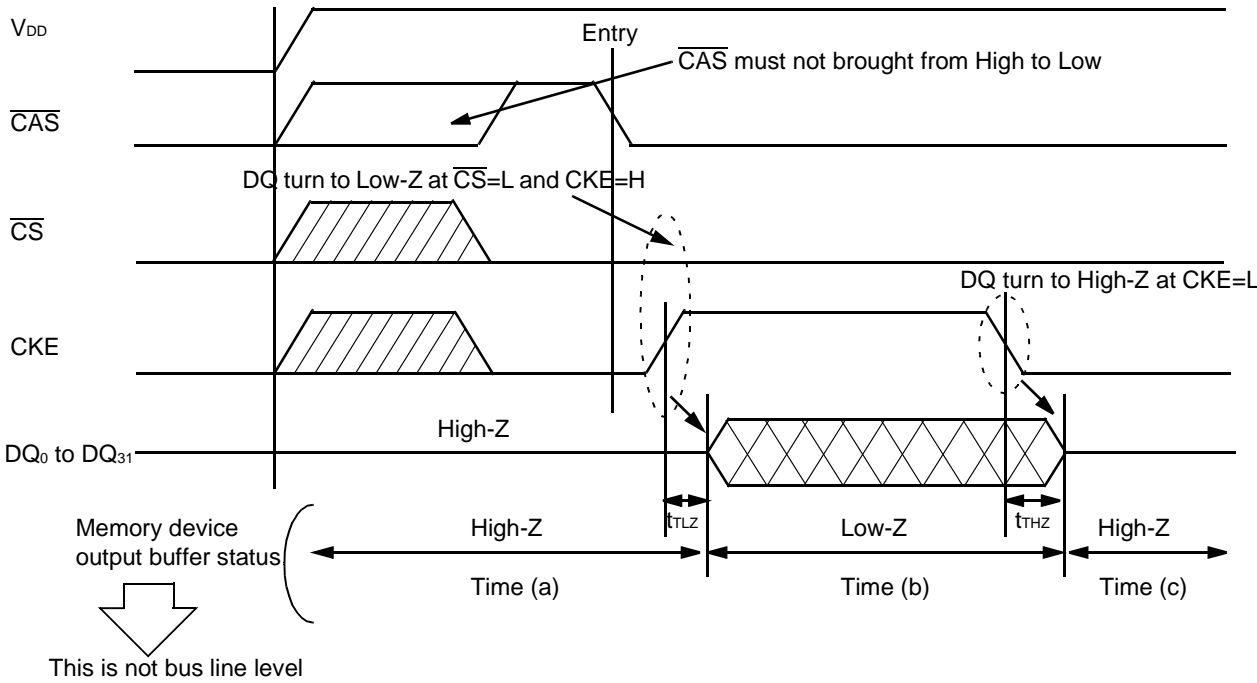
\*2. PRE or PALL commands must not be asserted. Test mode is disable by those commands.

\*3. Outputs must be disabled by  $\overline{CS} = H$  or  $CKE = L$  before Exit.

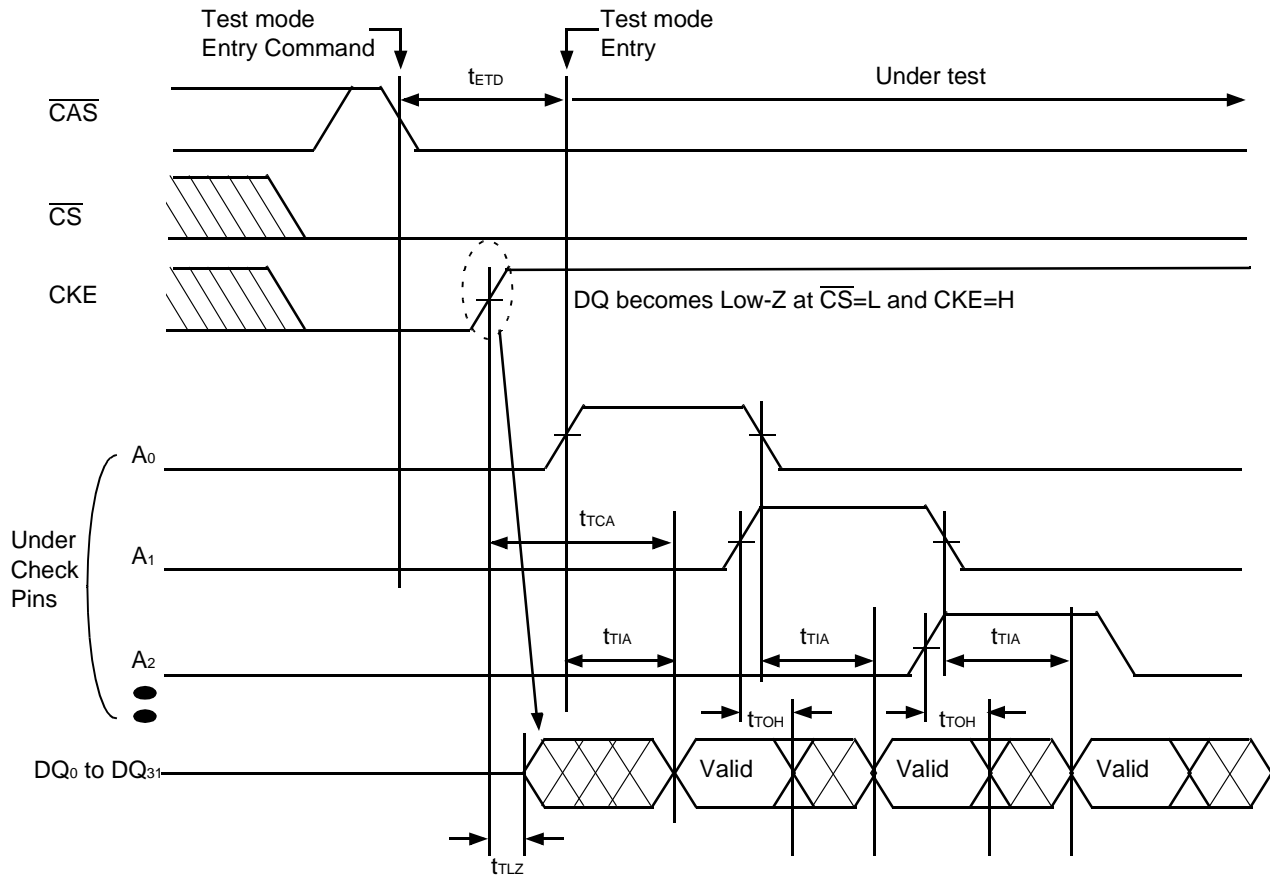
TIMING DIAGRAM – 3 : OUTPUT CONTROL (1)



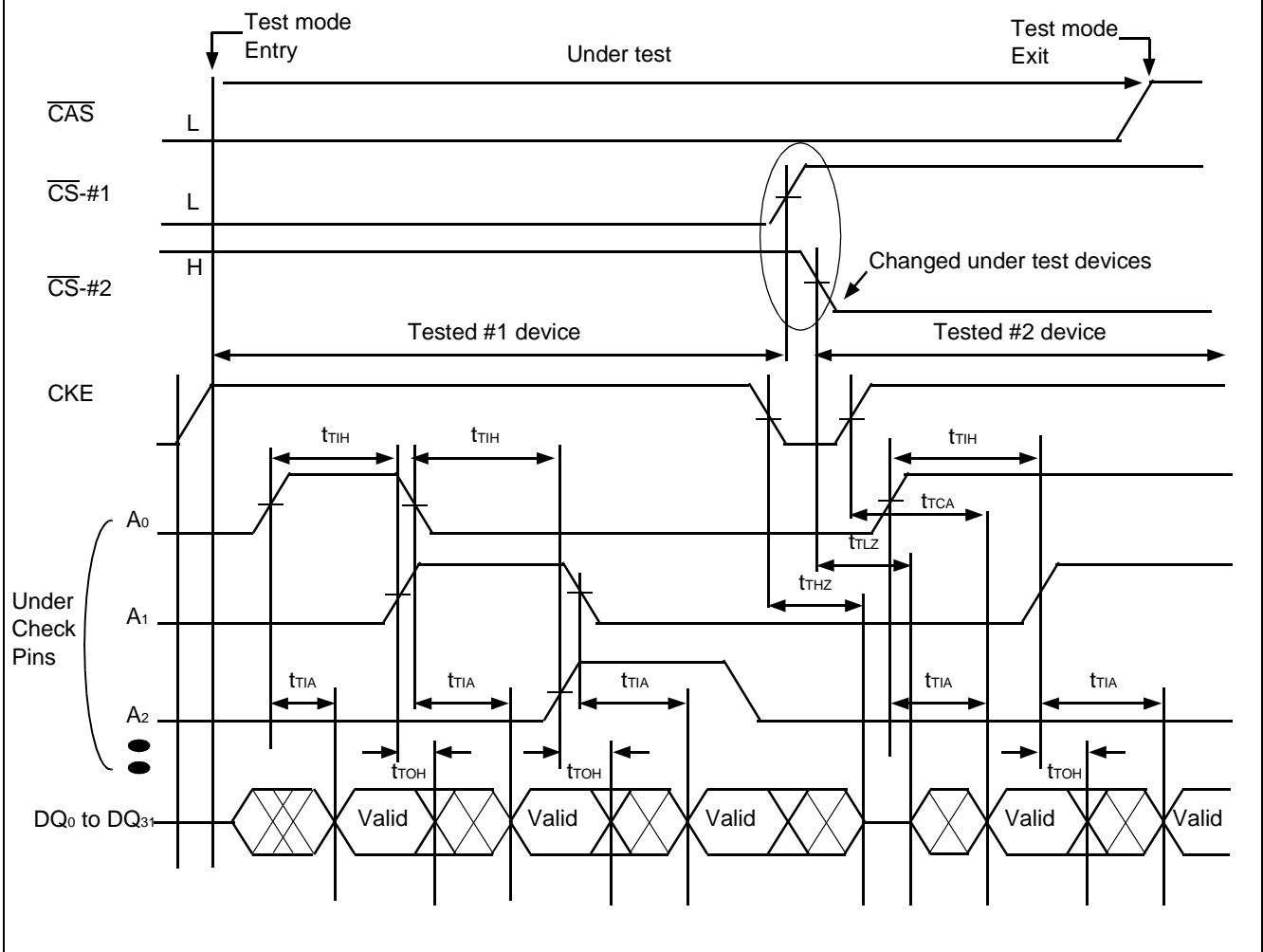
TIMING DIAGRAM – 4 : OUTPUT CONTROL (2)



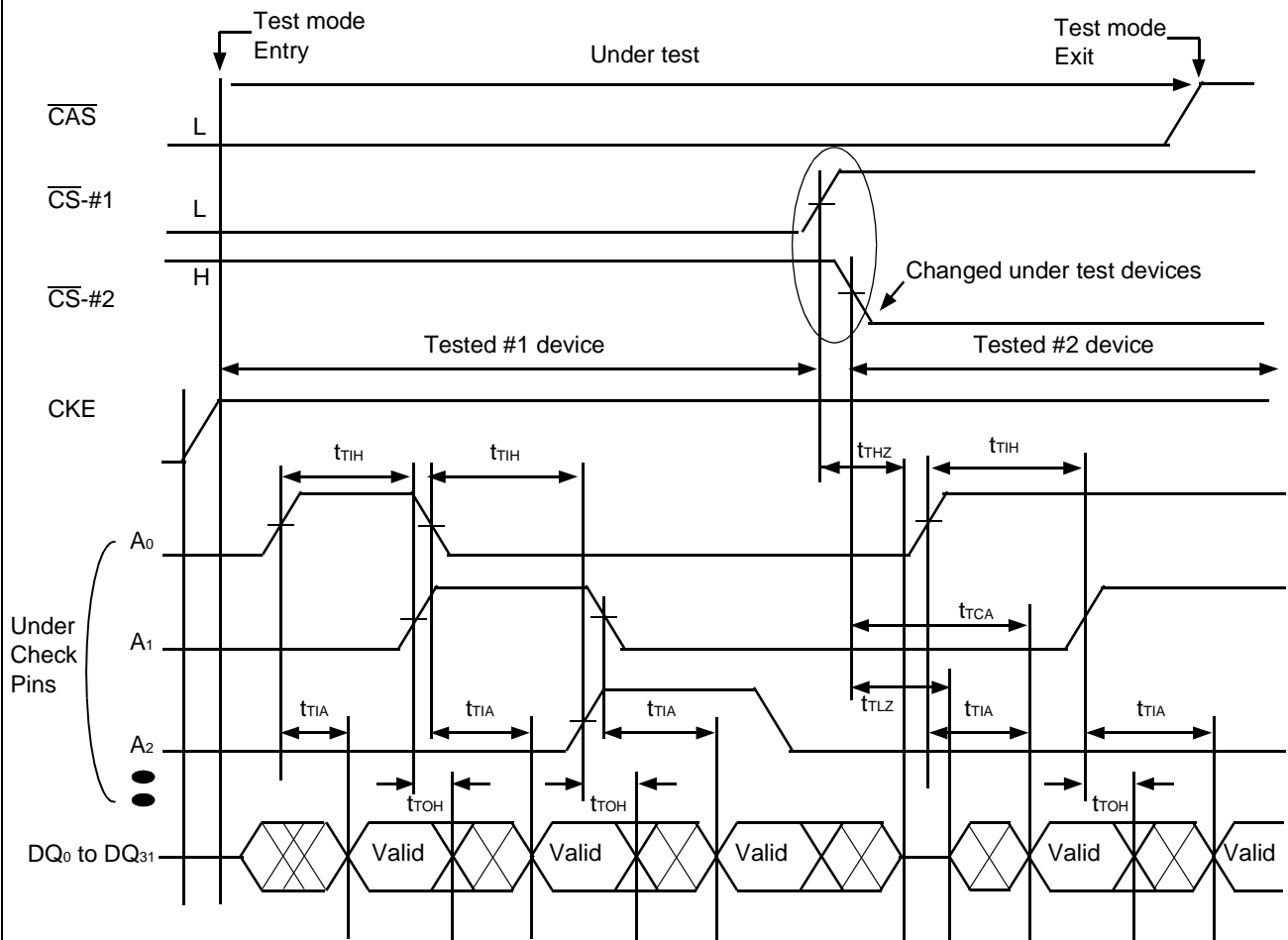
**TIMING DIAGRAM – 5 : TEST TIMING (1)**



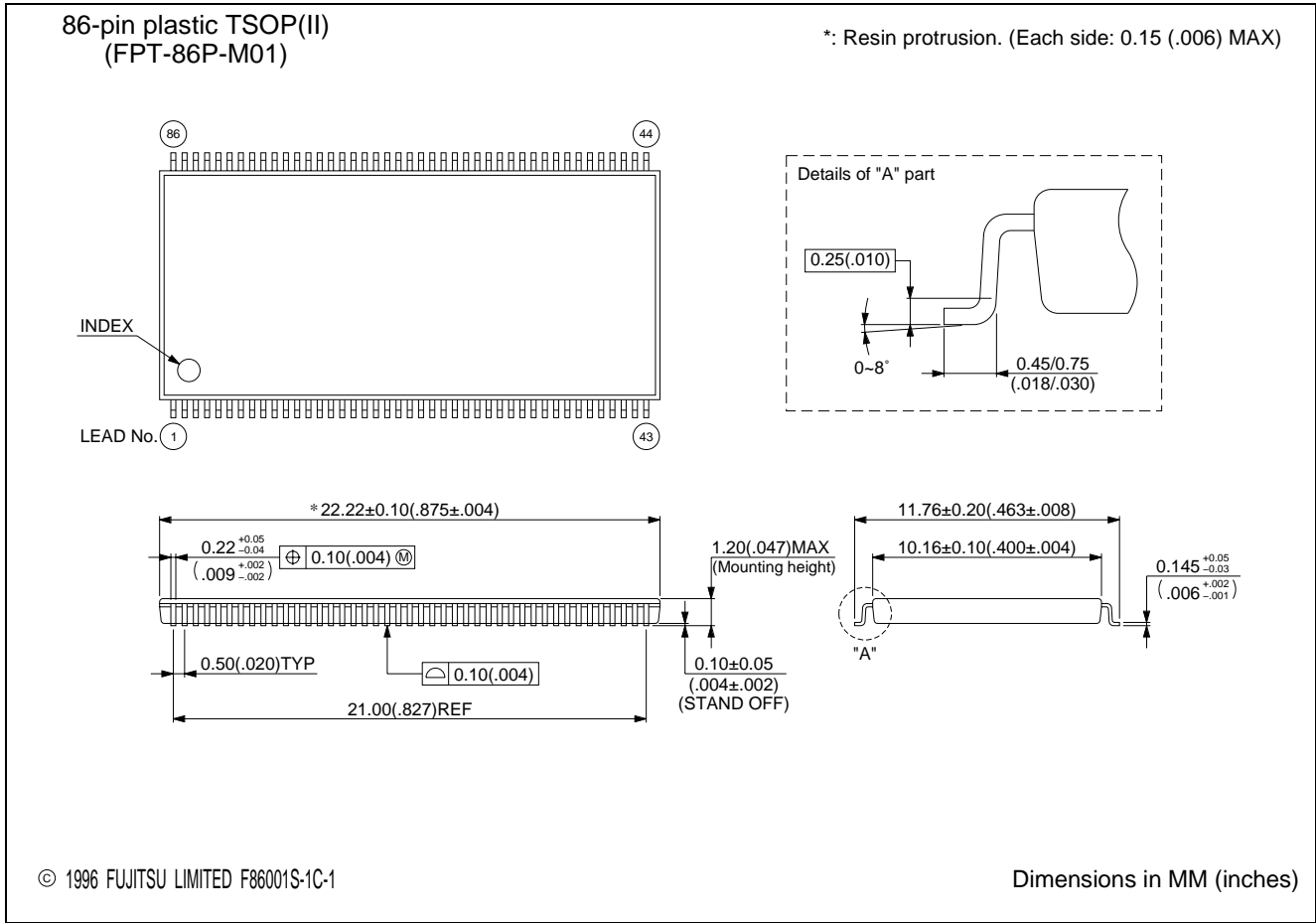
TIMING DIAGRAM – 6 : TEST TIMING (2)



**TIMING DIAGRAM – 7 : TEST TIMING (3)**



■ PACKAGE DIMENSION



**MEMO**

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