March 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C75-25/-30/-35
CMOS 64K-BIT HIGH-SPEED SRAM

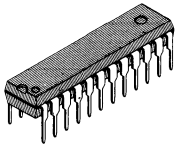
1

16K Words x 4 Bits High-Speed CMOS Static Random Access Memory

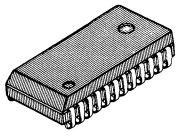
The Fujitsu MB81C75 is a 16,384 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and it may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB81C75 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 16,384 words x 4 bits
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB81C75-25)
  $t_{OE} = 10$ ns max.
  $t_{AA} = t_{ACS} = 30$ ns max. (MB81C75-30)
  $t_{OE} = 13$ ns max.
  $t_{AA} = t_{ACS} = 35$ ns max. (MB81C75-35)
  $t_{OE} = 15$ ns max.
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 24-pin Plastic Package:
  DIP MB81C75-xxP
  SOJ MB81C75-xxPJ
- Standard 28-pad Ceramic Package:
  LCC (metal seal) MB81C75-xxCV

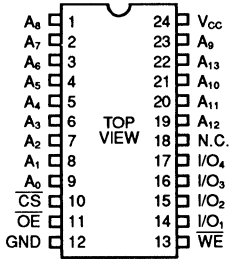


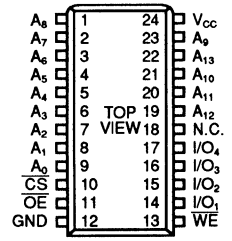
PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT





Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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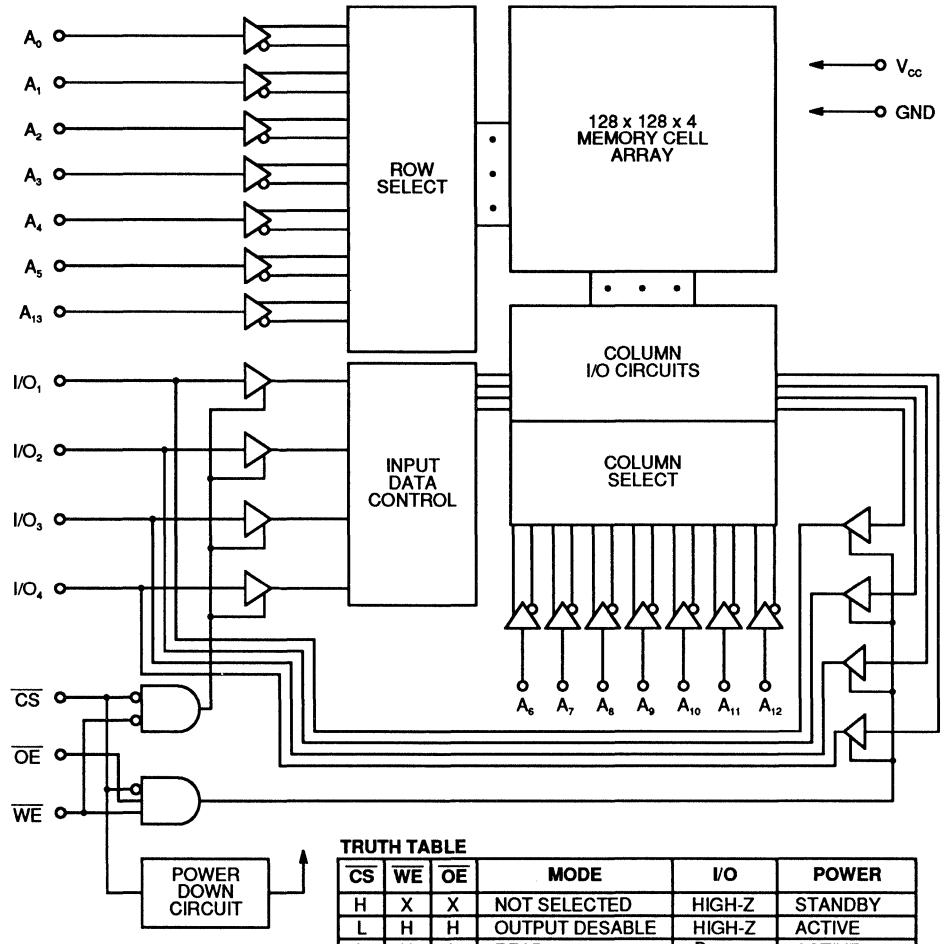
Fig. 1 – MB81C75 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O	POWER
H	X	X	NOT SELECTED	HIGH-Z	STANDBY
L	H	H	OUTPUT DESABLE	HIGH-Z	ACTIVE
L	H	L	READ	D_{OUT}	ACTIVE
L	L	X	WRITE	D_{IN}	ACTIVE

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

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DC CHARACTERISTICS

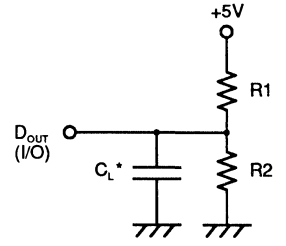
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Value		Unit
			Min	Max	
Standby Supply Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	I_{SB1}		10	mA
	$\overline{CS}=V_{IH}$	I_{SB2}		20	
Active Supply Current	$\overline{CS}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH}, I_{OUT}=0mA	I_{CC1}		60	mA
Operating Supply Current	Cycle=Min., I_{OUT}=0mA, $\overline{CS}=V_{IL}$	I_{CC2}		100	
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	–10	10	µA
Output Leakage Current	$\overline{CS}=V_{IH}$, $V_{I/O}$=0V to V_{CC}	$I_{LI/O}$	–10	10	µA
Input Low Voltage		V_{IL}	–2.0*	0.8	V
Input High Voltage		V_{IH}	2.2	6.0	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V

Note: All voltages are referenced to GND
* –2.0V Min, for pulse width less than 20ns. (V_{IL} Min=–0.5V at DC Level)

Fig. 2 – AC TEST CONDITIONS

- Output Load



* Including Scope and Jig Capacitance

- Input Pulse Levels : 0V to 3.0V
- Input Pulse Rise & Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : Input : 1.5V
  : Output: 1.5V

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}
Load II	480Ω	255Ω	5pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}

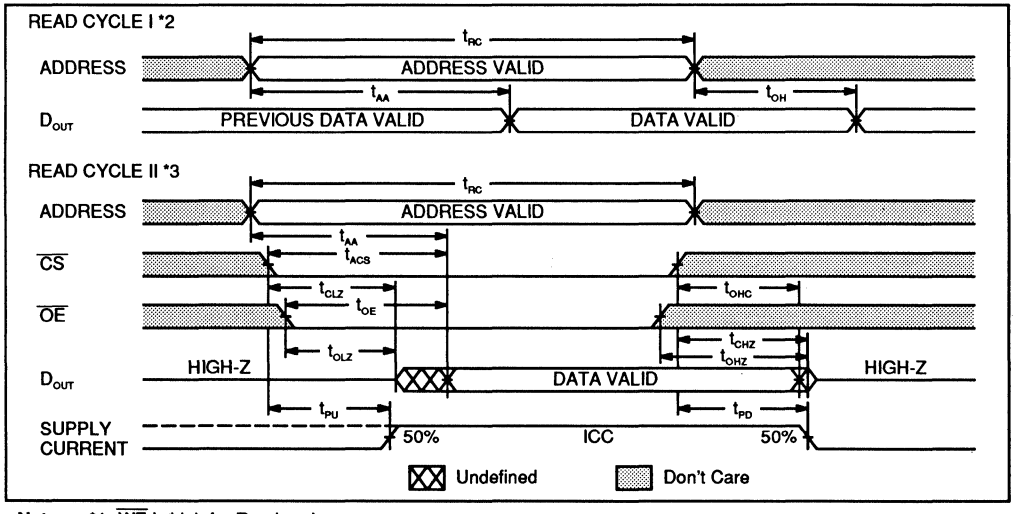
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB81C75-25		MB81C75-30		MB81C75-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time *2	t_{AA}		25		30		35	ns
$\overline{CS}$ Access Time *3	t_{ACS}		25		30		35	ns
$\overline{OE}$ Access Time *3	t_{OE}		10		13		15	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		3		ns
$\overline{CS}$ to Output Low-Z *4	t_{CLZ}	5		5		5		ns
$\overline{OE}$ to Output in Low-Z *4	t_{OLZ}	0		0		0		ns
$\overline{CS}$ to Output High-Z *4	t_{CHZ}		10		13		15	ns
$\overline{OE}$ to Output High-Z *4	t_{OHZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

READ CYCLE TIMING DIAGRAM *1

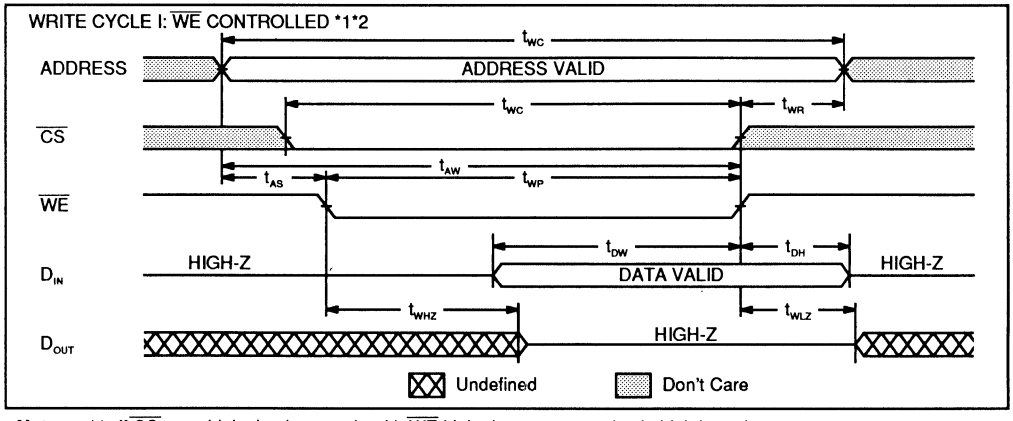


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}, $\overline{OE}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE *1

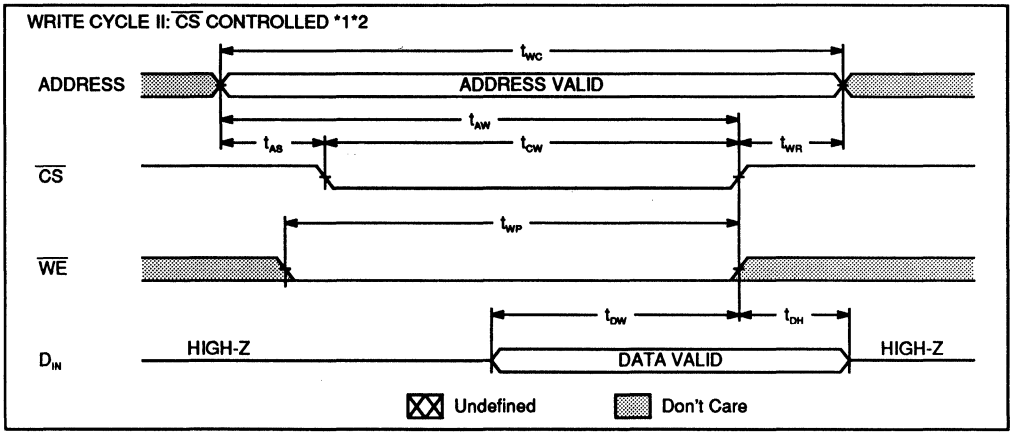
Parameter	Symbol	MB81C75-25		MB81C75-30		MB81C75-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	25		30		35		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Chip Select to End of Write	t_{CW}	20		25		30		ns
Data Valid to End of Write	t_{DW}	13		15		17		ns
Data Hold Time	t_{DH}	2		2		2		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Output High-Z from $\overline{WE}$ *3	t_{WHZ}	0		0		0		ns
Output Low-Z from $\overline{WE}$ *3	t_{WLZ}		10		13		15	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

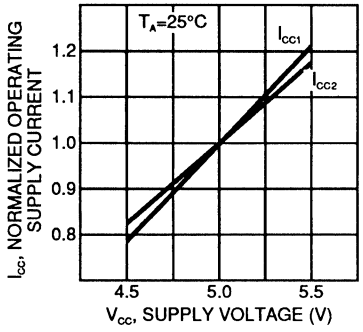


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

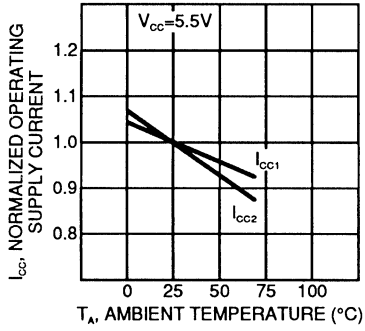


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

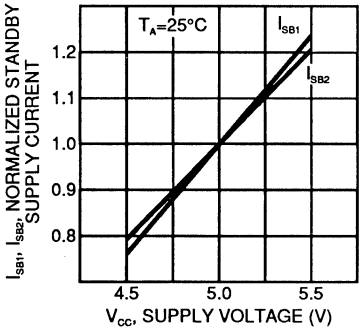


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

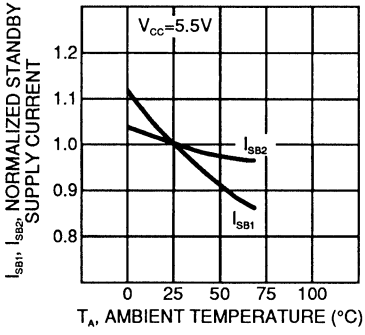
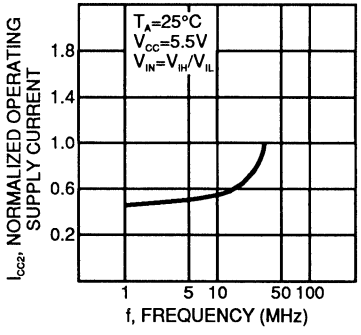


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

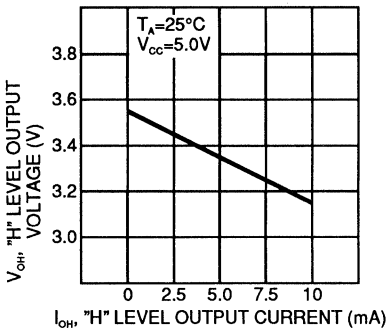


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

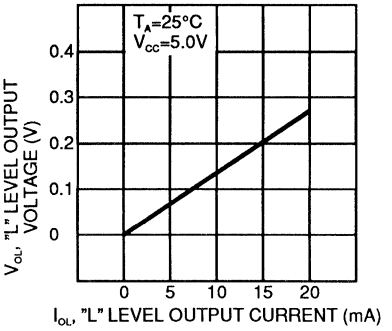


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

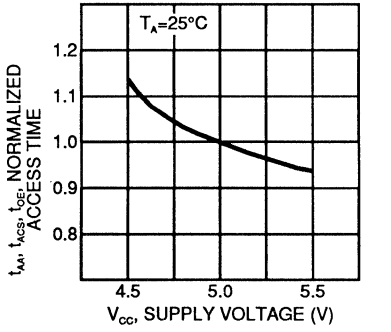


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

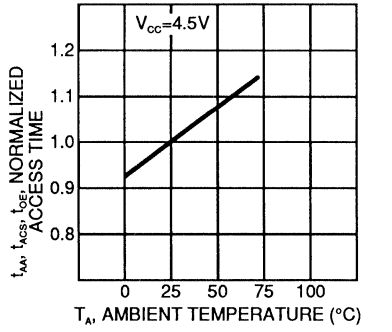
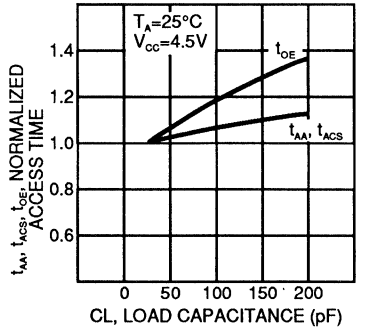


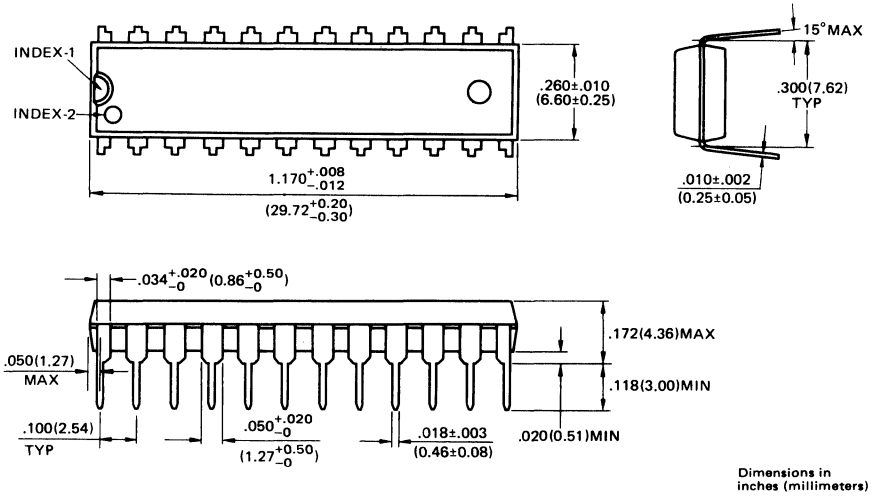
Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: P)

24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)

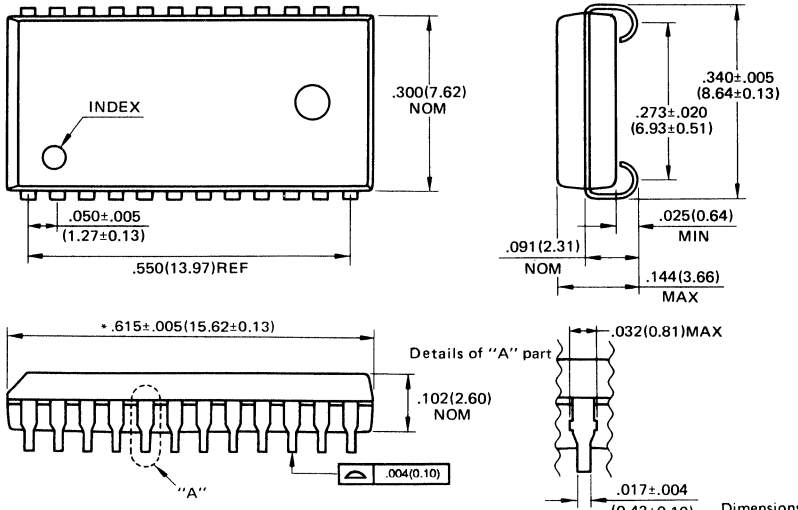


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PJ)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

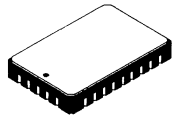


* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

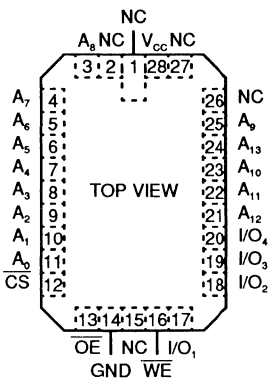
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

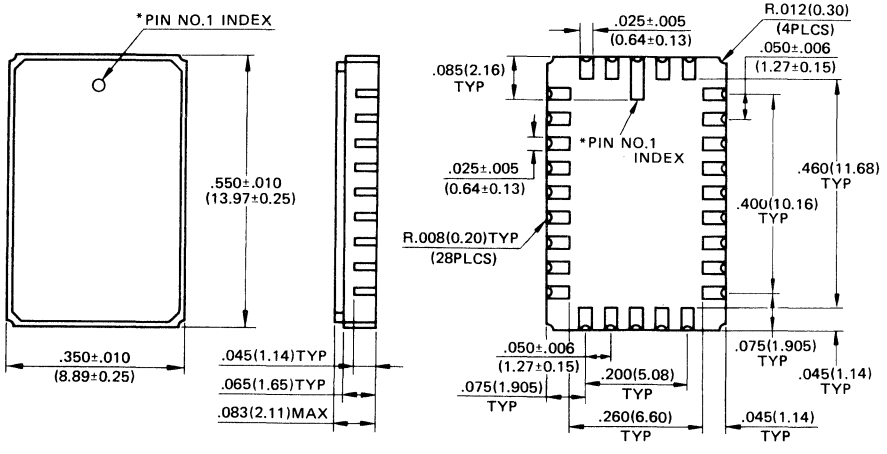
(Suffix: CV)



CERAMIC PACKAGE
LCC-28C-A03



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches
and (millimeters)