FUJITSU
MICROELECTRONICS

MB8168-55
MB8168-70

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

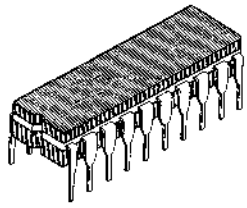
ADVANCE INFORMATION

DESCRIPTION

The Fujitsu MB8168 is a 4096 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{CS}$, the other deselected packages automatically power down.

All Fujitsu devices offer the advantages of low power dissipation, low cost and high performance.

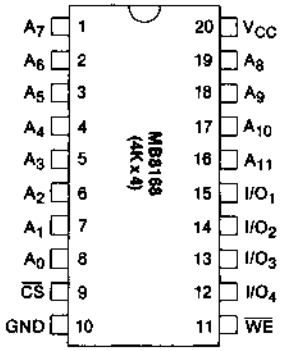


CERDIP PACKAGE
DIP-20C-C03

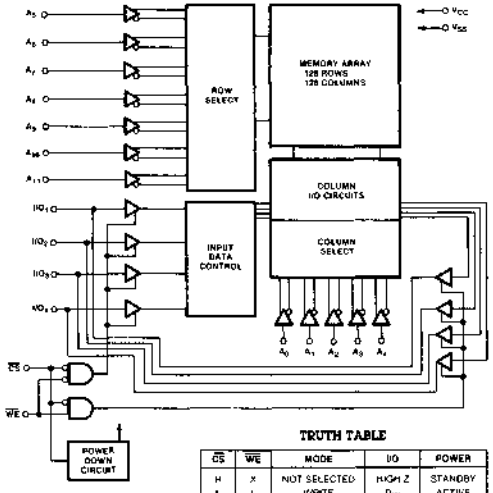
FEATURES

- **Organized as 4096 x 4**
- **Fully Static Operation, no clocks or timing strobe required**
- **Fast Access Time:**
  MB8168-55 55 ns Max.
  MB8168-70 70 ns Max.
- **Low Power Consumption:**
  I_{CC} = 150mA Max. (Active)
  I_{SB} = 40mA Max. (Standby)
- **Single +5V DC Supply Voltage, ±10% tolerance**
- **Common data input and output**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power-down**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2168**

PIN ASSIGNMENT



MB8168 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient 1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

NOTE: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

CAPACITANCE (T_A = 25°C, f = 1 MHz, this parameter is sampled, not 100% tested.)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address, $\overline{WE}$: V_{IN} = 0V	C_{IN}	—	7	pF
Input Capacitance	$\overline{CS}$: V_{IN} = 0V	$C_{\overline{CS}}$	—	8	pF
Output Capacitance	Data I/O, V_{OUT} = 0V	C_{OUT}	—	8	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	150	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	40	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min)	I_{PO}	—	50	mA
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})	I_{OS}	−200	200	mA

AC TEST CONDITIONS

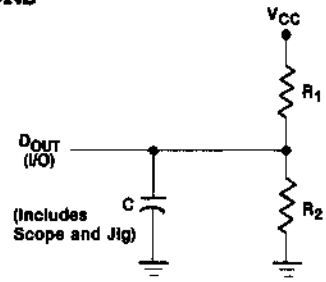
Input Conditions:

Input Pulse Levels:	**0V to 3.0V**
Input Pulse Rise/Fall Times:	**5 ns**
Input Timing Reference Level:	**1.5V**

Output Conditions:

Output Timing Reference Level:	**0.8V to 2.0V**
Output Load:	

	R_1	R_2	C	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ} and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}



OUTPUT LOAD

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

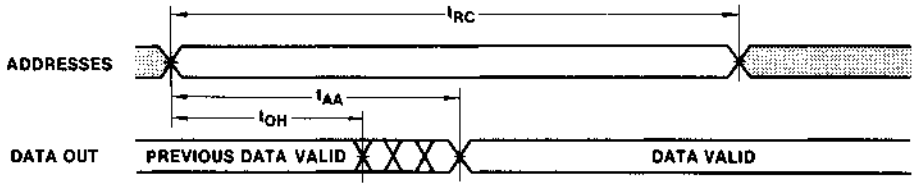
READ CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Select Access Time		t_{ACS}	—	—	55	—	—	70	ns
Output Hold from Address Change		t_{OH}	5	—	—	5	—	—	ns
Chip Select to Output Active	1 2	t_{LZ}	10	—	—	10	—	—	ns
Chip Select to Output in High Z	1 2	t_{HZ}	0	—	30	0	—	40	ns
Chip Select to Power Up Time		t_{PU}	0	—	—	0	—	—	ns
Chip Select to Power Down Time		t_{PD}	—	—	55	—	—	70	ns

Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig. 2. This parameter is sampled and not 100% tested.

READ CYCLE 3

READ CYCLE: ADDRESS CHANGING 4



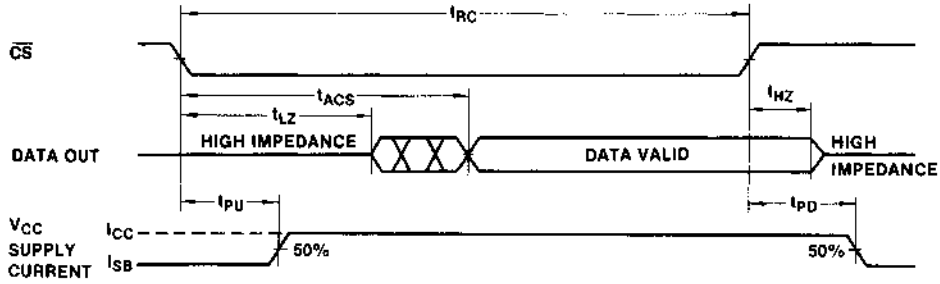
Notes: 3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected. $\overline{CS} = V_{IL}$.

Don't Care

Undefined Data

READ CYCLE [3] (Cont'd)

READ CYCLE: $\overline{CS}$ CHANGING[5]



Notes: 3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected. $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

Undefined Data

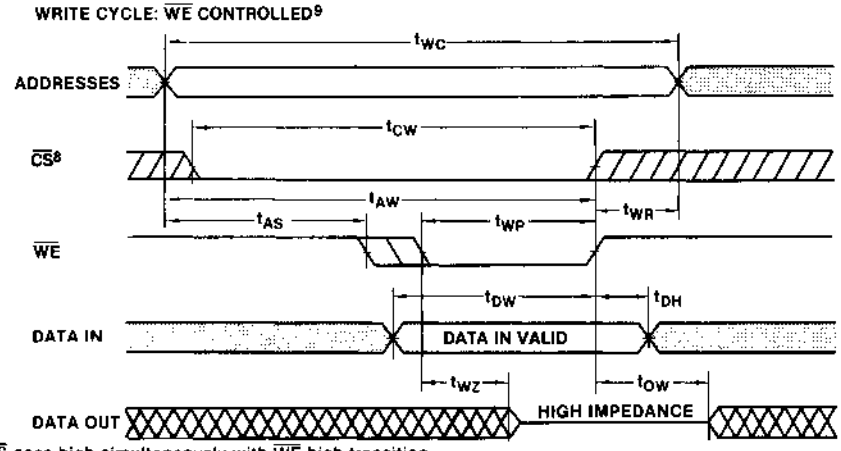
WRITE CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Write Cycle Time		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	55	—	—	70	—	—	ns
Chip Select to End of Write		t_{CW}	55	—	—	70	—	—	ns
Data Valid to End of Write		t_{DW}	25	—	—	30	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	55	—	—	70	—	—	ns
Write Recovery Time		t_{WR}	0	—	—	0	—	—	ns
Address Setup Time		t_{AS}	0	—	—	0	—	—	ns
Output Active From End of Write	[6] [7]	t_{OW}	0	—	—	0	—	—	ns
Write Enable to Output in High Z	[6] [7]	t_{WZ}	0	—	30	0	—	40	ns

Notes: 6. Transition is measured at the point of +500mV from steady state voltage.
7. This parameter is measured with specified loading in Fig. 2.

WRITE CYCLE

WRITE CYCLE: $\overline{WE}$ CONTROLLED[9]

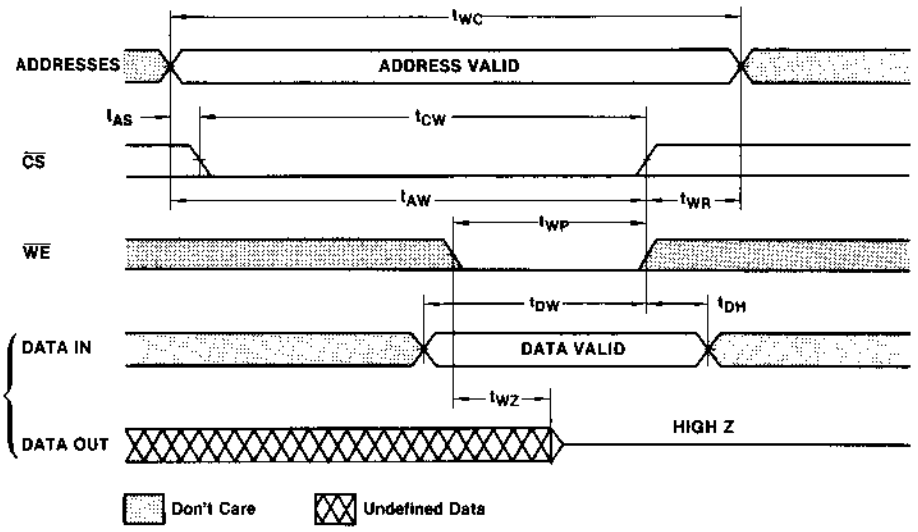


Note: *If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

Don't Care Undefined Data

WRITE CYCLE (Cont'd)

WRITE CYCLE: $\overline{CS}$ CHANGING[9]



Notes: 6. Transition is measureed at the point of ±500 mV from steady state voltage.
7. This parameter is measured with specified loading in Fig. 2.
8. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
9. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

The MB8168 from Fujitsu is a high performance part. It is designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The power requirements are achieved by the use of MB8168 chip select (active low). The MB8168 automatically enters standby drawing only I_{SB} whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MB8168 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.