FUJITSU
MICROELECTRONICS

MB8167-55
MB8167-70

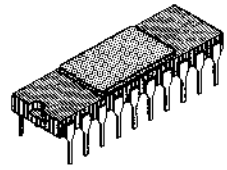
NMOS 16,384 BIT STATIC RANDOM ACCESS MEMORY

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MB8167A-55/MB8167A-45.

DESCRIPTION

The Fujitsu MB8167 is a 16384 words by 1 bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5V DC supply.

For ease of use, chip enable ($\overline{CE}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167. This device offers the advantages of low power dissipation, low cost, and high performance.

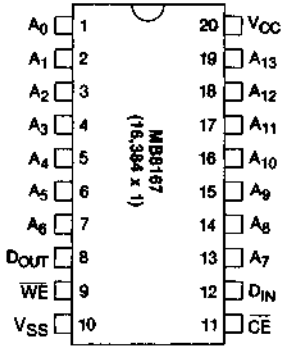


CERAMIC PACKAGE (METAL SEAL) DIP-20C-A01

FEATURES

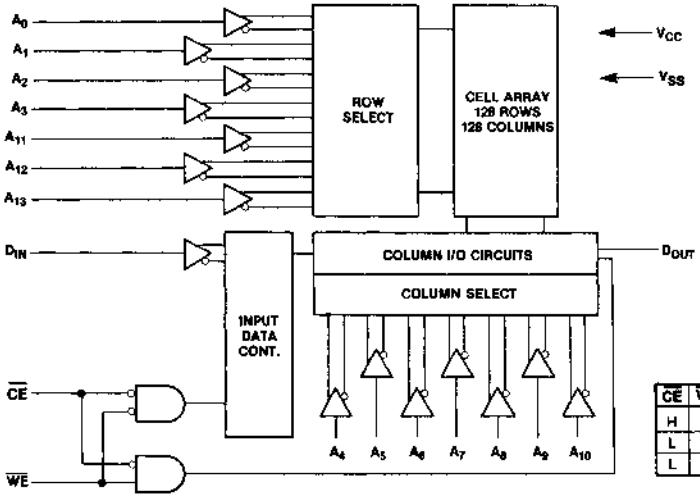
- **Organized as 16384 words X 1 Bit**
- **Static operation: no clocks or refresh required**
- **Fast Access Time:**
  MB8167-55 55 ns Max.
  MB8167-70 70 ns Max.
- **Single +5V DC supply voltage**
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion and automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2167**

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8167 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

NOTE: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 400 linear feet per minute.

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	6	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)		I_{LI}	−10	10	μA
Output Leakage Current ($\overline{CE}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC} Min, V_{CC} = Max)		I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA)	T_A = 25°C	I_{CC}	—	170	mA
	T_A = 0°C		—	180	
Output Low Voltage (I_{OL} = 8mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)		V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}		I_{SB}	—	30	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min)		I_{PO}	—	30	mA

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MB8167A-55/MB8167A-45.

AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.2V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Inputs: 1.5V
	Output: 1.5V

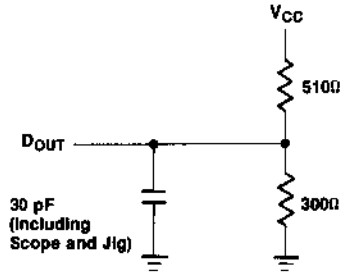


Fig. 1: OUTPUT LOAD

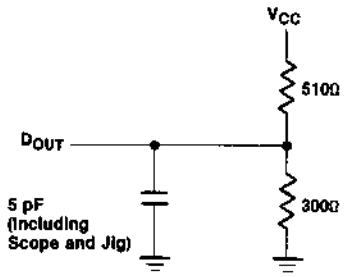


Fig. 2: OUTPUT LOAD for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

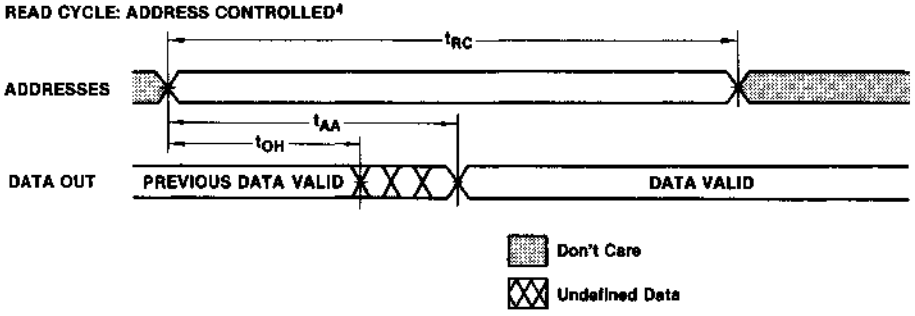
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

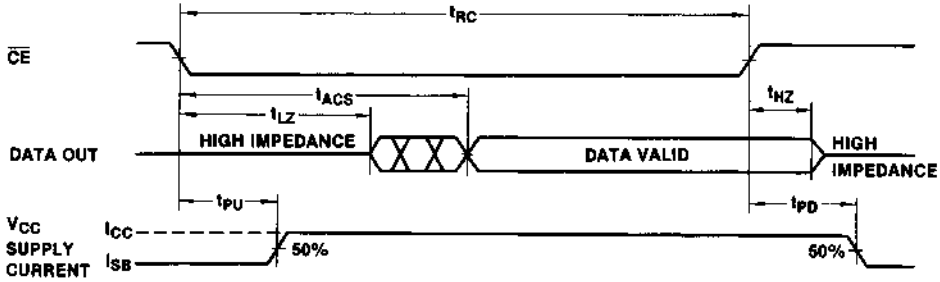
Parameter	NOTES	Symbol	MB8167-55			MB8167-70			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		t_{RC}	55	—	—	70	—	—	ns
Address Access Time		t_{AA}	—	—	55	—	—	70	ns
Chip Enable Access Time		t_{ACS}	—	—	55	—	—	70	ns
Output Hold from Address Change		t_{OH}	5	—	—	5	—	—	ns
Chip Enable to Output Active	1 2	t_{LZ}	10	—	—	10	—	—	ns
Chip Enable to Output in High Z	1 2	t_{HZ}	0	—	30	0	—	40	ns
Chip Enable to Power Up Time		t_{PU}	0	—	—	0	—	—	ns
Chip Enable to Power Down Time		t_{PD}	—	—	30	—	—	35	ns

READ CYCLE[3]



READ CYCLE[3] (Cont'd)

READ CYCLE: $\overline{CE}$ CONTROLLED[5]



Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig.2.
3. $\overline{WE}$ is high for Read Cycle.
4. Device is continuously selected, $\overline{CE}$ = V_{IL}.
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low.

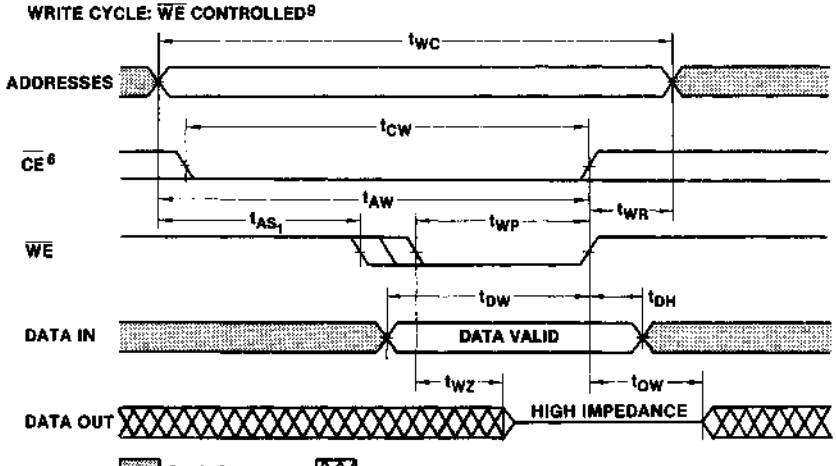
Undefined Data

WRITE CYCLE

Parameter	NOTES	Symbol	MB8167-55 Min	MB8167-55 Typ	MB8167-55 Max	MB8167-70 Min	MB8167-70 Typ	MB8167-70 Max	Unit
Write Cycle		t_{WC}	55	—	—	70	—	—	ns
Address Valid to End of Write		t_{AW}	45	—	—	50	—	—	ns
Chip Enable to End of Write		t_{CW}	50	—	—	60	—	—	ns
Data Valid to End of Write		t_{DW}	35	—	—	45	—	—	ns
Data Hold Time		t_{DH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WP}	35	—	—	45	—	—	ns
Write Recovery Time		t_{WR}	5	—	—	10	—	—	ns
Address Setup Time		t_{AS1}	5	—	—	10	—	—	ns
		t_{AS2}	0	—	—	0	—	—	
Output Active From End of Write	7 8	t_{OW}	0	—	—	0	—	—	ns
Write Enable to Output in High Z	7 8	t_{WZ}	0	—	30	0	—	35	ns

WRITE CYCLE

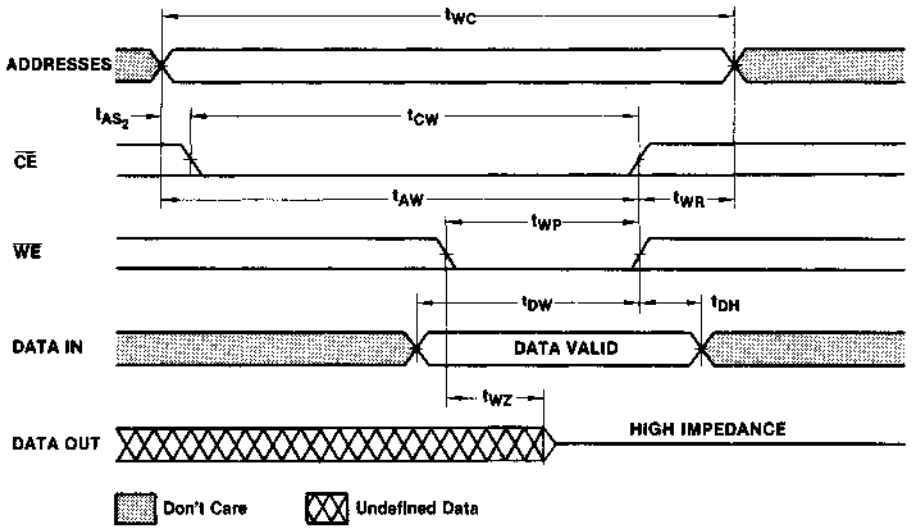
WRITE CYCLE: $\overline{WE}$ CONTROLLED[9]



Don't Care Undefined Data

WRITE CYCLE (Cont'd)

WRITE CYCLE: $\overline{CE}$ CONTROLLED[9]



Notes: 6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

The MB8167 from Fujitsu is a high performance part. It is designed for high speed and low power system requirements.

The high speed is obtained by advanced NMOS processing. The power requirements are achieved by the use of MB8167 chip enable (active low). The MB8167 automatically enters standby drawing only I_{SB} whenever the chip enable is high. Upon activation of chip enable ($\overline{CE}$ = LOW) the MB8167 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.