FUJITSU
MICROELECTRONICS

MB8118-10
MB8118-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

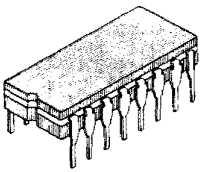
DESCRIPTION

The Fujitsu MB8118 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

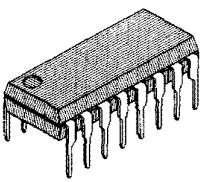
Multiplexed row and column address inputs permit the MB8118 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

The MB8118 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.



CERAMIC PACKAGE
DIP-16C-C03

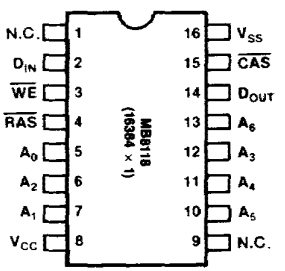


PLASTIC PACKAGE
DIP-16P-M01

FEATURES

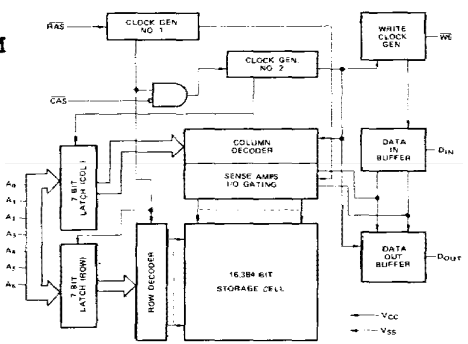
- **16,384 × 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Address access time:**
  - **100 ns max (MB8118-10)**
  - **120 ns max (MB8118-12)**
- **Cycle time:**
  - **235 ns min (MB8118-10)**
  - **270 ns min (MB8118-12)**
- **Low power:**
  - **182mW max (MB8118-10)**
  - **160mW max (MB8118-12)**
  - **16.5mW max (Standby)**
- **+5V single power supply, ± 10% tolerance**
- **On chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Hidden refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-In**
- **Pin compatible with Intel 2118 and MCM4517**

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8118 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic Plastic	T_{STG}	−55 to +150 −55 to +125	°C
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_6, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10		MB8118-12		Unit
			Min	Max	Min	Max	
OPERATING CURRENT Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min)	[1]	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		I_{CC2}	—	3.0	—	3.0	mA
REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min)	[1]	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min)	[1]	I_{CC4}	—	25	—	22	mA
INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 5.5) (Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Note: [1] I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS NOTES 1,2,3

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10			MB8118-12			Unit
			Min	Typ	Max	Min	Typ	Max	
Time Between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	—	320	—	—	ns
Page Mode Cycle Time		t_{PC}	125	—	—	145	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	100	—	—	120	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	55	—	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	45	0	—	50	ns
Transition Time		t_T	3	—	50	3	—	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	110	—	—	120	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	115	—	10000	140	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	70	—	—	85	—	—	ns
$\overline{CAS}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	—	55	—	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	60	—	—	70	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	—	10000	65	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100	—	—	120	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	[7] [8]	t_{RCD}	25	—	45	25	—	55	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	15	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	15	—	—	15	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	60	—	—	70	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time		t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	0	—	—	0	—	—	ns
Write Command Hold Time		t_{WCH}	30	—	—	35	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	75	—	—	90	—	—	ns
Write Command Pulse Width		t_{WP}	30	—	—	35	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	60	—	—	65	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	45	—	—	50	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	30	—	—	35	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	75	—	—	90	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	55	—	—	65	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	120	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	20	—	—	25	—	—	ns

Notes:

[1] An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

[2] Dynamic measurements assume t_T=5ns.

[3] V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

[4] Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

[5] Assumes that $t_{RCD} \geq t_{RCD}$ (max).

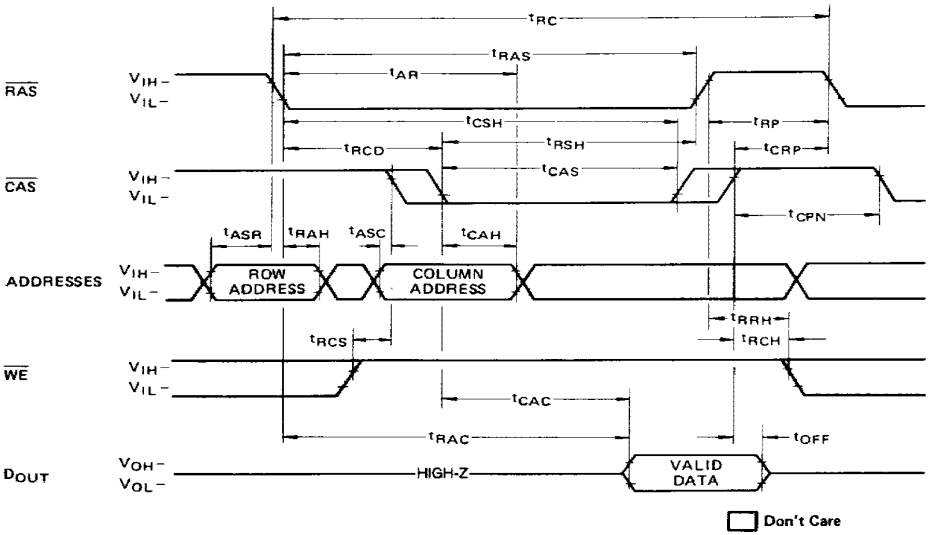
[6] Measured with a load equivalent to 2 TTL loads and 100pF.

[7] Operation within the t_{RCD} (max) limit insures that t_{RCD} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

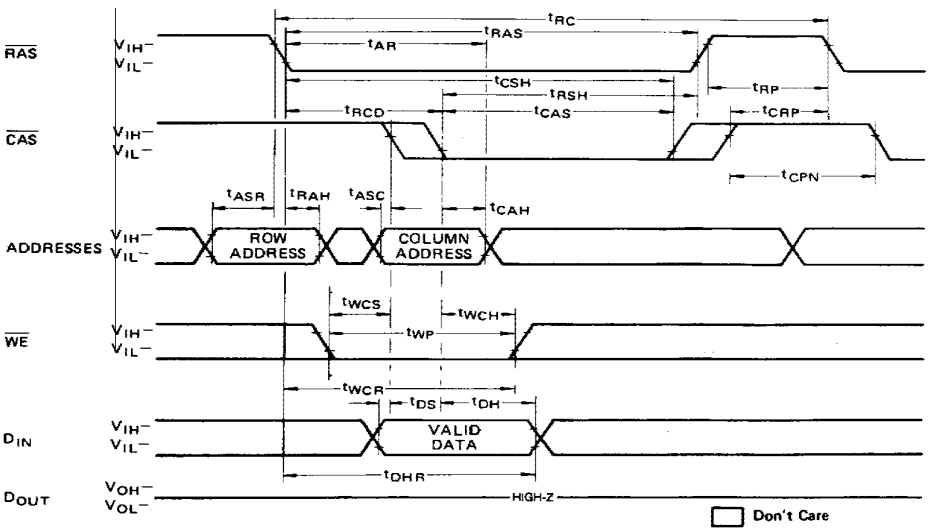
[8] $t_{RCD}(min) = t_{RAH}(min) + 2t_T(t_T = 5ns) + t_{ASC}(min)$.

[9] t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

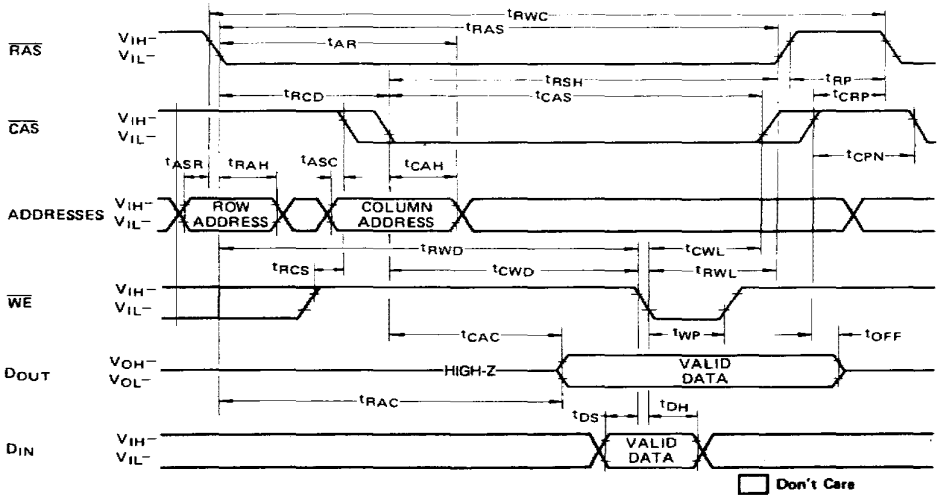
READ CYCLE TIMING DIAGRAM



WRITE CYCLE (EARLY WRITE)

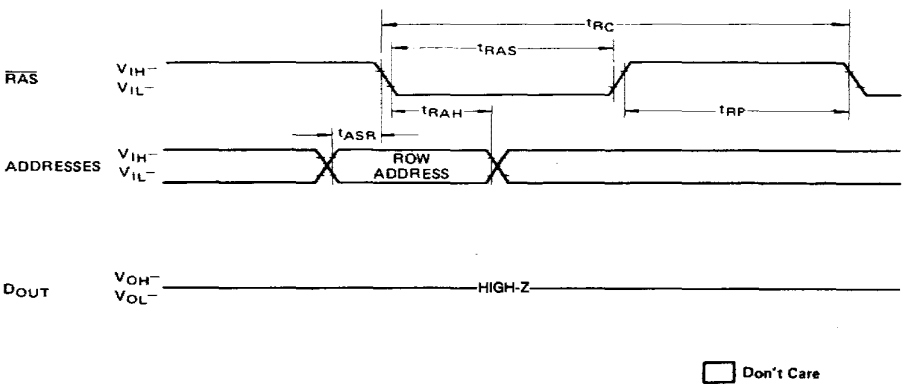


READ-WRITE/READ-MODIFY-WRITE CYCLE

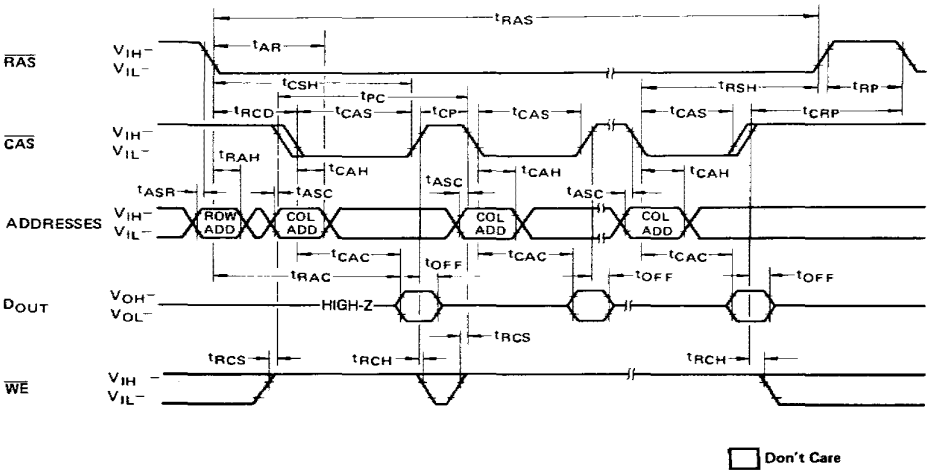


"RAS-ONLY" REFRESH CYCLE

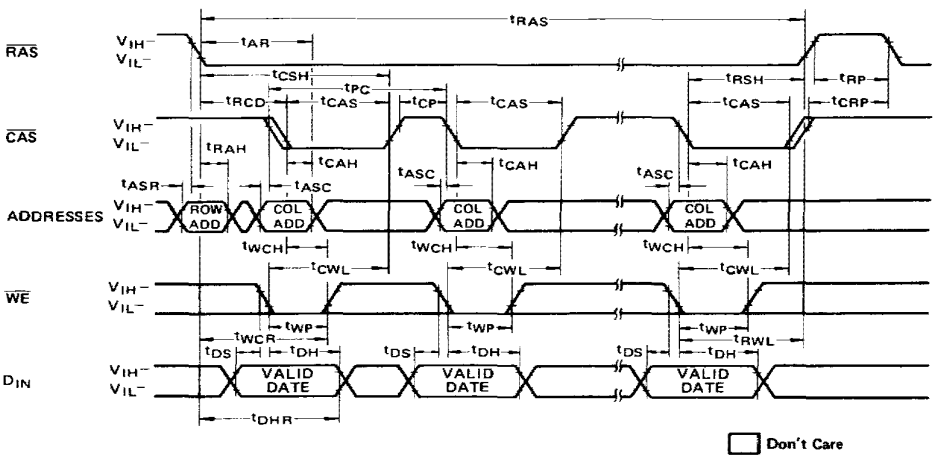
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



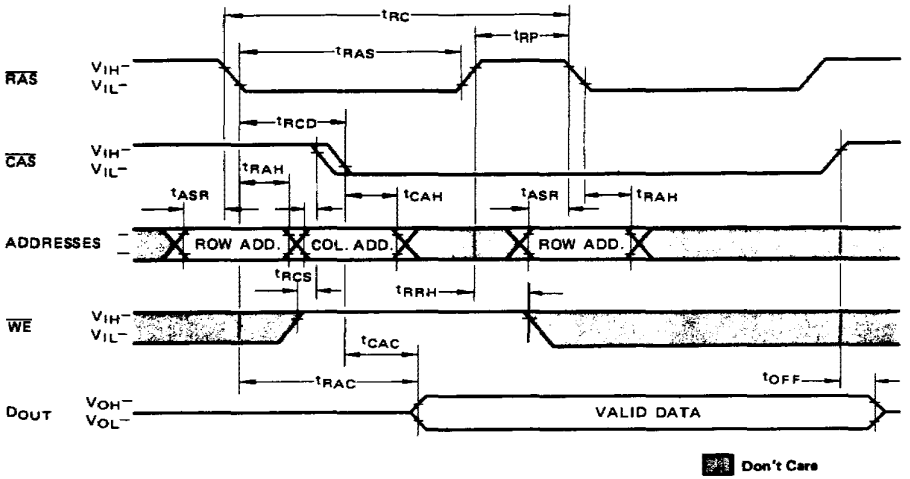
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE TIMING DIAGRAM



DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8118. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8118 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits latching the row-address into the MB8118 and maintaining $\overline{RAS}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. This saves the power required by a $\overline{RAS}$ cycle. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$-only refresh prevents any output during refresh because the output buffer is in the high impedance state since $\overline{CAS}$ is at V_{IH}. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in the memory to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle. (See Figure 1 below)

FIG. 1-HIDDEN REFRESH

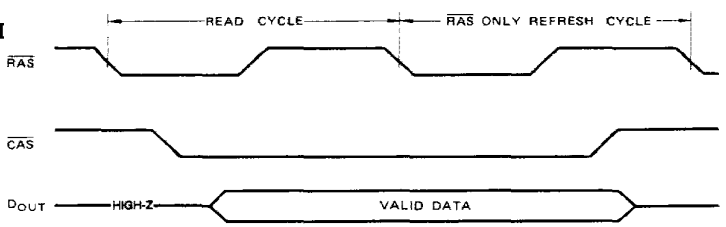
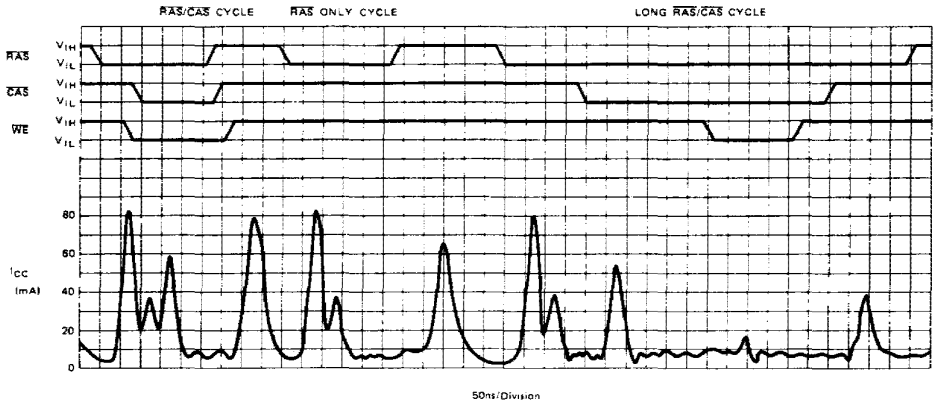
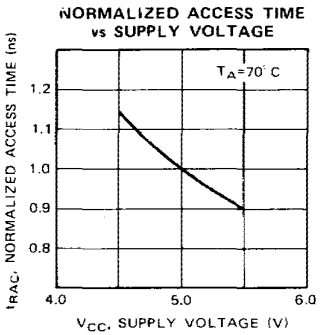
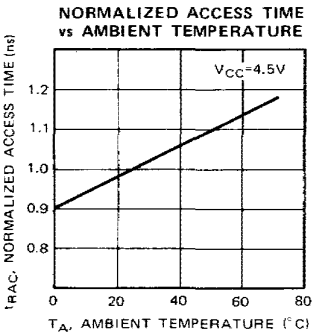


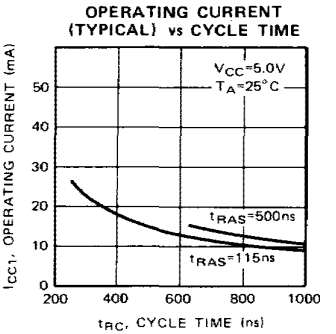
FIG. 2 — CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

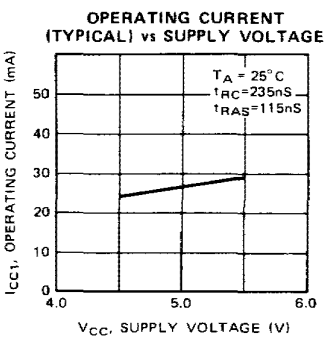


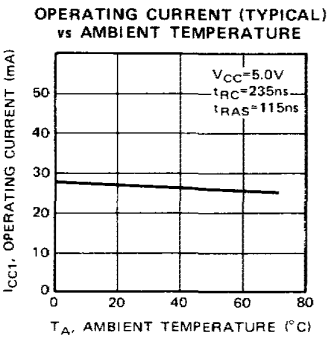
TYPICAL CHARACTERISTICS CURVES

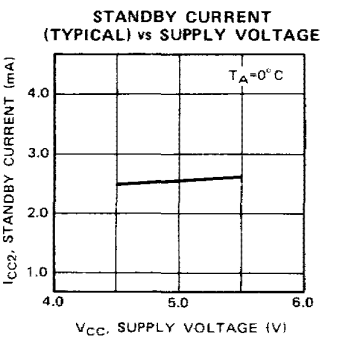






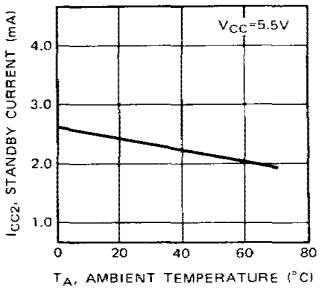




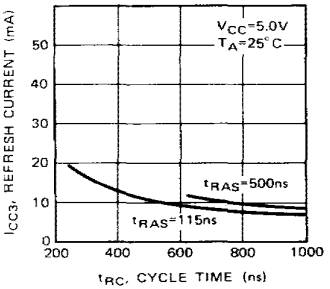


TYPICAL CHARACTERISTICS CURVES (continued)

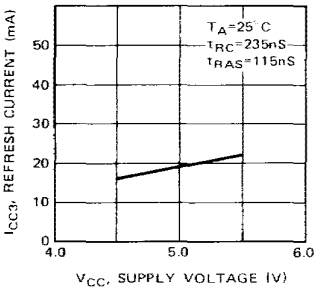
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



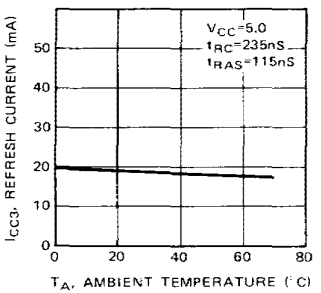
REFRESH CURRENT (TYPICAL) vs CYCLE TIME



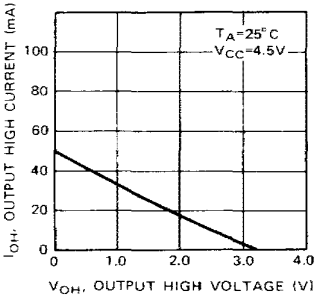
REFRESH CURRENT (TYPICAL) vs SUPPLY VOLTAGE



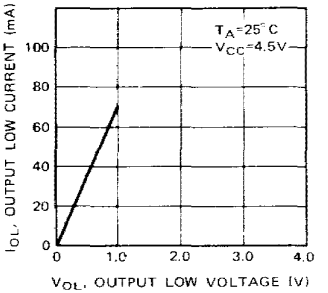
REFRESH CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

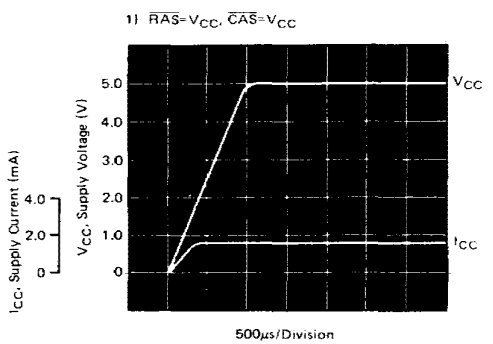


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE

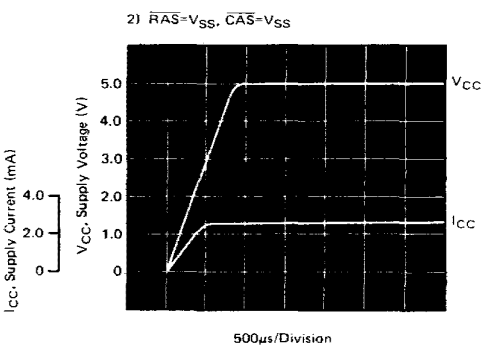


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS}$=V_{CC}, $\overline{CAS}$=V_{CC}

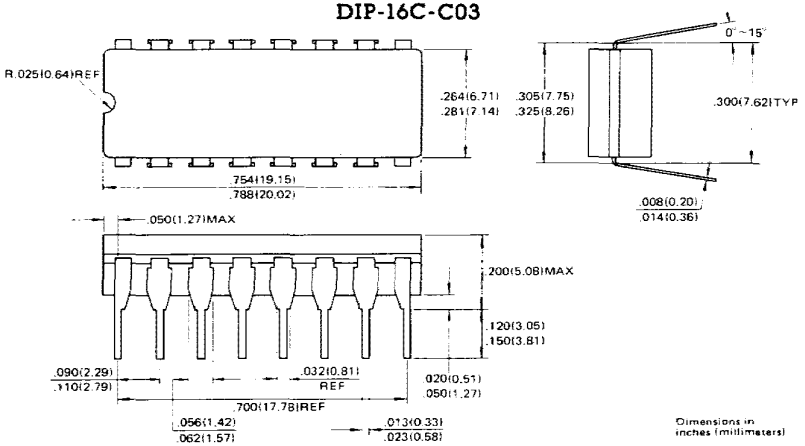


2) $\overline{RAS}$=V_{SS}, $\overline{CAS}$=V_{SS}



PACKAGE DIMENSIONS Dimensions in inches (millimeters)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
DIP-16C-C03



16-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-16P-M01