MB7127E/H
MB7128E/H

HIGH SPEED SCHOTTKY TTL 8192-BIT PROM

DESCRIPTION

The Fujitsu MB7127/MB7128 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7127 and three-state outputs on the MB7128, memory expansion is simple.

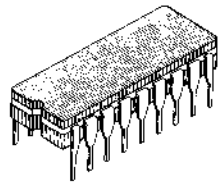
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutetic Aluminum Process) during a simple programming procedure.

The sophisticated Schottky TTL process enables small chip size and fast access time.

The extra test cells and unique testing methods provide extremely high programmability.

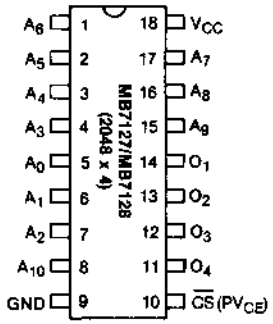
FEATURES

- **Organization:**
  2048 words by 4-bits
- **TTL compatible input/output**
- **Fast access time:**
  MB7127E/MB7128E:
  55 ns Max.
  30 ns Typ.
  MB7127H/MB7128H:
  45 ns Max.
  30 ns Max.
- **Low Power Dissipation:**
  155 mA Max.
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **MB7127: Open collector outputs**
- **MB7128: Three-state outputs**
- **Chip select leads for easy memory expansion**
- **Standard 18-pin DIP package**
- **MB7128 pin is compatible with industry standard products: 82S185, HM7685, 63S841, 27S185**
- **MB7127 pin compatible with 82S184, HM7684, 63S840, 27S184**



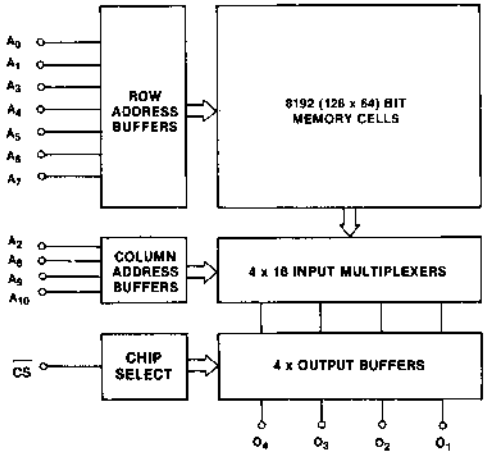
CERDIP PACKAGE
DIP-18C-C01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7127/MB7128 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to 5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0.0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)	I_{R1}	—	—	40	μA
Input Leakage Current (V_{IH} = 5.5V)	I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.45V)	I_F	—	—	−250	μA
Output Low Voltage (I_{OL} = 16 mA)	V_{OL}	—	—	0.50	V
Output Leakage Current (V_{OL} = 2.4V, chip disabled from a low)	I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.45V, chip disabled from a high)	I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −18mA)	V_{IC}	—	—	−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	I_{CC}	—	110	155	mA
Output High Voltage (I_O = −2.4mA)	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	I_{OS}*	−1.5	—	−60	mA

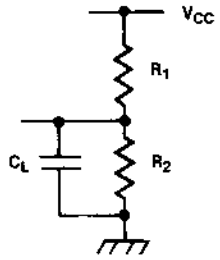
***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC CHARACTERISTICS

Full guaranteed operating ranges unless otherwise noted.

Parameter	Symbol	MB7127E/MB7128E		MB7127H/MB7128H		Unit
		Typ	Max	Typ	Max	
Address Access Time	t_{AA}	30	55	30	45	ns
Output Disable Time	t_{DIS}	—	40	—	30	ns
Output Enable Time	t_{EN}	—	40	—	30	ns

AC TEST CONDITIONS

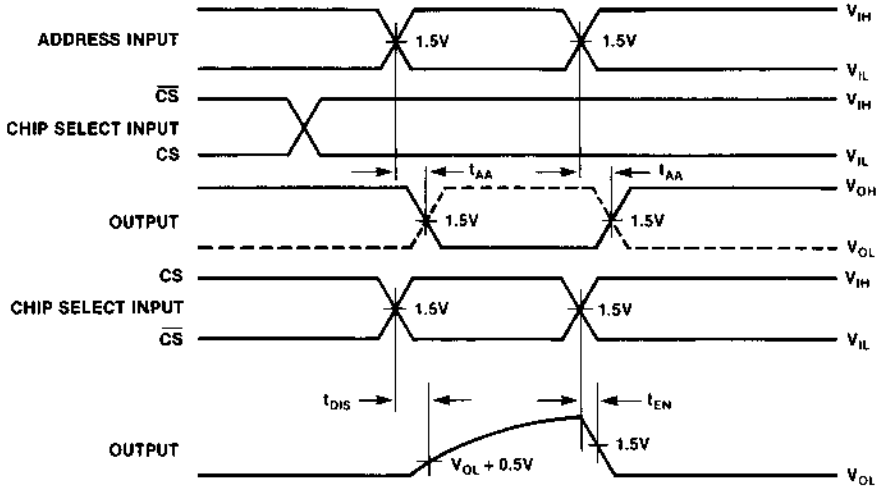


INPUT CONDITIONS

Amplitude	0V to 3V
Rise and Fall Time	5 ns from 1V to 2V
Frequency	1 MHz

MB7127/MB7128		
R_1	R_2	C_L
300Ω	600Ω	30pF

OPERATION TIMING DIAGRAM



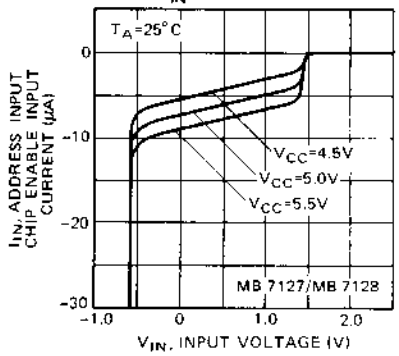
Notes: Output disable time is the time taken for the output to reach a high impedance state when either chip enable is taken to the inactive state. Output enable time is the time taken for the output to become active when both chip enables are taken to the active state. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

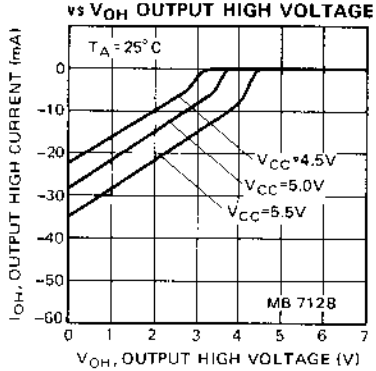
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	15	pF

TYPICAL CHARACTERISTICS CURVES

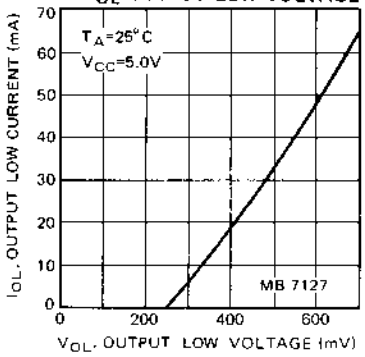
I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



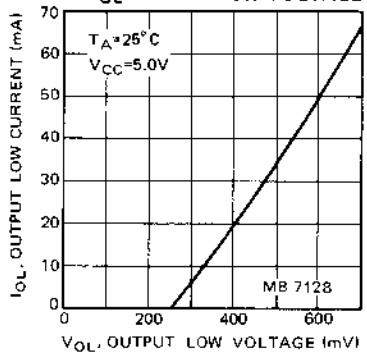
I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



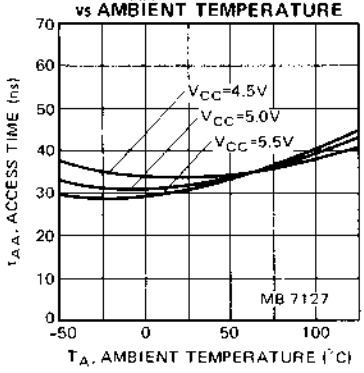
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



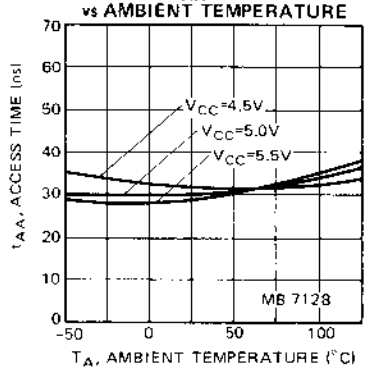
I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE



t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

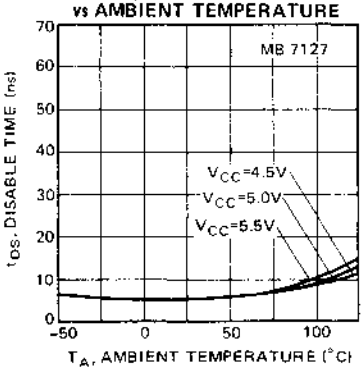


t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

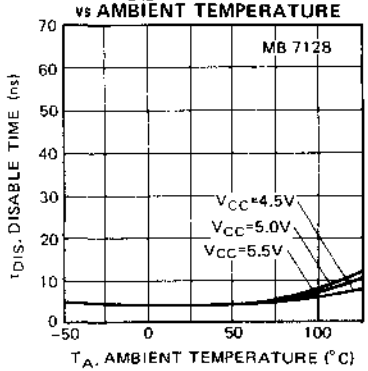


TYPICAL CHARACTERISTICS CURVES (Continued)

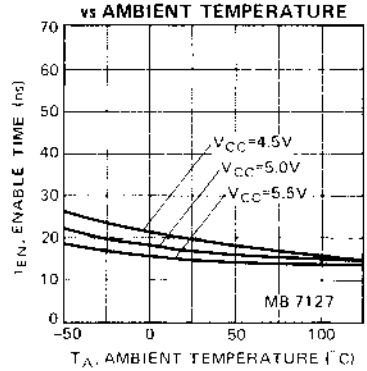
t_{OS} DISABLE TIME vs AMBIENT TEMPERATURE



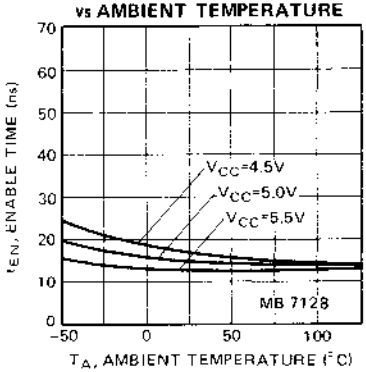
t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



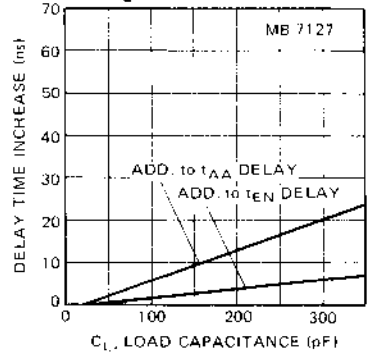
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



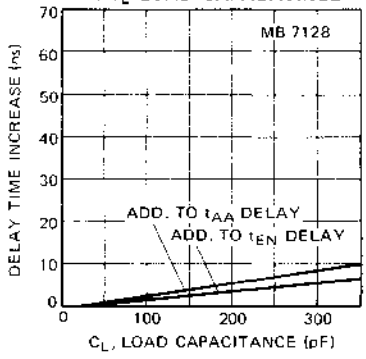
t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Shottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL-totem pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7128 (3-state) compared to 0mA for the MB7127 (open collector).

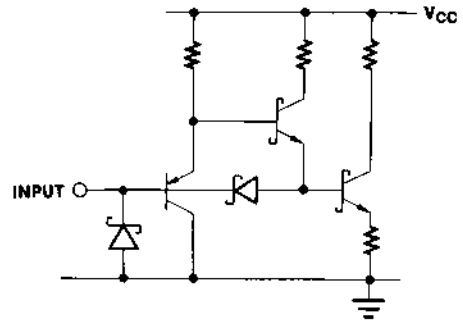
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH, and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a defineable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line drive capacity), plus the ability to connect to bus-organized systems.

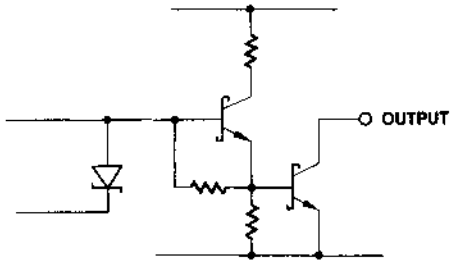
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease load on the Chip Enable circuit.

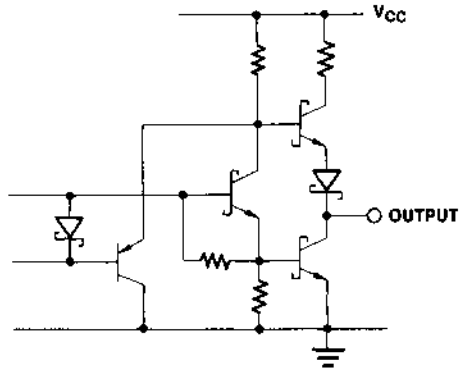
MB7127/MB7128 INPUT CIRCUIT



MB7127 OUTPUT CIRCUIT



MB7128 OUTPUT CIRCUIT



MB7127/MB7128 BIT MAP

	A_8 A_9 A_2 A_{10}
O_1	0 0 0 0 ≀ 1 1 1 0
O_2	0 0 0 0 ≀ 1 1 1 0
O_3	0 0 0 0 ≀ 1 1 1 0
O_4	0 0 0 0 ≀ 1 1 1 0

A_7	0	0
A_6	0	0
A_5	0	1
A_4	1	0
A_1	0	1
A_0	0	1
A_3	0	1

Multiplexer

A_8	A_9	A_2	A_{10}
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

Decoder/Driver

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111