FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-24100-4E

ASSP

PCM Coders/Decoders

MB6021A/MB6022A

■ DESCRIPTION

The Fujitsu CMOS MB6020A series consists of both μ-law and A-law single-chip coder/decoder (CODEC) filter ICs for either synchronous-only or synchronous/asynchronous operation. These monolithic, single-channel, voice-frequency CODECs incorporate both transmit and receive circuitries that are used for pulse coded modulation (PCM) systems.

■ FEATURES

- Transmit high-pass and low-pass filters
- Receive low-pass filter with SinX/X Correction
- Anti-aliasing filter
- Conforms to CCITT and AT & T specifications
- Synchronous and asynchronous operation
- Serial data rates of 64 kHz to 3.152 MHz
- PLL circuits serve as an internal clock generator
- Internal voltage reference
- Internal auto-zero circuit
- TTL-compatible digital interface
- Input gain adjust amplifier

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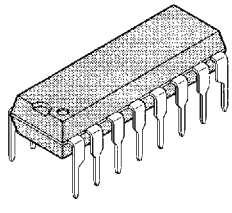
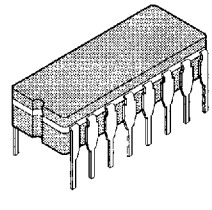
■ PACKAGES

16 pin, Plastic DIP



(DIP-16P-M03)

16 pin, Ceramic DIP



(DIP-16C-C04)

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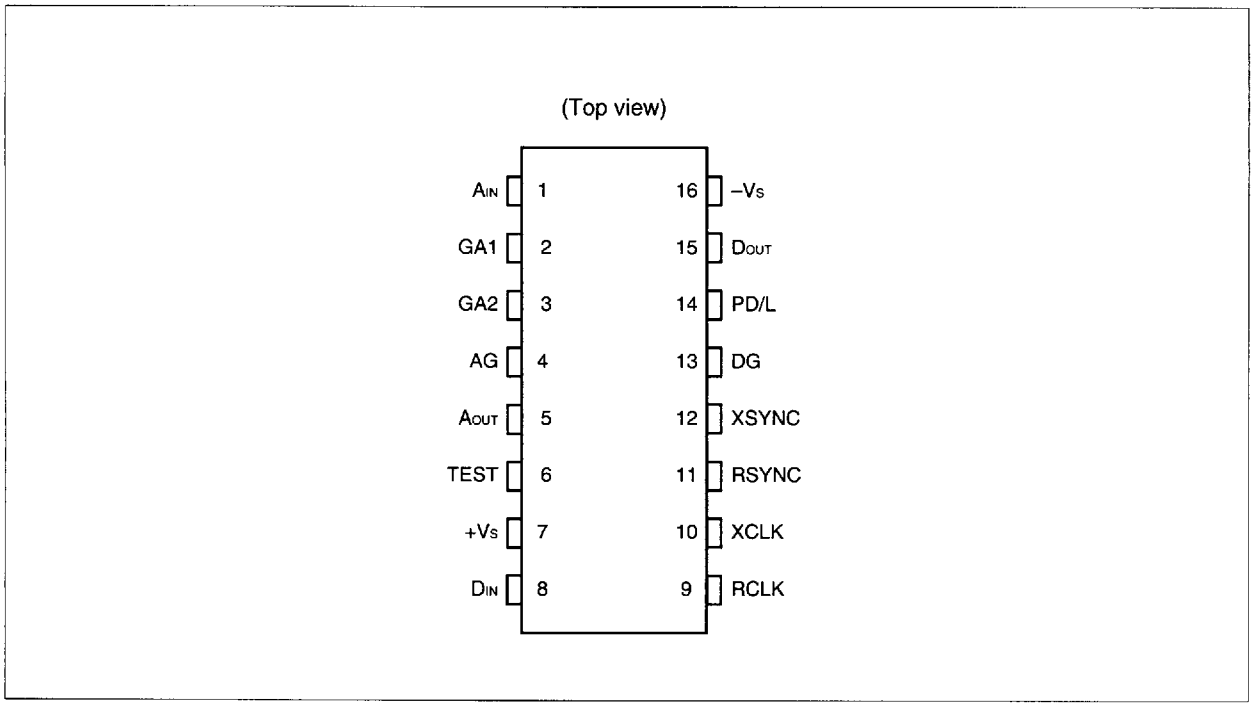
- Pin selectable on-chip analog loopback
- μ-law: MB6021A
  A-law: MB6022A
- Package and Ordering Information: 16-pin plastic DIP package
  Order as MB6021AP and MB6022AP

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin Name	Description
1	A_{IN}	**Analog Input** This is an input pin for analog signals to be filtered and coded.
2 3	GA1 GA2	**Gain Adjust1** **Gain Adjust2** These pins are provided for adjusting the gain of the Transmit Section. GA1 and GA2 are the inverted input and output of the amplifier, respectively. GA2 can drive a load impedance of 10 to 20 kΩ and 50 pF or less.
4	AG	**Analog Ground** All analog signals are referenced to this pin.
5	A_{OUT}	**Analog Output** This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 3 kΩ or greater, and 100 pF or less. This output is forced to AG level in the Analog Loopback Mode and Power-down Mode.
6	TEST	**Test** If this pin is at the TTL low level or left open, normal operating mode is selected. If it is connected to–Vs, the TEST mode is selected. In TEST mode, A_{IN} is internally connected to the coder input and its output is available on the D_{OUT} pin. Decoder output is available on the A_{OUT} pin. Applied voltage should not exceed 2.0 V.
7	+Vs	**Positive Voltage Supply:** +5 V ± 5%
8	D_{IN}	**Digital Input** This is a TTL-compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK.
9	RCLK	**Receive Clock** This TTL-compatible input defines the bit rate on the receive PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PMC codes are accepted on the falling edge of the clock.
10	XCLK	**Transmit Clock** This TTL-compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (D_{OUT}) pin on the rising edge of the XCLK.
11	RSYNC	**Receive Synchronization Clock** This TTL-compatible input defines the beginning of the recieve time slot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one RCLK cycle.
12	XSYNC	**Transmit Synchronization Clock** This TTL-compatible input defines the beginning of the transmit time slot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one XCLK cycle.
13	DG	**Digital Ground** All digital signals are referenced to this pin.

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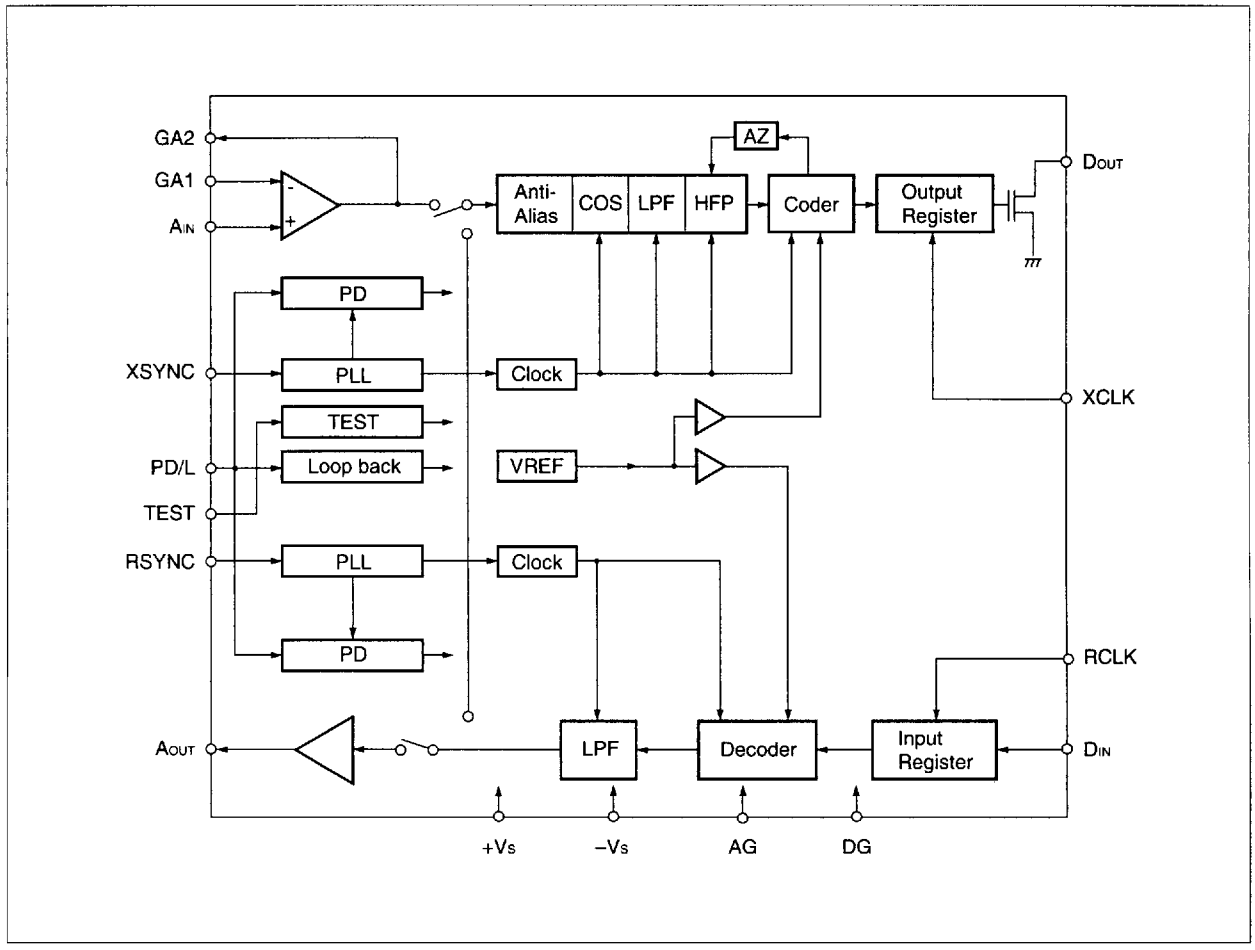
Pin No.	Pin Name	Description
14	PD/L	**Power-down/Analog Loopback** This three-level input is provided for the selection of the Power-down Mode or Analog Loopback Mode. If this pin is at the TTL high level, the normal operation is selected. If this pin is at the TTL low level, the device is powered down regardless of the synchronization clocks. If this pin is connected to–Vs, the Analog Loopback Mode is selected. In this mode, the output of the receive filter is internally connected to the input of the transmit filter and A_{OUT} is forced to AG level.
15	D_{OUT}	**Digital Output** This is a TTL-compatible open-drain output. A pull-up resistor with greater than 0.5 kΩ must be connected to +Vs. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
16	$-V_S$	**Positive Voltage Supply:** –5 V ± 5%

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

Figure 1 shows a simplifed block diagram of MB6021A and MB6022A.

The Transmit Section in the upper-half of the block diagram is comprised of an input gain amplifier, an anti-aliasing filter (Anti-Alias), a band-pass filter (COS, LPT, and HPF), and a compressing coder (Coder). An auto-zero circuit (AZ) is also included in this section. The Receive Section in the lower half of the block diagram is comprised of an expanding decoder (Decoder) and a low-pass filter (LPF).

Transmit Section

The Transmit Section receives analog signals that are input to an operational amplifier to provide gain adjustment. The signal from the op amp is transmitted to a second-order analog anti-aliasing filter (Anti-Alias). This filter provides attenuation of 40 dB (typical) at the 256 kHz effective clock frequency of the switched capacitor cosine filter (COS). From the cosine filter, the signals enter a fifth-order low-pass filter (LPF) clocked at 128 kHz. From the LPF, the signals pass into a third-order high-pass filter (HPF) clocked at 128 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCIT G. 712 recommendation. The output of the high-pass filter is then sampled by the coder (Coder) at 8 kHz. This coder transforms the analog signals into 8-bit words using compression law. The encoded PCM data is then output serially from the Output Register at a frequency determined by the external clock, 64 kHz to 3.152 MHz. An auto-zero circuit (AZ) is utilized for DC offset correction.

Receive Section

The Receive Section's Input Register filter smooths the decoded signals and corrects for SinX/X attenuation caused by the 8 kHz sample and hold operation. The decoder reconstructs the analog signals from the PCM data using expansion law. The output from the decoder is transmitted to a fifth-order low-pass filter (LPF). This LPF smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

Internal Clocks

Two independent phase locked loops (PLLs) generate internal clocks for the Transmit and Receive Sections from the respective synchronization clocks (XSYNC and RSYNC).

■ OPERATING MODES

Analog Loopback Mode

The Analog Loopback Mode allows all decoding and coding functions to be exercised without using the analog input (A_{IN}) and analog output (A_{OUT}). In this mode, a digital input signal is decoded and internally routed to the transmit filters. The output is available from the digital output (D_{OUT}). The analog output (A_{OUT}) is forced to the analog ground (AG) level. The Analog Loopback Mode is selected by connecting the PD/L input to the negative supply voltage (−Vs).

Power-down Mode

Two Power-down Modes are provided. The Transmit and Receive Sections independently go into power-down operation in the absence of the respective synchronization clocks (XSYNC and RSYNC). If the external power down input (PD/L) is connected to a TTL low level, both the Transmit and Receive Sections are powered down regardless of the synchronization clocks. During power-down operation, A_{OUT} is forced to the level of AG, and D_{OUT} goes into a high-impedance state.

Test Mode

In the Test Mode the TEST pin is connected to −Vs. The Test Mode allows independent evaluation of the coder and decoder. In this mode, A_{IN} is internally connected to the input of the coder and its output is available on the D_{OUT} pin. The output of the decoder is made available on the A_{OUT} pin.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Pin No.	Symbol	Rating		Unit
			Min.	Max.	
Positive supply voltage	7	$+V_S$	–0.3	7	V
Negative supply voltage	16	$-V_S$	–7	0.3	V
Test	6	TEST	$-V_S$	$+V_S$	V
Analog input voltage	1	V_{AIN}	$-V_S - 0.3$	$+V_S + 0.3$	V
Digital input voltage	8, 9, 10, 11, 12	V_{DIN1}	–0.3	$+V_S + 0.3$	V
Digital input voltage	6, 14	V_{DIN2}	$-V_S - 0.3$	$+V_S + 0.3$	V
Storage temperature	—	Tstg	–55	150	°C

WARNING: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Pin No.	Symbol	Value			Unit
			Min.	Typ.	Max.	
Positive supply voltage	7	$+V_S$	+4.75	+5.0	+5.25	V
Negative supply voltage	16	$-V_S$	–5.25	–5.0	–4.75	V
Digital output load resistance	15	R_{DL}	0.5	—	—	kΩ
Digital output load capacitance	15	C_{DL}	—	—	144	pF
Analog output load resistance	5	R_L	3	—	—	kΩ
Analog output load capacitance	5	C_L	—	—	100	pF
Operating temperature	—	T_{OP}	0	25	70	°C

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Pin No.	Conditions	Value			Unit
				Min.	Typ.	Max.	
Positive supply current	$+I_{VS}$	7	Operating	—	7.0	10.0	mA
Negative supply current	$-I_{VS}$	16	Operating	−10.0	−5.0	—	mA
Positive supply current power down mode	$+I_{VSST}$	7	XSYNC= RSYNC=V_{IL} SYNC=V_{IL}	—	1.0	2.0	mA
			PD/L = V_{IL}	—	0.3	1.0	mA
Negative supply current power down mode	$-I_{VSST}$	16	XSYNC= RSYNC=V_{IL} SYNC=V_{IL}	−0.5	−0.1	—	mA
			PD/L = V_{IL}	−0.5	−0.1	—	mA
Digital input high voltage	V_{IH}	8, 9, 10, 11, 12, 14	—	2.0	—	+VS	V
Digital input low voltage	V_{IL}	8, 9, 10, 11,12,14	—	0	—	0.8	V
Digital input high current	I_{IH}	8, 9, 10, 11, 12, 14	—	—	—	10	μA
Digital input low current	I_{IL}	8, 9, 10, 11,12,14	—	−10	—	—	μA
Digital input capacitance	C_{DIN1}	8, 9, 10, 11,12,14	—	—	—	10	pF
Digital input capacitance	C_{DIN2}	—	—	—	—	20	pF
Digital output low voltage	V_{OL1}	15	R_{DL}= 0.5 kΩ $+I_{OL}$ = 0.4 mA	—	—	0.4	V
Digital output leakage current	I_{LO}	15	—	—	—	10	μA
Digital output capacitance	C_{DOUT}	15	—	—	—	12	pF
Analog input offset voltage	A_{INOFF}	1	—	−200	0	200	mV
Analog input resistance	R_{AIN}	1	—	300	—	—	kΩ
Analog input capacitance	C_{AIN}	1	—	—	—	10	pF
Analog output offset voltage	A_{OUTOFF}	5	—	−150	—	150	mV
Analog output resistance	R_{AOUT}	5	—	—	10	30	Ω
Pull down current	I_{PLD}	6	V_{IN} = +2.0 V	0	—	80	μA

2. AC Characteristics

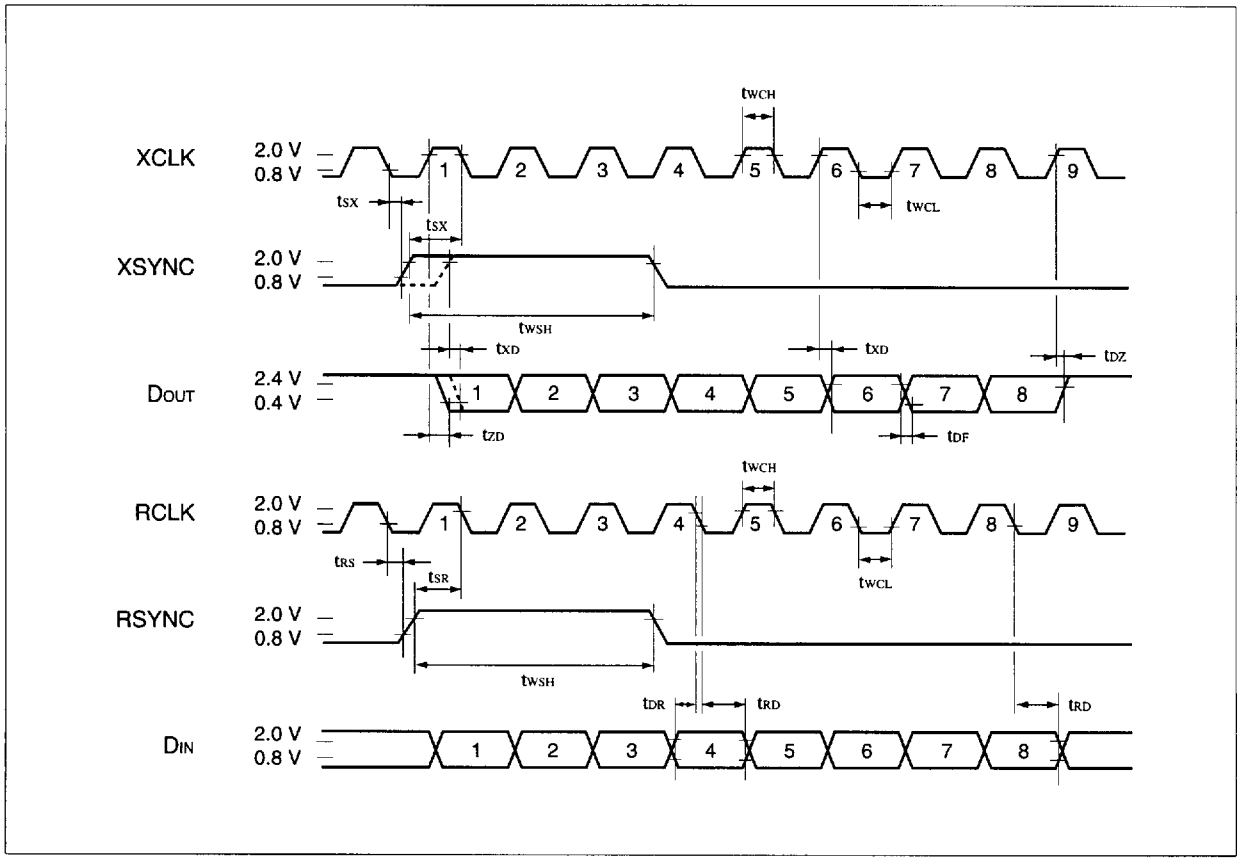
Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Pin No.	Conditions	Value			Unit
				Min.	Typ.	Max.	
Digital input rise time	t_r	8, 9, 10, 11, 12	0.8V → 2.0V	—	—	50	ns
Digital input fall time	t_f	8, 9, 10, 11, 12	2.0V → 0.8V	—	—	50	ns
Shift clock frequency	F_C	9, 10	—	64	—	3152	kHz
Shift clock high width	t_{WCH}	9, 10	V_{IH} = 2.0 V	140	—	—	ns
Shift clock low width	t_{WCL}	9, 10	V_{IL} = 0.8 V	140	—	—	ns
Synchronization frequency	F_S	11, 12	—	—	8	—	kHz
Synchronization high width	t_{WSH}	11,12	V_{IH} = 2.0 V	1/F_C F_C:MHz	—	117	µA
XSYNC to XCLK delay	t_{SX}	10,12	—	100	—	—	ns
XCLK to XSYNC delay	t_{XS}	10,12	—	50	—	—	ns
RSYNC to RCLK delay	t_{SR}	9, 11	—	100	—	—	ns
RCLK to RSYNC delay	t_{RS}	9, 11	—	50	—	—	ns
RCLK to D_{IN} delay	t_{RD}	8,9	—	50	—	—	ns
D_{IN} to RCLK delay	t_{DR}	8,9	—	50	—	—	ns
XCLK or XSYNC to D_{OUT} delay*1	t_{ZD}	10, 12, 15	—	30	—	200	ns
XCLK to D_{OUT} delay*2	t_{XD}	10, 15	—	30	—	200	ns
XCLK to D_{OUT} disable time	t_{DZ}	10, 15	High-Z	30	—	200	ns
D_{OUT} fall time	t_{DF}	15	—	10	—	100	ns

*1: Bit 1 D_{OUT} load conditions: R_{DL} = 0.5 kΩ, C_{DL} = 144 pF, $+I_{OL}$ = 0.4 mA

*2: Bit 2 to 8 D_{OUT} load conditions: R_{DL} = 0.5 kΩ, C_{DL} =144 pF, $+I_{OL}$ = 0.4 mA

■ TIMING DIAGRAM



■ TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A)

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Signal to distortion (A to A)	SDA	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	35.0 30.0 25.0	—	—	dB dB dB
Signal to distortion (A to D)	SDX	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
Signal to distortion (D to A)	SDR	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
Gain tracking (A to A)	GTA	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.4 –0.8 –2.0	—	0.4 0.8 2.0	dB dB dB
Gain tracking (A to D)	GTX	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Gain tracking (D to A)	GTR	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Frequency response (A to A)	FRA	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6 	dB dB dB dB dB dB
Frequency response (A to D)	FRX	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB
Frequency response (D to A)	FRR	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB

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Notes: 1. $29\,(1 - \mathrm{Sin}\,\frac{\pi\,(4000-f)}{1200})$

2. $29\,(1 - \mathrm{Sin}\,\frac{\pi\,(4000-f)}{1200})$

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Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Idle channel noise (A to A)	ICNA	C message	—	–80	–72.0	dBm0c
Idle channel noise (A to D)	ICNX	C message	—	–83	–74.0	dBm0c
Idle channel noise (D to A)	ICNR	C message	—	–83	–78.0	dBm0c
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute level	VABS	Overload Level 3.17 dBm0	—	2.500	—	V_{OP}
Analog input level	AIL	1020 Hz, 0dBm0 ±Vs = ±5.0 V, Ta = +25°C	—	1.227	—	V_{rms}
Analog output level	AOL	1020 Hz, 0dBm0 ±Vs = ±5.0 V, Ta = +25°C	1.206	1.227	1.248	V_{rms}
Gain accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF	–0.5	0	+0.5	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.3	0	+0.3	dB
Gain accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Gain accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.15	0	+0.15	dB
		Variation with power supply		±0.02		dB
		Variation with temperature		±0.001		dB/°C
Propagation delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	µs
Delay to distortion (A to A)	DDA	500 to 600 Hz	—	—	1.5	ms
		600 to 1000 Hz			0.75	ms
		1000 to 2600 Hz			0.25	ms
		2600 to 2800 Hz			1.5	ms
		1020 Hz, 0dBm0 Relative to minimum delay				

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Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle Channel Noise (C Message) +Vs +50 m Vop AIN = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle Channel Noise (C Message) –Vs +50 m Vop AIN = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	AIN a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 AOUT (2a – b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	AIN a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 AOUT (a – b)	—	—	–52	dBm0
Signal frequency noise (A to A)	SFNA	0 to 4 kHz 4 to 200 kHz AIN = AG	—	—	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	AIN = 0dBm0 4.6 to 200 kHz	30	—	—	dB
In band spurious (A to A)	IBSA	2nd, 3rd Harmonic AIN = 0dBm0, 700 – 1100 Hz	43	—	—	dB

■ TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A)

At recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Signal to distortion (A to A)	SDA	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 30.0 25.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	28.0 35.5 33.5 28.5 13.5	—	—	dB dB dB dB dB
Signal to distortion (A to D)	SDX	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB
Signal to distortion (D to A)	SDR	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB
Gain tracking (A to A)	GTA	CCITT G.712 Method 2 1020 Hz tone	+3 to −30 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.4 −0.8 −2.0	—	0.4 0.8 2.0	dB dB dB
		CCITT G.712 Method 1	−10 to −50 dBm0 −55 to −60 dBm0	−0.5 −1.0	—	0.5 1.0	dB dB
Gain tracking (A to D)	GTX	CCITT G.712 Method 2 1020 Hz tone	+3 to −30 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.2 −0.4 −0.8	—	0.2 0.4 0.8	dB dB dB
		CCITT G.712 Method 1	−10 to −50 dBm0 −50 to −55 dBm0 −55 to −60 dBm0	−0.25 −0.4 −0.8	—	0.25 0.4 0.8	dB dB dB

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Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Gain tracking (D to A)	GTR	CCITT G.712 Method 2 1020 Hz tone	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
		CCITT G.712 Method 1	–10 to –50 dBm0	–0.25	—	0.25	dB
			–50 to –55 dBm0	–0.4		0.4	dB
			–55 to –60 dBm0	–0.8		0.8	dB
Frequency response (A to A)	FRA	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6	dB dB dB dB dB dB
Frequency response (A to D)	FRX	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8	dB dB dB dB dB dB
Frequency response (D to A)	FRR	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8	dB dB dB dB dB

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Notes: 1. $29\,(1 - \mathrm{Sin}\,\frac{\pi\,(4000-f)}{1200})$

2. $14.5\,(1 - \mathrm{Sin}\,\frac{\pi\,(4000-f)}{1200})$

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Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Idle channel noise (A to A)	ICNA	P Message	—	–80	–72.0	dBm0p
Idle channel noise (A to D)	ICNX	P Message	—	–83	–74.0	dBm0p
Idle channel noise (D to A)	ICNR	P Message	—	–83	–78.0	dBm0p
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute level	VABS	Overload Level 3.14 dBm0	—	2.500	—	V_{OP}
Analog input level	AIL	1020 Hz, 0dBm0 Internal VREF ±Vs = ±5.0 V, Ta = +25°C	—	1.231	—	V_{rms}
Analog output level	AOL	1020 Hz, 0dBm0 Internal VREF ±Vs = ±5.0 V, Ta = +25°C	1.210	1.231	1.252	V_{rms}
Gain accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF	–0.5	0	+0.5	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.3	0	+0.3	dB
Gain accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Gain accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = +25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Propagation delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	µs

(Continued)

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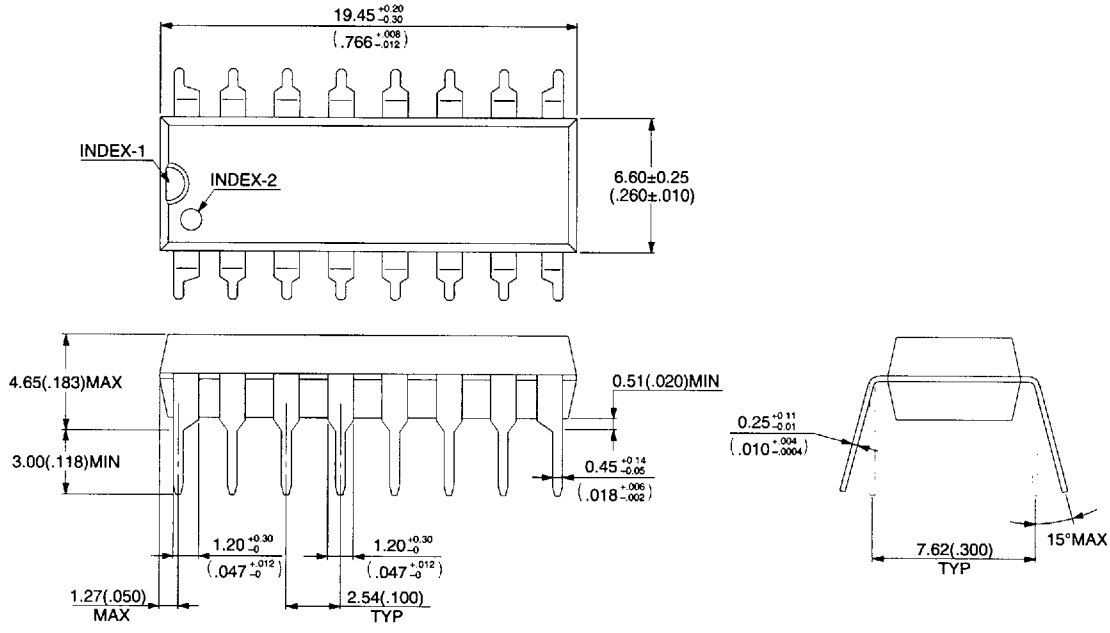
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Delay to distortion (A to A)	DDA	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to minimum delay	— — — —	— — — —	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle channel noise (P Message) +V_S +50 m V_{OP} A_{IN} = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle channel noise (P Message) +V_S +50 m V_{OP} A_{IN} = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	A_{IN} a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 A_{OUT} (2a – b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	A_{IN} a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 A_{OUT} (a – b)	—	—	–52	dBm0
Signal frequency noise (A to A)	SFNA	0 to 4 kHz 4 kHz to 200 kHz A_{IN} = AG	— —	— —	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	A_{IN} = 0dBm0 4.6 kHz to 200 kHz	30	—	—	dB
In band spurious (A to A)	IBSA	2nd, 3rd harmonic A_{IN} = 0dBm0, 700 to 1100 Hz	43	—	—	dB

■ PACKAGE DIMENSIONS

16 pin, Plastic DIP
(DIP-16P-M03)

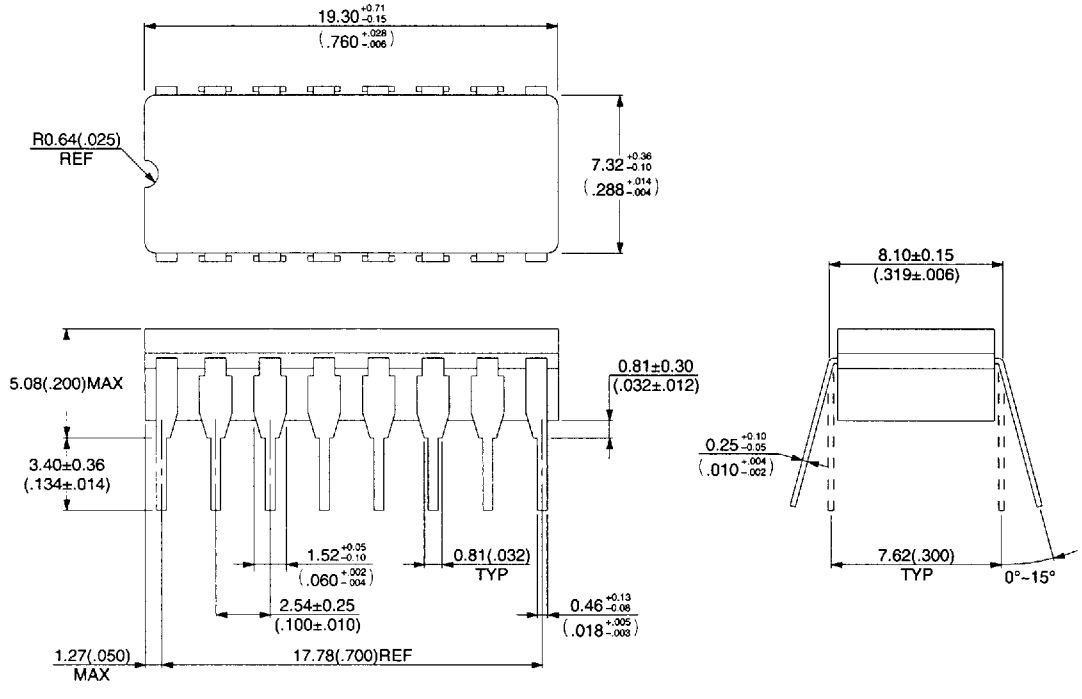


Dimensions in mm (inches)

(Continued)

(Continued)

16 pin, Ceramic DIP
(DIP-16C-C04)



Dimensions in mm (inches)