FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27243-1E

ASSP For Power Supply Applications

(Switching FET Integrated DC/DC Converter)

1ch PFM/PWM Synchronous Rectification Step-down Regulator

MB39C001

■ DESCRIPTION

The MB39C001 is a synchronous rectification type of single-channel, step-down DC/DC converter IC using current mode control.

The MB39C001 integrates switching FETs, an oscillator, error amplifier, voltage detector, and a reference voltage generator in a 18-pin BCC package. The required external components are only a coil and decoupling capacitors.

The MB39C001 is small in size, and can achieve a DC/DC converter highly effective in the full load range, and it is the best for internal power supplies for portable devices such as cellular phones, PDAs and DSC.

■ FEATURES

- High efficiency : 96% Max
- Quiescent current : 20 µA (in PFM mode)
- Output current (DC/DC) : 600 mA Max
- Input voltage range : 2.5 V to 5.5 V
- Oscillation frequency : 1.0 MHz (in PWM mode)
- No flyback diode needed
- Low dropout operation : 100% on-duty support

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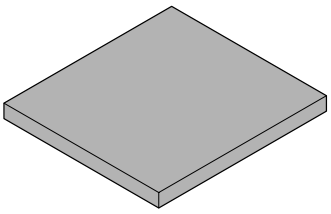
■ PACKAGE

18-pin plastic BCC



(LCC-18P-M05)

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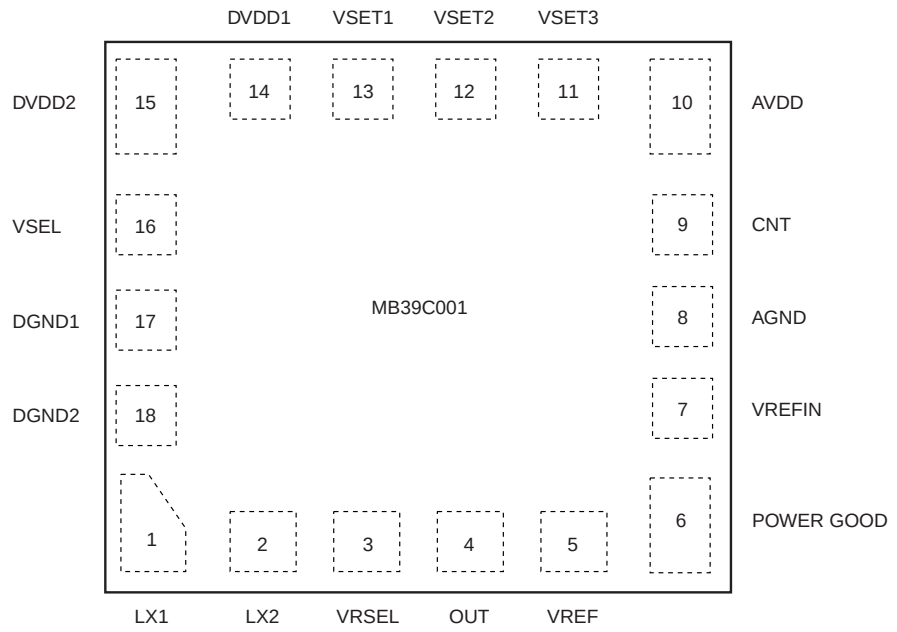
- High-precision reference voltage generator integrated : 1.25 V ± 2% (with no load)
- Output voltage select function integrated : Capable of selecting internal setting (3 bits) or external setting
- Built-in switching FETs : PMOS 0.43 Ω (Typ) , NMOS 0.32 Ω (Typ)
- Current mode control providing quick transition response to inputs/loads
- Built-in temperature protection function
- Low consumption current at shutdown mode : 1 μA or less
- Built-in undervoltage lockout protection circuit (UVLO) : Circuit actuation voltage of 2.3 V (Typ)
- Small package : BCC-18P

■ PIN ASSIGNMENT

(TOP VIEW)

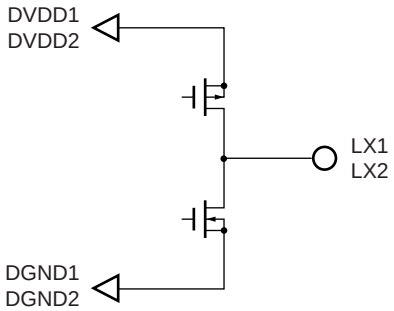


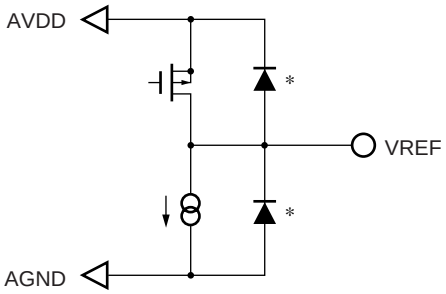
LCC-18P-M05

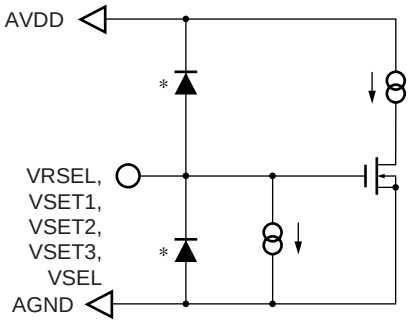
■ PIN DESCRIPTION

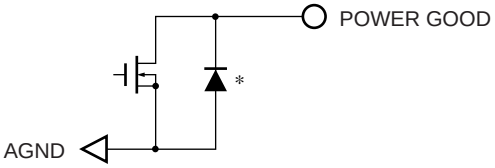
Pin No.	Symbol	I/O	Description
1, 2	LX1, LX2	O	Inductor connection output terminals. Connect mutually and use the LX1 and LX2 terminal. They enter the high impedance state at shutdown.
3	VRSEL	I	Reference voltage switch terminal. (Refer (2) “Setting output voltages” in ■ APPLICATION NOTES)
4	OUT	I	Output voltage feedback terminal.
5	VREF	O	Reference voltage (1.25 V) output terminal.
6	POWER GOOD	O	POWERGOOD circuit output terminal. An N-ch MOS open-drain circuit is connected.
7	VREFIN	I	Error amplifier (ErrorAmp) noninverting input terminal.
8	AGND	—	Control block ground terminal.
9	CNT	I	Control input terminal (L : Shutdown, H : Normal operation) .
10	AVDD	—	Control block power-supply terminal.
11	VSET3	I	Output voltage setting terminal. (Refer (2) “Setting output voltages” in ■ APPLICATION NOTES)
12	VSET2	I	
13	VSET1	I	
14, 15	DVDD1, DVDD2	—	Drive block power-supply terminal.
16	VSEL	I	Output voltage switch terminal. (Refer (2) “Setting output voltages” in ■ APPLICATION NOTES.)
17, 18	DGND1, DGND2	—	Drive block ground terminal.

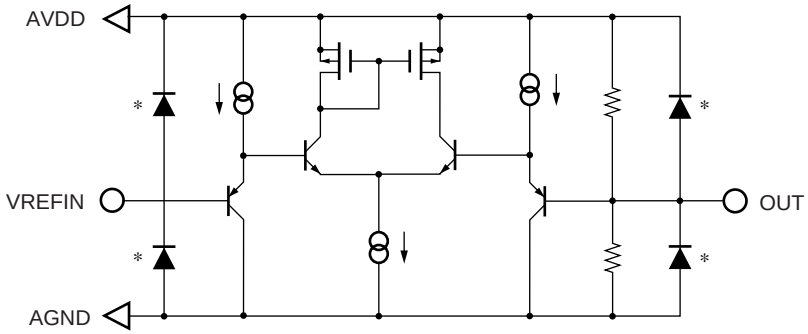
■ I/O TERMINAL EQUIVALENT CIRCUIT DIAGRAM

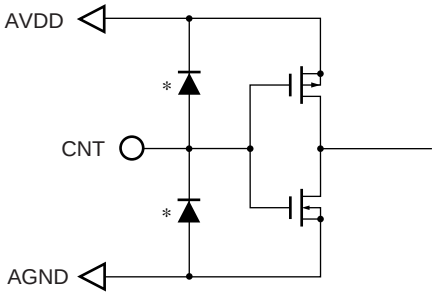






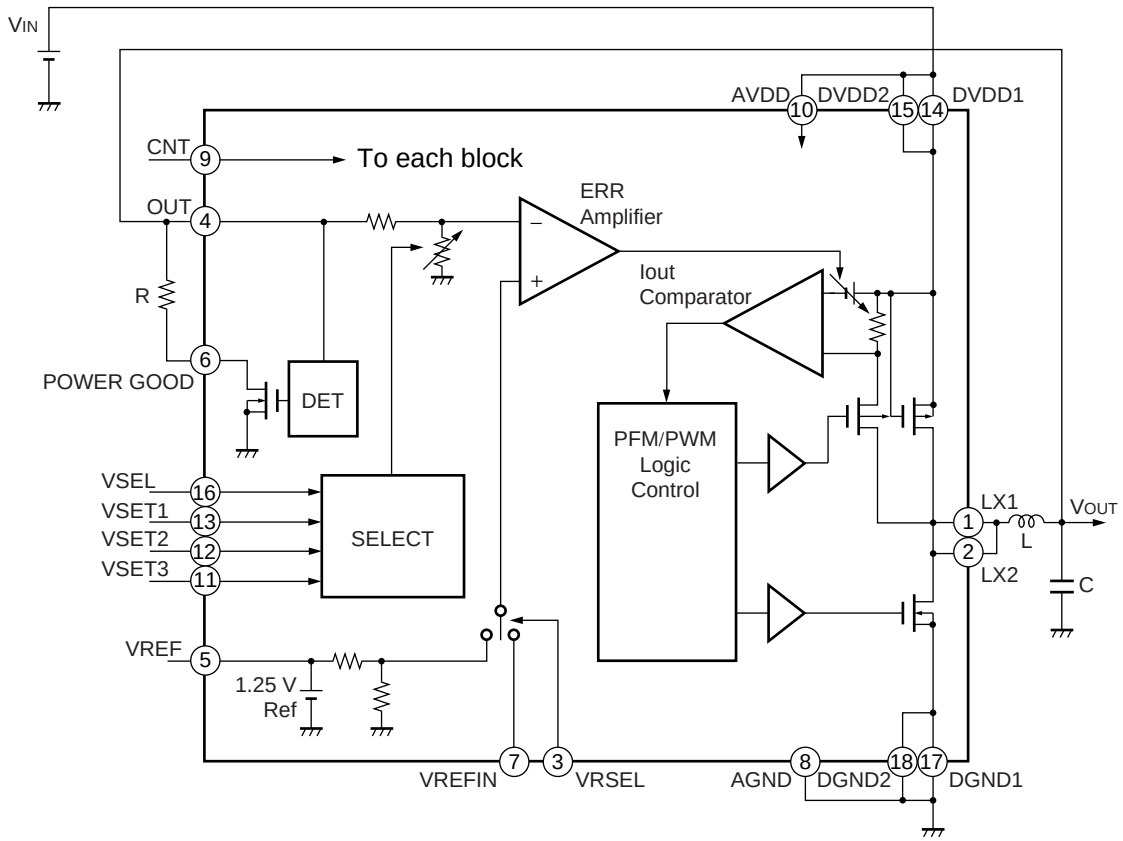






* : ESD protection element

■ BLOCK DIAGRAM



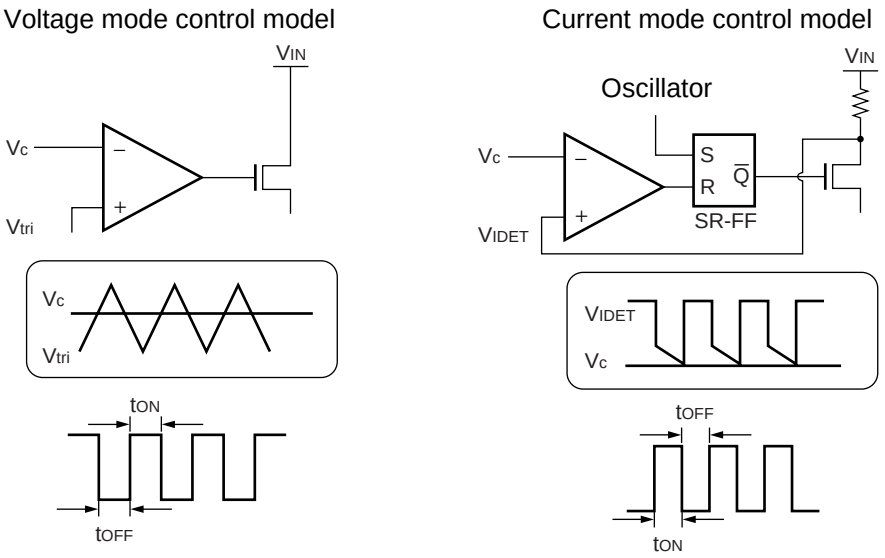
■ FUNCTIONS

About the Current Mode

Conventional voltage mode control compares the voltage (Vc) obtained by applying negative feedback to the output voltage using the ErrAmp with the reference triangular waveform (Vtri) to control the on-duty cycle, thereby regulating the output voltage.

Current mode control uses the oscillator (rectangular waveform generator) , and the voltage (V_{IDET}) obtained by applying I-V conversion to the current which flows into SW FET, and uses them in place of the triangular waveform.

Current-mode control compares the voltage (Vc) obtained by applying negative feedback to the output voltage using the ErrAmp with V_{IDET} to control the on-duty cycle, thereby regulating the output voltage.



Note : The above models illustrate principles of operation; they are slightly different from actual operations of the IC.

Function of Each Block

- PFM/PWM Logic Control Circuit
  This circuit controls the synchronous rectification of internal P-channel MOS FET and N-channel MOS FET at the frequency (1 MHz), set by the internal oscillator (rectangular waveform oscillator) during normal operation. Under light loads, the circuit performs intermittent (burst) operation.
  The precaution of the penetration current caused by synchronous rectification and the reverse current flowing during discontinuous operation are performed to this circuit.

- Iout Comparator Circuit
  This circuit detects the current (I_{LX}) flowing from the internal P-channel MOS FET to the external inductor. The circuit compares the output of ErrAmp with V_{IDET}, obtained by applying I-V conversion to the I_{LX} peak current (I_{PK}), and approaches the PFM/PWM Logic Control circuit to turn off the internal P-channel MOS FET.

- ErrAmp phase compensation circuit
  This circuit compares reference voltages such as VREF with output voltages. The IC contains a phase compensation circuit and adjusted for the best operation of this IC, and it is eliminating the need for nominating a phase compensation circuit and adding an external component for phase compensation.

- VREF circuit
  A high-accuracy reference voltage is generated by a BGR (band gap reference) circuit. The output voltage is 1.25 V (Typ).

- SELECT circuit
  This circuit is used to select a pre-set output voltage. The voltage can be set by changing the division resistance value at the earlier stage of the ErrAmp.

- DET circuit
  This circuit monitors the OUT terminal voltage. When that voltage reaches the output set voltage, the open-drain output at the POWER GOOD terminal is turned on.

- Protection circuit
  An over temperature protection circuit is built in the IC as a protection circuit.
  The over temperature protection circuit turns off both of the N-channel and P-channel SW FETs when the junction temperature reaches 135°C.
  Also, when the junction temperature falls to 110 °C, the over temperature protection circuit operates normally.
  Although the IC has no overcurrent protection circuit as a dedicated circuit, it uses current mode control for voltage control, and thus the peak-current value is monitored and controlled at any time. (The maximum peak-current value is 1 A.)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings		Unit
			Min	Max	
Power supply voltage	V_{IN}	AVDD, DVDD1, and DVDD2 terminals	—	7	V
Input voltage	V_I	OUT terminal	–0.3	V_{DD} + 0.3	V
		CNT, VSEL, VSET1, VSET2, VSET3, and VRSEL terminals	–0.3	V_{DD} + 0.3	
		VREFIN terminal	–0.3	V_{DD} + 0.3	
POWER GOOD pull-up voltage	VI_{PG}	—	—	7	V
LX voltage	V_{LX}	LX1/LX2 terminal	–0.3	V_{DD} + 0.3	V
LX peak current	I_{PK}	LX1/LX2 terminal	—	1.3	A
Power dissipation	P_D	Ta ≤ + 25 °C	—	540*	mV
Operating ambient temperature	Ta	—	–40	+ 85	°C
Storage temperature	T_{STG}	—	– 55	+ 125	°C

* : The package is mounted on a 10x10-cm square, dual sided epoxy board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power supply voltage	V_{IN}	AVDD, DVDD1, and DVDD2 terminals	2.5	3.7	5.5	V
VREFIN voltage	V_{RIN}	—	0.3	—	0.7	V
LX current	I_{LX}	$V_{IN} - V_{OUT} \geq 0.7$ V*	—	—	600	mA
POWERGOOD current	I_{PG}	—	—	—	1	mA

* : The output possible current can be tends to decrease when the voltage difference between the power supply voltage (V_{IN}) and DC/DC converter output voltage (V_{OUT}) is small. This is because of an effect of slope compensation; it does not lead to the breakdown of the device. If it is the using condition which suppresses the output current, it is possible to use it also with "V_{IN}-V_{OUT}<0.7 V".

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified , V_{IN} = 3.7 V, CNT = 3.7 V, VSET1 = VSET2 = 0 V, VSET3 = VSEL = 3.7 V, VRSEL = 0 V, Ta = +25°C)

Parameter		Symbol	Pin No.	Condition	Values			Unit
					Min	Typ	Max	
DC/DC converter block	Reference voltage	V_{REF}	5	VREF = 0 mA	1.21	1.25	1.29	V
	Input current	I_{REFIN}	7	VREFIN = 0.6 V, VRSEL = 3.7 V	–100	–40	—	nA
	Output voltage	V_{OUT}	4	Load current = –200 mA*1	1.764	1.8	1.836	V
	Input stability	Line		2.5 V < DVDD = AVDD < 5.5 V*2 Load current = 0 mA	—	—	40	mV
	Load stability	Load		–200 mA > Load current > –600 mA	—	—	20	mV
	OUT terminal Input impedance	R_{OUT}		OUT = 2.0 V	—	1.01	—	MΩ
	LX peak current	I_{PK}	1, 2	OUT = 90%	—	1	—	A
	Oscillation frequency	fosc		—	0.8	1.0	1.2	MHz
		f_{SHORT}		OUT = 0 V	100	170	240	kHz
	Rise delay time	t_{PG}	6	—	—	80	—	µs
	SW PMOS-FET ON resistor	R_{PMOS}	1, 2	LX1 + LX2 = –100 mA	—	0.43	—	Ω
	SW NMOS-FET ON resistor	R_{NMOS}		LX1 + LX2 = 100 mA	—	0.32	—	Ω
	SW FET leak current	I_{LEAK}		—	—	—	1	µA
Output voltage select block	Input threshold voltage	V_{TH}	3,9,11, 12,13,16	CNT, VSEL, VSET1, VSET2, VSET3, VRSEL terminal	0.3	1.0	1.5	V
	Input current	I_I	9	CNT terminal	—	0	1	µA
			3,11,12, 13,16	VSEL, VSET1, VSET2, VSET3, VRSEL terminal	—	0.1	1	µA
Protection circuit block	Over temperature protection (junction temperature)	T_{OTPH}	4	—	—	135*	—	°C
		T_{OTPL}		—	—	110*	—	°C
	UVLO threshold voltage	V_{THH}	4, 10, 14, 15	—	—	2.3	—	V
		V_{THL}		—	—	2.15	—	V
	UVLO hysteresis width	V_{HYS}		—	—	0.15	—	V

* : Standard design value

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(Unless otherwise specified , V_{IN} = 3.7 V, CNT = 3.7 V, VSET1 = VSET2 = 0 V, VSET3 = VSEL = 3.7 V, VRSEL = 0 V, Ta = +25°C)

Parameter		Symbol	Pin No.	Condition	Values			Unit
					Min	Typ	Max	
POWER GOOD circuit block	Threshold voltage	V_{THHPG}	4, 6	*3	86	90	94	%
		V_{THLPG}			84	88	92	%
	Hysteresis width	V_{HYSPG}		—	—	2	—	%
	Output voltage	V_{OL}	6	POWER GOOD = 25 µA	—	—	0.1	V
	Output current	I_{OH}		POWER GOOD = 5.5 V	—	—	1	µA
General	Power supply current at shutdown	I_{VDD1}	10, 14, 15	CNT = 0 V, All circuits = OFF*4	—	—	1	µA
	Power supply current on standby	I_{VDD2}		Load current = 0 mA	—	20	35	µA
	Power supply current during operation	I_{VDD3}		VOUT = 90% or OUT = 1.62 V*5	—	300	400	µA

* : Standard design value

*1 : Refer (2) “Setting output voltages” in ■ APPLICATION NOTES.)

*2 : The minimum V_{IN} value is 2.5 V or “output voltage setting value + 0.4 V”, either high one.

*3 : Detection to the output voltage setting value by VSET1 to VSET3. Refer (2) “Setting output voltages” in ■ APPLICATION NOTES.)

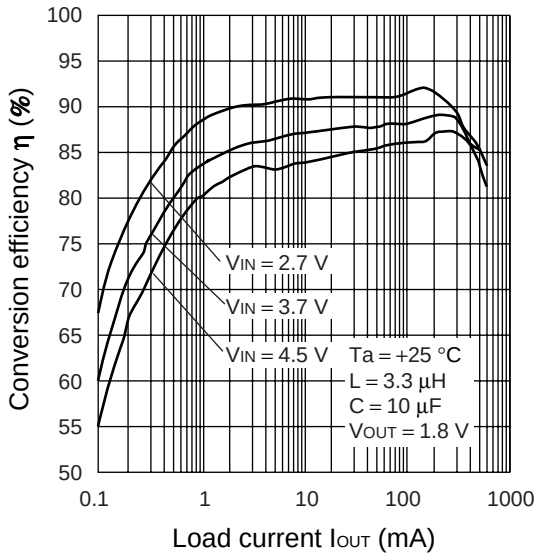
*4 : The sum of the currents flowing to the AVDD terminal, DVDD1 terminal, and DVDD2 terminal.

*5 : Current consumption at a duty cycle of 100% (with the main SW FET full-on). The SW FET gate drive current is not included because of a full-on state (not performing SW operation). And, the load current is not similarly included.

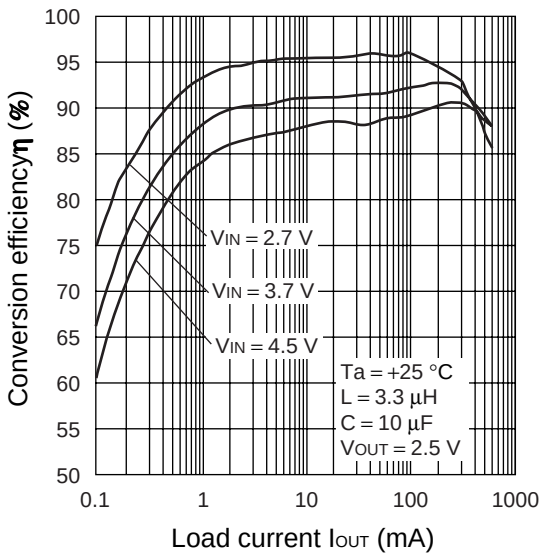
■ TYPICAL OPERATING CHARACTERISTICS

(The following characteristics are provided for setup reference purposes only; they are not guaranteed characteristics.)

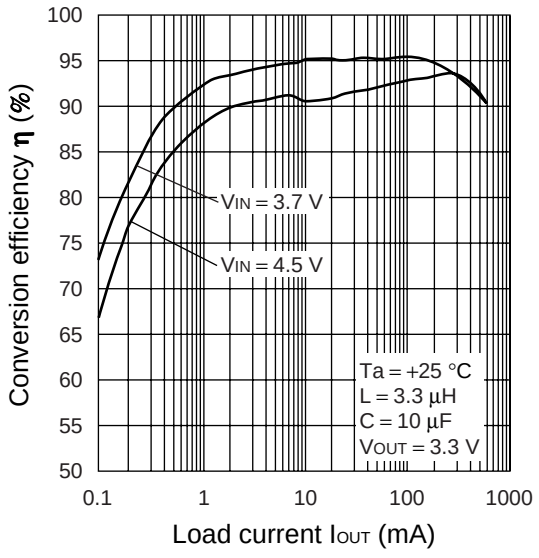
Conversion efficiency vs. Load current



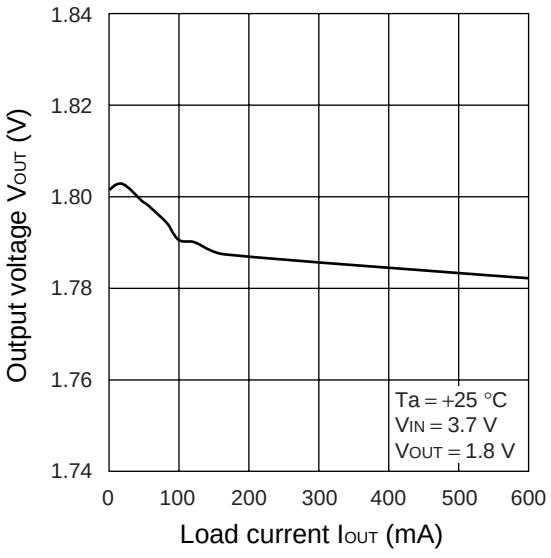
Conversion efficiency vs. Load current



Conversion efficiency vs. Load current



Output voltage vs. Load current



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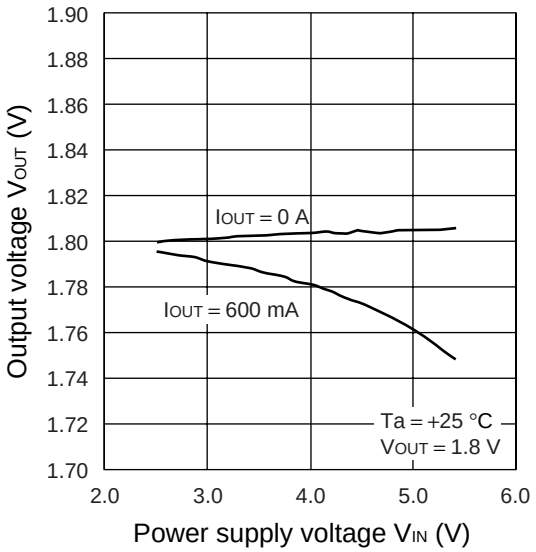
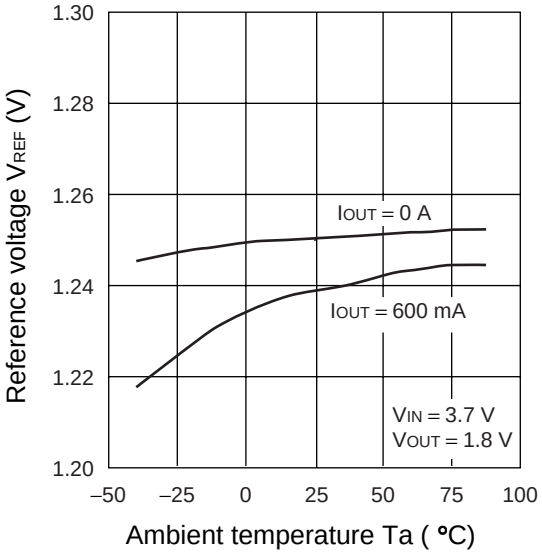
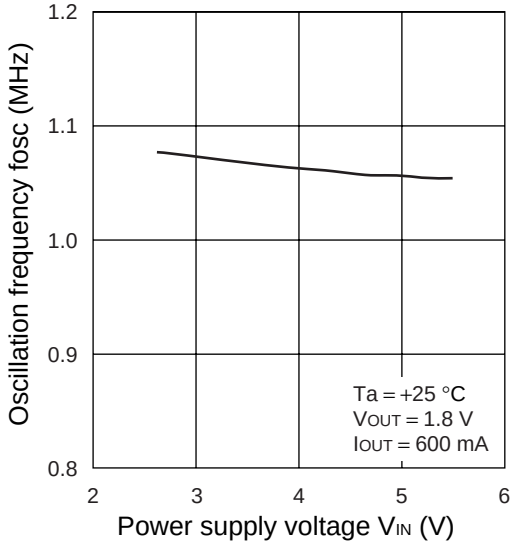
Output voltage vs. Power supply voltage



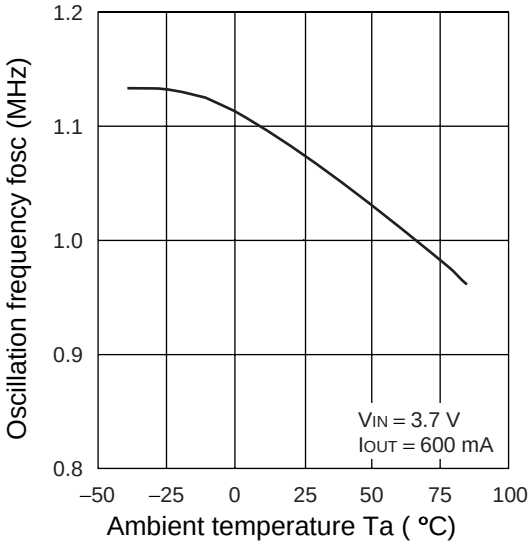
Reference voltage vs. Ambient temperature



Oscillation frequency vs. Power supply voltage



Oscillation frequency vs. Ambient temperature



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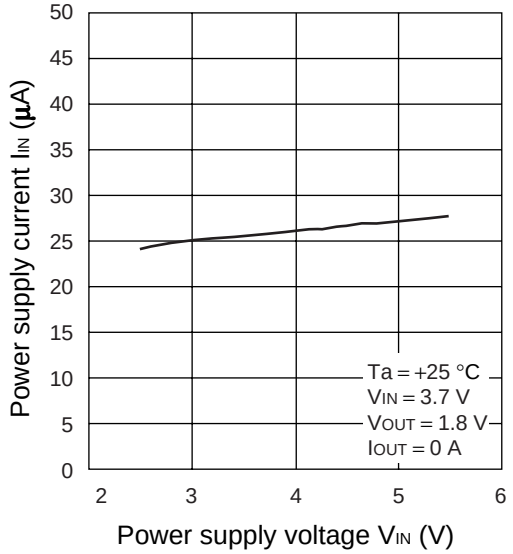
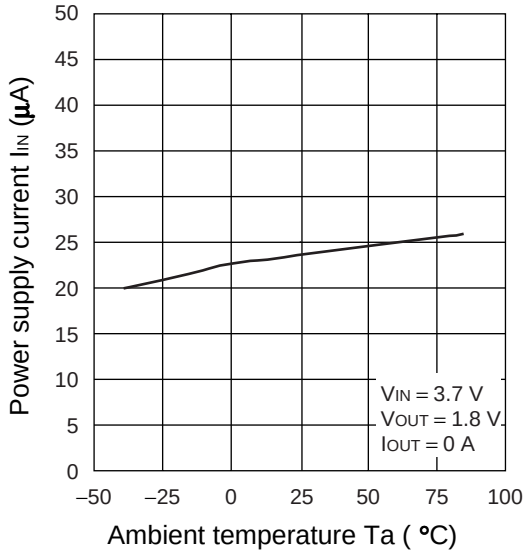
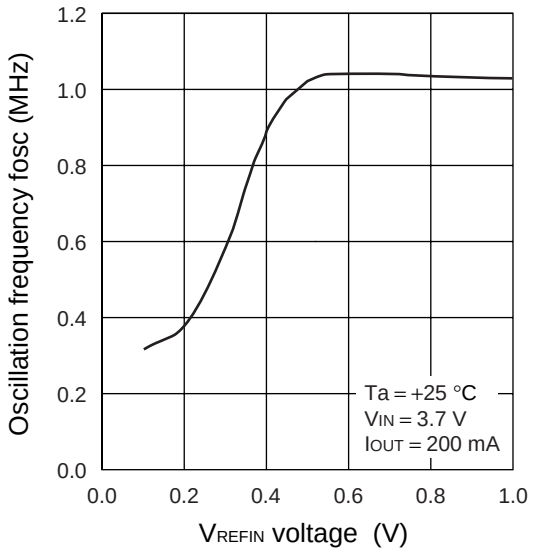
Power supply current vs.
Power supply voltage



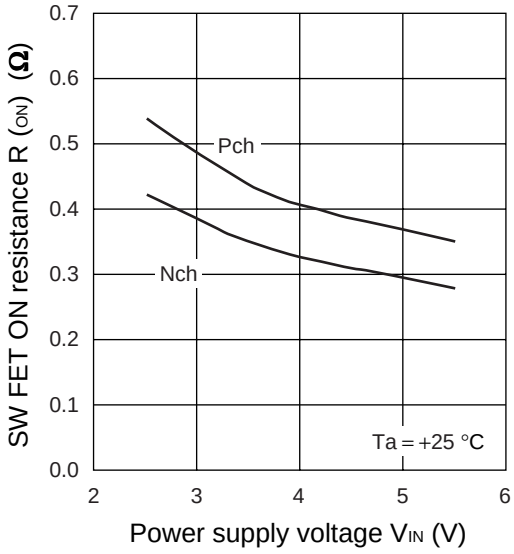
Power supply current vs.
Ambient temperature



Oscillation frequency – V_{REFIN} voltage



SW FET ON resistance vs.
Power supply voltage



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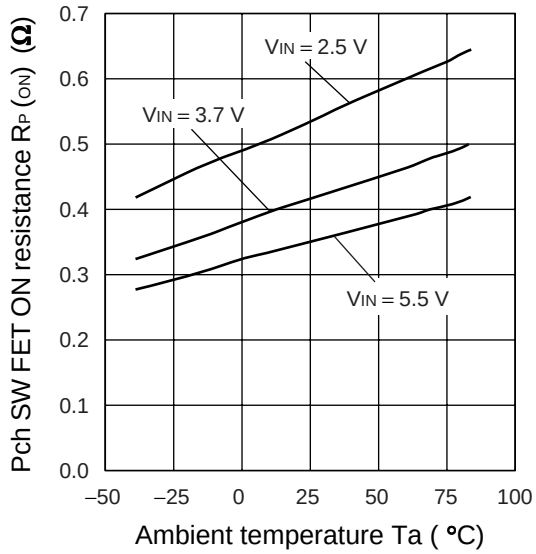
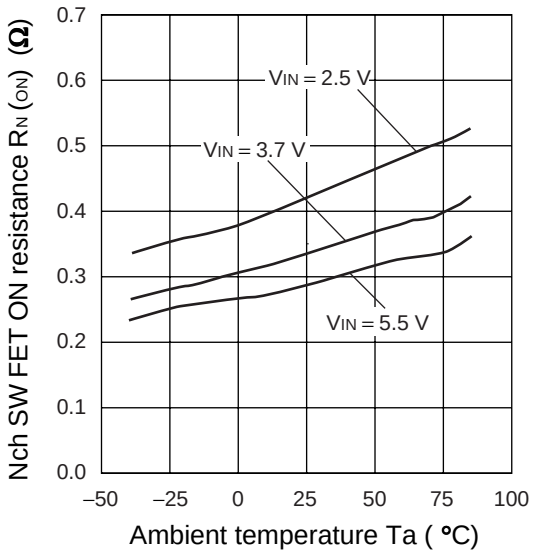
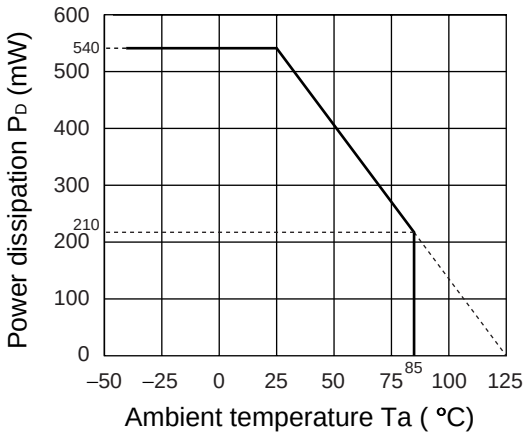
Pch SW FET ON resistance vs.
Ambient temperature



Nch SW FET ON resistance vs.
Ambient temperature



Power dissipation vs.
Ambient temperature



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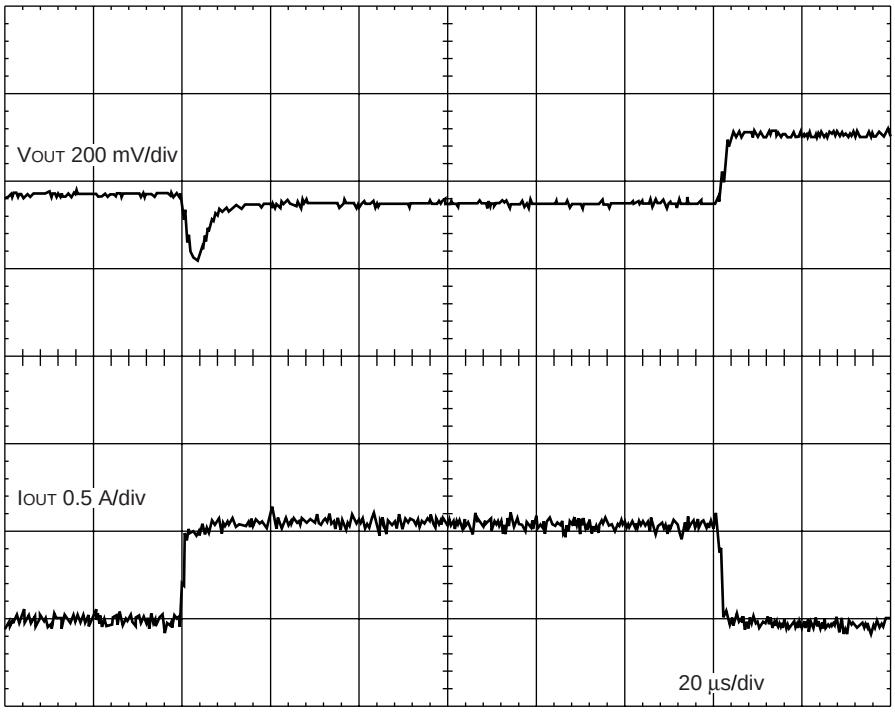
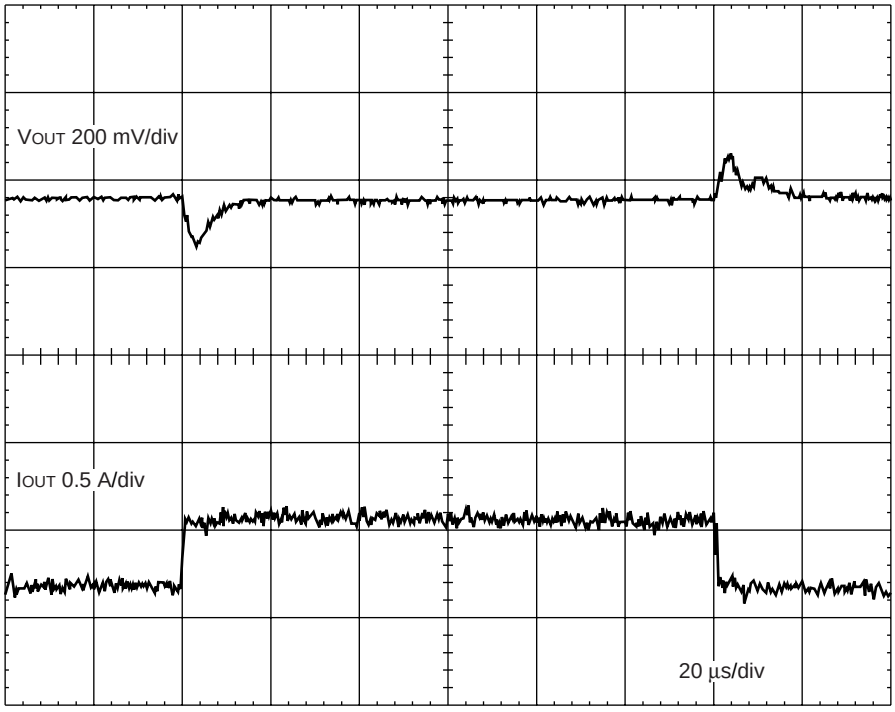
Output waveforms at load sudden changes



V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 0 mA to 600 mA

Output waveforms at load sudden changes



V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 200 mA to 600 mA

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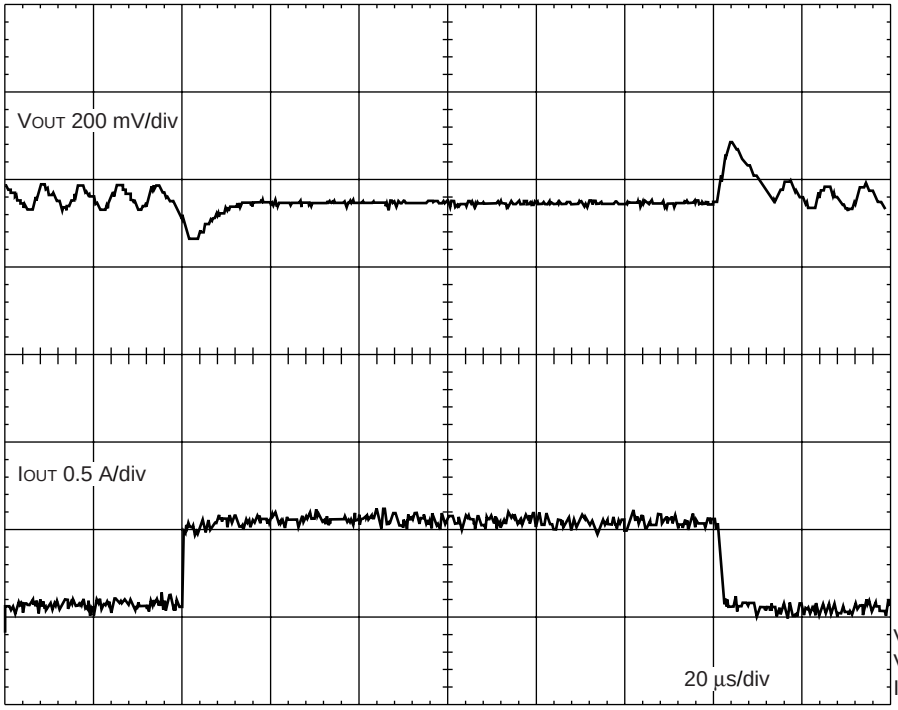
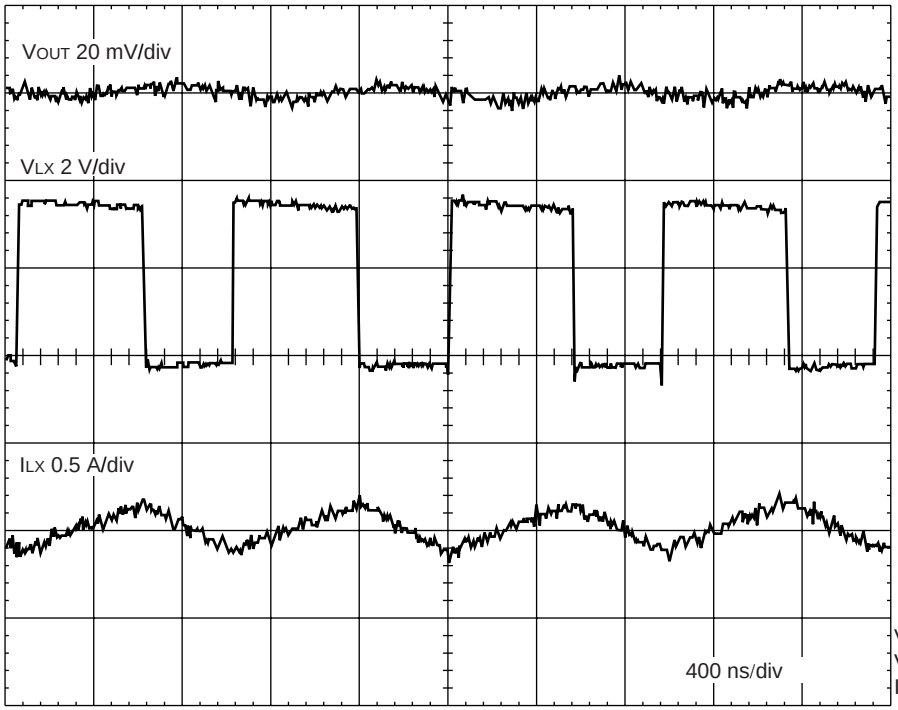
Output waveforms at load sudden changes



V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 100 mA to 600 mA

Switching waveforms (continuous operation)



V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 600 mA

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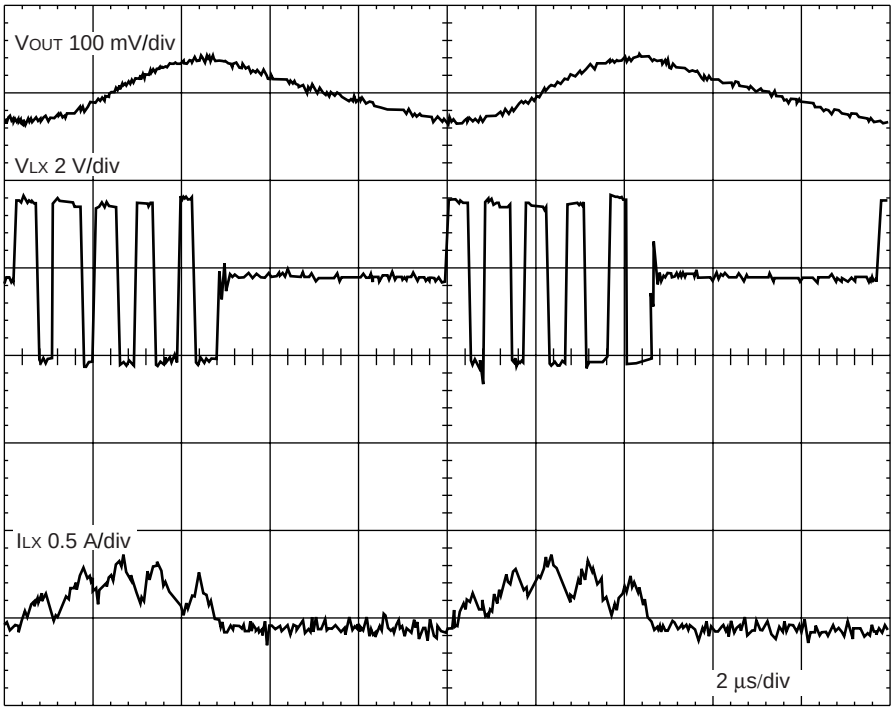
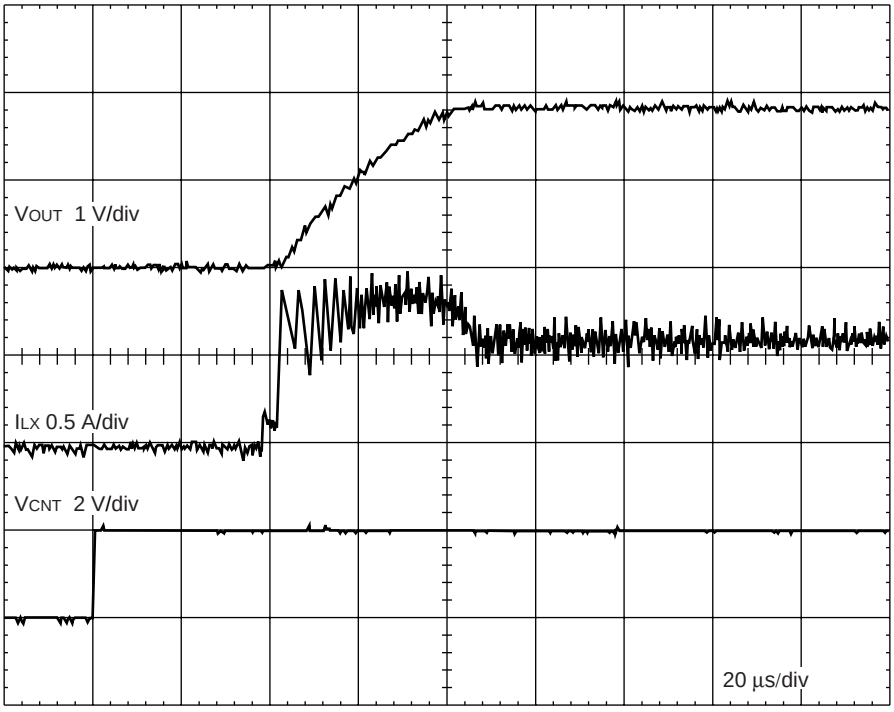
Switching waveforms (during burst operation)



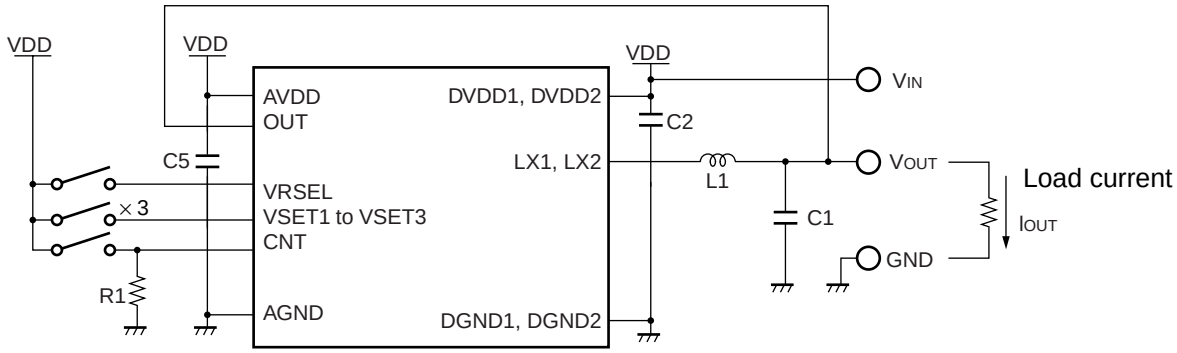
V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 100 mA

CNT terminal response characteristics



V_{IN} = 3.7 V
V_{OUT} = 1.8 V
I_{OUT} = 600 mA

■ TYPICAL OPERATING CHARACTERISTICS MEASUREMENT CIRCUIT



COMPONENT	ITEM	Specification	Vendor	Parts No.
R1	Resistor	1 MΩ	ssm	PFR05Q-105-D-1
C2	Ceramic condenser	4.7 μF	TDK	C2012JB1A475K
C5	Ceramic condenser	0.01 μF	TDK	C1608JB1H103K
C1	Ceramic condenser	10 μF	TDK	C2012JB0J106M
L1	Inductor	3.3 μH	TDK	VLF4012AT-3R3M

ssm : SUSUMU CO., LTD.
TDK : TDK Corporation

Note : The above components are recommended parts confirmed by Fujitsu to operate normally.

■ APPLICATION NOTES

(1) Selection of components

• Selection of external inductor

The design of the inductor is basically unnecessary. This IC is designed to operate efficiently with a 3.3 μH inductor.

Select the inductor whose rated saturation current is larger than the LX peak current in the operating conditions, and select the inductor whose DC resistance is as low as possible (150 mΩ or less is recommended) .

The LX peak current value (I_{PK}) is obtained from the following formula :

$$I_{PK} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{L} \bullet \frac{D}{fsw} \bullet \frac{1}{2} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{2 \bullet L \bullet fsw \bullet V_{IN}}$$

L : External inductor value

I_{OUT} : Load current

V_{IN} : Power supply voltage

V_{OUT} : Output setting voltage

D : Switching on-duty cycle (= V_{OUT} / V_{IN})

fosc : Switching frequency (fixed at 1 MHz)

Example : Peak current maximum value (I_{PK}) : At V_{IN} = 3.7 V, V_{OUT} = 1.8 V, I_{OUT} = 0.6 A, L = 3.3 μH.

$$I_{PK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{2 \bullet L \bullet fsw \bullet V_{IN}} = 0.6\ A + \frac{(3.7\ V - 1.8\ V) \bullet 1.8\ V}{2 \bullet 3.3\ \mu H \bullet 1\ MHz \bullet 3.7\ V} \fallingdotseq 0.74\ A$$

• Selection of I/O condenser

- Select the DVDD input condenser whose equivalent series resistance (ESR) is low in particular, to suppress the loss by ripple currents.

- Better line regulation and load regulation characteristics can be obtained by adding an input condenser immediately close to AVDD. Although the appropriate capacitance may be different depending on the layout design, the reference range for selection is from , 1000 pF to 0.01 μF.

- The output condenser should also have low equivalent series resistance (ESR). The ripple current of the fluctuation portion of the inductor current, it flows into the output condenser. The ripple voltage is the product of this fluctuation portion and ESR, it is generated at the output. The output capacitance significantly affects the stability of operation as a DC/DC converter. In principle, an output condenser of about 10 μF is recommended. If there is a problem with the ripple voltage, you can work around the problem by selecting one with large capacitance.

- Condenser types
  Selecting ceramic condenser for both of input and output is effective for reduction in ESR and size. Since power supply circuits are heat generators, you should avoid using ceramic condenser which have an F temperature characteristic (-80% to +20%). You should use those with a B characteristic (±10% to ±20%) or the like. Avoid using normal electrolytic condenser as their ESR is high.
  Tantalum condenser are effective for reduction in ESR but are very dangerous as they have a disadvantage, they establish a short mode if a failure occurs. When using a Tantalum condenser, choose one with a fuse.

(2) Setting output voltages

When output voltages are set in advance, only treat the control terminals as shown in the table below. Any additional component such as a voltage dividing resistor is not required.

As VSET1 to VSET3, VSEL, and VRSEL terminals have built-in pull-down equal circuits, their level is equal to “L” when opened.

Note : For a circuit configuration example, refer (1) “Setting 1.8-V output using the internal reference voltage” in ■ APPLICATION EXAMPLES.

• Output voltage setting table 1

VSET1	VSET2	VSET3	VSEL	VRSEL	V_{OUT}
L	L	L	X	L	1.1 V
H	L	L	L		0.8 V
H	L	L	H		1.2 V
L	H	L	X		1.3 V
H	H	L	L		1.1 V
H	H	L	H		1.5 V
L	L	H	L		1.1 V
L	L	H	H		1.8 V
H	L	H	X		2.5 V
L	H	H	X		2.8 V
H	H	H	X		3.3 V

X : Don’t care

To set arbitrary voltages other than above, set VRSEL to “H” and apply voltage to VREFIN. The voltage applied to VREFIN is supplied either from external or by dividing VREF using a resistor. The output voltage using VREFIN with VREF resistor-divided is obtained from the following formula :

$$V_{OUT} = \text{(Output voltage setting value)} \bullet Kv \qquad Kv = \frac{R8}{R7 + R8} \bullet \frac{1.25}{0.6}$$

$$\text{(VREFIN voltage : } \frac{R8}{R7 + R8} \times 1.25 \text{ Refer (4) “VREFIN terminal in ■ NOTES ON CIRCUIT DESIGN”.}$$

Note : For a circuit configuration example, refer (2) “Supplying the VREF terminal voltage to the reference voltage external input (VREFIN) after resistor voltage division and setting the V_{OUT} voltage to 1.25 V with V_{OUT} setting gain doubled” in ■ APPLICATION EXAMPLES.

The output voltage is determined by the resistor ratio. Select the resistance value so that the current flowing through the resistor does not exceed the rated VREF current (1 mA) .

• **Output voltage setting table 2**

VSET1	VSET2	VSET3	VSEL	VRSEL	V_{OUT} (Output voltage setting value × Kv)
L	L	L	X	H	1.1 V × Kv
H	L	L	L		0.8 V × Kv
H	L	L	H		1.2 V × Kv
L	H	L	X		1.3 V × Kv
H	H	L	L		1.1 V × Kv
H	H	L	H		1.5 V × Kv
L	L	H	L		1.1 V × Kv
L	L	H	H		1.8 V × Kv
H	L	H	X		2.5 V × Kv
L	H	H	X		2.8 V × Kv
H	H	H	X		3.3 V × Kv

X : Don't care

(3) About conversion efficiency

The conversion efficiency can be improved by reducing the loss of the DC/DC converter circuit.

The total loss (P_{LOSS}) of the DC/DC converter is roughly divided as follows :

$$P_{LOSS} = P_{CONT} + P_{SW} + P_C$$

P_{CONT} : Control system circuit loss (The power used for this IC to operate, including the the gate driving power for internal SW FETs)

P_{SW} : Switching loss (The loss caused during switching of the IC's internal SW FETs)

P_C : Continuity loss (The loss caused when currents flow through the IC's internal SW FETs and external circuits)

The IC's control circuit loss (P_{CONT}) is extremely small, which is about 1 mW (I_{IN} = 300 μA) * , at V_{IN} = 3.7 V. As the IC contains FETs which can switch faster with smaller power, the continuity loss (P_C) is more predominant as the loss during heavy-load operation than the control circuit loss (P_{CONT}) and switching loss (P_{SW}) .

Further the continuity loss (P_C) is divided roughly, into the loss by internal SW FET ON-resistance and by external inductor series resistance.

$$P_C = I_{OUT}^2 \bullet (RDC + D \bullet RONp + (1 - D) \bullet RONn)$$

D : Switching on-duty cycle (= V_{OUT} / V_{IN})

RONp : Internal Pch SW FET ON resistance

RONn : Internal Nch SW FET ON resistance

RDC : External inductor series resistance

I_{OUT} = Load current

The above formula indicates that it is important to reduce RDC as much as possible to improve efficiency by selecting components.

* : The loss is caused during continuous operation. When the load is light, the IC performs burst operation, thereby further suppressing the loss (I_{IN} = about 30 μA with no load). The mode is changed depending on the peak current value Ipk flowing into SW FETs, at a threshold value of about 150 mA.

(4) Power dissipation and temperature examination

The IC is so efficient that no examination is required in most cases. But if the IC is used at a low power supply voltage, heavy load, high output voltage, or high temperature, it requires further examination for higher efficiency.

The internal loss (P) is roughly obtained from the following formula :

$$P = I_{OUT}^2 \bullet (D \bullet RONp + (1 - D) \bullet RONn)$$

D : Switching on-duty cycle (= V_{OUT} / V_{IN})

RONp : Internal Pch SW FET ON resistance

RONn : Internal Nch SW FET ON resistance

I_{OUT} = Load current

The loss expressed by the above formula is mainly continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

In this IC with RONp greater than RONn, the larger the on-duty cycle, the greater the loss.

When assuming V_{IN} = 3.7 V, Ta = 70 °C, V_{OUT} = 1.8 V, and I_{OUT} = 0.6 A, for example, RONp = 0.48 Ω and RONn = 0.39 Ω according to the graph “SW FET ON resistance vs. Ambient temperature”. The IC's internal loss P is 156 mW. According to the graph “Power dissipation vs. ambient temperature”, the power dissipation at an ambient temperature Ta of 70 °C is 300 mW and the internal loss is smaller than the power dissipation.

(5) Transient response

The IC contains an optimized version of ErrAmp, providing favorable transient response characteristics.

The response characteristics such as response time, overshoot, and undershoot, are checked usually by changing suddenly I_{OUT}, with V_{IN} and V_{OUT} left constant.

(6) Example of designing board layout

For stable operation, the IC requires the optimized design of board layout.

Pay attention to the following points during layout design.

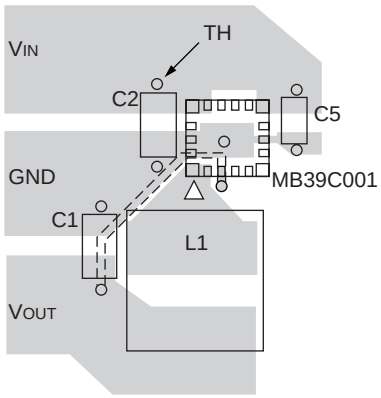
- Connect the GND terminals (AGND, DGND1, DGND2) and power terminals (AVDD, DVDD1, DVDD2) immediately near the IC.
- Place the DVDD input condenser (C2) near DVDD and DGND. If the power supply or ground plains exists on any other board layer, place TH (through hole) close to the condenser terminal.
- Place the AVDD input condenser (C5) near AVDD and AGND. If the power supply or ground plains exists on any other board layer, place TH (through hole) close to the condenser terminal.

- Place the GND side terminal of the output condenser (C1) as near DGND of the IC and the GND side terminal of the input condenser (C2). If the ground plains exists on any other board layer, place TH close to the GND side terminal of the condenser. For wiring to OUT, start close to the V_{OUT} side terminal of the output condenser (CI). Note that the OUT terminal is highly sensitive and should be wired as apart from the wiring of the LX terminal of the IC.

- Large currents flow among the input condenser (C2, C5), output condenser (C1), external inductor (L1), and this IC. Place these components near the IC, to minimize the loop area made up of these components. Also, mount these components on the same layer and wire them without using any TH. Wire these nets using as bold, short, and straight patterns (plains layout is advisable).

- For the IC mounted layer, provide a ground plane.

Recommended layout drawing (with only important wiring)



■ NOTES ON CIRCUIT DESIGN

(1) GND Potential

Connect AGND and DGND to GND of the power supply circuit, so that they have equal potential.

(2) Control input terminals

- The voltages applied to the CNT, VSET1 to VSET3, VSEL, and VRSEL terminals must not exceed the absolute maximum rating (VDD + 0.3 V). Applying a voltage exceeding the absolute maximum rating may cause permanent damage to the LSI. If it is inevitable, insert a resistor of about 20 kΩ between a terminal of the controller (such as a CPU) and the control terminal of the IC. This prevents a latch-up to some extent.

Note : Finally, judge right or wrong of the adoption after confirming it is unquestionable under your system requirements as permanent measure.

- The CNT terminal has no internal pull-down resistor function (while the VSET1 to VSET3, VSEL, and VRSEL have one). If the terminal of the controller (such as the CPU) connected to the CNT terminal can enter a high impedance state an unpredictable malfunction may occur. To prevent this, a pull-down resistor (of about 1 MΩ) should be connected to the CNT terminal.

- If the fall time of the CNT terminal is long, the output (V_{OUT}) may cause an overshoot when the load is light. Be careful not to let the rise time and fall time exceed 500 μs.

(3) Power supply input

- If the rise time or fall time of the supply voltage (V_{IN}) is long, a malfunction may occurs. Be careful not to let the rise time and fall time exceed 100 ms.

- If the power supply voltage fluctuates around the UVLO detection voltage (between 2.15 and 2.3 V) when the power supply is turned on or shut off. The output is stopped by under-voltage and restarted by restored voltage repeatedly and there is a possibility that chattering is generated in V_{OUT}. Although the UVLO detection voltage has a hysteresis of 0.15 V, fluctuation over 0.15 V cannot be suppressed. Be careful to prevent the supply voltage from going up and down near UVLO.

- If the CNT terminal becomes "L" from "H" when the supply voltage (V_{IN}) becomes lower than the output voltage (V_{OUT}), the IC may cause a latch-up by the action of an external inductor. Although this is an operating condition unintended for normal use, it can occur frequently when the power supply voltage is shut off with light loads. Even if a latch-up occurs by normal shutdown, the latch-up is cleared when the power supply voltage goes below 0.8 V. Therefore, there are few things which become problem, when the power supply is turned back on again. If the power supply is turned back on with the power supply voltage exceeding 0.8 V, the IC may be broken by an excessive current due to a latch-up. This problem can be worked around by either of the following two methods :

  - When the CNT terminal becomes "L" from "H" as the power supply voltage goes down, be sure to lower the power supply voltage to 0.8 V or less before turning the power supply back on again.
  - Add a Schottky barrier diode as shown in the latch-up preventive circuit example.
    Note, however, that this work around adversely affects the regulation or conversion efficiency when the application uses an extremely small load current. When selecting the Schottky barrier diode, pay attention to the following points :

    Reverse current [I_R]

    Select a diode whose reverse current is smaller than the load current. (If a diode whose reverse current is greater than the load current is adopted, the output voltage (V_{OUT}) is raised by the reverse current, and the regulation deteriorates.

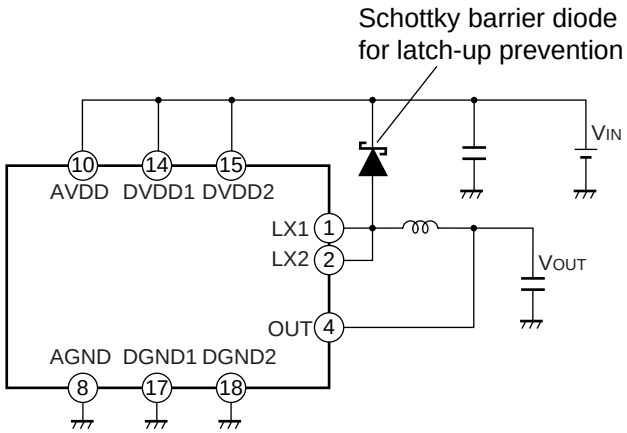
Forward voltage [V_F]

The forward voltage must be smaller than the voltage triggering latch-up. Select a diode whose forward voltage is about 0.5 V or less.

Non repetitive peak surge current [I_{FSM}]

Select a diode whose non repetitive peak surge current is greater than the peak reverse current. The peak current is different depending on the operating conditions; the reference value is 1 A to 3 A.

Latch-up preventive circuit example



(4) VREFIN terminal

When the VREFIN terminal is used, the switching frequency is lowered if the VREFIN voltage is 0.5 V or less. When the load current (I_{OUT}) is 100 mA or less, the VREFIN voltage should fall within the range of 0.5 to 0.7 V. The VREFIN voltage can be between 0.3 and 0.7 V if the switching frequency lowered is acceptable when the load current (I_{OUT}) is 100 mA or less.

(5) POWER GOOD terminal

The POWER GOOD terminal always monitors the OUT terminal voltage, with no exception, even when the output voltage is changed by switching the terminals such as VSET1 to VSET3 and VSEL. When the output voltage rises slowly with heavy loads, the POWER GOOD terminal become "H" until the output voltage becomes 90% of the setting voltage.

Be careful when using the POWER GOOD terminal to reset a load circuit which uses a CPU. Be careful that the POWER GOOD terminal temporarily becomes “H” level when dynamically changing the voltage, thereby resetting the circuit accidentally at an unintended timing.

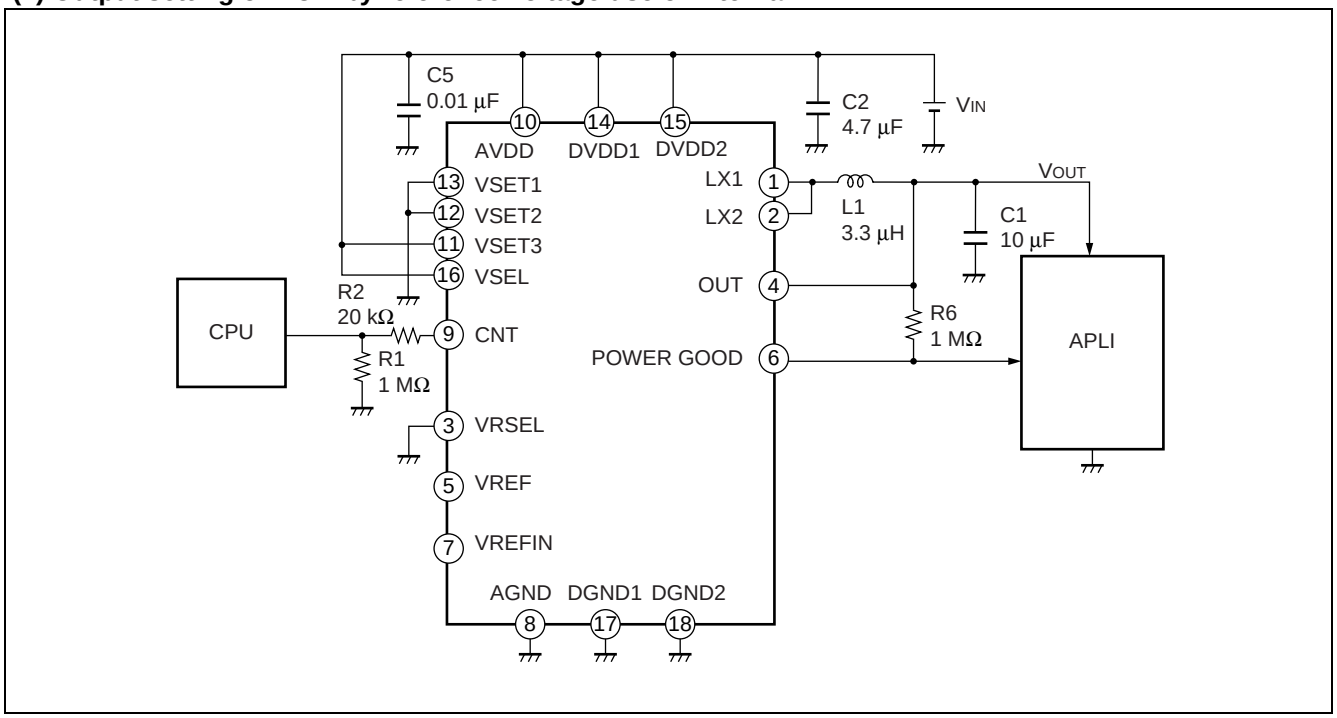
(6) Output overcurrent protection

This IC uses current mode control which provides a certain level of overcurrent protection. If LX is connected to VDD or GND, or V_{OUT} is connected to GND with an extremely low resistor of 0.1 Ω or less, the IC may not be protected from overcurrents and it is break down.

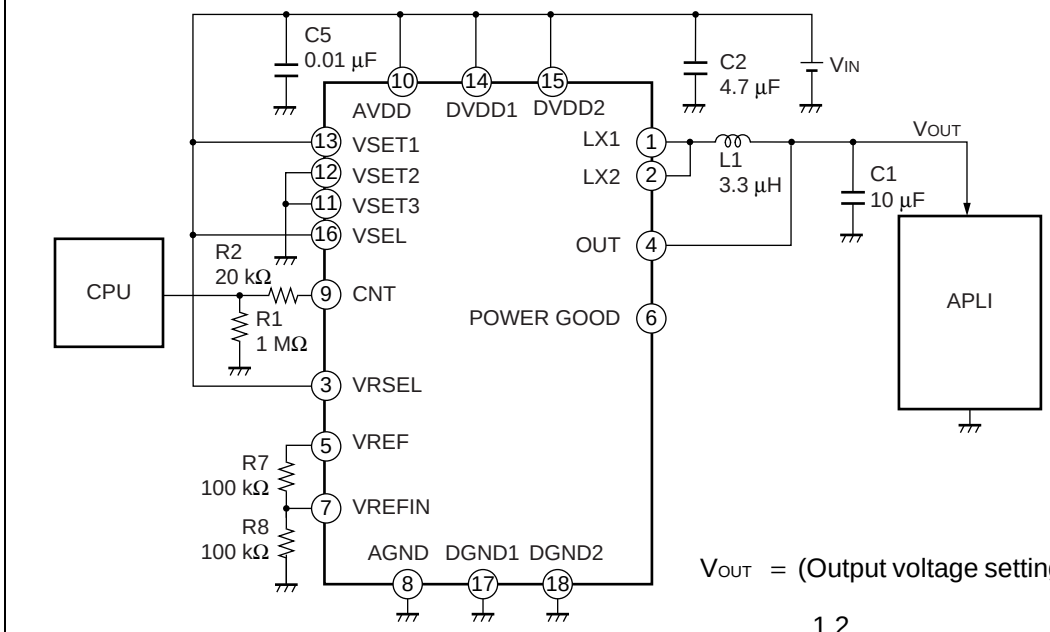
The IC is apt to break down, when the inductance element of the short-circuit route is large or when the output voltage is high. To prevent the IC from breaking due to a short-circuit, it is advisable to insert a resistor of about 1 kΩ between the OUT terminal and V_{OUT}.

■ APPLICATION EXAMPLES

(1) Output setting of 1.8 V by reference voltage use of internal



(2) Supplying the VREF terminal voltage to the reference voltage external input (VREFIN) after resistor voltage division, the V_{OUT} voltage is set to 1.25 V by the OUT setting gain twice

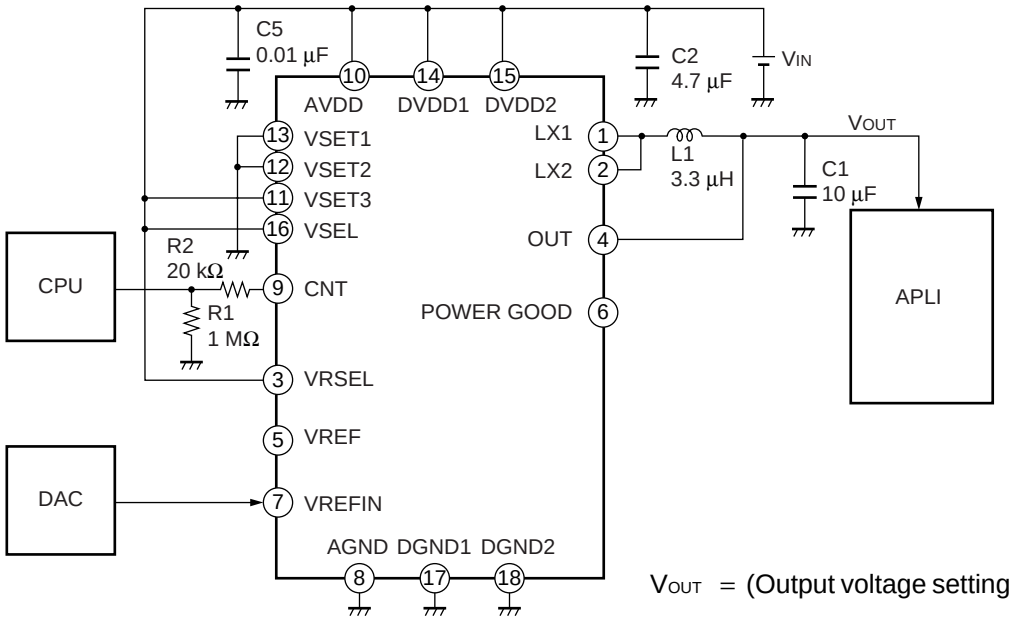


$$V_{OUT} = (\text{Output voltage setting value}) \times \frac{VREFIN}{0.6}$$

$$= \frac{1.2}{0.6} \bullet VREFIN = 2 \times \frac{R8}{R7 + R8} VREF$$

$$= 2 \times \frac{100\ k}{100\ k + 100\ k} \times 1.25 = 1.25\ V$$

(3) Supplying an external voltage to the reference voltage external input (VREFIN), the V_{OUT} voltage is set by the V_{OUT} setting gain triple



$$V_{OUT} = (\text{Output voltage setting value}) \times \frac{VREFIN}{0.6}$$

$$= \frac{1.8}{0.6} \bullet VREFIN = 3 \times VREFIN$$

The components for the above example are listed below.

Component	Part name	Specification		Manufacturer	Model name
L1	Inductor	3.3 µH	20% R_{DC} = 120 mΩ	TDK	VLF4012AT-3R3M
C1	Ceramic condenser	10 µF	20% 6.3 V	TDK	C2012JB0J106M
C2	Ceramic condenser	4.7 µF	10% 10 V	TDK	C2012JB1A475K
C5	Ceramic condenser	0.0 1 µF	10% 50 V	TDK	C1608JB1H103K
R1	Resistor	1 MΩ	0.5%	ssm	PFR05Q-105-D-1
R2	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R6	Resistor	1 MΩ	0.5%	ssm	PFR05Q-105-D-1
R7	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R8	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D

TDK : TDK Corporation
ssm : SUSUMU CO., LTD.

■ NOTES ON USE

1. Do not exceed maximum ratings.

Using the LSI beyond maximum ratings may generate a parasitic transistor, resulting in permanent damage to the LSI due to a latch-up. The LSI should be used under the recommended operating conditions and exceeding any of the recommended conditions may adversely affect LSI reliability.

2. Use under recommended operating conditions.

The recommended operating conditions are reommended values that guarantee the normal operation of the LSI. The values of electrical characteristics are guaranteed when the LSI is used under the recommended operating conditions with each parameter falling in the specified range.

3. Take measures against static electricity.

- Containers for semiconductors must be antistatic or conductive.
- When storing or carrying a printed circuit board with components mounted, put it in a conductive bag or container.
- The work table, tools, and measuring instruments must be properly grounded.
- The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

4. Do not apply a negative voltage.

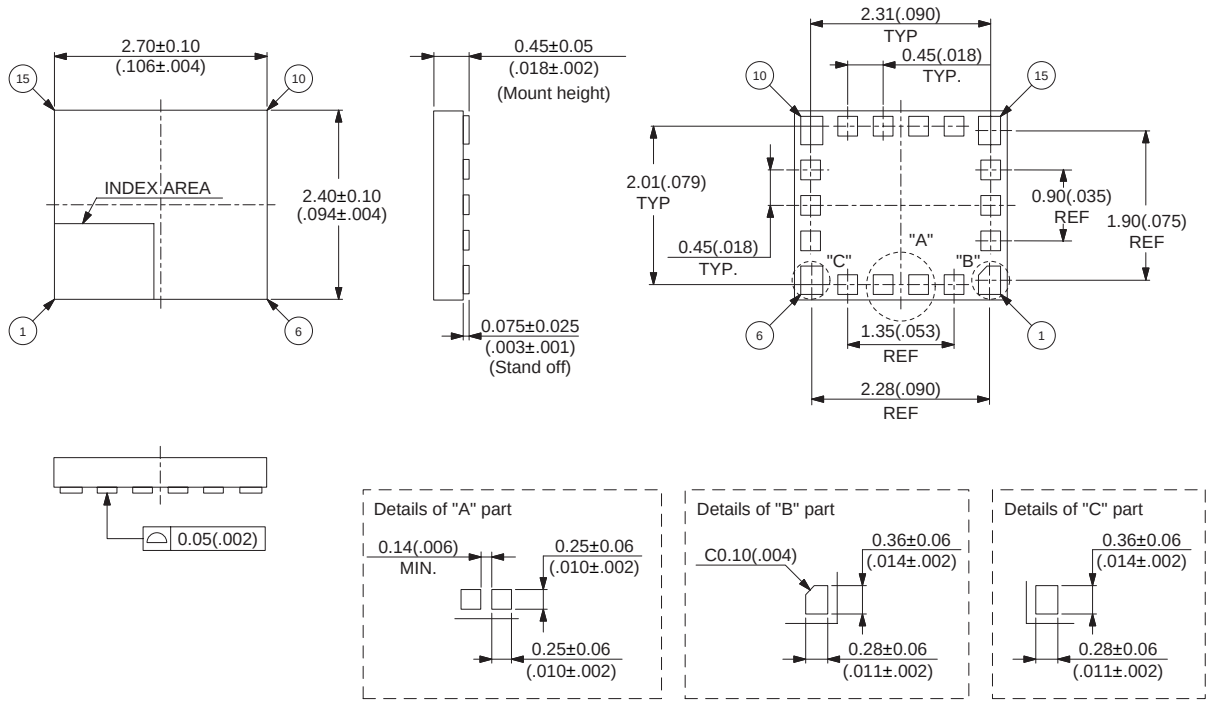
Applying a negative voltage of − 0.3 V or less to an LSI may generate a parasitic transistor, resulting malfunction.

■ ORDERING INFORMATION

Model	Package	Remarks
MB39C001PVB	18-pin plastic BCC (LCC-18P-M05)	

■ PACKAGE DIMENSIONS

18-pin plastic BCC
(LCC-18P-M05)



Unit : mm (inches)
Note : Parenthesized values are reference values.

■ EVALUATION BOARD SPECIFICATIONS

The MB39C001 evaluation board is a surface-mounting board of a single-channel down-conversion circuit. The output voltage can be set by switch of each SW (*1), and supplies the current of up to 600 mA at a power supply voltage from 2.5 V to 5.5 V (*2).

*1 : For setting the output voltage, refer (2) "Setting output voltages" in ■ APPLICATION NOTES.

*2 : The current can be supplied when "V_{IN} - V_{OUT} ≥ 0.7 V". It can be supplied even "V_{IN} - V_{OUT} < 0.7 V" when under operating conditions in which the output current is suppressed.

• Terminal Description

Symbol	Function
VIN	Power supply terminal. VIN = 2.5 V to 5.5 V (3.7 V Typ)
OUT	DC/DC converter output terminal.
VCTL	Power supply terminal for mode setting SW. Connect with VIN and use it.
CNT	Power control terminal. VCNT = 0 V to 0.3 V : Shutdown VCNT = 1.5 V to VIN : Normal operation
POWER_GOOD	Fixed at "L" (= 0 V) , when the OUT voltage reaches the output setting voltage.
VREF	Reference voltage output terminal.
VREFIN	External reference voltage input terminal. When an external reference voltage is used, this terminal supplies it.
GND	DC/DC converter ground terminal.
AGND	MB39C001 ground terminal.

• Switch Description

SW	Name	FUNCTION	Remarks
1	VSEL	Output voltage setting	For details on each setting, refer (2) "Setting output voltages" in ■ APPLICATION NOTES.
2	VSET1	Output voltage setting	
3	VSET2	Output voltage setting	
4	VSET3	Output voltage setting	
5	VRSEL	Reference voltage setting	

• Setup and checkup

(1) Setup

Connect the power supply terminal of the power supply to VIN, VCTL, and CNT and its ground terminal to GND. Connect the OUT side to the required loading device or measuring instrument.

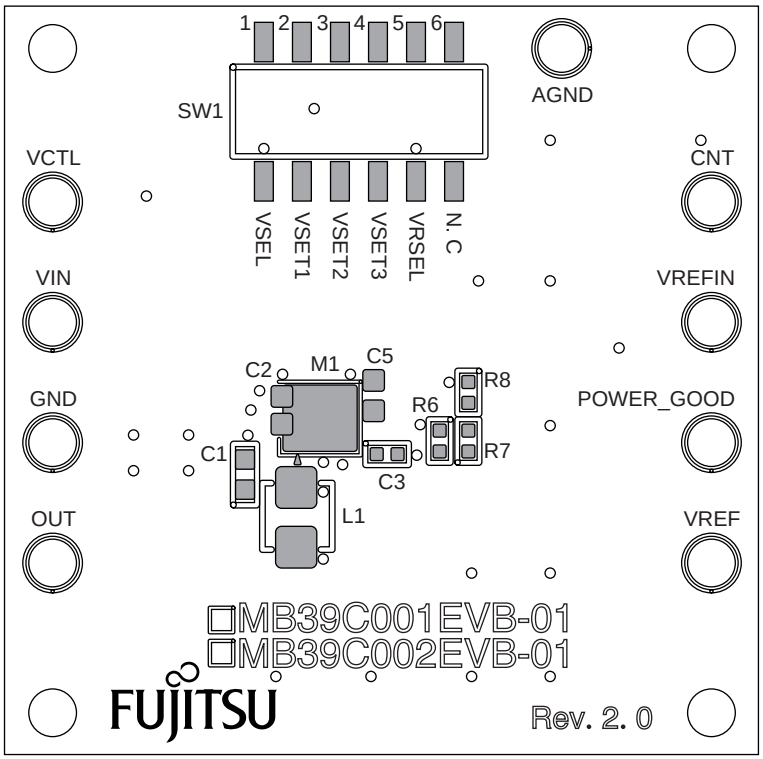
Set SW1 (VSEL) and SW4 (VSET3) to ON; SW2 (VSET1), SW3 (VSET2), and SW5 (VRSEL) to OFF. (Set the output to 1.8 V using the internal reference voltage.)

(2) Checkup

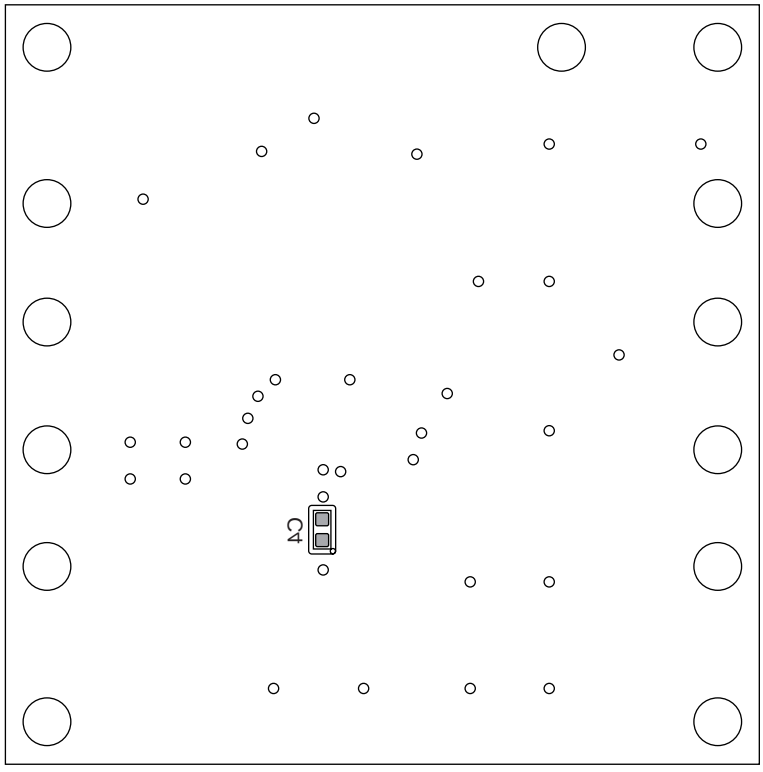
Supply power to VIN. The IC is working normally when the OUT voltage is 1.8 V (Typ) .

• On-board Component Layout

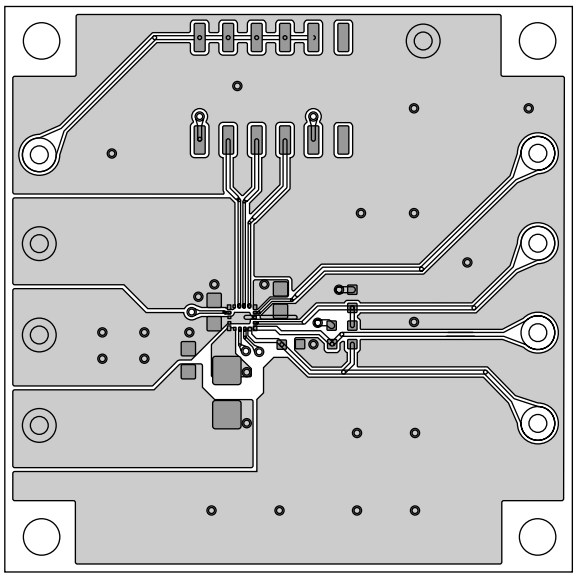
Top side (Top View)



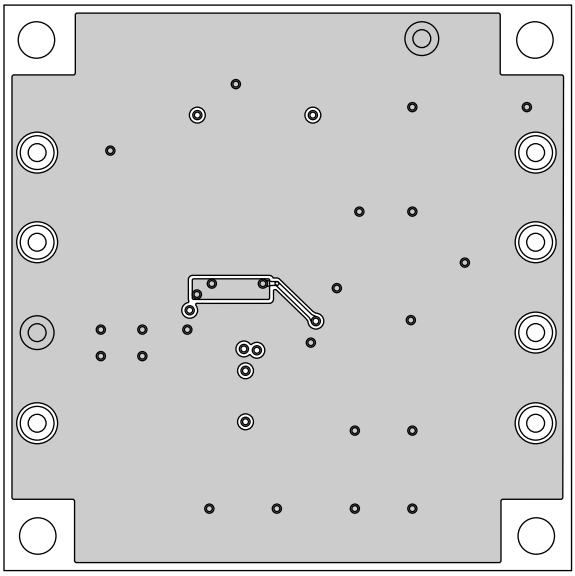
Bottom side (Top View)



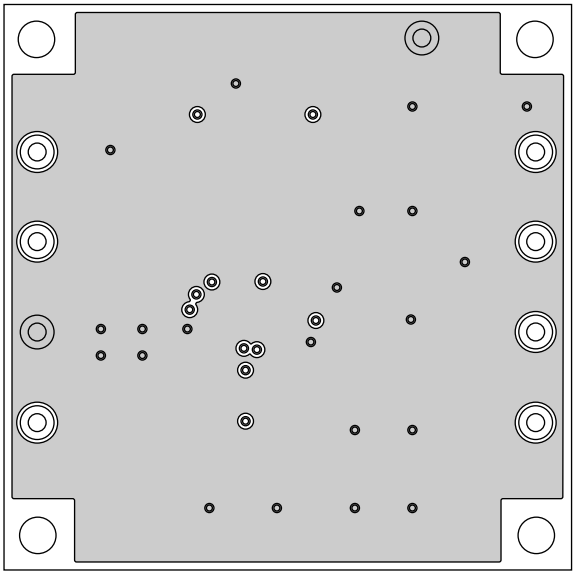
Board Layout



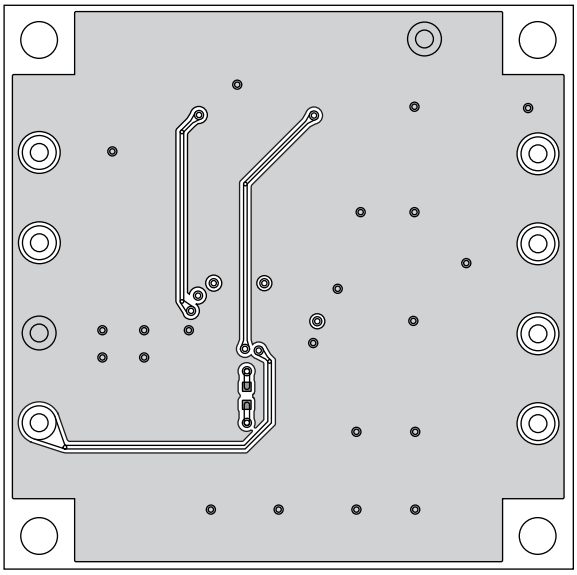
Top Side (Layer1)



In Side VIN & GND (Layer2)

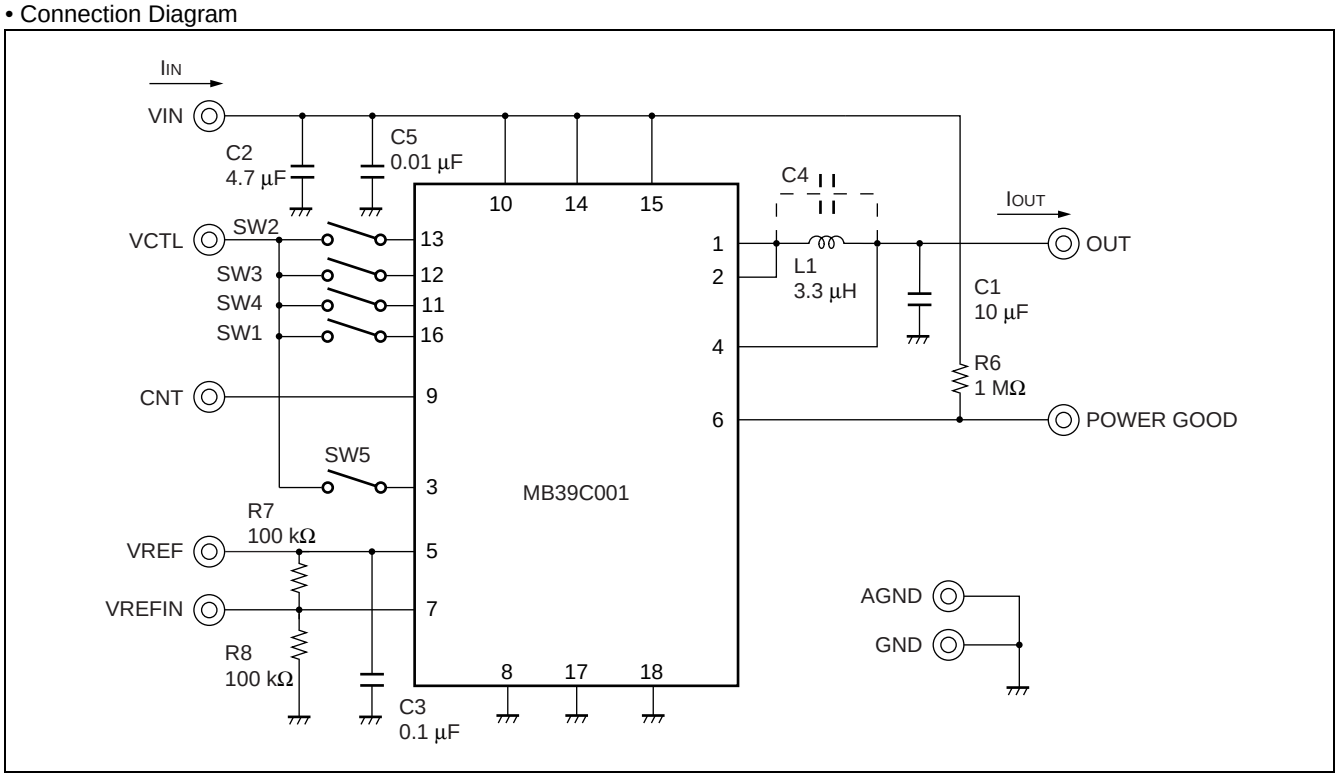


Inside GND (Layer3)



Bottom Side (Layer4)

• Connection Diagram



• Parts List

Symbol	Part name	Model name	Specification	Package	Manufacturer	Remarks
L1	Inductor	VLF4012AT-3R3M	3.3 µH, RDC = 120 mΩ	SMD	TDK	
C1	Ceramic capacitor	C2012JB0J106M	10 µF (6.3 V)	2012	TDK	
C2	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK	
C3	Ceramic capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	
C4	—	—	—	—	—	Not mounted
C5	Ceramic capacitor	C1608JB1H103K	0.01 µF (50 V)	1608	TDK	
R6	Resistor	PFR05Q-105-D-1	1 MΩ ± 0.5%	1005	ssm	
R7	Resistor	RR0816P-104-D	100 kΩ ± 0.5%	1608	ssm	
R8	Resistor	RR0816P-104-D	100 kΩ ± 0.5%	1608	ssm	
SW	Switch	DMS-6H	6 poles	—	MATSUKYU	
—	Terminal pins	WT-2-1	WT-2-1	—	MacEight	

TDK : TDK Corporation
ssm : SUSUMU CO., LTD.
MATSUKYU : Matsukyu Co., Ltd.
MacEight : MacEight Co., Ltd.

• Ordering Information

EV board part No.	EV board version No.	Remarks
MB39C001EVB-01	MB39C001EV Board Rev.2.0	

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