19-5139; Rev 1; 3/11

EVALUATION KIT AVAILABLE

Low-Power, High-Performance Dual I²S Stereo Audio Codec

General Description

The MAX9880A is a high-performance, stereo audio codec designed for portable consumer applications such as smartphones and tablets. Operating from a single 1.8V supply to ensure low-power consumption, the MAX9880A offers a variety of input and output configurations for design flexibility. The MAX9880A can be combined with an audio subsystem, such as the MAX9877 or MAX9879, for a complete audio solution for portable applications.

The MAX9880A's stereo differential microphone inputs can support either analog or digital microphones. A stereo single-ended line input, with a configurable preamplifier, can either be recorded by the ADC or routed directly to the headphone or line output amplifiers. The stereo headphone amplifiers can be configured as differential, single ended, or capacitorless. The stereo line outputs have dedicated level adjustment.

There are two digital audio interfaces. The primary interface is intended for voiceband applications, while the secondary interface can be used for high performance stereo audio data. Two digital input streams can be processed simultaneously and both digital interfaces support TDM and I²S data formats.

The flexible clocking circuitry utilizes any available 10MHz to 60MHz system clock, eliminating the need for an external PLL and multiple crystal oscillators. Both the ADC and DAC can be operated synchronously or asynchronously in master or slave mode. The ADC can be operated from 8kHz to 48kHz sample rates, while the DAC can be operated up to 96kHz.

The MAX9880A prevents click and pop during volume changes and during power-up and power-down. Audio quality is further enhanced with user-configurable digital filters for voice and audio data. Voiceband filters provide extra attenuation at the GSM packet frequency and greater than 70dB stopband attenuation at $f_S/2$. An I²C or SPI™ serial interface provides control for volume levels, signal mixing, and general operating modes.

The MAX9880A is available in space-saving, 48-bump, 2.7mm x 3.5mm, 0.4mm-pitch WLP and 48-pin, 6mm x 6mm TQFN packages.

Applications

Cellular Phones

Tablet PCs

Portable Gaming Devices

Portable Multimedia Players

SPI is a trademark of Motorola, Inc.

Features

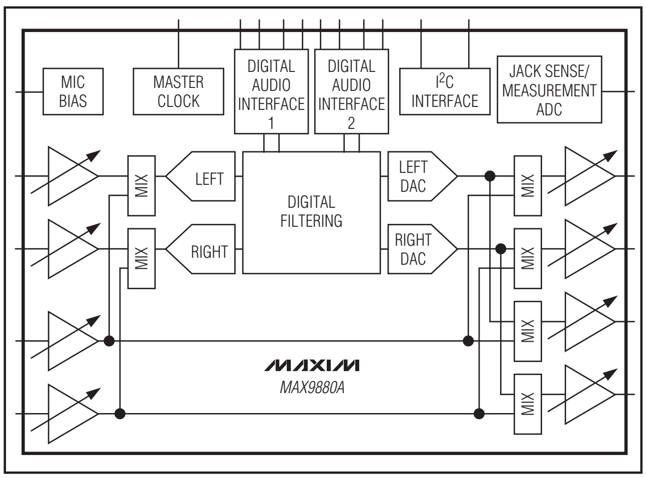
- ♦ 1.8V Single-Supply Operation
- ♦ 10.6mW Playback Power Consumption
- ♦ 8kHz to 96kHz Stereo DAC with 96dB Dynamic Range
- ♦ 8kHz to 48kHz Stereo ADC with 82dB Dynamic Range
- ♦ Support for Any Master Clock Between 10MHz to 60MHz
- ♦ Stereo Microphone Inputs Support Digital Microphones
- ♦ Stereo Headphone Amplifiers: Differential (30mW), Single-Ended, or Capacitorless (10mW)
- ♦ Stereo Line Inputs and Stereo Line Outputs
- ♦ Voiceband Filters with Stopband Attenuation Greater than 70dB
- ♦ Battery-Measurement Auxiliary ADC
- ♦ Comprehensive Headset Detection
- ♦ Dual I²S- and TDM-Compatible Digital Audio Interfaces
- ♦ I²C- or SPI-Compatible Control Bus with 3.6V Tolerant Inputs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9880AEWM+	-40°C to +85°C	48 WLP
MAX9880AETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Block Diagram



Functional Diagram/Typical Operating Circuit appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)
DVDD, AVDD, PVDD ....-0.3V to +2V
DVDDS1, JACKSNS, MICVDD ....-0.3V to +3.6V
DGND, PGND..-0.1V to +0.1V
PREG, REF, REG....................................-0.3V to (V_{AVDD} + 0.3V)
MICBIAS ....-0.3V to (V_{MICVDD} + 0.3V)
MCLK, LRCLKS1, BCLKS1,
SDINS1, SDOUTS1..........................-0.3V to (V_{DVDDS1} + 0.3V)
X1, X2, LRCLKS2, BCLKS2, SDINS2,
SDOUTS2, DOUT, MODE ....-0.3V to (V_{DVDD} + 0.3V)
SDA/DIN, SCL/SCLK, $\overline{CS}$, $\overline{IRQ}$ ....-0.3V to +3.6V
LOUTP, LOUTN, ROUTP, ROUTN,
LOUTL, LOUTR ....(V_{PGND} - 0.3V) to (V_{PVDD} + 0.3V)
LINL, LINR, MICLP/DIGMICDATA,
MICLN/DIGMICCLK, MICRP/SPDMDATA,
MICRN/SPDMCLK ....-0.3V to (V_{AVDD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
48-Bump WLP (derate 12.5mW/°C above +70°C) 1000mW
48-Pin TQFN (derate 37mW/°C above +70°C) 2963mW
Junction Temperature..+150°C
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...............27°C/W
Junction-to-Case Thermal Resistance (θ_{JC})......................1°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})................42°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).......................5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		PVDD, DVDD, AVDD		1.65	1.8	1.95	V
		DVDDS1, MICVDD		1.65	1.8	3.6	
Total Supply Current	I_{VDD}	Full-duplex 8kHz mono (Note 3)	Analog (AVDD + PVDD + MICVDD)		5.33	8	mA
			Digital (DVDD + DVDDS1)		1.4	2	
		DAC playback 48kHz stereo (Note 3)	Analog (AVDD + PVDD + MICVDD)		3.5	6	
			Digital (DVDD + DVDDS1)		2.5	4	
		Full-duplex 48kHz stereo (Note 3)	Analog (AVDD + PVDD + MICVDD)		8.4	12	
			Digital (DVDD + DVDDS1)		3.0	5	
		Stereo line-in to line-out only, T_A = +25°C	Analog (AVDD + PVDD + MICVDD)		4.9	8	
			Digital (DVDD + DVDDS1)		0.012	0.05	
Shutdown Supply Current		T_A = +25°C	Analog (AVDD + PVDD + MICVDD)		0.3	2	µA
			Digital (DVDD + DVDDS1)		2.6	8	
Shutdown to Full Operation		Excludes PLL lock time			10		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC (Note 4)							
Dynamic Range (Note 5)	DR	f_S = 48kHz, AV_{VOL} = 0dB, T_A = +25°C	Master or slave mode		96		dB
			Slave mode	88			
Full-Scale Output		Differential mode			1		V_{RMS}
		Capacitorless and single-ended modes			0.56		
Gain Error		DC accuracy, measured with respect to full-scale output			1	5	%
Voice Path Phase Delay	P_{DLY}	1kHz, 0dB input, highpass filter disabled measured from digital input to analog output; MODE = 0 (IIR voice)	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion	THD	f_{MCLK} = 12.288MHz, f_S = 48kHz, 0dBFS, measured at headphone outputs			-75		dB
DAC Attenuation Range	AV_{DAC}	VDACA/SDACA = 0xF to 0x0		-15		0	dB
DAC Gain Adjust	AV_{GAIN}	VDACG = 00 to 11		0		+18	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V			85		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			85		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			74		
DAC VOICE MODE DIGITAL IIR LOWPASS FILTER (6x Interpolation)							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.448 x f_S		Hz
		-3dB cutoff			0.451 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.476 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz		75			dB
DAC VOICE MODE DIGITAL 5th-ORDER IIR HIGHPASS FILTER							
5th-Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{DHPPB}	DVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)			0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)			0.0312 x f_S		
		DVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)			0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)			0.0625 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0042 x f_S		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
5th-Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable)	f_{DHPSB}	DVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)			0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)			0.0156 x f_S		
		DVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)			0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)			0.0312 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	DVFLT not equal to 000			90		dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER (DHF = 0 for f_{LRCLK} < 50kHz)							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.43 x f_S		Hz
		-3dB cutoff			0.47 x f_S		
		-6.02dB cutoff			0.50 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz; f = 0.58 f_S to 7.42 f_S			0.58 x f_S		Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER (DHF = 1 for f_{LRCLK} > 50kHz)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.24 x f_S		Hz
		-3dB cutoff			0.33 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f = 0.5 f_S to 3.5 f_S			0.5 x f_S		Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DAC STEREO AUDIO MODE DIGITAL DC-BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1 (DAI1), DCB = 1 (DAI2)			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	DVFLT = 0x1 (DAI1), DCB = 1 (DAI2)			90		dB
ADC (Note 6)							
Dynamic Range (Note 5)	DR	f_S = 8kHz, MODE = 0 (IIR voice), T_A = +25°C		72	82		dB
		f_S = 8kHz to 48kHz, MODE = 1 (FIR audio) (Note 7)			84		
Full-Scale Input		Differential MIC input or stereo line inputs, AV_{PRE} = 0dB, AV_{PGAM} = 0dB			1		V_{P-P}
Gain Error (Note 7)		DC accuracy, measured with respect to 80% of full-scale output			1	5	%
Voice Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output; MODE = 0 (IIR voice)	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.61		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f = 1kHz, f_S = 8kHz, T_A = +25°C, -20dB input		-80	-70	dB
ADC Level Adjust	AV_{ADC}	AVL/AVR = 0xF to 0x0	-12		+3	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		80		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		78		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		72		
ADC VOICE MODE DIGITAL IIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.445 x f_S		Hz
		-3dB cutoff		0.449 x f_S		
Passband Ripple		f < f_{PLP}		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.469 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz	74			dB
ADC VOICE MODE DIGITAL 5th-ORDER IIR HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		AVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		AVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
ADC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.48 x f_S		
		-6.02dB cutoff		0.5 x f_S		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.58 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz			60		dB
ADC STEREO AUDIO MODE DIGITAL DC-BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	AVFLT = 0x1			90		dB
OUTPUT VOLUME CONTROL							
Output Volume Control (Note 8)		VOLL/VOLR = 0x00		8.1	8.6	9.2	dB
		VOLL/VOLR = 0x01		7.6	8.1	8.6	
		VOLL/VOLR = 0x02		7.1	7.6	8.1	
		VOLL/VOLR = 0x04		6.1	6.6	7.2	
		VOLL/VOLR = 0x08		3.1	3.6	4.3	
		VOLL/VOLR = 0x10		-5.9	-5.4	-4.9	
		VOLL/VOLR = 0x20		-60	-55.1	-52	
		VOLL/VOLR = 0x27		-94	-84	-81	
Output Volume Control Step Size		VOLL/VOLR = 00x00 to 0x06 (+9dB to +6dB)			0.5		dB
		VOLL/VOLR = 00x06 to 0x0F (+6dB to +3dB)			1		
		VOLL/VOLR = 00x0F to 0x17 (-3dB to -19dB)			2		
		VOLL/VOLR = 00x17 to 0x27 (-19dB to -81dB)			4		
Output Volume Control Mute Attenuation		f = 1kHz			100		dB
HEADPHONE AMPLIFIER (Note 9)							
Output Power (Differential Mode)	P_{OUT}	f = 1kHz, 0dBFS input, THD < 1%, T_A = +25°C	R_L = 16Ω	25	48		mW
			R_L = 32Ω		30		
Output Power (Capacitorless Mode)	P_{OUT}	f = 1kHz, 0dBFS input, THD < 1%, T_A = +25°C	R_L = 16Ω		17		mW
			R_L = 32Ω		10		
Total Harmonic Distortion + Noise (Differential Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-78	-67	dB
			R_L = 32Ω		-79		
Total Harmonic Distortion + Noise (Capacitorless Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-73	-60	dB
			R_L = 32Ω		-75		
Total Harmonic Distortion + Noise (Single-Ended Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-70	-60	dB
			R_L = 32Ω		-70		
Dynamic Range (Notes 5, 7)	DR	AV_{VOL} = +6dB		77	90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 7)	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			72		
Output Offset Voltage	V_{OS}	AV_{VOL} = -81dB, differential mode	LOUTP to LOUTN, ROUTP to ROUTN, T_A = +25°C		±0.2		mV
		AV_{VOL} = -81dB, capacitorless mode	LOUTP to LOUTN, ROUTP to LOUTN, T_A = +25°C		±0.6		
Crosstalk	XTALK	Differential, P_{OUT} = 5mW, f = 1kHz			90		dB
		Capacitorless mode, P_{OUT} = 5mW, f = 1kHz			45		
Capacitive Drive Capability		No sustained oscillations	R_L = 32Ω		500		pF
			R_L =		100		
Click-and-Pop Level (Differential, Capacitorless Modes)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-70		dBV
			Out of shutdown		-70		
Click-and-Pop Level (Single-Ended Mode)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-70		dBV
			Out of shutdown		-70		
LINE OUTPUTS (Note 7)							
Full-Scale Output					0.5		V_{RMS}
Line Output Level Adjust	AV_{LO}	LOGL/LOGR = 0x00		-0.7	-0.1	+0.6	dB
		LOGL/LOGR = 0x01		-2.6	-2.1	-1.6	
		LOGL/LOGR = 0x02		-4.6	-4.1	-3.6	
		LOGL/LOGR = 0x04		-8.6	-8.1	-7.6	
		LOGL/LOGR = 0x08		-16.6	-16	-15.6	
		LOGL/LOGR = 0x0F		-31.1	-29.9	-29.1	
Line Output Mute Attenuation		f = 1kHz			90		dB
Total Harmonic Distortion + Noise	THD+N	R_L = 1kΩ, f = 1kHz, V_{OUT} = 1.4V_{P-P} (Note 9)			-67	-59	dB
Signal-to-Noise Ratio		R_L = 1kΩ, LINL/LINR = 1µF to GND	20Hz < f < 20kHz		86		dB
			A-weighted		90		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V			46		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			76		
Capacitive Drive Capability		R_L = 10kΩ, no sustained oscillations			100		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MICROPHONE AMPLIFIER						
Preamplifier Gain	AV_{PRE}	PALEN/PAREN = 01	-0.5	0	+0.5	dB
		PALEN/PAREN = 10	19.5	20	20.5	
		PALEN/PAREN = 11	29.3	30	30.5	
MIC PGA Gain	AV_{PGAM}	PGAML/PGAMR = 0x1F	-0.5	0	+0.6	dB
		PGAML/PGAMR = 0x00	19.3	19.9	20.4	
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV$_{P-P}$, f = 217Hz		50		dB
MIC Input Resistance	RIN_MIC	All gain settings	30	50		kΩ
Total Harmonic Distortion + Noise	THD+N	AV_{PRE} = 0dB, V_{IN} = 1V$_{P-P}$, f = 1kHz, A-weighted		-80		dB
		AV_{PRE} = +30dB, V_{IN} = 32mV$_{P-P}$, f = 1kHz, A-weighted		-65		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		78		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		72		
MICROPHONE BIAS						
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA, V_{MICVDD} = 1.8V, MBIAS = 0	1.48	1.52	1.56	V
		I_{LOAD} = 1mA, V_{MICVDD} = 3V, MBIAS = 0	2.15	2.2	2.25	
Load Regulation		I_{LOAD} = 1mA to 2mA, MBIAS = 0		0.6	10	V/A
Line Regulation		V_{AVDD} = 1.8V, V_{MICVDD} = 1.65V to 1.95V, MBIAS = 0		1.55		mV/V
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = 100mV$_{P-P}$		100		dB
		f = 10kHz, V_{RIPPLE} = 100mV$_{P-P}$		90		
Noise Voltage		A-weighted		9.5		µV$_{RMS}$
LINE INPUT						
Full-Scale Input	V_{IN}	AV_{LINE} = 0dB		1.0		V$_{P-P}$
Line Input Level Adjust	AV_{LINE}	LIGL/LIGR = 0x00	22.8	23.9	24.9	dB
		LIGL/LIGR = 0x01	20.7	21.9	22.9	
		LIGL/LIGR = 0x02	18.9	20	20.9	
		LIGL/LIGR = 0x04	14.9	16	16.9	
		LIGL/LIGR = 0x08	6.9	8	8.9	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Input Mute Attenuation		f = 1kHz			100		dB
Input Resistance	R_{IN_LINE}	AV_{LINE} = +24dB		20			kΩ
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 0.1V_{P-P}, f = 1kHz			-74		dB
AUXIN INPUT							
Input DC Voltage Range		AUXEN = 1		0		0.738	V
AUXIN Input Resistance	R_{IN}	AUXEN = 1, 0V ≤ V_{AUXIN} ≤ 0.738V		10	40		MΩ
JACK DETECT							
JACKSNS High Threshold	V_{TH1}	$\overline{SHDN}$ = 1		0.92 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
		$\overline{SHDN}$ = 0			0.95 x V_{MICVDD}		
JACKSNS Low Threshold	V_{TH2}	$\overline{SHDN}$ = 1		0.06 x $V_{MICBIAS}$	0.10 x $V_{MICBIAS}$	0.17 x $V_{MICBIAS}$	V
		$\overline{SHDN}$ = 0			0.08 x V_{MICVDD}		
JACKSNS Sense Voltage	V_{SENSE}	$\overline{SHDN}$ = 0			V_{MICVDD}		V
JACKSNS Sense Resistance	R_{SENSE}	$\overline{SHDN}$ = 0		1.9	2.3	3.1	kΩ
JACKSNS Deglitch Period	t_{GLITCH}			12		300	ms
Headphone Sense Threshold					8		Ω
1-BIT SPDM OUTPUT							
Dynamic Range (Note 5)	DR	f_S = 48kHz, A-weighted, 20Hz to 20kHz, AV_{VOL} = 0dB; master or slave mode, T_A = +25°C			90		dB
Output Operational Range		0dB signal 1's density		25		75	%
DIGITAL SIDETONE (MODE = 1 IIR Voice Mode Only)							
Sidetone Gain Adjust Range	AV_{STGA}	Differential output mode		-60		0	dB
Voice Path Phase Delay	P_{DLY}	MIC input to headphone output, f = 1kHz, HP filter disabled	f_S = 8kHz		2.2		ms
			f_S = 16kHz		1.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	For any LRCLK sample rate		10		60	MHz
MCLK Input Duty Cycle		Prescaler = /1 mode		40		60	%
		/2 or /4 modes		30		70	
Maximum MCLK Input Jitter		Maximum allowable RMS for performance limits			100		ps
LRCLK Sample Rate (Note 10)		DHF = 0		8		48	kHz
		DHF = 1		48		96	
LRCLK Average Frequency Error (Master and Slave Modes) (Note 11)		FREQ1 mode = 0x8 to 0xF		0		0	%
		PCLK = 192x, 256x, 384x, 512x, 768x, and 1024x		0		0	
		FREQ1 mode = Any clock other than above		-0.025		+0.025	
LRCLK PLL Lock Time		Any allowable LRCLK and PCLK rate, slave mode	Rapid lock mode		2	7	ms
			Nonrapid lock mode		12	25	
LRCLK Acceptable Jitter for Maintaining PLL Lock		Allowable LRCLK period change from nominal for slave PLL mode at any allowable LRCLK and PCLK rates				±100	ns
Soft-Start/Stop Time					10		ms
CRYSTAL OSCILLATOR							
Frequency		Fundamental mode only			12.288		MHz
Maximum Crystal ESR					100		Ω
Input Leakage Current	I_{IH}, I_{IL}	X1, T_A = +25°C		-1		+1	µA
Input Capacitance	C_{X1}, C_{X2}				4		pF
Maximum Load Capacitor	C_{L1}, C_{L2}				45		pF
DIGITAL INPUT (MCLK)							
Input High Voltage	V_{IH}			1.2			V
Input Low Voltage	V_{IL}					0.6	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C		-1		+1	µA
Input Capacitance					10		pF
DIGITAL INPUTS (SDINS1, BCLKS1, LRCLKS1)							
Input High Voltage	V_{IH}			0.7 x V_{DVDDS1}			V
Input Low Voltage	V_{IL}					0.3 x V_{DVDDS1}	V
Input Hysteresis					200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C		-1		+1	µA
Input Capacitance					10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL, DIN, SCLK, $\overline{CS}$, MODE, SDINS2, BCLKS2, LRCLKS2)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
DIGITAL INPUTS (DIGMICDATA)						
Input High Voltage	V_{IH}		0.65 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.35 x V_{DVDD}	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-35		+35	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLKS1, LRCLKS1, SDOUTS1)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{DVDDS1} - 0.4			V
CMOS DIGITAL OUTPUTS (BCLKS2, LRCLKS2, SDOUTS2)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{DVDD} - 0.4			V
CMOS DIGITAL OUTPUTS (DOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA, $\overline{CS}$ = DVDD			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA, $\overline{CS}$ = DVDD	V_{DVDD} - 0.4			V
Output Low Current	I_{OL}	MODE = DVDD, DOUT = 0, T_A = +25°C	-1		+1	µA
Output High Current	I_{OH}	MODE = DVDD, DOUT = DVDD, T_A = +25°C	-1		+1	µA
CMOS DIGITAL OUTPUTS (DIGMICCLK, SPDMDATA, SPDMCLK)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	V_{DVDD} - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = V_{DVDD}, T_A = +25°C	-1		+1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.2 x V_{DVDD}	V

Low-Power, High-Performance Dual I²S Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE TIMING CHARACTERISTICS (V_{DVDD} = 1.8V)							
DIGMICCLK Frequency	f_{MICCLK}	f_{MCLK} = 12.288MHz	MICCLK = 00		1.536		MHz
			MICCLK = 01		2.048		
			MICCLK = 10		$64f_S$		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU, MIC}$	Either clock edge		20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD, MIC}$	Either clock edge		0			ns
SPDM TIMING CHARACTERISTICS							
SPDMCLK Frequency	$f_{SPDMCLK}$	f_{MCLK} = 12.288MHz	SPDMCLK = 00		1.536		MHz
			SPDMCLK = 01		2.048		
			SPDMCLK = 10		3.072		
SPDMCLK to SPDMDATA Delay Time	$t_{DLY,SPDM}$	Rising edge SPDMCLK to right-channel valid SPDMDATA and falling edge SPDMCLK to left-channel valid SPDMDATA	Minimum, f_{MCLK} = 20MHz		15		ns
			Maximum, f_{MCLK} = 10MHz		65		
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (TDM = 0, V_{DVDD} = 1.8V)							
BCLK Cycle Time	t_{BCLKS}			75			ns
BCLK High Time	t_{BCLKH}	T_A = +25°C		30			ns
BCLK Low Time	t_{BCLKL}	T_A = +25°C		30			ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master operation, C_L = 15pF			7		ns
SDIN or LRCLK to BCLK Setup Time	t_{SU}			20			ns
SDIN or LRCLK to BCLK Hold Time	t_{HD}			5			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	C_L = 30pF		0		40	ns
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (TDM = 1, Figure 3, V_{DVDD} = 1.8V)							
TDM Clock Frequency	$1/t_{CLK}$	TDM mode (TDM = 1)		128		2048	kHz
TDM Clock Time High	t_{CLKH}	TDM mode (TDM = 1), T_A = +25°C		220			ns
TDM Clock Time Low	t_{CLKL}	TDM mode (TDM = 1), T_A = +25°C		220			ns
TDM Short-Sync Setup Time	$t_{SYNCSET}$	Short TDM mode (TDM = 1, FSW = 0), master mode (MAS = 1)			200		ns
		Short TDM mode (TDM = 1, FSW = 0), slave mode (MAS = 0)		20			

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2μF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1μF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TDM Short Sync Hold Time	$t_{SYNCHOLD}$	Short TDM mode (TDM = 1, FSW = 0), master mode (MAS = 1)		200		ns
		Short TDM mode (TDM = 1, FSW = 0), slave mode (MAS = 0)	20			
TDM Short Sync Tx Data Delay	t_{SYNCTX}	Short TDM mode (TDM = 1, FSW = 0)		12		ns
TDM Long Sync Start Delay	$t_{CLKSYNC}$	Long TDM mode (TDM = 1, FSW = 1)		3.4		ns
TDM Long Sync End Time Setup	$t_{ENDSYNC}$	Long TDM mode (TDM = 1, FSW = 1)		51		ns
TDM Data Delay from Clock	t_{CLKTX}	TDM mode (TDM = 1)			40	ns
TDM High-Impedance State Setup from Data	t_{HIZOUT}	TDM mode (TDM = 1)		120		ns
TDM Rx Data Setup Time	t_{SETUP}	TDM mode (TDM = 1)	20			ns
TDM Rx Data Hold Time	t_{HOLD}	TDM mode (TDM = 1)	20			ns
I²C TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			μs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			μs
SCL Pulse-Width Low	t_{LOW}		1.3			μs
SCL Pulse-Width High	t_{HIGH}		0.6			μs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			μs
Data Hold Time	$t_{HD,DAT}$	$R_{PU,SDA}$ = 475Ω	0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 12)	20 + $0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 12)	20 + $0.1C_B$		300	ns
SDA Transmitting Fall Time	t_F	$R_{PU,SDA}$ = 475Ω (Note 12)	20 + $0.1C_B$		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

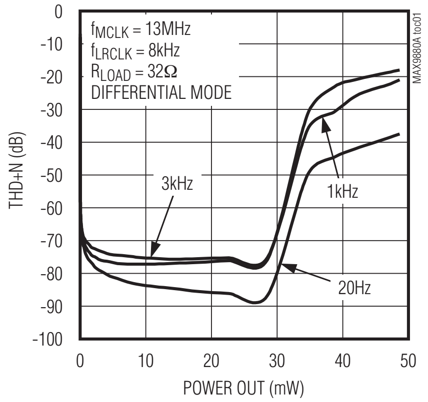
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
SPI TIMING CHARACTERISTICS						
Minimum SCLK Clock Period	t_{CP}			40		ns
Minimum SCLK Pulse-Width Low	t_{CL}			18		ns
Minimum SCLK Pulse-Width High	t_{CH}			18		ns
Minimum $\overline{CS}$ Setup Time	t_{CSS}			20		ns
Minimum $\overline{CS}$ Hold Time	t_{CSH}			20		ns
Minimum $\overline{CS}$ Pulse-Width High	t_{CSW}			20		ns
Minimum DIN Setup Time	t_{DS}			5		ns
Minimum DIN Hold Time	t_{DH}			5		ns
Minimum Output Data Propagation Delay	t_{DO}	C_L = 50pF		9		ns
Minimum Output Data Enable Time	t_{DEN}			5		ns
Minimum Output Data Disable Time	t_{DZ}			5		ns

Note 2: The MAX9880A is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Clocking all zeros into the DAC. Master mode. Differential headphone mode.
Note 4: DAC performance measured at headphone outputs.
Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 6: Performance measured using microphone inputs, unless otherwise stated.
Note 7: Performance measured using line inputs.
Note 8: Performance measured using line inputs to line outputs.
Note 9: Performance measured using DAC. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, unless otherwise stated.
Note 10: LRCLK can be any rate in the indicated range. Asynchronous or noninteger MCLK/LRCLK ratios can exhibit some full-scale performance degradation compared to synchronous integer-related MCLK/LRCLK ratios.
Note 11: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 12: C_B is in pF.

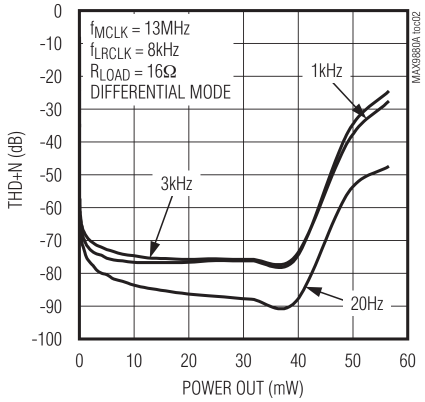
Typical Operating Characteristics

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

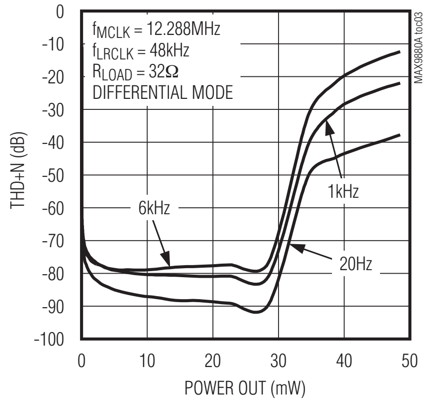
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



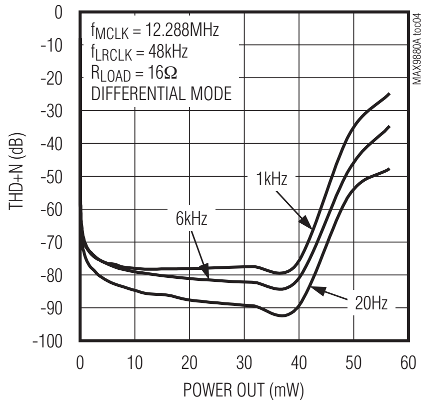
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



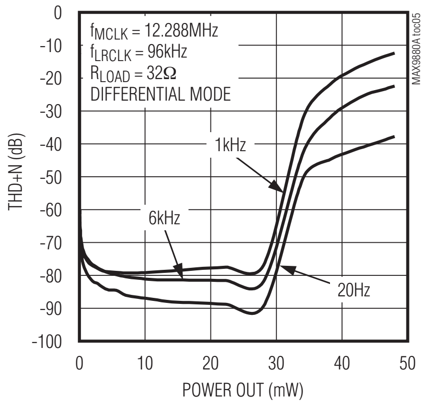
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



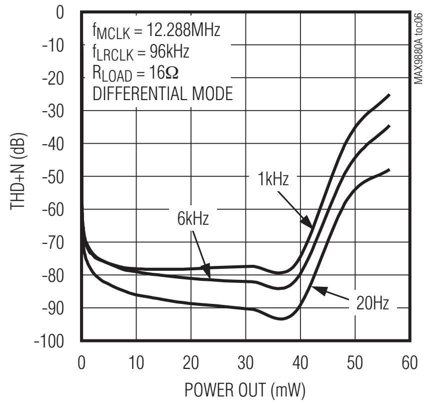
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



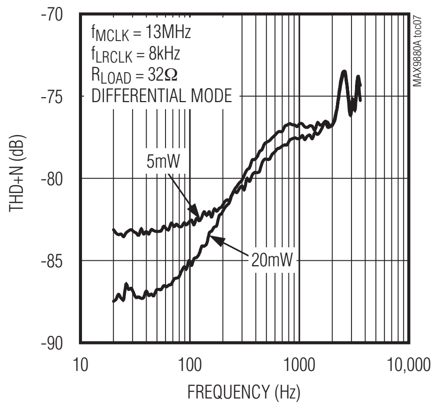
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



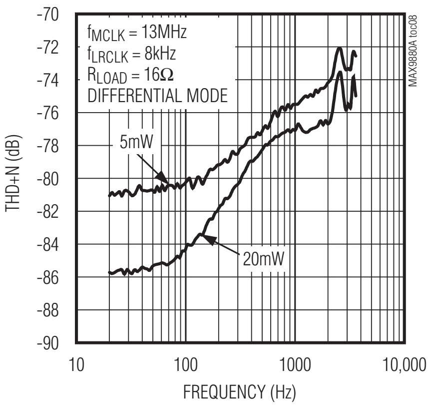
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



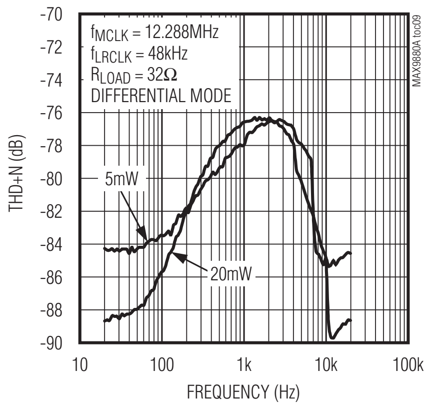
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)

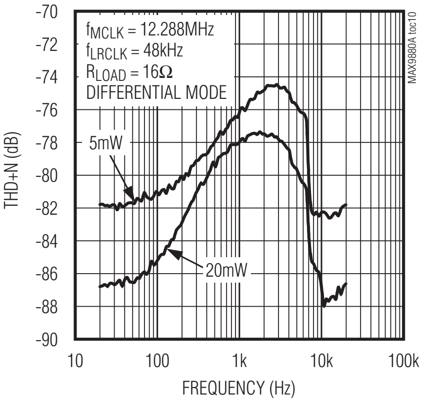


Low-Power, High-Performance Dual I²S Stereo Audio Codec

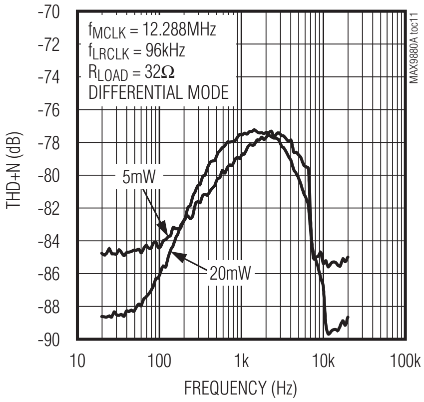
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1}$ = +1.8V, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS} = C_{PREG} = C_{REG}$ = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

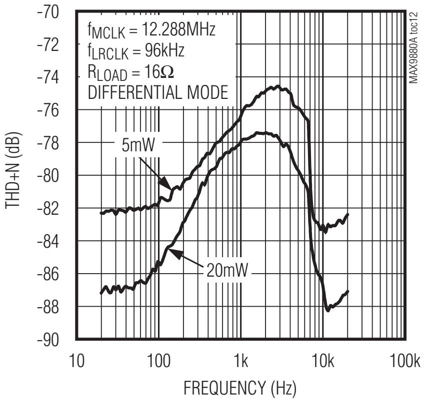
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



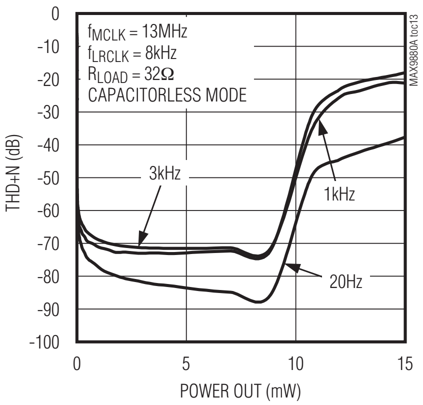
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



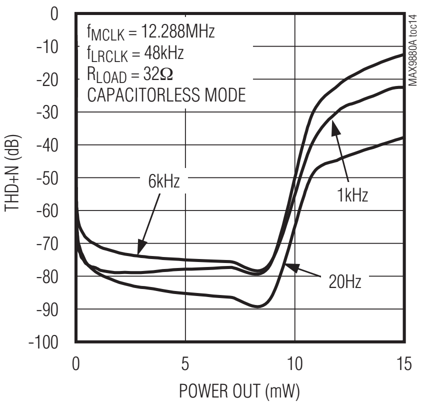
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



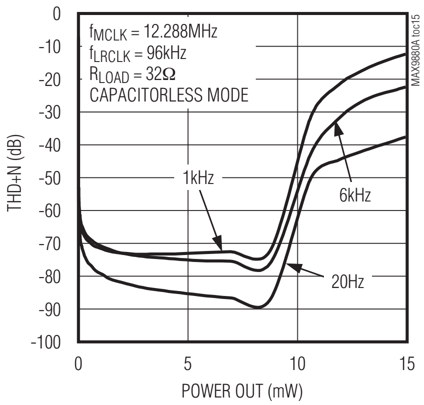
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



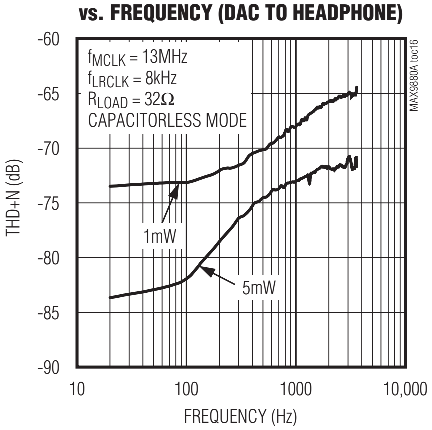
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



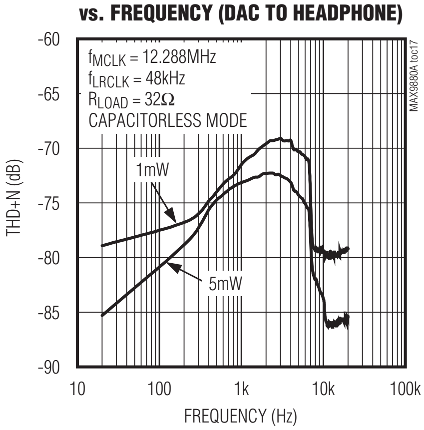
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



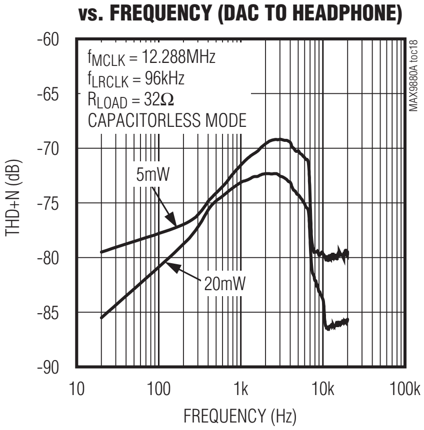
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



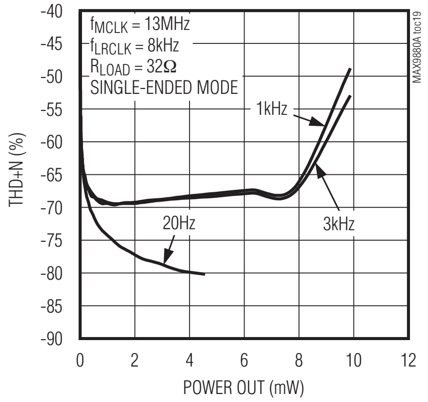
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



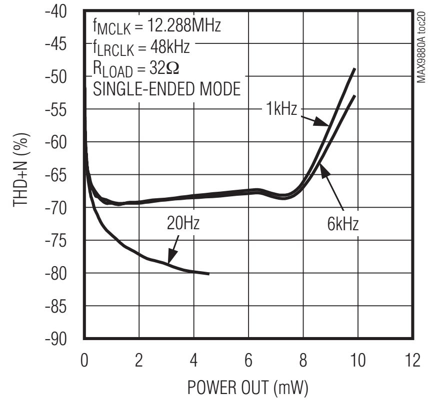
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1}$ = +1.8V, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS} = C_{PREG} = C_{REG}$ = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

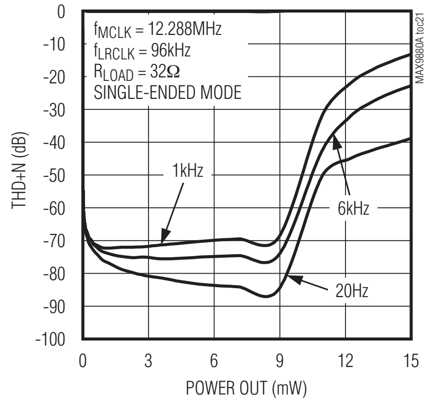
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



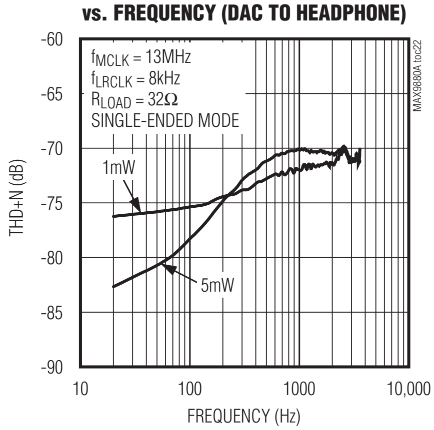
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



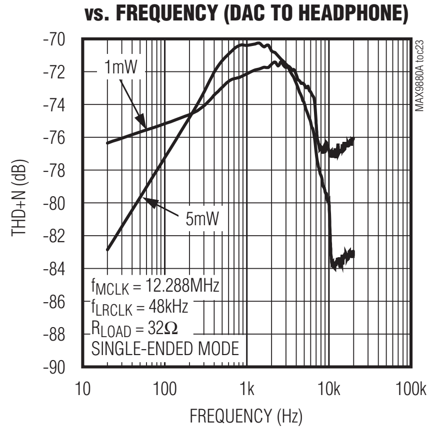
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



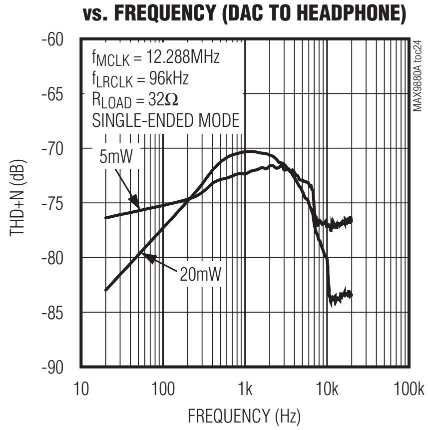
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



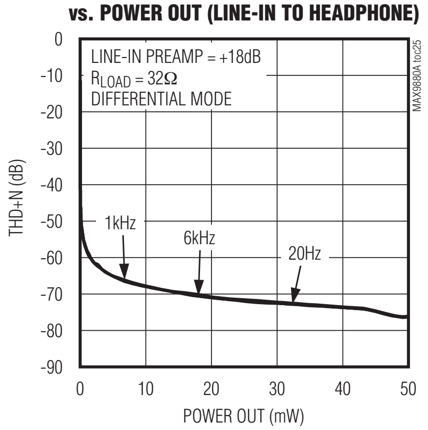
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



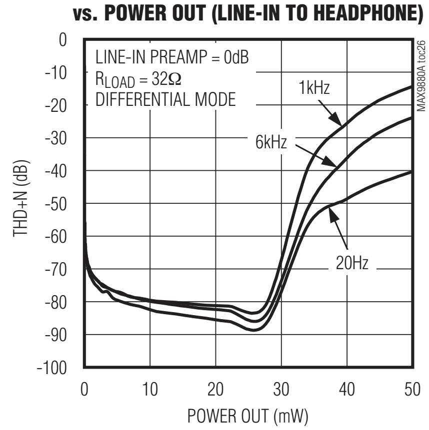
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



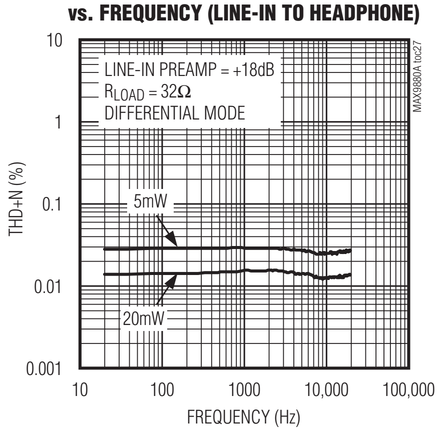
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE-IN TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE-IN TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE-IN TO HEADPHONE)

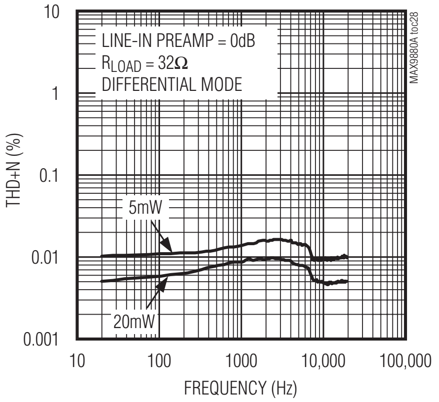


Low-Power, High-Performance Dual I²S Stereo Audio Codec

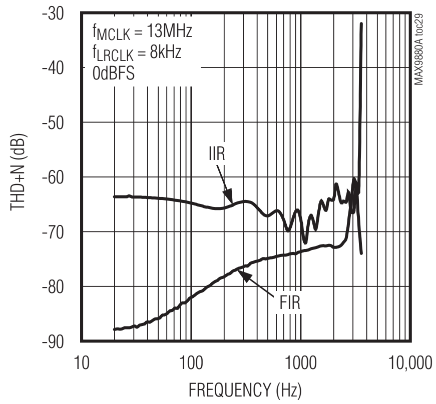
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V$, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, $C_{REF} = 2.2\mu F$, $C_{MICBIAS} = C_{PREG} = C_{REG} = 1\mu F$, $AV_{PRE} = +20dB$, $AV_{PGAM} = 0dB$, $AV_{DAC} = 0dB$, $AV_{LINE} = +20dB$, $AV_{VOL} = 0dB$, $AV_{LO} = 0dB$, $f_{MCLK} = 13MHz$, differential output, unless otherwise noted.)

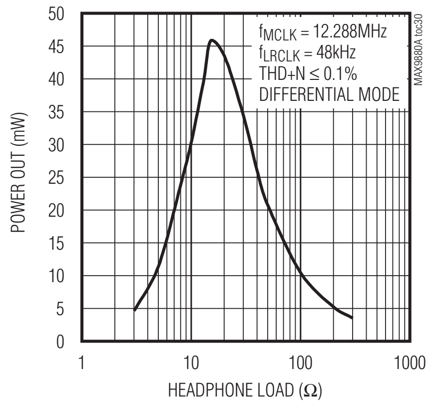
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE-IN TO HEADPHONE)



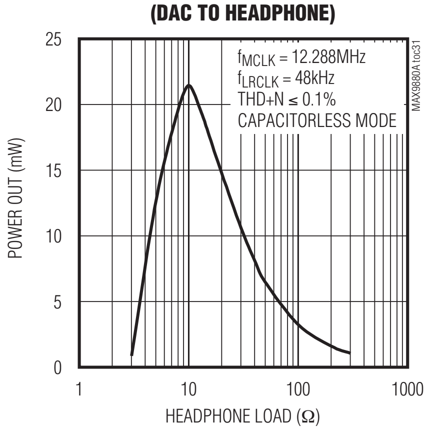
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO LINE-OUT)



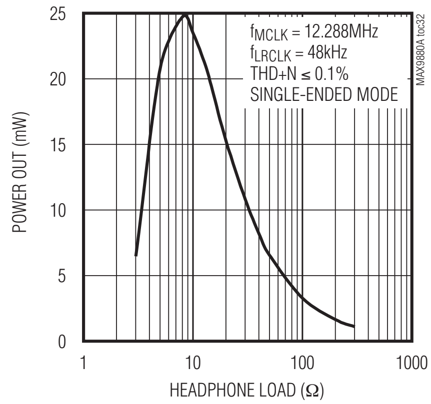
POWER OUT vs. HEADPHONE LOAD



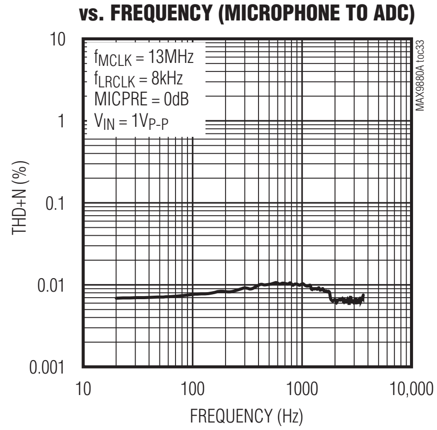
OUTPUT POWER vs. LOAD RESISTANCE (DAC TO HEADPHONE)



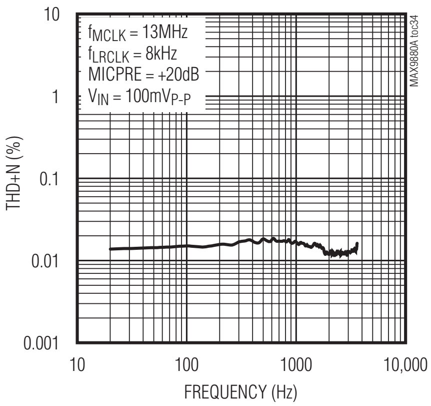
POWER OUT vs. HEADPHONE LOAD



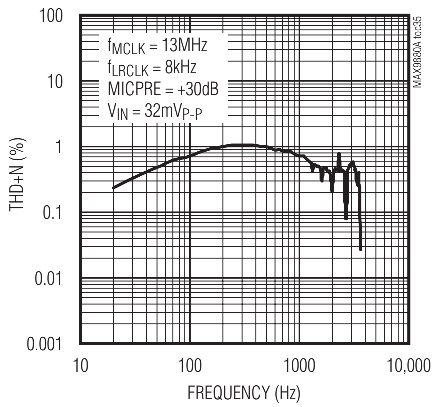
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



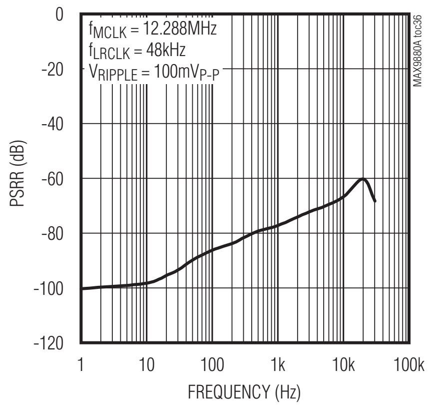
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



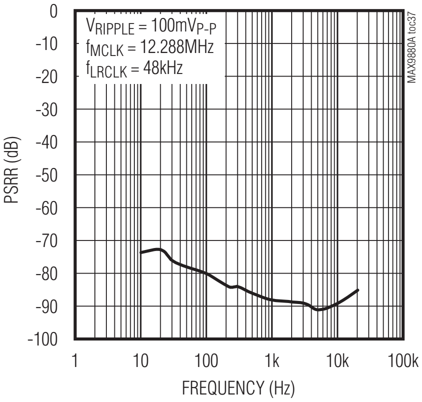
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



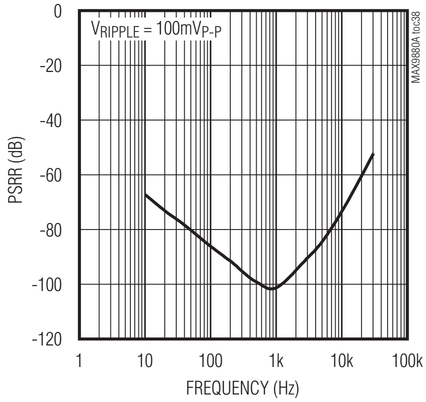
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V$, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, $C_{REF} = 2.2\mu F$, $C_{MICBIAS} = C_{PREG} = C_{REG} = 1\mu F$, $AV_{PRE} = +20dB$, $AV_{PGAM} = 0dB$, $AV_{DAC} = 0dB$, $AV_{LINE} = +20dB$, $AV_{VOL} = 0dB$, $AV_{LO} = 0dB$, $f_{MCLK} = 13MHz$, differential output, unless otherwise noted.)

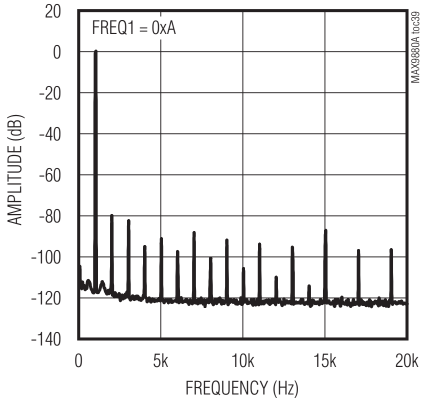
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICROPHONE TO ADC)



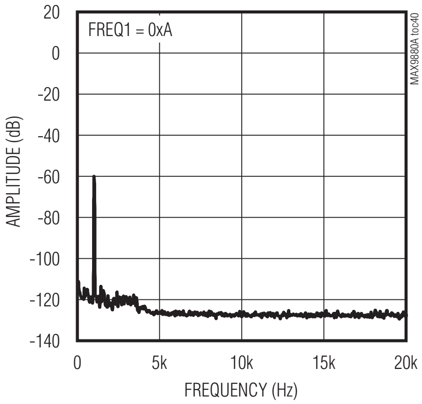
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICBIAS)



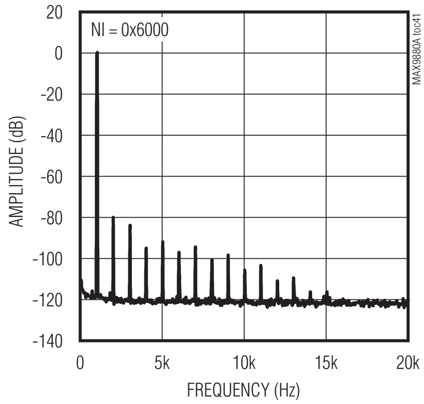
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



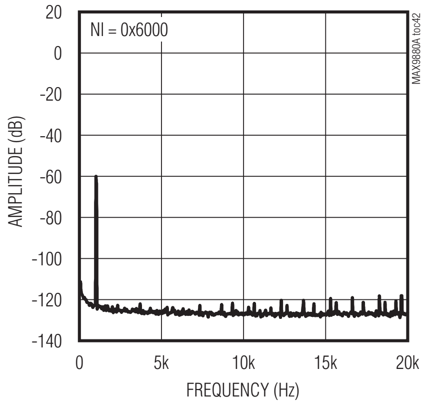
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



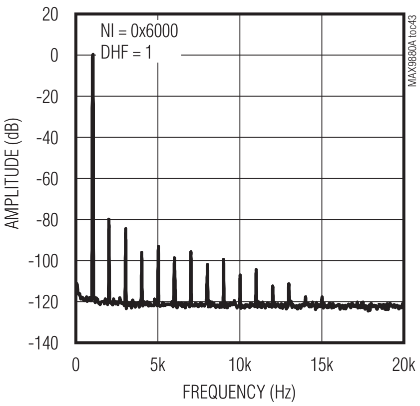
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



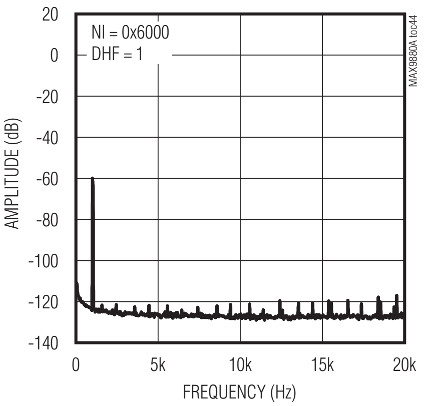
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



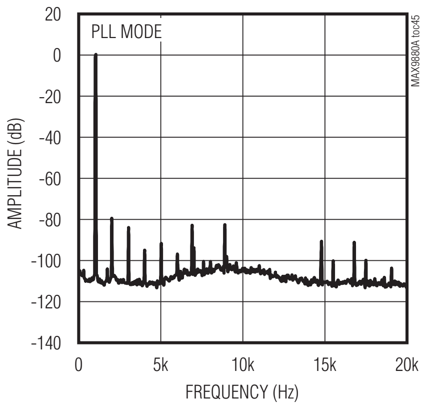
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 96kHz



FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 96kHz



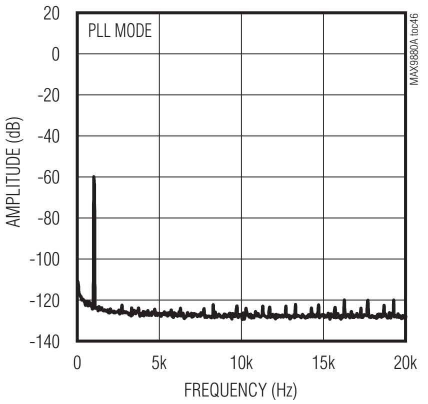
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



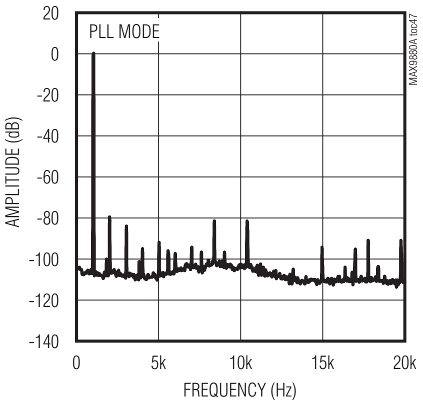
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

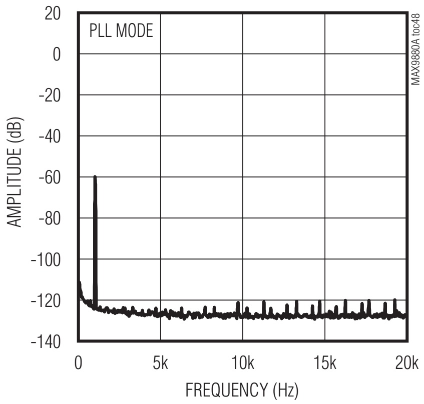
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



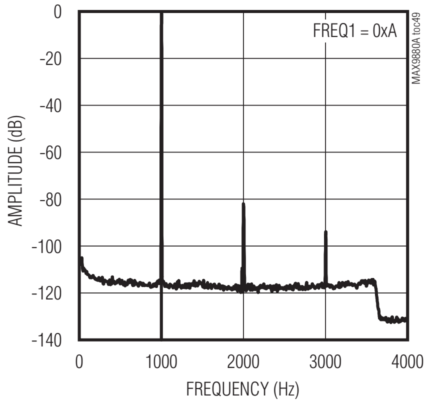
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 44.1kHz



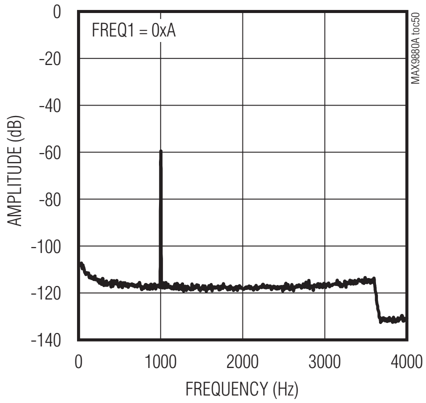
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 44.1kHz



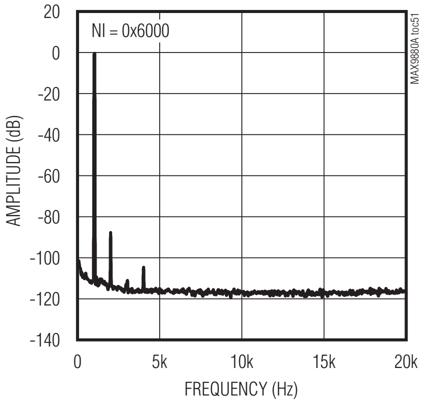
FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



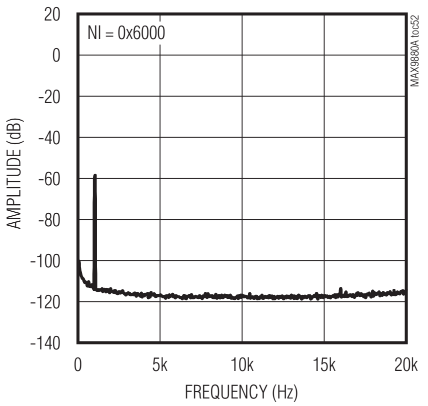
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



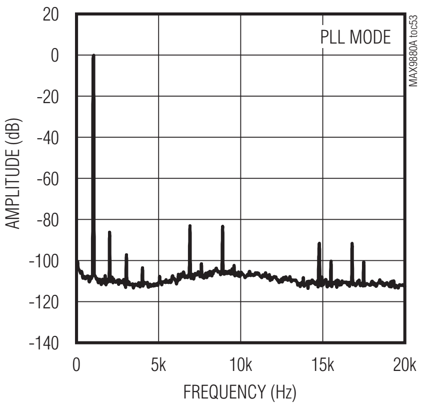
FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



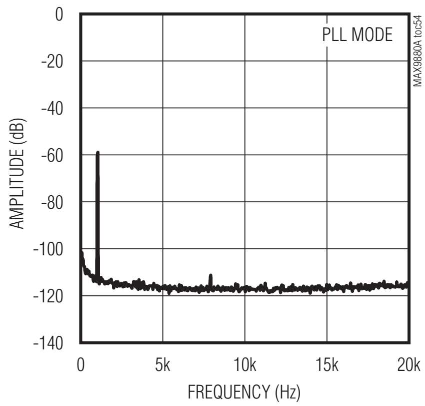
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



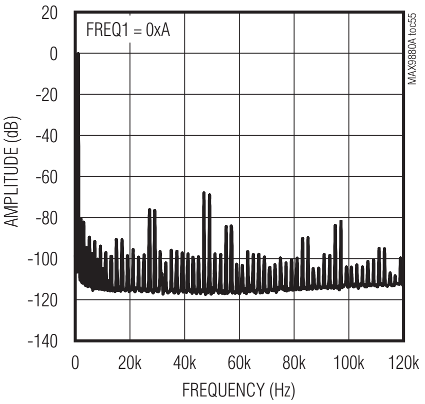
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



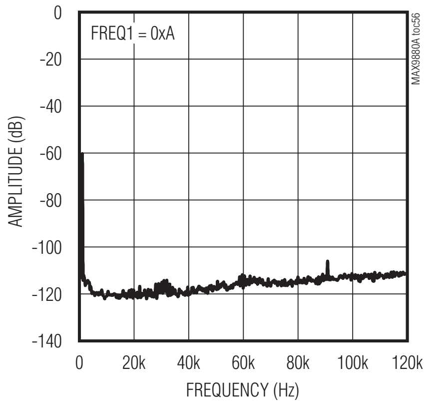
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V$, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, $C_{REF} = 2.2µF$, $C_{MICBIAS} = C_{PREG} = C_{REG} = 1µF$, $AV_{PRE} = +20dB$, $AV_{PGAM} = 0dB$, $AV_{DAC} = 0dB$, $AV_{LINE} = +20dB$, $AV_{VOL} = 0dB$, $AV_{LO} = 0dB$, $f_{MCLK} = 13MHz$, differential output, unless otherwise noted.)

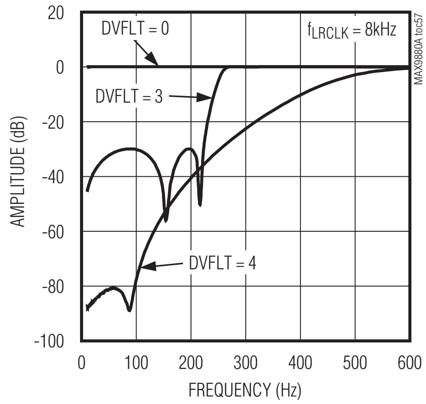
WIDEBAND FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



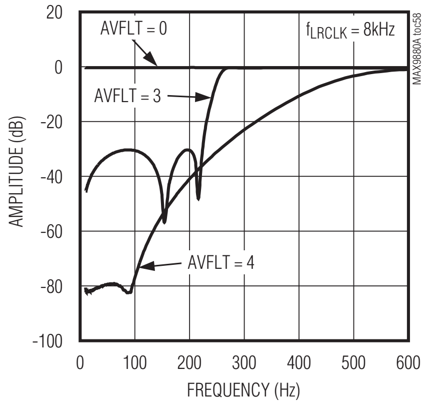
WIDEBAND FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



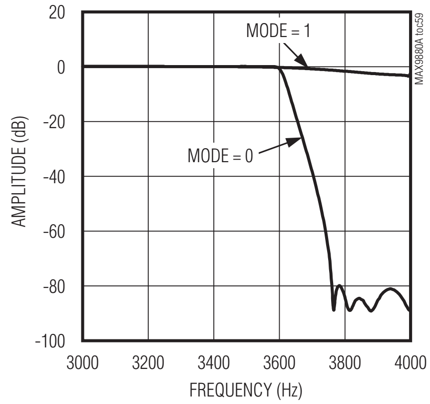
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



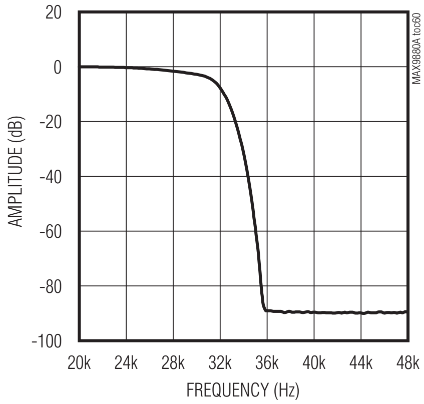
ADC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



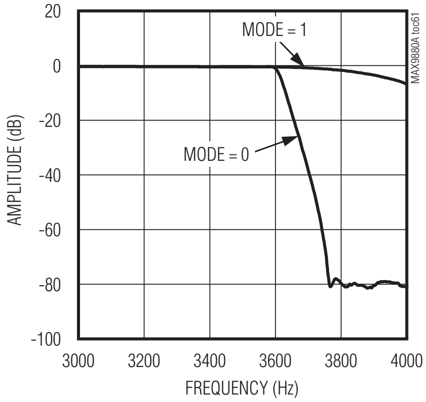
DAC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 8kHz)



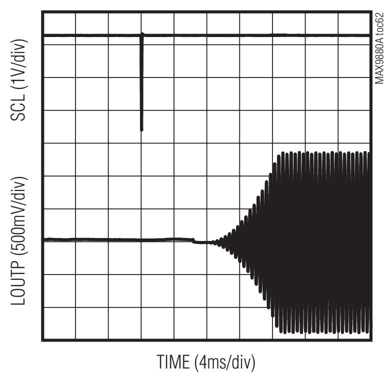
DAC FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 96kHz)



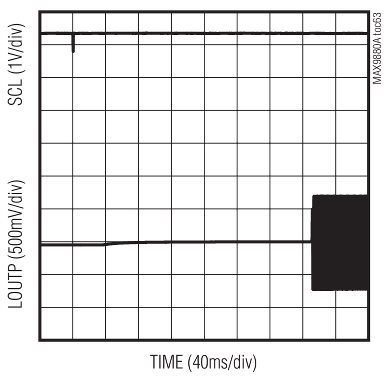
ADC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 8kHz)



SHUTDOWN TO FULL OPERATION (DIFFERENTIAL)



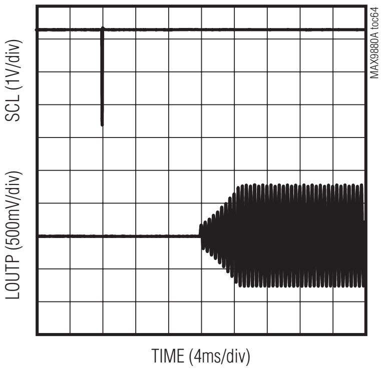
SHUTDOWN TO FULL OPERATION (SE CLICKLESS)



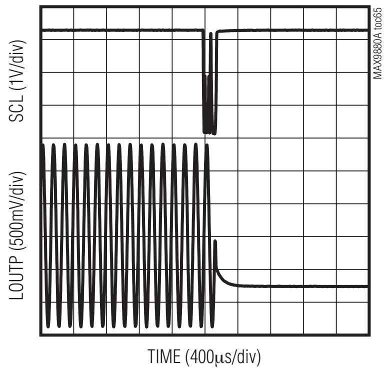
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1}$ = +1.8V, $R_L = \infty$, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS} = C_{PREG} = C_{REG}$ = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

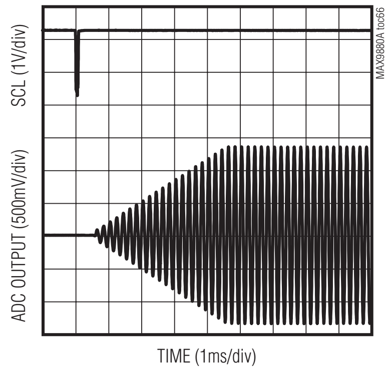
SHUTDOWN TO FULL OPERATION (SE FAST TURN ON)



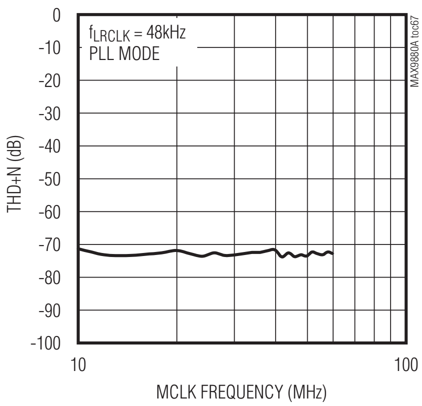
FULL OPERATION TO SHUTDOWN



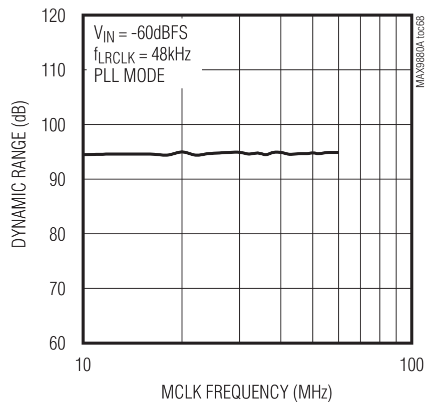
SOFT-START ADC



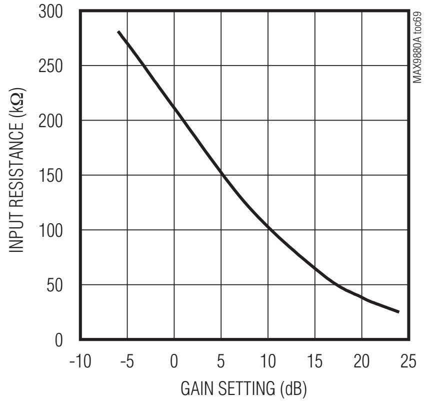
TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS



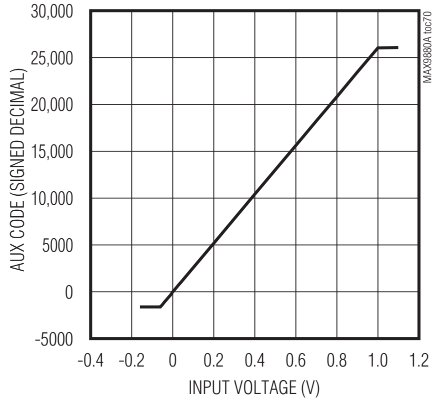
DYNAMIC RANGE vs. MCLK FREQUENCY



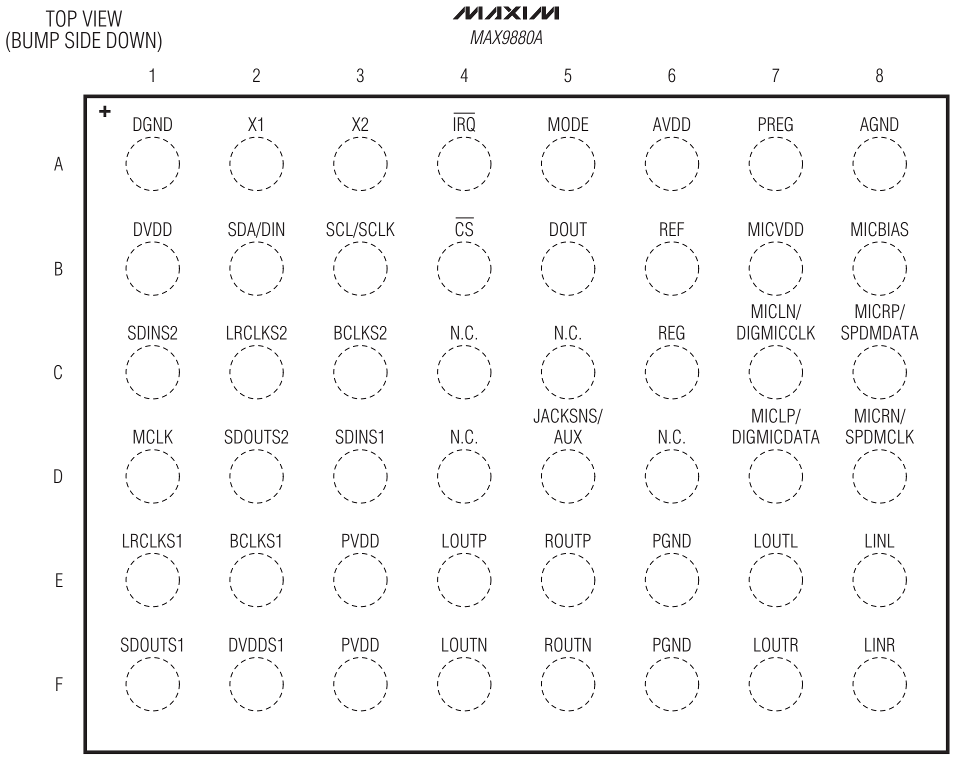
LINE INPUT RESISTANCE vs. GAIN SETTING



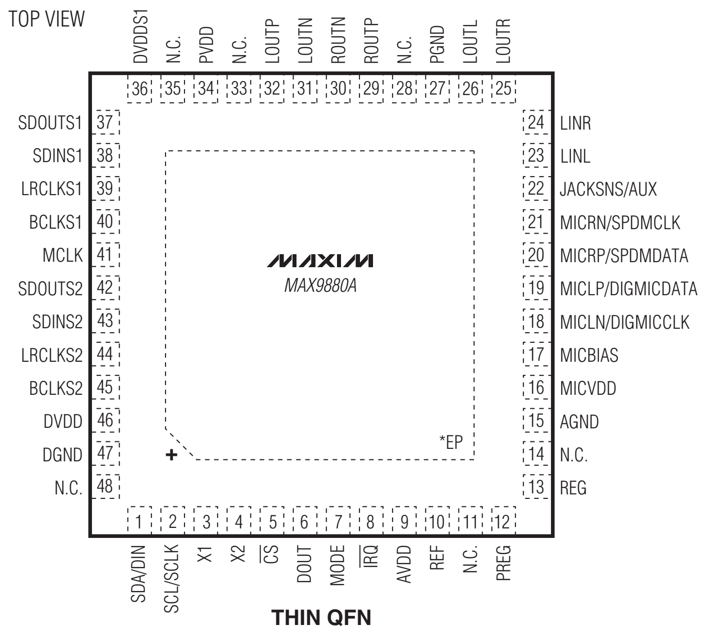
AUX CODE vs. INPUT VOLTAGE



Pin Configurations



WLP



THIN QFN
(6mm × 6mm)

*EP = EXPOSED PAD

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Pin Description

PIN		NAME	FUNCTION
TQFN-EP	WLP		
1	B2	SDA/DIN	I²C Serial-Data Input/Output (MODE = 0). Connect a pullup resistor to DVDD for full output swing. SPI compatible serial-data input (MODE = 1).
2	B3	SCL/SCLK	I²C Serial-Clock Input (MODE = 0). Connect a pullup resistor to DVDD for full output swing. SPI-compatible serial clock input (MODE = 1).
3	A2	X1	Crystal Oscillator Input. Connect load capacitor and one terminal of the crystal to this pin. Acceptable input frequency range: 10MHz to 30MHz.
4	A3	X2	Crystal Oscillator Output. Connect load capacitor and second terminal of the crystal to this pin.
5	B4	$\overline{\text{CS}}$	SPI-Compatible, Active-Low Chip-Select Input
6	B5	DOUT	SPI-Compatible Serial-Data Output
7	A5	MODE	I²C/SPI Mode Select Input (MODE = 0 for I²C mode, MODE = 1 for SPI mode)
8	A4	$\overline{\text{IRQ}}$	Hardware Interrupt Output. $\overline{\text{IRQ}}$ can be programmed to go low when bits in the status register 0x00 are set. Read status register 0x00 to clear $\overline{\text{IRQ}}$ once set. Repeat faults have no effect on $\overline{\text{IRQ}}$ until it is cleared by reading the I²C status register 0x00. Connect a 10kΩ pullup resistor to DVDD for full output swing.
9	A6	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
10	B6	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor (1.23V nominal).
11, 14, 28, 33, 35, 48	C4, D4, C5, D6	N.C.	No Connection. Connect to GND.
12	A7	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (1.6V nominal).
13	C6	REG	PREG/2 Voltage Reference. Bypass to AGND with a 1µF capacitor (0.8V nominal)
15	A8	AGND	Analog Ground
16	B7	MICVDD	Microphone Bias Power Supply. Bypass to AGND with a 1µF capacitor.
17	B8	MICBIAS	Low-Noise Microphone Bias. Connect a 2.2kΩ to 470Ω resistor to the positive output of the microphone. Bypass to AGND with a 1µF capacitor.
18	C7	MICLN/ DIGMICCLK	Left Negative Differential Microphone Input. AC-couple a microphone with a series 1µF capacitor. Also digital microphone clock output. Selectable through I²C.
19	D7	MICLP/ DIGMICDATA	Left Positive Differential Microphone Input. AC-couple a microphone with a series 1µF capacitor. Also digital microphone data input. Selectable through I²C.
20	C8	MICRP/ SPDMDATA	Right Positive Differential Microphone Input or SPDM Data Output. AC-couple a microphone with a series 1µF capacitor. Selectable through I²C.
21	D8	MICRN/ SPDMCLK	Right Negative Differential Microphone Input or SPDM Clock Output. AC-couple a microphone with a series 1µF capacitor. Selectable through I²C.
22	D5	JACKSNS/AUX	Jack Sense. Detects the presence or absence of a jack. See the *Headset Detection* section. When used as an auxiliary ADC input, AUX is used to measure DC voltages.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN-EP	WLP		
23	E8	LINL	Left-Line Input. AC-couple analog audio signal to LINL with a 1µF capacitor.
24	F8	LINR	Right-Line Input. AC-couple analog audio signal to LINR with a 1µF capacitor.
25	F7	LOUTR	Right-Line Output
26	E7	LOUTL	Left-Line Output
27	E6, F6	PGND	Headphone Power Ground
29	E5	ROUTP	Positive Right-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
30	F5	ROUTN	Negative Right-Channel Headphone Output. Unused in capacitorless and single-ended mode.
31	F4	LOUTN	Negative Left-Channel Headphone Output. Common headphone return in capacitorless mode. Unused in single-ended mode.
32	E4	LOUTP	Positive Left-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
34	E3, F3	PVDD	Headphone Power Supply. Bypass to PGND with a 1µF capacitor.
36	F2	DVDDS1	S1 Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
37	F1	SDOUTS1	S1 Digital Audio Serial-Data ADC Output
38	D3	SDINS1	S1 Digital Audio Serial-Data DAC Input
39	E1	LRCLKS1	S1 Digital Audio Left-Right Clock Input/Output. LRCLKS1 is the audio sample rate clock and determines whether the audio data on SDINS1 is routed to the left or right channel. In TDM mode, LRCLKS1 is a frame sync pulse. LRCLKS1 is an input when the MAX9880A is in slave mode and an output when in master mode.
40	E2	BCLKS1	S1 Digital Audio Bit Clock Input/Output. BCLKS1 is an input when the MAX9880A is in slave mode and an output when in master mode.
41	D1	MCLK	Master Clock Input. Acceptable input frequency range: 10MHz to 60MHz.
42	D2	SDOUTS2	S2 Digital Audio Serial-Data ADC Output
43	C1	SDINS2	S2 Digital Audio Serial-Data DAC Input
44	C2	LRCLKS2	S2 Digital Audio Left-Right Clock Input/Output. LRCLKS2 is the audio sample rate clock and determines whether the audio data on SDINS2 is routed to the left or right channel. In TDM mode, LRCLKS2 is a frame sync pulse. LRCLKS2 is an input when the MAX9880A is in slave mode and an output when in master mode.
45	C3	BCLKS2	S2 Digital Audio Bit Clock Input/Output. BCLKS2 is an input when the MAX9880A is in slave mode and an output when in master mode.
46	B1	DVDD	Digital Power Supply. Supply for the digital core and I²C/SPI interface. Bypass to DGND with a 1.0µF capacitor.
47	A1	DGND	Digital Ground
—	—	EP	Exposed Pad. Connect the exposed thermal pad to AGND.

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Detailed Description

The MAX9880A is a low-power stereo audio codec designed for portable applications requiring minimum power consumption.

The stereo playback path accepts digital audio through flexible digital audio interfaces compatible with I²S, TDM, and left-justified audio signals. The MAX9880A can process two simultaneous digital input streams that can be mixed digitally. The primary interface is intended for voiceband applications, while the secondary interface can be used for stereo audio data. An oversampling sigma-delta DAC converts the mixed incoming digital data stream to analog audio and outputs through the stereo headphone amplifier and stereo-line outputs. The headphone amplifier can be configured in differential, single-ended, and capacitorless output modes.

The stereo record path has two differential analog microphone inputs with selectable gain. The microphones are powered by an integrated microphone bias. The MAX9880A can retask the left analog microphone input to accept data from up to two digital microphones. An oversampling sigma-delta ADC converts the microphone signals and outputs the digital bit stream over the digital audio interface. An auxiliary ADC allows accurate measurements of DC voltages by retasking the right audio ADC. DC voltages can be read through the registers.

The MAX9880A also includes two line inputs. These inputs allow a stereo single-ended signal to be gain adjusted and then recorded by the ADCs and output by the headphone amplifier and line output amplifiers. A jack detection function allows the detection of headphone, microphone, and headset jacks. Insertion and removal events can be programmed to trigger a hardware interrupt and flag a register bit.

The MAX9880A's flexible clock circuitry utilizes a programmable clock divider and a digital PLL to allow the DAC and ADC to operate at maximum dynamic range for all combinations of master clock (MCLK) and sample rate (LRCLK) without consuming extra supply current. Any master clock between 10MHz and 60MHz is supported as are all sample rates from 8kHz to 48kHz for the record path and 8kHz to 96kHz for the playback path. Master and slave modes are supported for maximum flexibility.

The right analog microphone input can be retasked to output SPDM data. Integrated digital filtering provides a range of notch and highpass filters for both the playback and record paths to limit undesirable low-frequency signals and GSM transmission noise. The digital filtering provides attenuation of out-of-band energy by over 70dB, eliminating audible aliasing. A digital sidetone function allows audio from the record path to be summed into the playback path after digital filtering.

I²C/SPI Registers

Forty internal registers program and report the status of the MAX9880A. Table 1 lists all of the registers, their addresses, and power-on-reset states. Registers 0x00–0x03 are read-only while all of the other registers are read/write. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted. All bits in the read-only registers are not programmable. Read operations of unused bits return zero.

I²C Slave Address

The MAX9880A is preprogrammed with a slave address of 0x20 or 0010000. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX9880A to read mode. Set the read/write bit to zero to configure the MAX9880A to write mode. The address is the first byte of information sent to the MAX9880A after the START (S) condition.

Table 1. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)	POR STATE	R/W
STATUS											
Status	CLD	SLD	ULK	—	*	*	JDET	—	0x00	—	R
Jack Status	JKSNS[1:0]		—	—	—	—	—	—	0x01	—	R
AUX High	AUX[15:8]								0x02	—	R
AUX Low	AUX[7:0]								0x03	—	R
Interrupt Enable	ICLD	ISLD	IULK	0	0*	0*	IJDET	0	0x04	0x00	R/W
SYSTEM CLOCK CONTROL											
System Clock	0	0	PSCLK		FREQ1				0x05	0x00	R/W

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)	POR STATE	R/W
DAI1 CLOCK CONTROL											
Stereo Audio Clock Control High	PLL1	NI1[14:8]							0x06	0x00	R/W
Stereo Audio Clock Control Low	NI1[7:1]							RLK1/NI1[0]	0x07	0x00	R/W
DAI1 CONFIGURATION											
Interface Mode A	MAS1	WCI1	BCI1	DLY1	HIZOFF1	TDM1	FSW1	0	0x08	0x00	R/W
Interface Mode B	DL1	SEL1	SDOEN1	SDIEN1	DMONO1	BSEL1			0x09	0x00	R/W
Time-Division Multiplex	SLOTL1		SLOTR1		SLOTDLY1[3:0]				0x0A	0x00	R/W
DAI2 CLOCK CONTROL											
Stereo Audio Clock Control High	PLL2	NI2[14:8]							0x0B	0x00	R/W
Stereo Audio Clock Control Low	NI2[7:1]							RLK2/NI2[0]	0x0C	0x00	R/W
DAI2 CONFIGURATION											
Interface Mode A	MAS2	WCI2	BCI2	DLY2	HIZOFF2	TDM2	FSW2	WS2	0x0D	0x00	R/W
Interface Mode B	DL2	SEL2	SDOEN2	SDIEN2	DHF	BSEL2			0x0E	0x00	R/W
Time-Division Multiplex	SLOTL2		SLOTR2		SLOTDLY2[3:0]				0x0F	0x00	R/W
DIGITAL MIXERS											
DAC-L/R Mixer	MIXDAL				MIXDAR				0x10	0x00	R/W
DIGITAL FILTERING											
Codec Filters	MODE	AVFLT			DCB	DVFLT			0x11	0x00	R/W
SPDM OUTPUTS											
Configuration	SPDMCLK		SPDML	SPDMR	0	0	0	0	0x12	0x00	R/W
Input	MIXSPDML				MIXSPDMR				0x13	0x00	R/W
REVISION ID											
Rev ID location (replicated for SPI mode)	REV								0x14	0x42	R/W
LEVEL CONTROL											
Sidetone	DSTS		0	DVST					0x15	0x00	R/W
Stereo DAC Level	0	SDACM	0	0	SDACA				0x16	0x00	R/W
Voice DAC Level	0	VDACM	VDACG		VDACA				0x17	0x00	R/W
Left ADC Level	0	0	AVLG		AVL				0x18	0x00	R/W
Right ADC Level	0	0	AVRG		AVR				0x19	0x00	R/W
Left-Line Input Level	0	LILM	0	0	LIGL				0x1A	0x00	R/W
Right-Line Input Level	0	LIRM	0	0	LIGR				0x1B	0x00	R/W
Left Volume Control	0	VOLLM	VOLL						0x1C	0x00	R/W
Right Volume Control	0	VOLRM	VOLR						0x1D	0x00	R/W
Left-Line Output Level	0	LOLM	0	0	LOGL				0x1E	0x00	R/W
Right-Line Output Level	0	LORM	0	0	LOGR				0x1F	0x00	R/W
Left Microphone Gain	0	PALEN		PGAML					0x20	0x00	R/W
Right Microphone Gain	0	PAREN		PGAMR					0x21	0x00	R/W
CONFIGURATION											
Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x22	0x00	R/W
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	MBIAS	0x23	0x00	R/W
Mode	DSLEW	$\overline{\text{VSEN}}$	$\overline{\text{ZDEN}}$	0	0	HPMODE			0x24	0x00	R/W
Jack Detect	JDETEN	0	JDWK	0	0	0	JDEB		0x25	0x00	R/W

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)	POR STATE	R/W
POWER MANAGEMENT											
Enable	LNLEN	LNREN	LOLEN	LOREN	DALEN	DAREN	ADLEN	ADREN	0x26	0x00	R/W
System Shutdown	$\overline{\text{SHDN}}$	0	0	0	XTEN	$\overline{\text{XTOSC}}$	0	0	0x27	0x00	R/W
REVISION ID											
Revision ID	REV								0xFF	0x42	R/W

*Reserved.

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

Device Status

Status registers 0x00 and 0x01 are read-only registers that report the status of various device functions. The status register bits are cleared upon reading the status register and are set the next time the event occurs. Registers 0x02 and 0x03 report the DC level applied to AUX. See the *ADC* section for more details.

Bits in status register 0x00 are set when an alert condition exists. All bits in status register 0x00 are automatically cleared upon a read operation of the register and are set again if the condition remains or occurs following the read of this register.

Table 2. Status Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Status	CLD	SLD	ULK	—	*	*	JDET	—	0x00
Jack Status	JKSNS[1:0]		—	—	—	—	—	—	0x01
AUX High	AUX[15:8]								0x02
AUX Low	AUX[7:0]								0x03

*Reserved.

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

Table 3. Status Register Bits

BITS	FUNCTION	
CLD	**Clip Detect Flag**. Indicates that a signal has become clipped in the ADC or DAC. To resolve a clip condition in the signal path, the DAC gain settings and analog input gain settings should be lowered. As the CLD bit does not indicate where the overload has occurred, identify the source by lowering gains individually.	
SLD	**Slew Level Detect Flag**. When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value. SLD is also set when soft start or stop is complete.	
ULK	**Digital PLL Unlock Flag**. Indicates that the digital audio PLL has become unlocked and digital signal data is not reliable.	
JDET	**Headset Configuration Change Flag.** JDET reports changes in JKSNS[1:0]. Changes to JKSNS[1:0] are debounced before setting JDET. The debounce period is programmable using the JDEB bits.	
JKSNS[1:0]	JKSNS reports the status of the JACKSNS pin when JDETEN = 1. JKSNS is not debounced and should be interpreted according to the following information.	
	JKSNS[1:0]	**DESCRIPTION**
	00	JACKSNS is below V_{TH2}.
	01	JACKSNS is between V_{TH1} and V_{TH2}.
	10	Invalid.
	11	JACKSNS is above V_{TH1}.
AUX	**Auxiliary Input Measurement.** AUX is a 16-bit signed two's complement number representing the voltage measured at JACKSNS/AUX. Before reading a value from AUX, set AUXCAP to 1 to ensure a stable reading. After reading the value, set AUXCAP to 0. Use the following formula to convert the AUX value into an equivalent JACKSNS/AUX voltage: $\text{Voltage} = 0.738\text{V} \times \left(\frac{\text{AUX}}{\text{k}}\right)$ k = AUX value when AUXGAIN = 1. See AUXGAIN for details on determining the value of k, the calibration constant.	

Hardware Interrupts

Hardware interrupts are reported on the open-drain $\overline{IRQ}$ pin. When an interrupt occurs, $\overline{IRQ}$ remains low until the interrupt is serviced by reading the status register 0x00.

If a flag is set, it is reported as a hardware interrupt only if the corresponding interrupt enable is set. Each bit enables interrupts for the status flag in the respective bit location in register 0x00.

Table 4. Interrupt Enable

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Interrupt Enable	ICLD	ISLD	IULK	0	0*	0*	IJDET	0	0x04

*Reserved.

Grayed boxes = Not used.

***Note:** Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

Clock Control

The MAX9880A can work with a master clock (MCLK) supplied from any system clock within the 10MHz to 60MHz range. Internally the MAX9880A requires a 10MHz to 20MHz clock. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the MAX9880A.

The MAX9880A can support any sample rate from 8kHz to 48kHz for the digital audio path DAI1 (DAC and ADC) and 8kHz to 96kHz for the DAI2 (high-fidelity DAC path), including all common sample rates (8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 96kHz). To accommodate a wide range of system architectures, the MAX9880A supports three main clocking modes:

- **Normal mode:** This mode uses a 15-bit clock divider coefficient to set the sample rate relative to the prescaled MCLK input (PCLK). This allows high flexibility in both the MCLK and LRCLK frequencies and can be used in either master or slave mode.
- **Exact integer mode:** Common MCLK frequencies (12MHz, 13MHz, 16MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ1 bits instead of the NI high, NI low, and PLL control bits.
- **PLL mode:** When operating in slave mode, a PLL can be enabled to lock onto externally generated LRCLK signals that are not integer related to PCLK. Prior to enabling the interface, program NI to the nearest desired ratio and set the NI[0] = 1 to enable the PLL's rapid lock mode. If NI[0] = 0, then NI is ignored and PLL lock time is slower.

Table 5. System and Audio Clock Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
SYSTEM CLOCK CONTROL									
System Clock	0	0	PSCLK		FREQ1				0x05
DAI1 CLOCK CONTROL									
Stereo Audio Clock Control High	PLL1	NI1[14:8]							0x06
Stereo Audio Clock Control Low	NI1[7:1]							RLK1/NI1[0]	0x07
DAI2 CLOCK CONTROL									
Stereo Audio Clock Control High	PLL2	NI2[14:8]							0x0B
Stereo Audio Clock Control Low	NI2[7:1]							RLK2/NI2[0]	0x0C

Grayed boxes = Not used.

***Note:** Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

Table 5. System and Audio Clock Registers (continued)

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td>PSCLK</td><td colspan="4">MCLK Prescaler. Divides MCLK down to generate a PCLK between 10MHz and 20MHz.
00 = Disable clock for low-power shutdown.
01 = Select if MCLK is between 10MHz and 20MHz. PCLK = MCLK.
10 = Select if MCLK is between 20MHz and 40MHz. PCLK = MCLK/2.
11 = Select if MCLK is greater than 40MHz. PCLK = MCLK/4.</td></tr>
<tr><td rowspan="9">FREQ1</td><td colspan="4">Exact Integer Modes. Allows integer sampling for specific PCLK (prescaled MCLK) frequencies and 8kHz or 16kHz sample rates.</td></tr>
<tr><td>FREQ1[3:0]</td><td>PCLK (MHz)</td><td>LRCLK (kHz)</td><td>PCLK/LRCLK</td></tr>
<tr><td>0x00</td><td colspan="3">Normal or PLL mode</td></tr>
<tr><td>0x1–0x7</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0x8
0x9</td><td>12
12</td><td>8
16</td><td>1500
750</td></tr>
<tr><td>0xA
0xB</td><td>13
13</td><td>8
16</td><td>1625
812.5</td></tr>
<tr><td>0xC
0xD</td><td>16
16</td><td>8
16</td><td>2000
1000</td></tr>
<tr><td>0xE
0xF</td><td>19.2
19.2</td><td>8
16</td><td>2400
1200</td></tr>
<tr><td colspan="4">Modes 0x8 to 0xF are available in either master or slave mode. In slave mode, if the indicated PCLK/LRCLK ratio cannot be guaranteed, use PLL mode instead.</td></tr>
<tr><td>PLL1/PLL2</td><td colspan="4">PLL Mode Enable
0 = (Valid for slave and master mode) The frequency of LRCLK is set by the NI divider bits. In master mode, the MAX9880A generates LRCLK using the specified divide ratio. In slave mode, the MAX9880A expects an LRCLK as specified by the divide ratio.
1 = (Valid for slave mode only) A digital PLL locks on to any externally supplied LRCLK signal.</td></tr>
<tr><td>RLK1/RLK2</td><td colspan="4">Rapid Lock Mode. To enable rapid lock mode set NI_ to the nearest desired ratio and set RLK_ = 1 before enabling the interface.</td></tr>
<tr><td>NI1/NI2</td><td colspan="4">Normal Mode LRCLK Divider. When PLL = 0, the frequency of LRCLK is determined by NI. See Table 6 for common NI values.
For LRCLK = 8kHz to 48kHz operation (DHF = 0 for DAI2):
NI = (65,536 x 96 x f_{LRCLK})/f_{PCLK}
f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled internal MCLK frequency (PCLK)
For LRCLK > 50kHz operation (DHF = 1 for DAI2):
NI = (65,536 x 48 x f_{LRCLK})/f_{PCLK}
f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled internal MCLK frequency (PCLK)</td></tr>
</table>

Table 6. Common NI Values

LRCLK (kHz)		(DAI1, DAI2 for DHF = 0)									(DAI2 for DHF = 1)		
		8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**64**	**88.2**	**96**
PCLK (MHz): (Note: Any PCLK from 10MHz to 20MHz with any LRCLK 7.8kHz to 50kHz can be used.)	**10**	13A9	1B18	1D7E	2752	3631	3AFB	4EA5	6C61	75F7	4EA5	6C61	75F7
	11	11E0	18A2	1ACF	23BF	3144	359F	477E	6287	6B3E	477E	6287	6B3E
	11.2896	116A	**1800**	1A1F	22D4	**3000**	343F	45A9	**6000**	687D	45A9	**6000**	687D
	12	1062	1694	1893	20C5	2D29	3127	4189	5A51	624E	4189	5A51	624E
	12.288	**1000**	160D	**1800**	**2000**	2C1A	**3000**	**4000**	5833	**6000**	**4000**	5833	**6000**
	13	F20	14D8	16AF	1E3F	29AF	2D5F	3C7F	535F	5ABE	3C7F	535F	5ABE
	14	E0B	135B	1511	1C16	26B5	2A21	382C	4D6A	5443	382C	4D6A	5443
	15	D1B	1210	13A9	1A37	2420	2752	346E	4841	4EA5	346E	4841	4EA5
	16	C4A	10EF	126F	1893	21DE	24DD	3127	43BD	49BA	3127	43BD	49BA
	16.9344	B9C	**1000**	116A	1738	**2000**	22D4	2E71	**4000**	45A9	2E71	**4000**	45A9
	17	B91	FF0	1159	1721	1FE0	22B2	2E43	3FC1	4564	2E43	3FC1	4564
	18	AEC	F0E	1062	15D8	1E1B	20C5	2BB1	3C36	4189	2BB1	3C36	4189
	18.432	AAB	EB3	**1000**	1555	1D66	**2000**	2AAB	3ACD	**4000**	2AAB	3ACD	**4000**
	19	A59	E43	F86	14B2	1C85	1F0B	2964	390B	3E16	2964	390B	3E16
	20	9D5	D8C	EBF	13A9	1B18	1D7E	2752	3631	3AFB	2752	3631	3AFB

Note: *Values in bold and underline are exact integers that provide maximum full-scale performance.*

Digital Audio Interface

The MAX9880A's dual digital audio interface supports a wide range of operating modes to ensure maximum compatibility. See Figures 1 to 5 for timing diagrams. In master mode, the MAX9880A outputs LRCLK and BCLK, while in slave mode they are inputs. When operating in master mode, BCLK can be configured in a number of ways to ensure compatiblity with other audio devices.

The MAX9880A has two sets of digital audio interface pins, S1 and S2, that can be connected to one of two digital audio paths, DAI1 or DAI2.

DAI1: Digital Audio Path 1 Operation

- DAC path with DR of 90dB and ADC path with DR of 82dB
- DAC path connectable to either S1 or S2
- ADC path connectable to either S1 or S2
- 8kHz to 48kHz sample rates
- I^2S and TDM-compatible modes
- Voice filters or audio filter modes

DAI2: Digital Audio Path 2 Operation

- High-fidelity DAC path with DR of 96dB
- DAC path connectable to either S1 or S2
- 8kHz to 96kHz sample rates
- I^2S and TDM-compatible modes
- Audio FIR filters
- No ADC clock control from DAI2 sample clock and no voice filter modes available in DAI2

Table 7. Digital Audio Interface Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
DAI1 CONFIGURATION									
Interface Mode A	MAS1	WCI1	BCI1	DLY1	HIZOFF1	TDM1	FSW1	0	0x08
Interface Mode B	DL1	SEL1	SDOEN1	SDIEN1	DMONO1	BSEL1			0x09
Time-Division Multiplex	SLOTL1		SLOTR1		SLOTDLY1[3:0]				0x0A
DAI2 CONFIGURATION									
Interface Mode A	MAS2	WCI2	BCI2	DLY2	HIZOFF2	TDM2	FSW2	WS2	0x0D
Interface Mode B	DL2	SEL2	SDOEN2	SDIEN2	DHF	BSEL2			0x0E
Time-Division Multiplex	SLOTL2		SLOTR2		SLOTDLY2[3:0]				0x0F

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

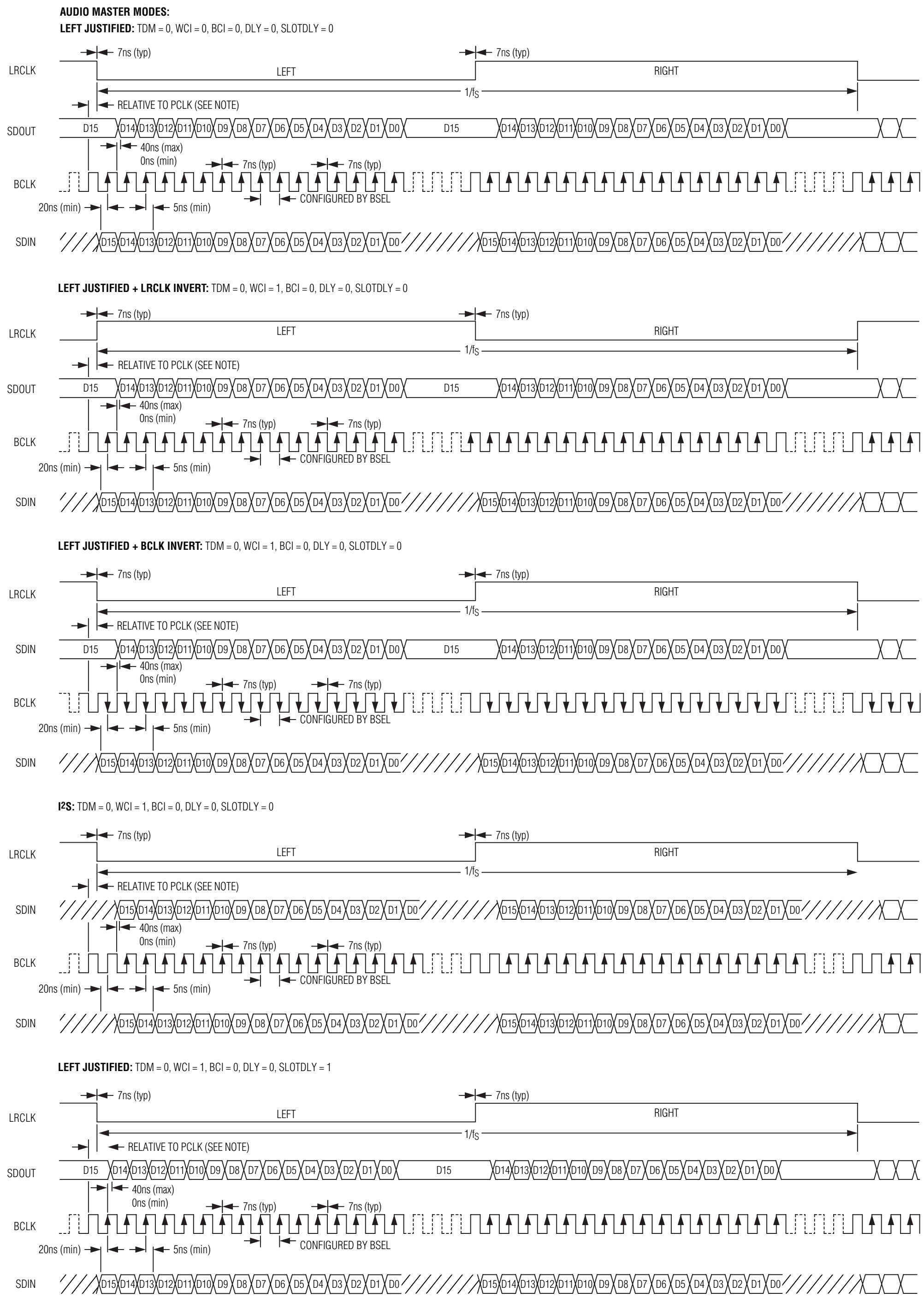
BITS	FUNCTION
MAS1/2	**Master Mode** 0 = The MAX9880A operates in slave mode with LRCLK and BCLK configured as inputs. 1 = The MAX9880A operates in master mode with LRCLK and BCLK configured as outputs.
WCI1/2	**LRCLK Invert (TDM1/2 = 0)** 0 = Left-channel data is input and output while LRCLK is low. 1 = Right-channel data is input and output while LRCLK is low.
BCI1/2	**BCLK Invert** In master and slave modes: 0 = SDIN is latched into the part on the rising edge of BCLK. SDOUT transitions immediately after the rising edge of BCLK. 1 = SDIN is latched into the part on the falling edge of BCLK. SDOUT transitions immediately after the falling edge of BCLK. In master mode: 0 = LRCLK changes state immediately after the rising edge of BCLK. 1 = LRCLK changes state immediately after the falling edge of BCLK.
DLY1/2	**Delay Mode.** DLY1/2 have two different functions in TDM and non-TDM mode. **In Non-TDM Mode (TDM1/TDM2 = 0):** The functionality is as follows: 1 = The most significant bit of an audio word is latched at the second BCLK edge after the LRCLK transition. 0 = The most significant bit of an audio word is latched at the first BCLK edge after the LRCLK transition. **In TDM Mode (TDM1/TDM2 = 1):** The functionality is as follows: 1 = The HOLD time on the SDOUT output is increased to be greater than 150ns. 0 = The HOLD time on the SDOUT output is the default (greater than 20ns but less than 150ns).
HIZOFF1/2	**SDOUT High-Impedance Mode** 0 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the MAX9880A, allowing SDOUT to be shared by other devices. 1 = SDOUT is set either high or low after all data bits have been transferred out of the MAX9880A. **Note:** High-impedance mode is intended for use when TDM = 1.

Table 7. Digital Audio Interface Registers (continued)

<table>
<tr><th>BITS</th><th>FUNCTION</th></tr>
<tr><td>TDM1/2</td><td>TDM Mode Select
1 = Enables time-division multiplex mode and configures the audio interface to accept PCM data.
0 = Disables time-division multiplex mode. LRCLK signal polarity indicates left and right audio.</td></tr>
<tr><td>FSW1/2</td><td>Frame Sync Width
1 = Frame sync pulse extended to the width of the entire 16-bit first slot 0 data word (TDM1/TDM2 = 1 only; SLOTDLY[0] must be 0 when FSW is set to 1).
0 = Frame sync pulse is 1 bit wide.</td></tr>
<tr><td>WS2</td><td>Word Size
0 = The number of bits per input data word sample is 16 bits, and at least 16 BCLKs per input word are required.
1 = The number of bits per input data word sample is 18 bits, and at least 18 BCLKs per input word transfer is required. These control bits are only recognized when TDM1/TDM2 are cleared to 0.</td></tr>
<tr><td>DL1/2</td><td>Data Loop. Enabling of these bits provides a bridge from one DAI interface to the other. Data format looping could occur in both directions simultaneously.
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>DL1 = 0</td><td>Normal operation</td></tr>
<tr><td>DL1 = 1, SEL2 = 1</td><td>Enables SDINS1 to SDOUTS2.</td></tr>
<tr><td>DL2 = 0</td><td>Normal operation</td></tr>
<tr><td>DL2 = 1, SEL1 = 0</td><td>Enables SDINS2 to SDOUTS1.</td></tr>
</table>
Note: The LRCLKS1 and LRCLKS2 interfaces must be identical.</td></tr>
<tr><td>SEL1/SEL2</td><td>Set the SEL1/2, SDOEN1/2, and SDIEN1/2 bits as shown in the table below to connect the S1 and S2 pins to the DAI1 and DAI2 paths in the MAX9880A.
<table>
<tr><th>SETTING</th><th>SEL1</th><th>SEL2</th><th>SDIEN1</th><th>SDOEN1</th><th>SDIEN2</th><th>SDOEN2</th></tr>
<tr><td>Connect S1 pins to DAI1 (DAC and ADC)</td><td>0</td><td>X</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Connect S2 pins to DAI1 (DAC and ADC)</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Connect S1 pins (DAC only) to DAI2</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Connect S2 pins (DAC only) to DAI2</td><td>X</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Connect S1 pins (DAC and ADC) to DAI1, connect S2 to DAI2 (DAC only)</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Connect S2 pins (DAC and ADC) to DAI1, connect S1 to DAI2 (DAC only)</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>SDOEN1/2</td><td>SDOUT Enable
1 = Serial-data output enabled on S1/S2 pins.
0 = Serial-data output disabled on S1/S2 pins.</td></tr>
<tr><td>SDIEN1/2</td><td>SDIN Enable
1 = Serial-data input to DAI1/2 audio path enabled.
0 = Serial-data input to DAI1/2 audio path disabled.</td></tr>
<tr><td>DMONO1</td><td>Mono Playback Mode
0 = Stereo data input on DAI1 path is processed separately.
1 = Stereo data input on DAI1 path is mixed to a single channel and routed to both the left and right DAC.
When operating in mono voice mode (MODE = 1), stereo data may still be input through DAI1 path and optionally mixed using DMONO1 = 1.</td></tr>
</table>

Table 7. Digital Audio Interface Registers (continued)

BITS	FUNCTION	
BSEL1/2	**BCLK Select.** Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices.	
	BSEL	**DESCRIPTION**
	000	Off (BCLK output held low)
	001	64x LRCLK (192x internal clock divided by 3)
	010	48x LRCLK (192x internal clock divided by 4)
	011	128x LRCLK (**Note:** Not a valid BSEL2 choice when DHF = 1.)
	100	PCLK/2
	101	PCLK/4
	110	PCLK/8
	111	PCLK/16
SLOTL1/2 SLOTR1/2	**TDM Slot Select.** Selects the time slot to use for left/right data according to the following information when operating in time-division multiplex mode.	
	SLOT	**DESCRIPTION**
	00	Time slot 1
	01	Time slot 2
	10	Time slot 3
	11	Time slot 4
SLOTDLY1/2	**Slot Data Delay (SLOTDLY1/SLOTDLY2)** **In TDM Mode:** Configures the data delay for each slot in TDM mode of operation according to the following information. **In Non-TDM Mode (TDM = 0):** SLOTDLY[1:0] does not have any effect.	
	SLOTDLY1/2[3:0]	**DESCRIPTION**
	0xxx	Data for slot 4 begins immediately.
	1xxx	Data for slot 4 delayed 1 BCLK cycle.
	x0xx	Data for slot 3 begins immediately.
	x1xx	Data for slot 3 delayed 1 BCLK cycle.
	xx0x	Data for slot 2 begins immediately.
	xx1x	Data for slot 2 delayed 1 BCLK cycle.
	xxx0	Data for slot 1 begins immediately.
	xxx1	Data for slot 1 delayed 1 BCLK cycle (not valid when FSW = 1).
DHF	**DAC High Sample Rate Mode (DHF) (Valid only for DAI2 audio path)** 1 = LRCLK is greater than 50kHz. 4x FIR interpolation filter used. 0 = LRCLK is less than 50kHz. 8x FIR interpolation filter used.	



NOTE: THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED-DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF f_{PCLK} = 12.288MHz, THEN THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45ns.

Figure 1. Digital Audio Interface Audio Master Mode

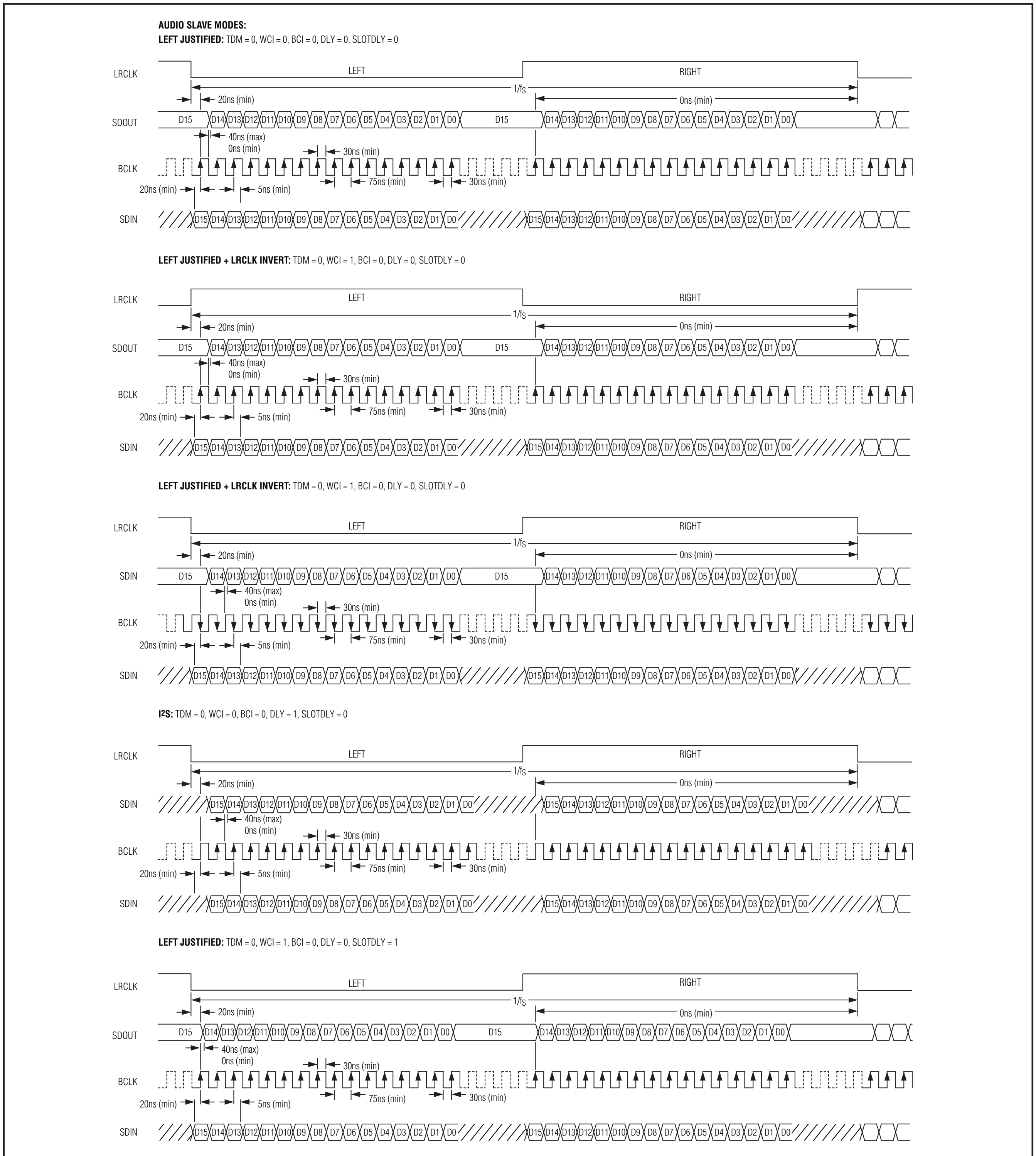


Figure 2. Digital Audio Interface Audio Slave Mode

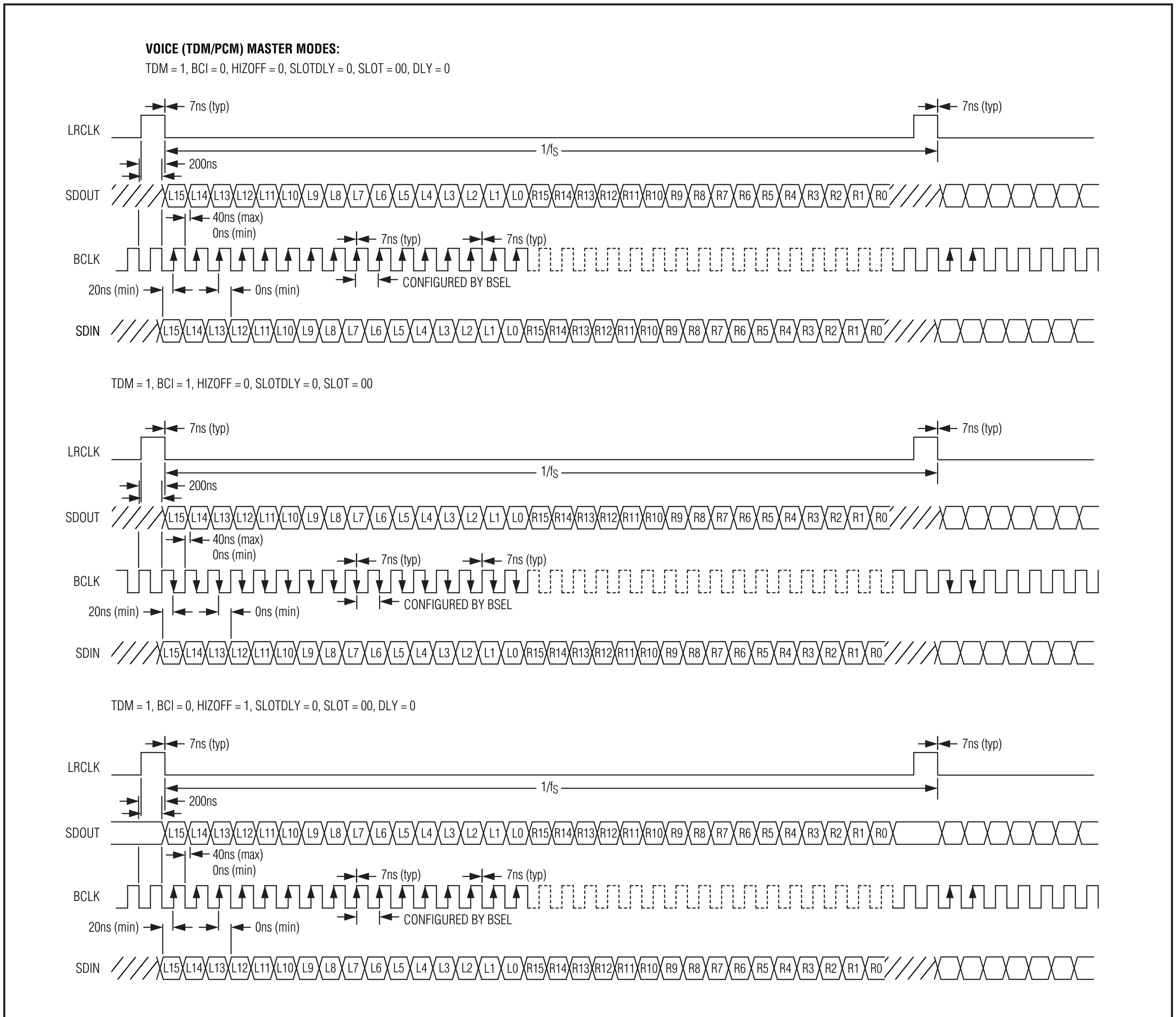


Figure 3. Digital Audio Interface Voice Master Mode

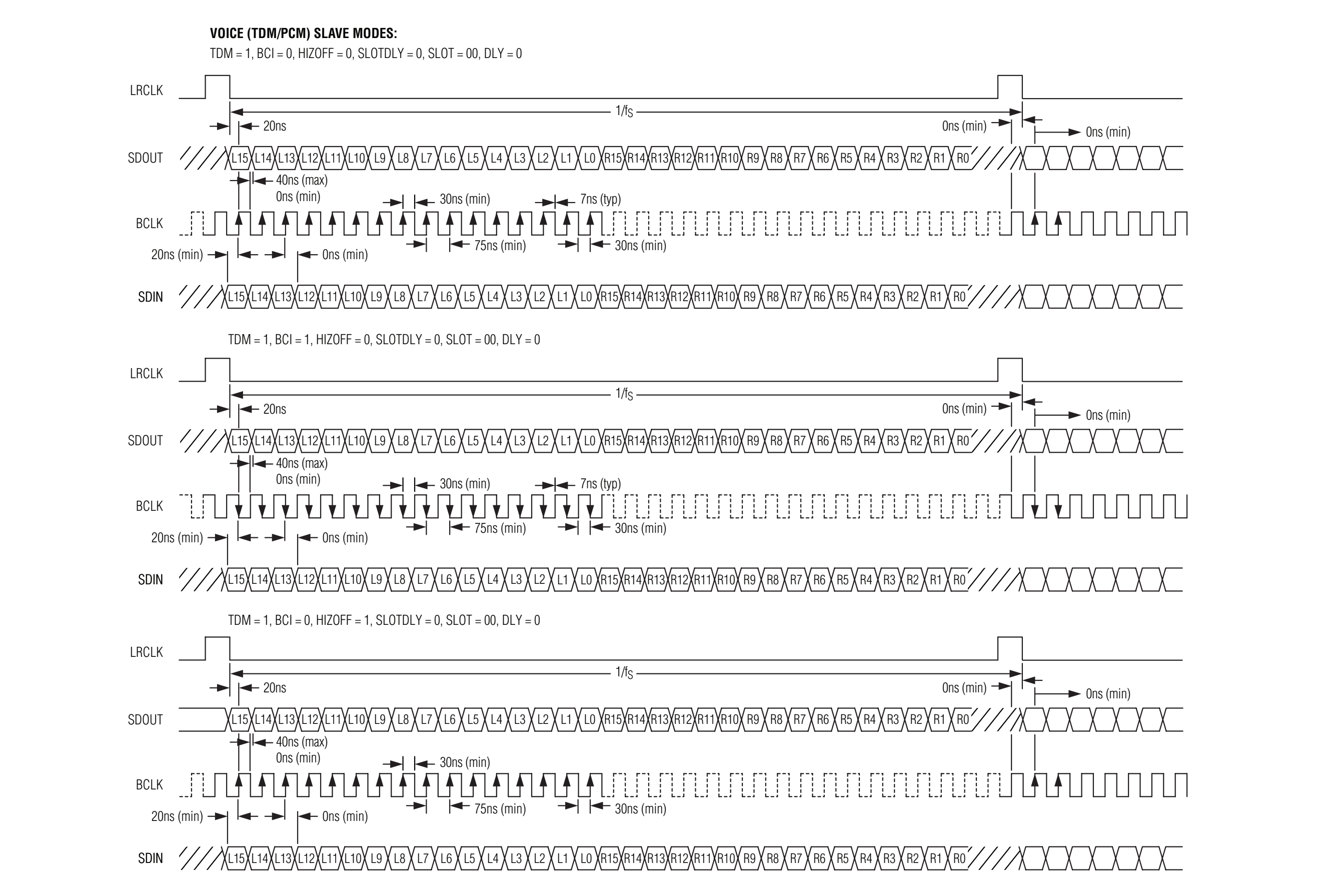


Figure 4. Digital Audio Interface Voice Slave Mode

Table 8. Digital Mixers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
DIGITAL MIXERS									
DAC-L/R Mixer	MIXDAL				MIXDAR				0x10

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION	
MIXDAL/ MIXDAR	**Digital Mixers (MIXDAL/MIXDAR).** Selects and mixes the audio source(s) for the DACs according to the information below.	
	MIXDAL/MIXDAR	**SOURCE**
	1xxx	DAI1 left-channel data
	x1xx	DAI1 right-channel data
	xx1x	DAI2 left-channel data
	xxx1	DAI2 right-channel data

Digital Filtering

The MAX9880A incorporates both IIR (voice) and FIR (audio) digital filters to accomodate a wide range of audio sources. The IIR fiilters provide over 70dB of stopband attenuation as well as selectable highpass filters. The FIR filters provide low power consumption and are linear phase to maintain stereo imaging.

Table 9. Digital Filtering Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
DIGITAL FILTERING									
Codec Filters	MODE	AVFLT			DCB	DVFLT			0x11

Note: *Register addresses listed are for I^2C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
MODE	**Digital Audio Filter Mode.** Selects the filtering mode for the DAI1 DAC and ADC signal paths. 0 = IIR voice filters 1 = FIR audio filters
AVFLT	**ADC Digital Audio Filter.** Configures the highpass filters for the DAI1 signal path. **MODE = 0** Select the desired digital filter response from Table 10. See the frequency response graphs in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter disabled. 0x1 = DC-blocking filter enabled.
DCB	1 = DC-blocking filter for DAI2 enabled. 0 = DC-blocking filter for DAI2 disabled.
DVFLT	**DAC Digital Audio Filter.** Configures the highpass filters for the DAI1 signal path. **MODE = 0** Select the desired digital filter response from Table 10. See the frequency response graphs in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter disabled. 0x1 = DC-blocking filter enabled.

Table 10. IIR Highpass Digital Filters

CODE	FILTER TYPE	VALID SAMPLE RATE (kHz)	HIGHPASS CORNER FREQUENCY	217Hz NOTCH
0x0	Disabled			
0x1	Elliptical	16	256Hz	Yes
0x2	Butterworth	16	500Hz	No
0x3	Elliptical	8	256Hz	Yes
0x4	Butterworth	8	500Hz	No
0x5	Butterworth	8 to 24	$f_S/240$	No
0x6 to 0x7	Reserved			

Table 11. SPDM Output Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Configuration	SPDMCLK		SPDML	SPDMR	0	0	0	0	0x12
Input	MIXSPDML				MIXSPDMR				0x13

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

The MAX9880A supports stereo PDM outputs. The PDM signals consist of PDM data outputs (SPDMDATA) and a clock output (SPDMCLK). The mixer at the input to the PDM modulators allows a mix/mux of the audio digital data stream from the digital audio ports SDINS1 and SDINS2. Figure 5 shows the SPDM interface timing diagram.

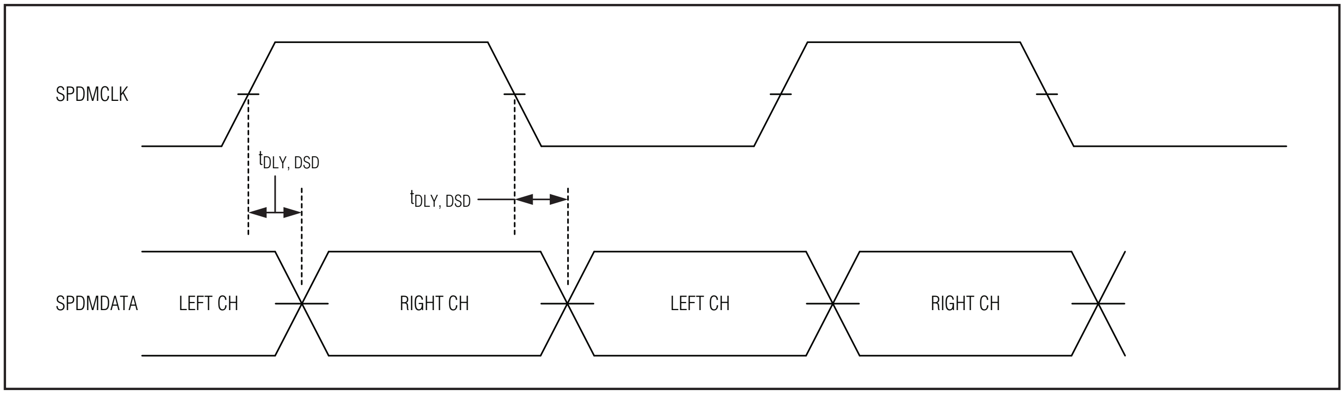


Figure 5. SPDM Timing Diagram

<table>
<tr><th>BITS</th><th colspan="2">FUNCTION</th></tr>
<tr><td>SPDMCLK</td><td colspan="2">SPDM Clock Rate (SPDMCLK)
00 = SPDMCLK is set to PCLK/8.
01 = SPDMCLK is set to PCLK6.
10 = SPDMCLK is set to PCLK/4.
11 = Reserved</td></tr>
<tr><td>SPDML/SPDMR</td><td colspan="2">0 = Disables SPDM data.
1 = Enables SPDM data.</td></tr>
<tr><td rowspan="6">MIXSPDML/
MIXSPDMR</td><td colspan="2">SPDM Input Mixers. Selects and mixes the audio source(s) for the SPDM output according to following information.</td></tr>
<tr><td>MIXSPDML/MIXSPDMR</td><td>SOURCE</td></tr>
<tr><td>1xxx</td><td>DAI1 left-channel data</td></tr>
<tr><td>x1xx</td><td>DAI1 right-channel data</td></tr>
<tr><td>xx1x</td><td>DAI2 left-channel data</td></tr>
<tr><td>xxx1</td><td>DAI2 right-channel data</td></tr>
</table>

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Digital Gain Control

The MAX9880A includes gain adjustment for the playback and record paths. Independent gain adjustment is provided for the two record channels. Sidetone gain adjustment is also provided to set the sidetone level relative to the playback level.

Table 12. Digital Gain Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
LEVEL CONTROL									
Sidetone	DSTS		0	DVST					0x15
Stereo DAC Level	0	SDACM	0	0	SDACA				0x16
Voice DAC Level	0	VDACM	VDACG		VDACA				0x17
Left ADC Level	0	0	AVLG		AVL				0x18
Right ADC Level	0	0	AVRG		AVR				0x19

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
DSTS	**Digital Sidetone Source Mixer** 00 = No sidetone selected. 01 = Left ADC 10 = Right ADC 11 = Left and right ADC
DVST	**Digital Sidetone Level Control.** All gain settings are relative to the ADC input voltage.

Differential Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-20	0x16	-42
0x01	0	0x0C	-22	0x17	-44
0x02	-2	0x0D	-24	0x18	-46
0x03	-4	0x0E	-26	0x19	-48
0x04	-6	0x0F	-28	0x1A	-50
0x05	-8	0x10	-30	0x1B	-52
0x06	-10	0x11	-32	0x1C	-54
0x07	-12	0x12	-34	0x1D	-56
0x08	-14	0x13	-36	0x1E	-58
0x09	-16	0x14	-38	0x1F	-60
0x0A	-18	0x15	-40	—	—

Capacitorless and Single-Ended Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-25	0x16	-47
0x01	-5	0x0C	-27	0x17	-49
0x02	-7	0x0D	-29	0x18	-51
0x03	-9	0x0E	-31	0x19	-53
0x04	-11	0x0F	-33	0x1A	-55
0x05	-13	0x10	-35	0x1B	-57
0x06	-15	0x11	-37	0x1C	-59
0x07	-17	0x12	-39	0x1D	-61
0x08	-19	0x13	-41	0x1E	-63
0x09	-21	0x14	-43	0x1F	-65
0x0A	-23	0x15	-45	—	—

Table 12. Digital Gain Registers (continued)

BITS	FUNCTION			
SDACM/ VDACM	**DAC Mute Enable** 0 = No mute 1 = Mute			
VDACG	**DAC Gain** 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB **Note:** VDACG is only used when MODE = 0. If MODE = 1, then the DAC gain is always 0dB.			
VDACA/SDACA	**DAC Level Control.** VDACA/SDACA works in all modes.			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	0	0x8	-8
	0x1	-1	0x9	-9
	0x2	-2	0xA	-10
	0x3	-3	0xB	-11
	0x4	-4	0xC	-12
	0x5	-5	0xD	-13
	0x6	-6	0xE	-14
	0x7	-7	0xF	-15
AVLG/AVRG	**ADC Gain Control.** Applies the specified gain to the digital ADC paths according to the following information.			
	SETTING	**GAIN (dB)**		
	0x0	0		
	0x1	+6		
	0x2	+12		
	0x3	+18		
AVL/AVR	**ADC Left/Right Level Control**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	+3	0x8	-5
	0x1	+2	0x9	-6
	0x2	+1	0xA	-7
	0x3	0	0xB	-8
	0x4	-1	0xC	-9
	0x5	-2	0xD	-10
	0x6	-3	0xE	-11
	0x7	-4	0xF	-12

Line Inputs

The MAX9880A include one pair of single-ended line inputs. When enabled the line inputs connect directly to the headphone amplifier and line outputs and can be optionally connected to the ADC for recording.

Playback Volume

The MAX9880A incorporates volume and mute control to allow level control for the playback audio path. Program registers 0x1C and 0x1D to set the desired volume.

Line Output Level

The MAX9880A incorporates gain and mute control to allow level control for the line outputs.

Table 13. Line Input Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Left-Line Input Level	0	LILM	0	0	LIGL				0x1A
Right-Line Input Level	0	LIRM	0	0	LIGR				0x1B

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION			
LILM/LIRM	**Line Input Left/Right Playback Mute** 0 = Line input is connected to the headphone amplifiers. 1 = Line input is disconnected from the headphone amplifiers.			
LIGL/LIGR	**Line Input Left/Right Gain**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	+24	0x8	+8
	0x1	+22	0x9	+6
	0x2	+20	0xA	+4
	0x3	+18	0xB	+2
	0x4	+16	0xC	0
	0x5	+14	0xD	-2
	0x6	+12	0xE	-4
	0x7	+10	0xF	-6

Table 14. Playback Volume Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Left Volume Control	0	VOLLM	VOLL						0x1C
Right Volume Control	0	VOLRM	VOLR						0x1D

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
VOLLM/ VOLRM	**Left/Right Playback Mute.** VOLLM and VOLRM mute both the DAC and line input audio signals. 0 = Audio playback is unmuted. 1 = Audio playback is muted. **Note:** $\overline{\text{VSEN}}$ has no effect on the mute function. When VOLLM or VOLRM is set, the output is muted immediately ($\overline{\text{ZDEN}}$ = 1) or at the next zero-crossing ($\overline{\text{ZDEN}}$ = 0).

Table 14. Playback Volume Registers (continued)

<table>
<tr><th>BITS</th><th colspan="6">FUNCTION</th></tr>
<tr><td rowspan="17">VOLL/VOLR</td><td colspan="6">Left/Right Playback Volume. VOLL and VOLR control the playback volume for both the DAC and line input audio signals.</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+9</td><td>0x0E</td><td>-2</td><td>0x1C</td><td>-39</td></tr>
<tr><td>0x01</td><td>+8.5</td><td>0x0F</td><td>-3</td><td>0x1D</td><td>-43</td></tr>
<tr><td>0x02</td><td>+8</td><td>0x10</td><td>-5</td><td>0x1E</td><td>-47</td></tr>
<tr><td>0x03</td><td>+7.5</td><td>0x11</td><td>-7</td><td>0x1F</td><td>-51</td></tr>
<tr><td>0x04</td><td>+7</td><td>0x12</td><td>-9</td><td>0x20</td><td>-55</td></tr>
<tr><td>0x05</td><td>+6.5</td><td>0x13</td><td>-11</td><td>0x21</td><td>-59</td></tr>
<tr><td>0x06</td><td>+6</td><td>0x14</td><td>-13</td><td>0x22</td><td>-63</td></tr>
<tr><td>0x07</td><td>+5</td><td>0x15</td><td>-15</td><td>0x23</td><td>-67</td></tr>
<tr><td>0x08</td><td>+4</td><td>0x16</td><td>-17</td><td>0x24</td><td>-71</td></tr>
<tr><td>0x09</td><td>+3</td><td>0x17</td><td>-19</td><td>0x25</td><td>-75</td></tr>
<tr><td>0x0A</td><td>+2</td><td>0x18</td><td>-23</td><td>0x26</td><td>-79</td></tr>
<tr><td>0x0B</td><td>+1</td><td>0x19</td><td>-27</td><td>0x27</td><td>-81</td></tr>
<tr><td>0x0C</td><td>0</td><td>0x1A</td><td>-31</td><td rowspan="2">0x28 to 0x3F</td><td rowspan="2">MUTE</td></tr>
<tr><td>0x0D</td><td>-1</td><td>0x1B</td><td>-35</td></tr>
<tr><td colspan="6">Note: Gain settings apply when the headphone amplifier is configured in differential mode. In the single-ended and capacitorless modes, the actual gain is 5dB lower. Assuming LOGL/LOGR = 0dB, line output gain is 6dB lower.</td></tr>
</table>

Table 15. Output Line-Level Registers

<table>
<tr><th>REGISTER</th><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th><th>REGISTER ADDRESS (SEE NOTE)</th></tr>
<tr><td>Left-Line Output Level</td><td>0</td><td>LOLM</td><td>0</td><td>0</td><td colspan="4">LOGL</td><td>0x1E</td></tr>
<tr><td>Right-Line Output Level</td><td>0</td><td>LORM</td><td>0</td><td>0</td><td colspan="4">LOGR</td><td>0x1F</td></tr>
</table>

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td>LOLM/LORM</td><td colspan="4">Left/Right Line Output Mute. LOLM and LORM mute both the DAC and line input audio signals.
0 = Line output is unmuted.
1 = Line output is muted.
Note: $\overline{\text{VSEN}}$ has no effect on the mute function. When LOLM or LORM is set the output is muted immediately ($\overline{\text{ZDEN}}$ = 1) or at the next zero-crossing ($\overline{\text{ZDEN}}$ = 0).</td></tr>
<tr><td rowspan="10">LOGL/LOGR</td><td colspan="4">Left/Right Line Output Gain. LOGL and LOGR set the line output gain according to the following information.</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>0</td><td>0x08</td><td>-16</td></tr>
<tr><td>0x01</td><td>-2</td><td>0x09</td><td>-18</td></tr>
<tr><td>0x02</td><td>-4</td><td>0x0A</td><td>-20</td></tr>
<tr><td>0x03</td><td>-6</td><td>0x0B</td><td>-22</td></tr>
<tr><td>0x04</td><td>-8</td><td>0x0C</td><td>-24</td></tr>
<tr><td>0x05</td><td>-10</td><td>0x0D</td><td>-26</td></tr>
<tr><td>0x06</td><td>-12</td><td>0x0E</td><td>-28</td></tr>
<tr><td>0x07</td><td>-14</td><td>0x0F</td><td>-30</td></tr>
</table>

Microphone Inputs

Two differential microphone inputs and a low noise 1.5V microphone bias for powering the microphones are provided by the MAX9880A. In typical applications, the left microphone records a voice signal and the right microphone records a background noise signal. In applications that require only one microphone, use the left microphone input and disable the right ADC. The microphone signals are amplified by two stages of gain and then routed to the ADCs. The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes. See Figure 6 for a detailed diagram of the microphone input structure.

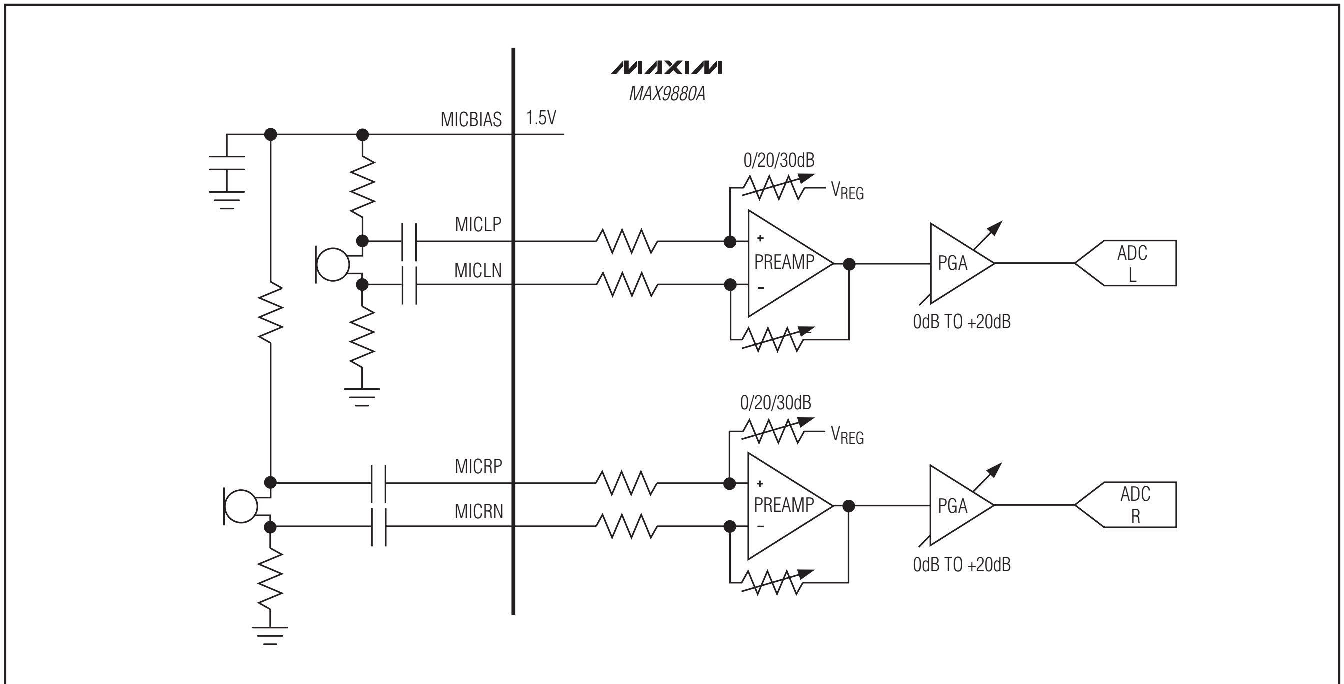


Figure 6. Microphone Input Block Diagram

Table 16. Microphone Input Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Left Microphone Gain	0	PALEN		PGAML					0x20
Right Microphone Gain	0	PAREN		PGAMR					0x21

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
PALEN/ PAREN	**Left/Right Microphone Preamplifier Gain.** Enables the microphone circuitry and sets the preamplifier gain. 00 = Disabled 01 = 0dB 10 = +20dB 11 = +30dB

Table 16. Microphone Input Registers (continued)

BITS	FUNCTION			
	Left/Right Microphone Programmable Gain Amplifier			
	SETTING	GAIN (dB)	SETTING	GAIN (dB)
PGAML/ PGAMR	0x00	+20	0x0B	+9
	0x01	+19	0x0C	+8
	0x02	+18	0x0D	+7
	0x03	+17	0x0E	+6
	0x04	+16	0x0F	+5
	0x05	+15	0x10	+4
	0x06	+14	0x11	+3
	0x07	+13	0x12	+2
	0x08	+12	0x13	+1
	0x09	+11	0x14 to 0x1F	0
	0x0A	+10		

ADC

The MAX9880A includes two 18-bit ADCs. The first ADC is used to record left-channel microphone and line-input audio signals. The second ADC can be used to record right-channel microphone and line-input signals or it can be configured to accurately measure DC voltages.

When measuring DC voltages both the left and right ADC must be enabled by setting ADLEN and ADREN in register 0x26. The input to the second ADC is JACKSNS/AUX and the output is reported in AUX (registers 0x02 and 0x03). Since the audio ADC is used to perform the measurement, the digital audio interface must be properly configured. If the left ADC is being used to convert audio, then the DC measurement is performed at the same sample rate. When not using the left ADC, configure the digital interface for a 48kHz sample rate to ensure the fastest possible settling time.

To ensure accurate results, the MAX9880A includes two calibration routines. Calibrate the ADC each time the MAX9880A is powered on. Calibration settings are not lost if the MAX9880A is placed in shutdown. When making a measurement, set AUXCAP to 1 to prevent AUX from changing while reading the registers.

Setup Procedure

1) Ensure a valid MCLK signal is provided and configure PSCLK appropriately.
2) Choose a clocking mode. The following options are possible:
   a. **Slave mode with LRCLK and BCLK signals provided.** The measurement sample rate is determined by the external clocks.
   b. **Slave mode with no LRCLK and BCLK signals provided.** Configure the device for normal clock mode using the NI ratio. Select f_S = 48kHz to allow for the fastest settling times.
   c. **Master mode with audio.** Configure the device in normal mode using the NI ratio or exact integer mode using FREQ1 as required by the audio signal.
   d. **Master mode without audio.** Configure the device in normal mode using the NI ratio. Select f_S = 48kHz to allow for the fastest settling times.
3) Ensure jack sense is disabled.
4) Enable the left and right ADC; take the MAX9880A out of shutdown.

Offset Calibration Procedure

Perform before the first DC measurement is taken after applying power to the MAX9880A.

1) Enable the AUX input (AUXEN = 1).
2) Enable the offset calibration (AUXCAL = 1).
3) Wait the appropriate time (see Table 17).
4) Complete calibration (AUXCAL = 0).

Gain Calibration Procedure

Perform the first time a DC measurement is taken after applying power to the MAX9880A or if the temperature changes significantly.

1) Enable the AUX input (AUXEN = 1).
2) Start gain calibration (AUXGAIN = 1).
3) Wait the appropriate time (see Table 17).
4) Freeze the measurement results (AUXCAP = 1).
5) Read AUX and store the value in memory to correct all future measurements (k = AUX[15:0], k is typically 19,500).
6) Complete calibration (AUXGAIN = AUXCAP = 0).

DC Measurement Procedure

Perform after offset and gain calibration are complete.

1) Enable the AUX input (AUXEN = 1).
2) Wait the appropriate time (see Table 17).
3) Freeze the measurement results (AUXCAP = 1).
4) Read AUX and correct with the gain calibration value
$$\left(V_{AUX} = 0.738\left(\frac{AUX[15:0]}{k}\right)\right).$$
5) Complete measurement (AUXCAP = 0).

Complete DC Measurement Example

f_{MCLK} = 13MHz, slave mode, BCLK, and LRCLK are not externally supplied.

1) Configure the digital audio interface for f_S = 48kHz (PSCLK = 01, FREQ1 = 0x0, PLL = 0, NI = 0x5ABE, MAS = 0).
2) Disable jack sense (JDETEN = 0).
3) Enable the left and right ADC; take the MAX9880A out of shutdown (ADLEN = ADREN = $\overline{SHDN}$ = 1).
4) Calibrate the offset:
   a. Enable the AUX input (AUXEN = 1).
   b. Enable the offset calibration (AUXCAL = 1).
   c. Wait 40ms.
   d. Complete calibration (AUXCAL = 0).
5) Calibrate the gain:
   a. Start gain calibration (AUXGAIN = 1).
   b. Wait 40ms.
   c. Freeze the measurement results (AUXCAP = 1).
   d. Read AUX and store the value in memory to correct all future measurements (k = AUX[15:0]).
   e. Complete calibration (AUXGAIN = AUXCAP = AUXEN = 0).
6) Measure the voltage on JACKSNS/AUX.
   a. Enable the AUX input (AUXEN = 1).
   b. Wait 40ms.
   c. Freeze the measurement results (AUXCAP = 1).
   d. Read AUX and correct with the gain calibration value.
   e. Complete measurement (AUXCAP = 0).
7) DC measurement is complete.

Table 17. AUX ADC Wait Times

LRCLK (kHz)	WAIT TIME (ms)
48	40
44.1	44
32	60
24	80
22.05	90
16	120
12	160
11.025	175
8	240

Table 18. ADC Input Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x22

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
MXINL/MXINR	**Left/Right ADC Audio Input Mixer** 00 = No input selected 01 = Left/right analog microphone 10 = Left/right line input 11 = Left/right analog microphone + line input **Note:** If the right line input is disabled, then the left line input is connected to both mixers. Enabling the left and right digital microphones disables the left and right audio mixer, respectively. See the DIGMICL/DIGMICR bit description for more details.
AUXCAP	**Auxiliary Input Capture** 0 = Update AUX with the voltage at JACKSNS/AUX. 1 = Hold AUX for reading.
AUXGAIN	**Auxiliary Input Gain Calibration** 0 = Normal operation 1 = The input buffer is disconnected from JACKSNS/AUX and connected to an internal voltage reference. While in this mode, read the AUX register and store the value. Use the stored value as a gain calibration factor, k, on subsequent readings. AUXCAL must remain set for time indicated in Table 17 to guarantee an accurate offset calibration.
AUXCAL	**Auxiliary Input Offset Calibration** 0 = Normal operation 1 = JACKSNS/AUX is disconnected from the input and the ADC automatically calibrates out any internal offsets. AUXCAL must remain set for time indicated in Table 17 to guarantee an accurate offset calibration.
AUXEN	**Auxiliary Input Enable** 0 = Use JACKSNS/AUX for jack detection. 1 = Use JACKSNS/AUX for DC measurements. **Note:** Set MXINR = 00, ADLEN = 1, and ADREN = 1 when AUXEN = 1.

Digital Microphone Input

The MAX9880A can accept audio from up to two digital microphones. When using digital microphones, the left analog microphone input is retasked as a digital microphone input. The right analog microphone input is still available to allow a combination of analog and digital microphones to be used. Figure 7 shows the digital microphone interface timing diagram.

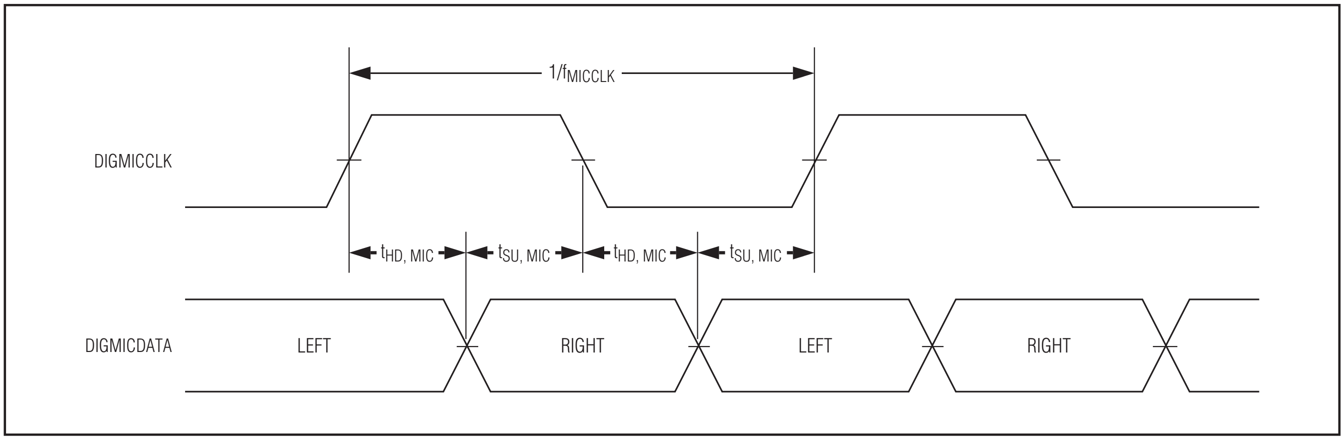


Figure 7. Digital Microphone Timing Diagram

Table 19. Digital Microphone Input Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	MBIAS	0x23

Grayed boxes = Not used.

***Note:** Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td>MICCLK</td><td colspan="4">Digital Microphone Clock
00 = PCLK/8
01 = PCLK/6
10 = 64f_S (high jitter clock)
11 = Reserved</td></tr>
<tr><td rowspan="7">DIGMICL/
DIGMICR</td><td colspan="4">Digital Left/Right Microphone Enable</td></tr>
<tr><td>DIGMICL</td><td>DIGMICR</td><td>LEFT ADC INPUT</td><td>RIGHT ADC INPUT</td></tr>
<tr><td>0</td><td>0</td><td>ADC input mixer</td><td>ADC input mixer</td></tr>
<tr><td>0</td><td>1</td><td>Line input (left analog microphone unavailable)</td><td>Right digital microphone</td></tr>
<tr><td>1</td><td>0</td><td>Left digital microphone</td><td>ADC input mixer</td></tr>
<tr><td>1</td><td>1</td><td>Left digital microphone</td><td>Right digital microphone</td></tr>
<tr><td colspan="4">Note: The left analog microphone input is never available when DIGMICL or DIGMICR = 1.</td></tr>
<tr><td>MBIAS</td><td colspan="4">Microphone Bias Output Voltage
Set MBIAS = 0 for nominal output of 1.52V (V_{MICVDD} = 1.8V)
Set MBIAS = 1 for nominal output of 2.2V (V_{MICVDD} = 3V)</td></tr>
</table>

Mode Configuration

The MAX9880A includes circuitry to minimize click-and-pop during volume changes, detect headsets, and configure the headphone amplifier mode. Both volume slewing and zero-crossing detection are included to ensure click-and-pop free volume transitions.

Headset Detection Overview

The MAX9880A contains headset detect circuitry that is capable of detecting the insertion or removal of a plug and providing information to assist the system controller in determining the configuration of an inserted plug. If programmed to do so, upon insertion or removal of a plug, the $\overline{IRQ}$ output is asserted (pulled low).

Table 20 shows the registers associated with the jack detect function in MAX9880A.

Table 20. Jack-Detect Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POR STATE	R/W
Status	CLD	SLD	ULK	—	*	*	JDET	—	0x00	—	R
Jack Status	JKSNS[1:0]		—	—	—	—	—	—	0x01	—	R
Interrupt Enable	ICLD	ISLD	IULK	0	0*	0*	IJDET	0	0x04	0x00	R/W
Jack Detect	JDETEN	0	JDWK	0	0	0	JDEB		0x25	0x00	R/W

Grayed boxes = Not used.

Jack Configuration Change Flag (JDET)

1 = Jack configuration has changed.

0 = No change in jack configuration.

JDET reports changes in JKSNS[1:0]. Changes to JKSNS[1:0] are debounced before setting JDET. The debounce period is programmable using the JDEB bits. Jack status register 0x01 is a read-only register that reports the status of the jack-detect circuitry when enabled.

Jack Sense (JKSNS)

JKSNS[1:0] reports the status of the JACKSNS pin when JDETEN = 1. JKSNS[1:0] should be interpreted according to Table 21.

Jack-Detect Interrupt Enable (IJDET)

Hardware interrupts are reported on the open-drain $\overline{IRQ}$ pin. When an interrupt occurs, $\overline{IRQ}$ remains low until the interrupt is serviced by reading the status register 0x00. If a flag is set, it is reported as a hardware interrupt only if the corresponding interrupt enable is set. Each bit enables interrupts for the status flag in the respective bit location in register 0x00. So IJDET must be set to enable interrupts for jack detect.

Jack-Detect Enable (JDETEN)

Enables the jack-detect circuitry.

Jack-Sense Weak Pullup (JDWK)

Enables a weak internal pullup current for reduced power loss when the chip is in shutdown or the MICBIAS is disabled.

JDWK = 0 enables a 2.2kΩ pullup to obtain full jack-detect operation. This mode can be used to detect insertion and removal of a plug as well as distinguish between headphone and headset accessories.

JDWK = 1 enables a 4µA pullup current source when $\overline{SHDN}$ = 0 or MICBIAS disabled. In this power-saving configuration, the circuit can detect insertion and removal of a plug but cannot distinguish between headphone and headset accessories.

The recommended usage follows: Set JDWK = 0 (or set any bit in the microphone preamplifier gain registers PALEN[1:0] or PAREN[1:0]). This enables the 2.2kΩ pullup. Once the jack has been inserted and the type of accessory determined, set JDWK = 1 to save power. Once the plug is removed, set JDWK = 0.

Table 21. Jack Sense (JKSNS)

JKSNS[1:0]	DESCRIPTION
00	JACKSNS is below V_{TH2} (low).
01	JACKSNS is between V_{TH1} and V_{TH2} (mid).
10	Invalid.
11	JACKSNS is above V_{TH1} (high).

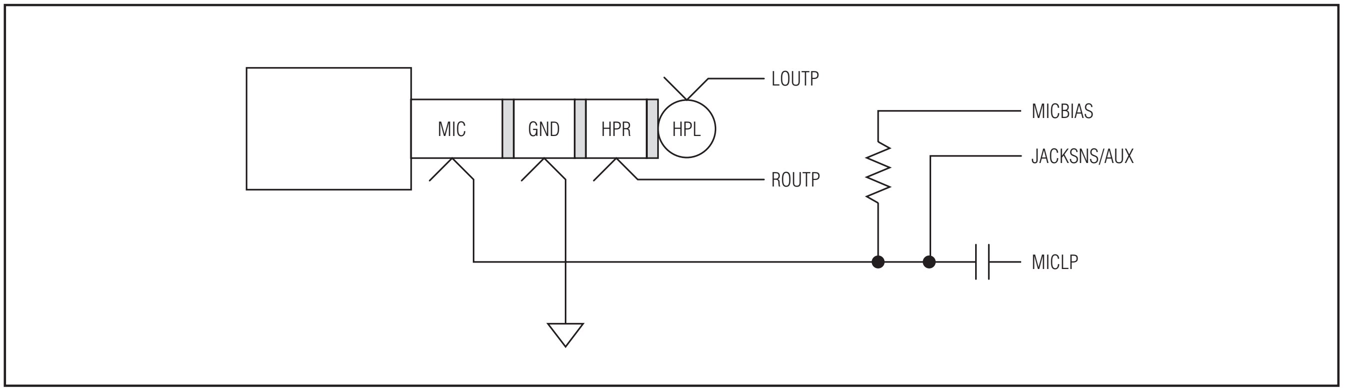


Figure 8. Typical Configuration for Headset Detection

Table 22. Debounce Time

JDEB	DEBOUNCE (ms)
00	25
01	50
10	100
11	200

Debounce (JDEB)

Configures the JDET debounce time for changes to JKSNS[1:0] according to Table 22.

For jack plug insertion/removal, the sequence of events is as follows:

Jack insertion: No jack is present. The MAX9880A has a power supply and is in low-power sleep mode (LOUTP/ROUTP are high impedance). When the JDETEN I2C bit is set, the JACKSNS pin has weak pullups to MICVDD. When a jack is subsequently inserted, JACKSNS should change state (indicated by I2C bits JKSNS[1:0]), and this causes the $\overline{IRQ}$ pin to be pulled low, which can trigger a system wakeup.

Jack present: After an interrupt has been sent to the system controller, the I2C must indicate unambiguously that a jack is present when the I2C registers are read. This is done with the JDET I2C bit, which goes high when there is a change of state of the JKSNS[1:0] bits. The MAX9880A jack-detect system monitors the JACKSNS pin and reports the voltage level as high (> 95% x MICBIAS), mid, or low (< 10% x MICBIAS). When connected to the microphone pin of the headset jack, this window comparator allows detection of:

- No headset (high)
- Cellular headset with microphone (high → mid)
- Stereo headset without microphone (high → low)
- Cellular headset button press (mid → low → mid)
- Headset removal (low or mid → high)

Jack removal: A jack is present. All output poles (headphones/line outs) are assumed driven by a low impedance amplifier. All input poles (microphones) are assumed to be biased with a voltage above ground but below 95% of the MICBIAS voltage. For the MAX9880A to sense when a jack is removed, the JACKSNS pin must be connected to the jack in such a way as to ensure either the JACKSNS pin gets pulled above 95% of MICBIAS (as would happen if JACKSNS is hooked to a microphone pole) or it changes state from low to high or vice versa (as would happen if JACKSNS is hooked to a ground pole which goes high impedance when the jack is removed, or is hooked to a regular jack insertion tab that shorts to ground when the jack is removed). Subsequently, $\overline{IRQ}$ is pulled low.

Jack absent: After an interrupt has been sent to the system controller, the I2C must indicate unambiguously that a jack is **not** present when the I2C registers are read. This is indicated by reading the status of the JKSNS[1:0] I2C read bits.

Table 23. Headset Detect Configuration

$\overline{SHDN}$	MICBIAS	JDWK	JACK ACTION		JKSNS		$\overline{IRQ}$ TOGGLES?	
			FROM	TO	FROM	TO	IJDET = 1	IJDET = 0
0	—	0	None	Headset	11	01	Yes	No
0	—	0	None	Headphone	11	00	Yes	No
0	—	0	Headset	None	01	11	Yes	No
0	—	0	Headphone	None	00	11	Yes	No
0	—	1	None	Headset	11	00	Yes	No
0	—	1	None	Headphone	11	00	Yes	No
0	—	1	Headset	None	00	11	Yes	No
0	—	1	Headphone	None	00	11	Yes	No
1	0	0	None	Headset	11	01	Yes	No
1	0	0	None	Headphone	11	00	Yes	No
1	0	0	Headset	None	01	11	Yes	No
1	0	0	Headphone	None	00	11	Yes	No
1	0	1	None	Headset	11	00	Yes	No
1	0	1	None	Headphone	11	00	Yes	No
1	0	1	Headset	None	00	11	Yes	No
1	0	1	Headphone	None	00	11	Yes	No
1	1	—	None	Headset	11	01	Yes	No
1	1	—	None	Headphone	11	00	Yes	No
1	1	—	Headset	None	01	11	Yes	No
1	1	—	Headphone	None	00	11	Yes	No

Note: *JDETEN = 1; MICBIAS enable; any bit of PALEN/PAREN set.*

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Headphone Modes

The MAX9880A's headphone amplifier supports differential, single-ended, and capacitorless output modes, as shown in Figure 9. In each mode, the amplifier can be configured for stereo or mono operation. The single-ended mode optionally includes click-and-pop reduction to eliminate the click-and-pop that would normally be caused by the output coupling capacitor. When click-and-pop reduction is not required leave LOUTN and ROUTN unconnected.

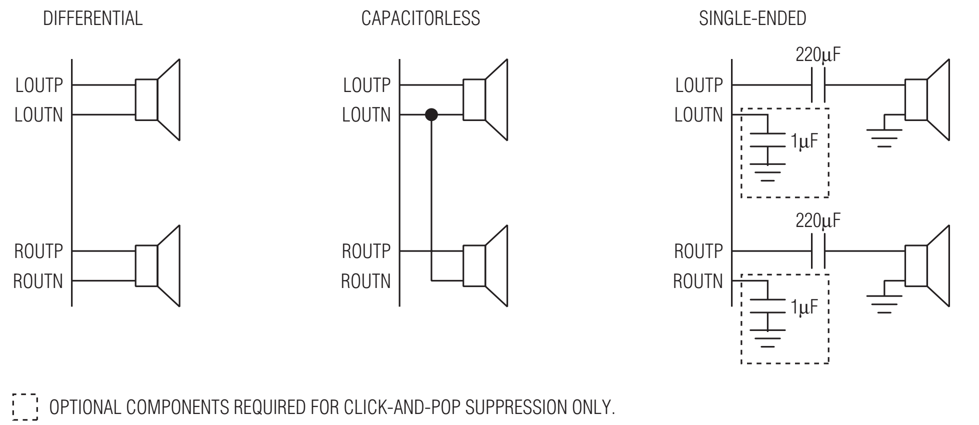


Figure 9. Headphone Amplifier Modes

Table 24. Mode Configuration Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Mode	DSLEW	$\overline{\text{VSEN}}$	$\overline{\text{ZDEN}}$	0	0	HPMODE			0x24
Jack Detect	JDETEN	0	JDWK	0	0	0	JDEB		0x25

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
DSLEW	**Digital Volume Slew Speed** 0 = Digital volume changes are slewed over 10ms. 1 = Digital volume changes are slewed over 80ms.
$\overline{\text{VSEN}}$	**Volume Change Smoothing** 0 = Volume changes slew through all intermediate values. 1 = Volume changes occur in one step.
$\overline{\text{ZDEN}}$	**Line Input Zero-Crossing Detection** 0 = Line input volume changes occur at zero crossings in the audio waveform or after 62ms if no zero crossing occurs. 1 = Line input volume changes occur immediately.

Table 24. Mode Configuration Register (continued)

BITS	FUNCTION	
HPMODE	**Headphone Amplifier Mode**	
	HPMODE	**MODE**
	000	Stereo differential
	001	Mono (left) differential
	010	Stereo capacitorless
	011	Mono (left) capacitorless
	100	Stereo single-ended (clickless)
	101	Mono (left) single-ended (clickless)
	110	Stereo single-ended (fast turn-on)
	111	Mono (left) single-ended (fast turn-on)
	Note: In mono operation, the right amplifier is disabled.	
JDETEN	**Jack-Detection Enable** **$\overline{\text{SHDN}}$ = 0: Sleep Mode.** Enables pullups on JACKSNS/AUX to detect jack insertion. **$\overline{\text{SHDN}}$ = 1: Normal Mode.** Enables the comparator circuitry on JACKSNS/AUX to detect voltage changes. **Note:** AUXEN must be set to 0 for jack detection to function.	
JDWK	**Jack-Sense Weak Pullup.** Enables an internal pullup. Set JDWK = 1 to enable an internal 4µA current source. Set JDWK = 0 for external pullup.	
JDEB	**Jack Detect Debounce.** Configures the JDET debounce time for changes to JKSNS[1:0] according to information below.	
	JDEB	**DEBOUNCE TIME (ms)**
	00	25
	01	50
	10	100
	11	200

Power Management

The MAX9880A includes complete power management control to minimize power usage. The DAC and both ADCs can be independently enabled so that only the required circuitry is active.

Revision Code

The MAX9880A includes a revision code to allow easy identification of the device revision. Revision code at register address 0xFF is not accessible through the SPI interface and so the revision code is accessible through SPI at an additional address of 0x214. The current revision code is 0x42.

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Table 25. Power Management Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Enable	LNLEN	LNREN	LOLEN	LOREN	DALEN	DAREN	ADLEN	ADREN	0x26
System Shutdown	$\overline{\text{SHDN}}$	0	0	0	XTEN	$\overline{\text{XTOSC}}$	0	0	0x27

Grayed boxes = Not used.

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

BITS	FUNCTION
LNLEN	**Left-Line Input Enable**. Enables the left-line input preamp and automatically enables the left and right headphone amplifiers. If LNREN = 0, the left-line input signal is also routed to the right ADC input mixer and right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
LNREN	**Right-Line Input Enable**. Enables the right-line input preamp and automatically enables the right headphone amplifiers. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
LOLEN	**Left-Line Output Enable**. Enables the left-line output.
LOREN	**Right-Line Output Enable**. Enables the right-line output.
DALEN	**Left DAC Enable**. Enables the left DAC and automatically enables the left and right headphone amplifiers. If DAREN = 0, the left DAC signal is also routed to the right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
DAREN	**Right DAC Enable**. Enables the right DAC. Right DAC operation requires DALEN = 1.
ADLEN	**Left ADC Enable.**
ADREN	**Right ADC Enable.** Enabling the right ADC must be done in the same I²C write operation that enables the left ADC. The right ADC can be enabled while the left ADC is running if used for DC measurements. SHDN must be toggled to disable the right ADC in this case. Right ADC operation requires ADLEN = 1.
$\overline{\text{SHDN}}$	**Shutdown**. Places the device in low power shutdown mode.
XTEN	**Crystal Clock Enable** 1 = Output of crystal oscillator and buffer routed to the clock prescaler. MCLK input disabled. 0 = MCLK input routed to the clock prescaler. Crystal oscillator and buffer disabled.
$\overline{\text{XTOSC}}$	**Crystal Clock Source** 1 = Disables the internal crystal oscillator. Provide an external clock on X1. 0 = Enables the internal crystal oscillator. Attach a crystal between X1 and X2. $\overline{\text{XTOSC}}$ is ignored if XTEN = 0.

Table 26. Revision Code Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS (SEE NOTE)
Revision ID	REV								0x14
Revision ID	REV								0xFF

Note: *Register addresses listed are for I²C. To get the SPI address, add 0x200 with the following exception: Register 0xFF is not accessible through SPI.*

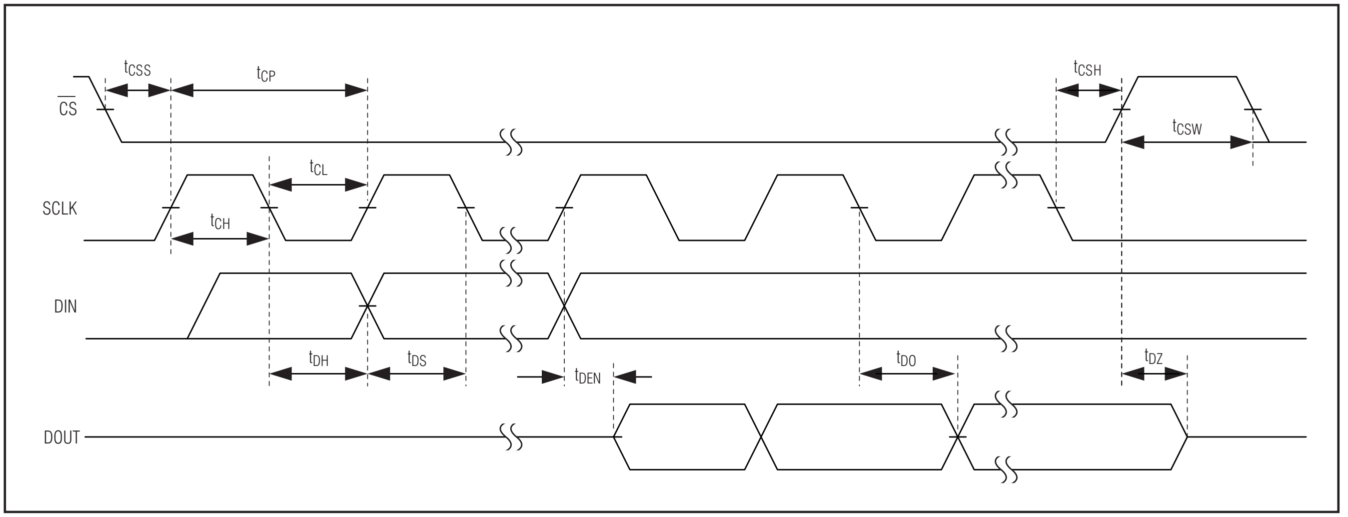

Figure 10. SPI Interface Timing Diagram

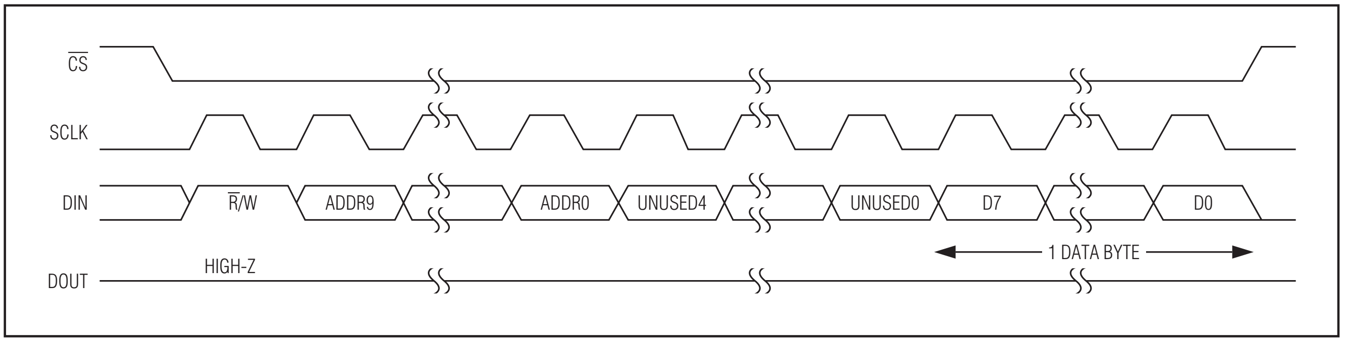

Figure 11. Writing 1 Byte of Data to the MAX9880A

Serial Peripheral Interface (SPI)

Chip Select ($\overline{CS}$)

The MAX9880A SPI interface is active only when $\overline{CS}$ is low. When $\overline{CS}$ is high, the MAX9880A configures the DOUT output for high impedance and resets the internal SPI logic. If $\overline{CS}$ goes high in the middle of an SPI transfer, all the data is discarded. When $\overline{CS}$ is low, unless the register address is correctly decoded by the MAX9880A, the DOUT output is high impedance.

Serial Clock (SCLK)

The SPI master provides the SCLK signal to clock the SPI interface. SCLK has an upper frequency limit of 25MHz. The MAX9880A samples the DIN input data on the falling edge of SCLK and changes the output data on the rising edge of SCLK. The MAX9880A ignores SCLK transitions when $\overline{CS}$ is high.

Serial-Data In (DIN) and Serial-Data Out (DOUT)

The SPI frame is organized into 24 bits. The first 16 bits consist of the $\overline{R}$/W enable bit, followed by the 10 register address bits and 5 unused bits. The next 8 bits are data bits, sent most significant bit first.

For an SPI write transfer, write a 1 to the $\overline{R}$/W bit, followed by the 10 register address bits, 5 unused bits, then the 8 data bits.

Figure 11 illustrates the proper frame format for writing one byte of data to the MAX9880A. Additional 24-bit frames can be sent while $\overline{CS}$ remains low. The DOUT output is high impedance during a write operation.

For an SPI read transfer, write a zero to the $\overline{R}$/W bit, followed by the 10 register address bits and 5 unused bits. Any data sent after the register address bits are ignored. The internal contents of the register being read

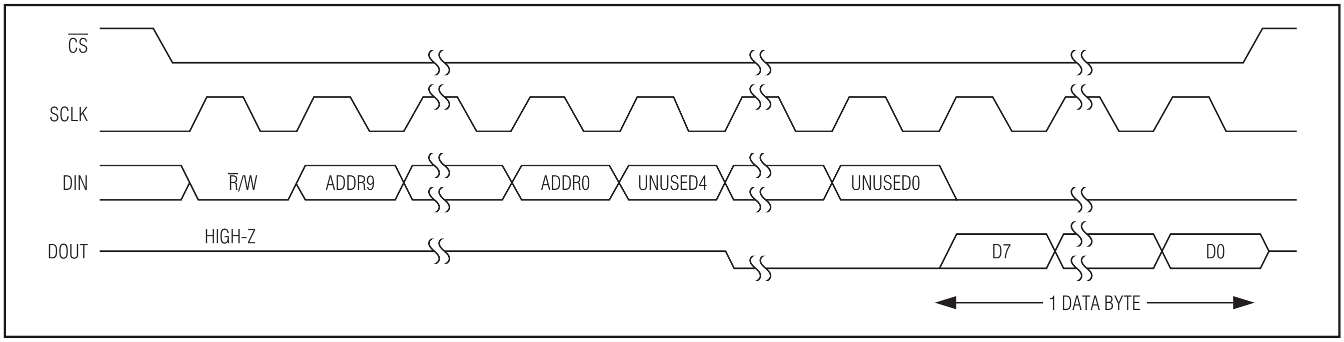

Figure 12. Reading 1 Byte of Data from the MAX9880A

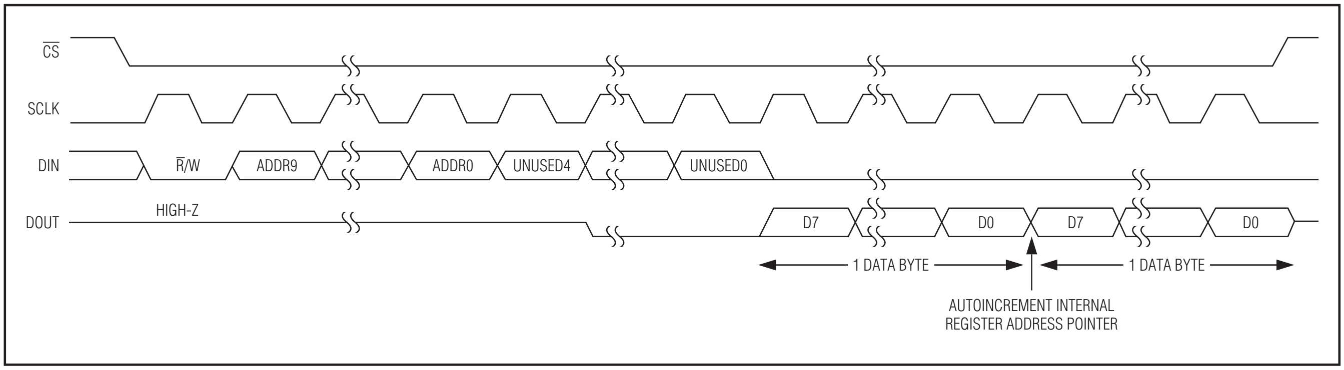

Figure 13. Reading n Bytes of Data from the MAX9880A

do not change until the transfer is complete. The DOUT output is high impedance when writing the register address bits. If the correct register address is decoded, DOUT is driven low at the first rising clock edge after the first unused bit.

Figure 12 illustrates the proper frame format for reading 1 byte of data from the MAX9880A.

When reading data from the MAX9880A, the address pointer autoincrements by one register address if $\overline{CS}$ is held low after reading the first 8 data bits. For each subsequent eight clock cycles, a byte of data is read. This autoincrement feature allows a master to read sequential registers within one continuous SPI register address range from 0x200 to 0x227. The register address does not autoincrement if a read is initiated at a register address lower than 0x200. If the register address increments beyond 0x227, the DOUT output is high impedance. Figure 13 illustrates the proper format for reading multiple bytes of data.

I²C Serial Interface

The MAX9880A features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9880A and the master at clock rates up to 400kHz. Figure 14 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9880A by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9880A is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9880A transmits the proper slave address followed by a series of nine SCL pulses. The MAX9880A transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read

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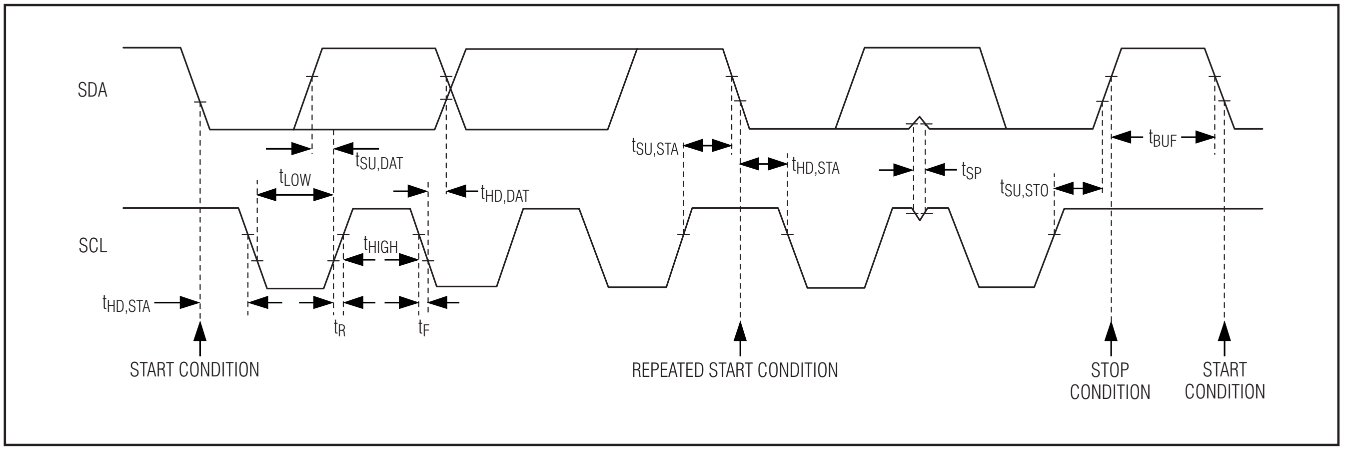

Figure 14. 2-Wire Interface Timing Diagram

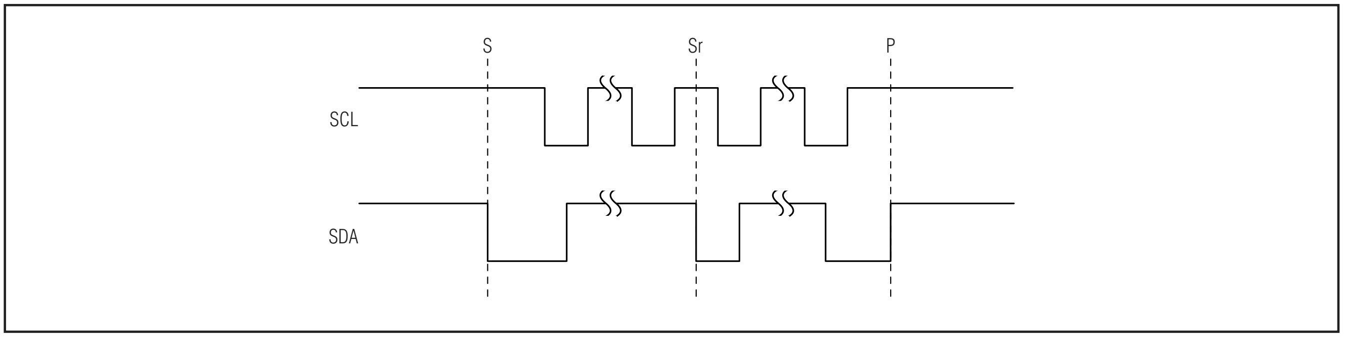

Figure 15. START, STOP, and Repeated START Conditions

sequence is framed by a START or repeated START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9880A from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 15). A START condition from the master signals the beginning of a transmission to the MAX9880A. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a repeated START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9880A recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

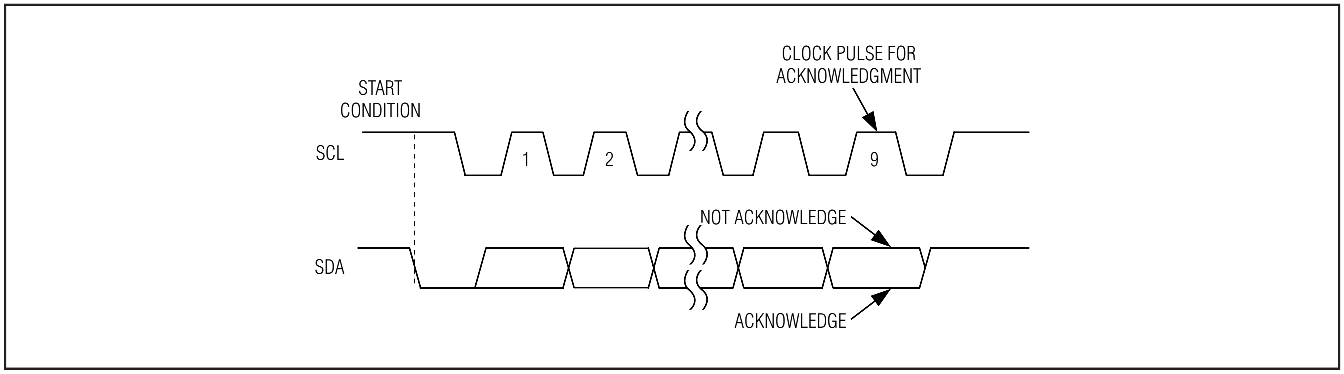

Figure 16. Acknowledge

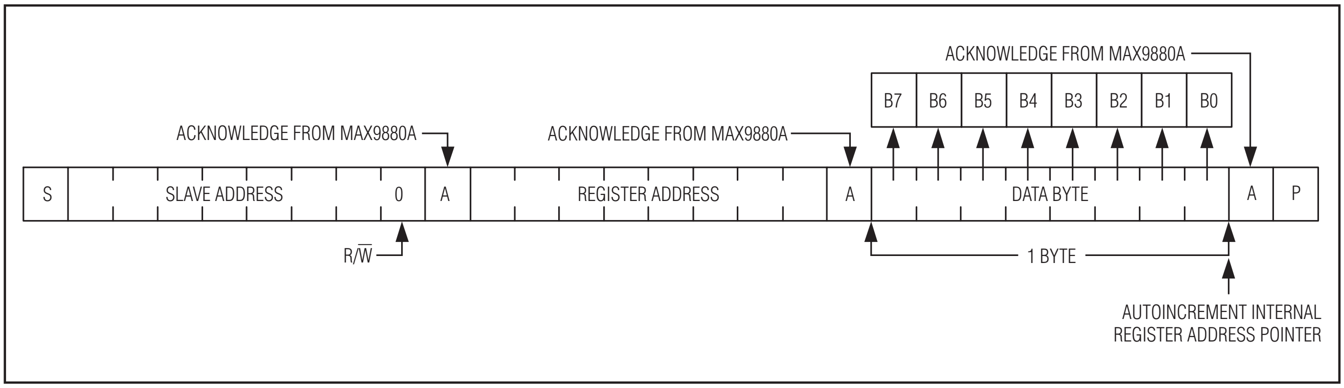

Figure 17. Writing 1 Byte of Data

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX9880A, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the MAX9880A for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the MAX9880A for write mode. The address is the first byte of information sent to the MAX9880A after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9880A uses to handshake receipt each byte of data when in write mode (see Figure 16). The MAX9880A pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9880A is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9880A, followed by a STOP condition.

Write Data Format

A write to the MAX9880A includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, 1 byte of data to configure the internal register address pointer, 1 or more bytes of data, and a STOP condition. Figure 17 illustrates the proper frame format for writing 1 byte of data to the MAX9880A. Figure 18 illustrates the frame format for writing n bytes of data to the MAX9880A.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9880A. The MAX9880A acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX9880A's internal register address pointer. The pointer tells the MAX9880A where to write the next byte of data. An acknowledge pulse is sent by the MAX9880A upon receipt of the address pointer data.

The third byte sent to the MAX9880A contains the data that is written to the chosen register. An acknowledge pulse from the MAX9880A signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x17 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9880A acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX9880A is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9880A's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A repeated START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9880A then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 19 illustrates the frame format for reading 1 byte from the MAX9880A. Figure 20 illustrates the frame format for reading multiple bytes from the MAX9880A.

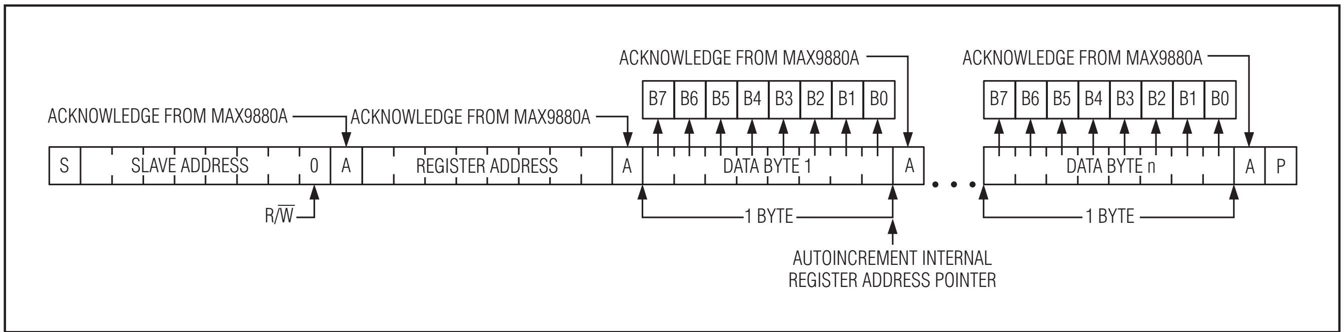

Figure 18. Writing n Bytes of Data

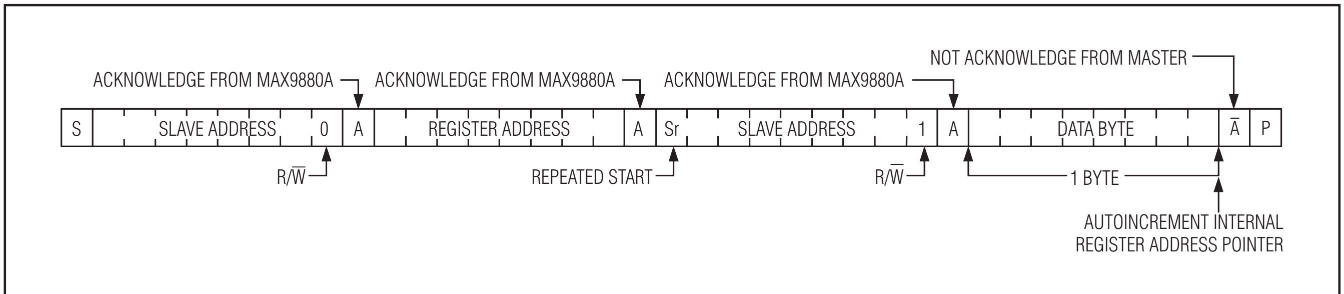

Figure 19. Reading 1 Byte of Data

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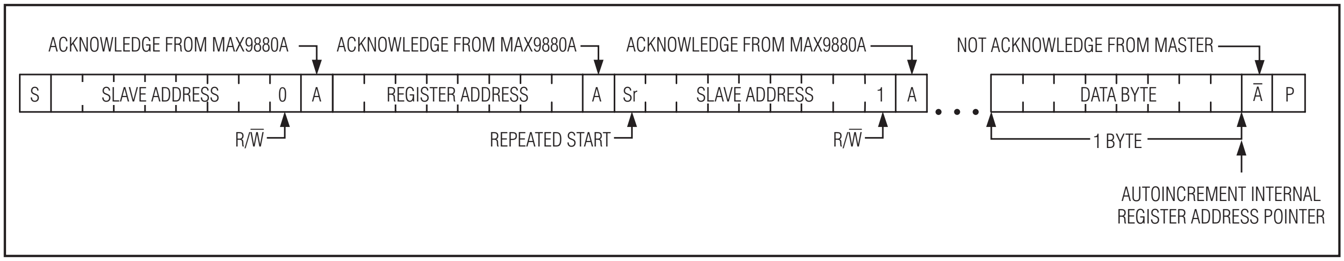


Figure 20. Reading n Bytes of Data

Applications Information

Proper layout and grounding are essential for optimum performance. When designing a PCB for the MAX9880A, partition the circuitry so that the analog sections of the MAX9880A are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND and DGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS, REG, PREG, and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND. Bypass AVDD directly to AGND.

Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD and DVDDS1 directly to DGND.

Route microphone signals from the microphone to the MAX9880A as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, ground the negative microphone input as close to the audio source as possible and then treat the positive and negative traces as differential pairs.

The MAX9880A TQFN package features an exposed thermal pad on its underside. Connect the exposed thermal pad to AGND.

An evaluation kit (EV kit) is available to provide an example layout for the MAX9880A. The EV kit allows quick setup of the MAX9880A and includes easy-to-use software allowing all internal registers to be controlled.

Startup Sequences

Table 27. Clock Initialization (Perform Before Any Playback or Record Setup)

SEQUENCE	DESCRIPTION	REGISTERS
1	$\overline{\text{SHDN}}$ = 0	0x27
2	Configure clocks	0x05, 0x06, 0x07, 0x0B, 0x0C
3	Configure digital audio interface	0x08, 0x09, 0x0A, 0x0D, 0x0E, 0x0F

Table 28. Music Playback

SEQUENCE	DESCRIPTION	REGISTERS
1	Select DAC audio source	0x10
2	Select music filters	0x11
3	Set output volume	0x1C, 0x1D
4	Set line output volume	0x1E, 0x1F
5	Select headphone mode	0x24
6	Enable line outputs and DAC as required	0x26
7	Enable LRCLK and BCLK (if operating in slave mode)	N/A
8	Enable MAX9880A	0x27
9	Enable external amplifier (if using)	N/A

Table 29. Line Input Playback

SEQUENCE	DESCRIPTION	REGISTERS
1	Set line input gain	0x1A, 0x1B
2	Set volume	0x1C, 0x1D
3	Set line output volume (if using)	0x1E, 0x1F
4	Select headphone mode	0x24
5	Enable line outputs and line inputs as required	0x26
6	Enable MAX9880A	0x27
7	Enable external amplifier (if using)	N/A

Table 30. Line Input Playback with Record

SEQUENCE	DESCRIPTION	REGISTERS
1	Select music filters	0x11
2	Set line input gain	0x1A, 0x1B
3	Set volume	0x1C, 0x1D
4	Set line output volume (if using)	0x1E, 0x1F
5	Configure ADC input mixer	0x22
6	Select headphone mode	0x24
7	Enable line outputs, line inputs, and ADC as required	0x26
8	Enable LRCLK and BCLK (if operating in slave mode)	N/A
9	Enable MAX9880A	0x27
10	Enable external amplifier (if using)	N/A

Table 31. Voice Playback

SEQUENCE	DESCRIPTION	REGISTERS
1	Select DAC audio source	0x10
2	Select voice filters	0x11
3	Set volume	0x1C, 0x1D
4	Set line output volume (if using)	0x1E, 0x1F
5	Select headphone mode	0x24
6	Enable line outputs and DAC as required	0x26
7	Enable LRCLK and BCLK (if operating in slave mode)	N/A
8	Enable MAX9880A	0x27
9	Enable external amplifier (if using)	N/A

Table 32. Voice Microphone Record

SEQUENCE	DESCRIPTION	REGISTERS
1	Select voice filters	0x11
2	Set ADC level to 0dB	0x18, 0x19
3	Configure microphone gain	0x20, 0x21
4	Set line output volume (if using)	0x1E, 0x1F
5	Configure ADC input mixer	0x22
6	Configure MICBIAS voltage	0x23
7	Enable ADC	0x26
8	Enable LRCLK and BCLK (if operating in slave mode)	N/A
9	Enable MAX9880A	0x27

Table 33. Voice Playback with Record

SEQUENCE	DESCRIPTION	REGISTERS
1	Select voice filters	0x11
2	Set ADC level to 0dB	0x18, 0x19
3	Configure microphone gain	0x20, 0x21
4	Set line output volume (if using)	0x1E, 0x1F
5	Configure ADC input mixer	0x22
6	Configure MICBIAS voltage	0x23
7	Enable ADCs and DACs as required	0x26
8	Enable LRCLK and BCLK (if operating in slave mode)	N/A
9	Enable MAX9880A	0x27

Example of Register Settings for Music Playback and Voice Duplex Senarios

Music Playback

f_{MCLK} = 12.288MHz (master clock supplied to codec), f_{LRCLK} = 48kHz, standard I²S format, codec in slave mode, music source connected through S2 pins to DAI2 audio path, and output on headphone amplifiers (output capacitorless mode).

Table 34. Music Playback

SEQUENCE	DESCRIPTION	REGISTER ADDRESS	REGISTER VALUE
1	$\overline{SHDN}$ = 0	0x27	04h
2	Configure system clock	0x05	10h
3	Configure DAI2 clock	0x0B	60h
4	Configure DAI2 clock	0x0C	00h
5	Configure DAI2 audio path	0x0D	11h
6	Configure DAI2 audio path	0x0E	50h
7	Select DAC audio source	0x10	21h
8	Select music filters	0x11	80h
9	Set output volume (0dB)	0x1C, 0x1D	09h
10	Set line output volume (muted)	0x1E, 0x1F	40h
11	Select headphone mode (output capacitorless mode)	0x24	02h
12	Enable line outputs and DAC as required	0x26	0Ch
13	Enable MAX9880A	0x27	84h

Voice Duplex

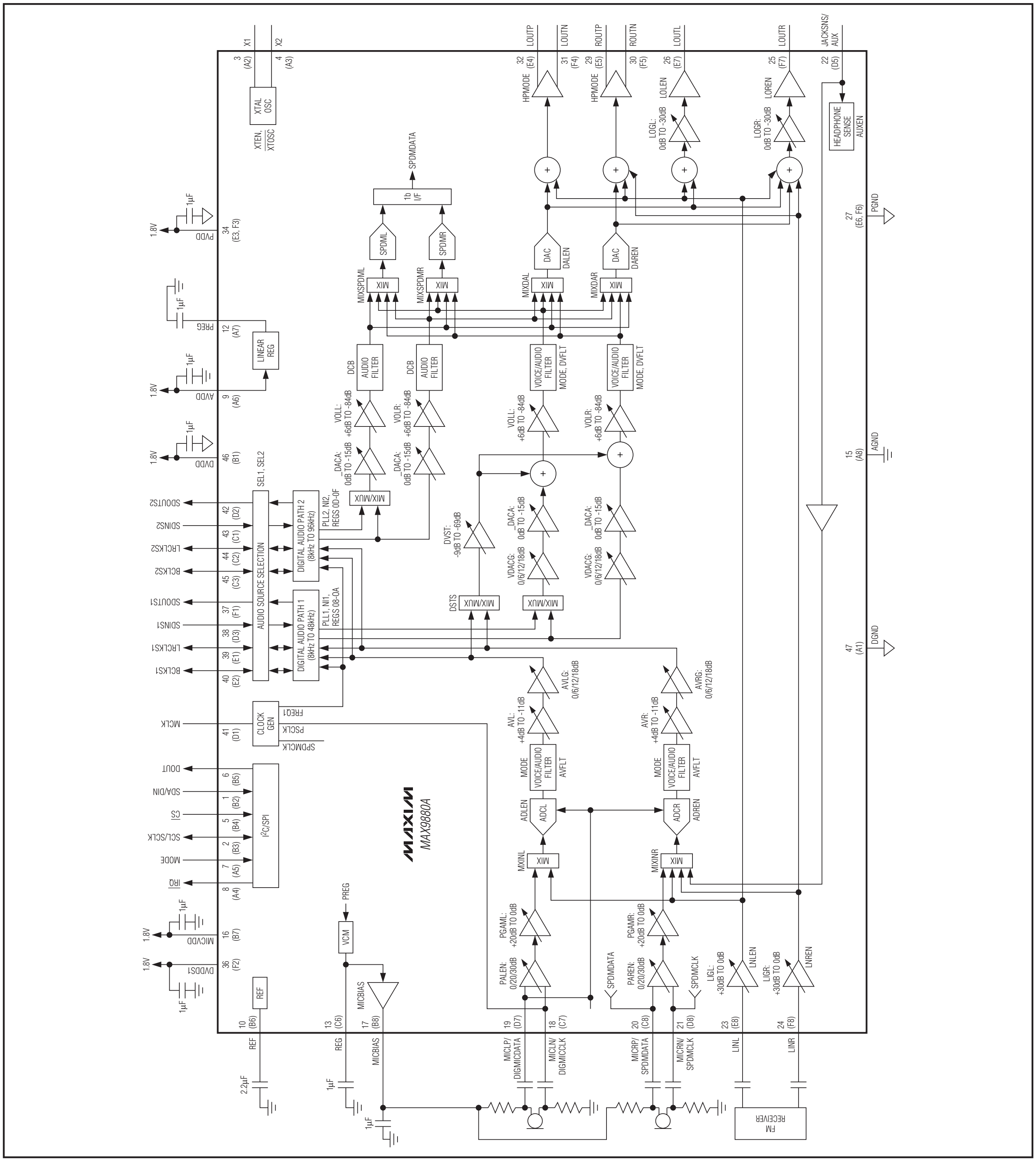
f_{MCLK} = 13MHz (master clock supplied to codec), f_{LRCLK} = 8kHz, TDM/PCM format, codec in slave mode, voice signals on S1 pins to DAI1 audio path and output on headphone amplifier left (differential mode).

Table 35. Voice Duplex

SEQUENCE	DESCRIPTION	REGISTER ADDRESS	REGISTER VALUE
1	$\overline{SHDN}$ = 0	0x27	04h
2	Configure system clock	0x05	10h
3	Configure DAI1 clock	0x0B	0Fh
4	Configure DAI1 clock	0x0C	1Fh
5	Configure DAI1 audio path	0x0D	04h
6	Configure DAI2 audio path	0x0E	30h
7	Select DAC audio source	0x10	21h
8	Select voice GSM filters	0x11	33h
9	Set ADC level to 0dB	0x18, 0x19	03h
10	Configure microphone gain (20dB preamp gain)	0x20, 0x21	54h
11	Set headphone volume	0x1C, 0x1D	09h
12	Set line output volume (if using)	0x1E, 0x1F	40h
13	Configure ADC input mixer	0x22	50h
14	Configure MICBIAS voltage (2.2V)	0x23	01h
15	Select headphone mode	0x24	01h
16	Enable line outputs, ADC and DAC as required	0x26	0Bh
17	Enable MAX9880A	0x27	84h

Low-Power, High-Performance Dual I²S Stereo Audio Codec

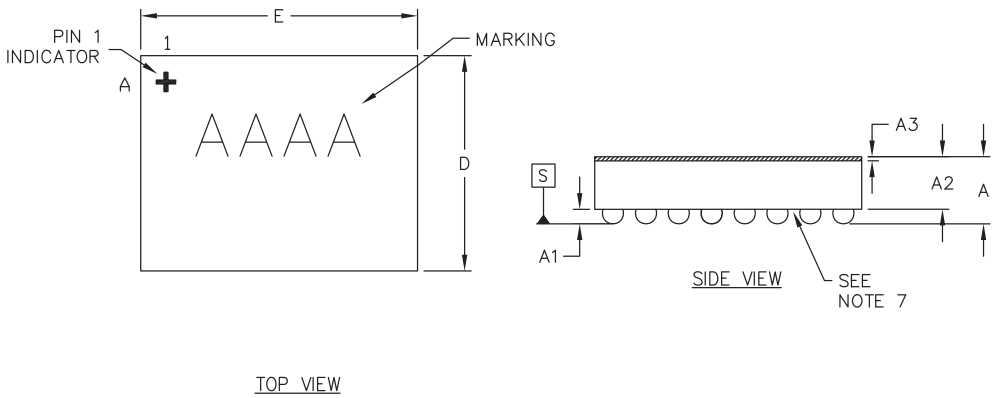
Functional Diagram/Typical Operating Circuit



Package Information

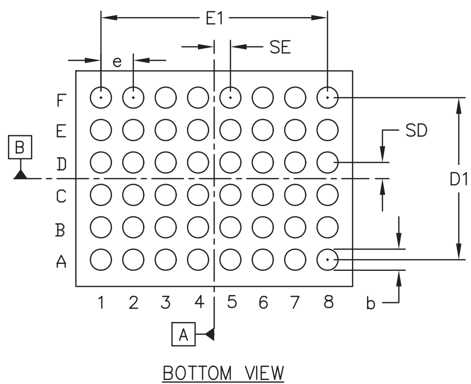
For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4866+1	**21-0141**	**90-0057**
48 WLP	W482A3+1	**21-0230**	Refer to **Application Note 1891**



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
b	ø0.27±0.03
D1	2.00 BASIC
E1	2.80 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W482A3+1	3.25	3.45	2.47	2.67	NONE



NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front–side finish can be either Black or Clear.

–DRAWING NOT TO SCALE–

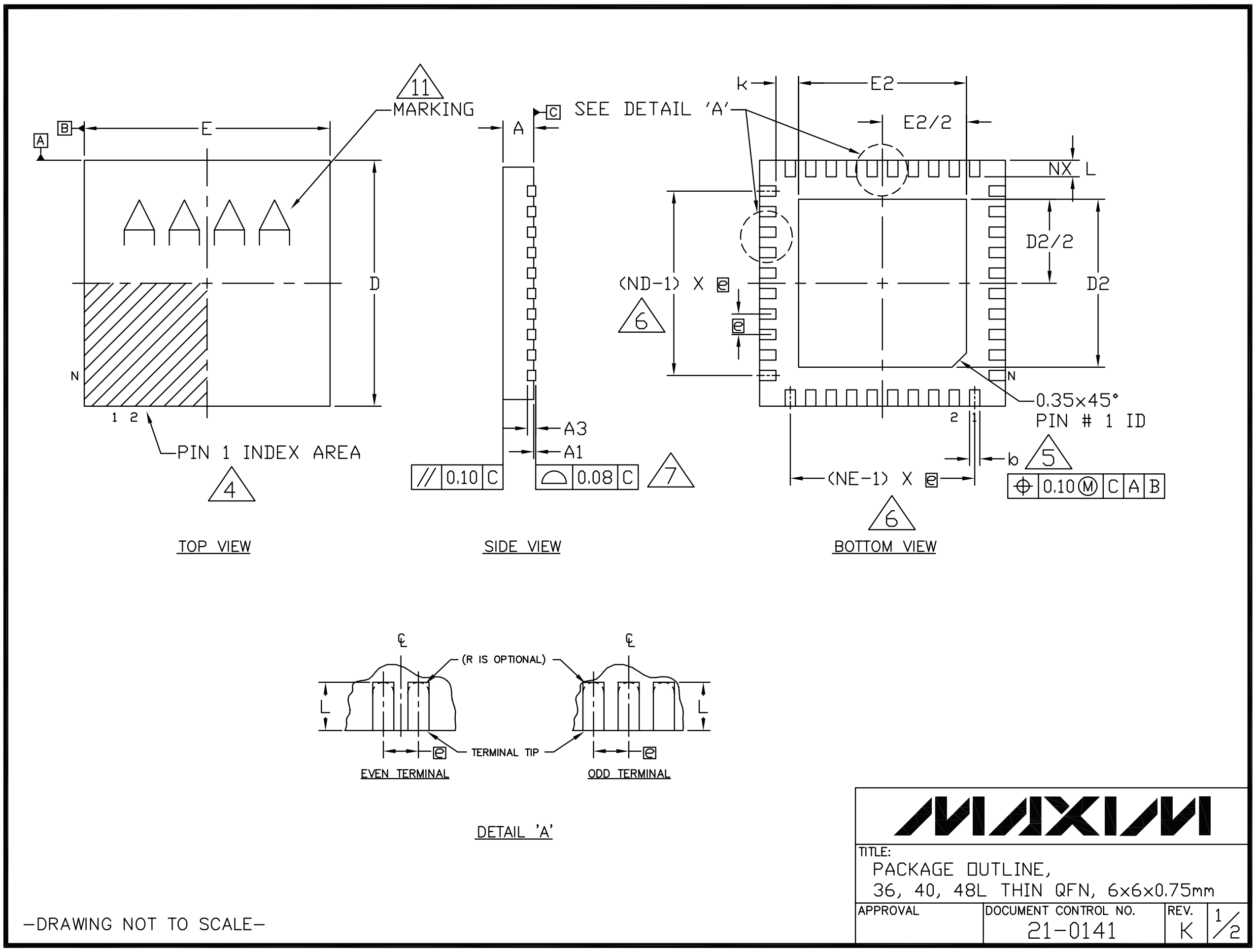
MAXIM

TITLE: PACKAGE OUTLINE
48 BUMPS, WLP PKG. 0.4 mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0230	D	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60
T4066MN-5	4.00	4.10	4.20	4.00	4.10	4.20

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES IN DEGREES UNLESS OTHERWISE SPECIFIED
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH: PACKAGE T4866.
9. N IS THE TOTAL NUMBER OF TERMINALS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.75mm

APPROVAL | DOCUMENT CONTROL NO. 21-0141 | REV. K | 2/2

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—
1	3/11	Various data sheet errors	15–22, 24, 29, 31, 47, 49, 51, 52, 55–58, 60, 61, 62, 66