



2:1 Multiplexers and 1:2 Demultiplexers with Loopback

General Description

The MAX9394/MAX9395 consist of a 2:1 multiplexer and a 1:2 demultiplexer with loopback. The multiplexer section (channel B) accepts two low-voltage differential signaling (LVDS) inputs and generates a single LVDS output. The demultiplexer section (channel A) accepts a single LVDS input and generates two parallel LVDS outputs. The MAX9394/MAX9395 feature a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A.

Three LVC MOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9394 provides high-level input fail-safe detection for HSTL, LVDS, and other GND-referenced differential inputs. The MAX9395 provides low-level fail-safe detection for CML, LVPECL, and other VCC-referenced differential inputs.

Ultra low 91ps_{p-p} (max) pseudorandom bit sequence (PRBS) jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 1.5GHz operation and less than 87ps (max) skew between channels.

LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS outputs drive 100Ω loads. The MAX9394/MAX9395 are offered in a 32-pin TQFP package and operate over the extended temperature range (-40°C to +85°C).

Applications

High-Speed Telecom/Datacom Equipment
Central Office Backplane Clock Distribution
DSLAM
Protection Switching
Fault-Tolerant Systems

Pin Configurations and Functional Diagram appear at end of data sheet.

Features

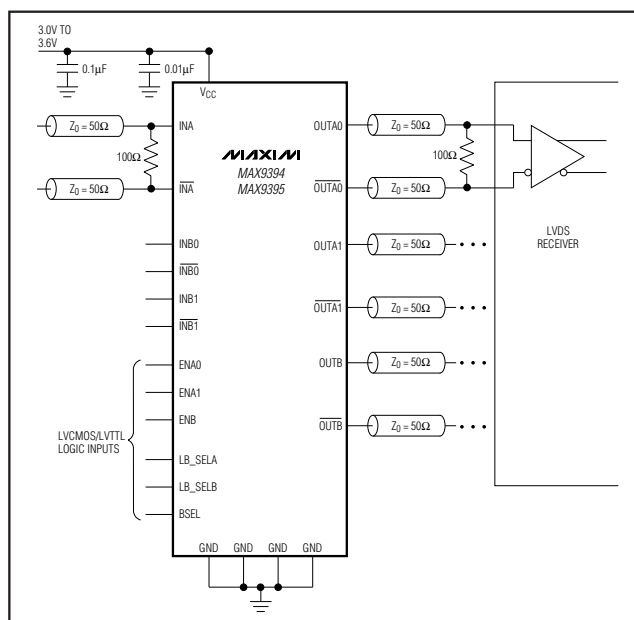
- ◆ Guaranteed 1.5GHz Operation with 250mV Differential Output Swing
- ◆ Simultaneous Loopback Control
- ◆ 2ps(RMS) (max) Random Jitter
- ◆ AC Specifications Guaranteed for 150mV Differential Input
- ◆ Signal Inputs Accept Any Differential Signaling Standard
- ◆ LVDS Outputs for Clock or High-Speed Data
- ◆ High-Level Input Fail-Safe Detection (MAX9394)
- ◆ Low-Level Input Fail-Safe Detection (MAX9395)
- ◆ 3.0V to 3.6V Supply Voltage Range
- ◆ LVC MOS/LVTTL Logic Inputs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9394EHJ	-40°C to +85°C	32 TQFP	H32-1
MAX9394EHJ+	-40°C to +85°C	32 TQFP	H32-1
MAX9395EHJ	-40°C to +85°C	32 TQFP	H32-1
MAX9395EHJ+	-40°C to +85°C	32 TQFP	H32-1

+Denotes a lead-free package.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND -0.3V to +4.1V
 IN_-, $\overline{\text{IN}}_-$, OUT_-, $\overline{\text{OUT}}_-$, EN_-, $\overline{\text{SEL}}$, LB_SEL_ to GND -0.3V to (V_{CC} + 0.3V)
 IN_- to $\overline{\text{IN}}_-$ $\pm 3\text{V}$
 Short-Circuit Duration (OUT_-, $\overline{\text{OUT}}_-$) Continuous
 Continuous Power Dissipation (T_A = +70°C)
 32-Pin TQFP (derate 13.1mW/°C above +70°C) 1047mW
 Junction-to-Ambient Thermal Resistance in Still Air
 32-Pin TQFP +76.4°C/W

Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 ESD Protection (Human Body Model)
 (IN_-, $\overline{\text{IN}}_-$, OUT_-, $\overline{\text{OUT}}_-$, EN_-, $\overline{\text{SEL}}$, LB_SEL_-) .. $\pm 2\text{kV}$
 Soldering Temperature (10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω $\pm 1\%$, EN_ = V_{CC}, V_{CM} = +0.05V to (V_{CC} - 0.6V) (MAX9394), V_{CM} = +0.06V to (V_{CC} - 0.05V) (MAX9395), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, |V_{ID}| = 0.2V, V_{CM} = 1.2V, T_A = +25°C.)
 (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVCMOS/LVTTL INPUTS (EN_-, BSEL, LB_SEL_-)							
Input High Voltage	V _{IH}			2.0		V _{CC}	V
Input Low Voltage	V _{IL}			0		0.8	V
Input High Current	I _{IH}	V _{IN} = 2.0V to V _{CC}		0		20	μA
Input Low Current	I _{IL}	V _{IN} = 0V to 0.8V		0		10	μA
DIFFERENTIAL INPUTS (IN_-, $\overline{\text{IN}}_-$)							
Differential Input Voltage	V _{ID}	V _{ILD} ≥ 0V and V _{IHD} ≤ V _{CC} , Figure 1		0.1		3.0	V
Input Common-Mode Range	V _{CM}	MAX9394		0.05		V _{CC} - 0.6	V
		MAX9395		0.6		V _{CC} - 0.05	
Input Current	I _{IN_-,} I _{$\overline{\text{IN}}_-$}	MAX9394	V _{ID} ≤ 3.0V	-75		10	μA
		MAX9395	V _{ID} ≤ 3.0V	-10		100	
LVDS OUTPUTS (OUT_-, $\overline{\text{OUT}}_-$)							
Differential Output Voltage	V _{OD}	R _L = 100Ω, Figure 2		250	350	450	mV
Change in Magnitude of V _{OD} Between Complementary Output States	ΔV _{OD}	Figure 2			1.0	50	mV
Offset Common-Mode Voltage	V _{OS}	Figure 2		1.125	1.25	1.375	V
Change in Magnitude of V _{OS} Between Complementary Output States	ΔV _{OS}	Figure 2			1.0	50	mV

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3.0V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$, $EN_ = V_{CC}$, $V_{CM} = 0.05V$ to $(V_{CC} - 0.6V)$ (MAX9394), $V_{CM} = 0.06V$ to $(V_{CC} - 0.05V)$ (MAX9395), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = 3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ C$.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current (Output(s) Shorted to GND)	I _{OSI}	V _{ID} = ±100mV (Note 4)	V _{OUT__} or V _{OUT__} = 0V		30	40	mA
			V _{OUT__} = V _{OUT__} = 0V		17	24	
Output Short-Circuit Current (Outputs Shorted Together)	I _{OSBI}	V _{ID} = ±100mV, V _{OUT__} = V _{OUT__} (Note 4)			5	12	mA
SUPPLY CURRENT							
Supply Current	I _{CC}	R _L = 100Ω, EN__ = V _{CC}			53	65	mA
		R _L = 100Ω, EN__ = V _{CC} , switching at 670MHz (1.34Gbps)			53	65	

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $3.6V$, $f_{IN} < 1.34GHz$, $t_{R_IN} = t_{F_IN} = 125ps$, $R_L = 100\Omega \pm 1\%$, $|V_{ID}| \geq 150mV$, $V_{CM} = 0.075V$ to $(V_{CC} - 0.6V)$ (MAX9394 only), $V_{CM} = 0.6V$ to $(V_{CC} - 0.075V)$ (MAX9395 only), $EN_ = V_{CC}$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = 3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $f_{IN} = 1.34GHz$, $T_A = +25^\circ C$.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEL to Switched Output	t_{SWITCH}	Figure 3			1.1	ns
Disable Time to Differential Output Low	t_{PHD}	Figure 4			1.7	ns
Enable Time to Differential Output High	t_{PDH}	Figure 4			1.7	ns
Switching Frequency	f_{MAX}	$V_{OD} \geq 250mV$	1.5	2.2		GHz
Low-to-High Propagation Delay	t_{PLH}	Figures 1, 5	340	567	720	ps
High-to-Low Propagation Delay	t_{PHL}	Figures 1, 5	340	562	720	ps
Pulse Skew $ t_{PLH} - t_{PHL} $	t_{SKEW}	Figures 1, 5 (Note 6)		12.4	86	ps
Output Channel-to-Channel Skew	t_{CCS}	Figure 6 (Note 7)		16	87	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	$f_{IN_} = 100MHz$, Figures 1, 5	112	154	187	ps
Output High-to-Low Transition Time (80% to 20%)	t_F	$f_{IN_} = 100MHz$, Figures 1, 5	112	152	187	ps
Added Random Jitter	t_{RJ}	$f_{IN_} = 1.34GHz$, clock pattern (Note 8)			2	ps(RMS)
Added Deterministic Jitter	t_{DJ}	1.34Gbps, $2^{23} - 1$ PRBS (Note 8)		60	91	psP-P

Note 1: Measurements obtained with the device in thermal equilibrium. All voltages referenced to GND except V_{ID} , V_{OD} , and ΔV_{OD} .

Note 2: Current into the device defined as positive. Current out of the device defined as negative.

Note 3: DC parameters production tested at $T_A = +25^\circ C$ and guaranteed by design and characterization for $T_A = -40^\circ C$ to $+85^\circ C$.

Note 4: Current through either output.

Note 5: Guaranteed by design and characterization. Limits set at ± 6 sigma.

Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output over the same conditions. $t_{SKEW} = |t_{PHL} - t_{PLH}|$.

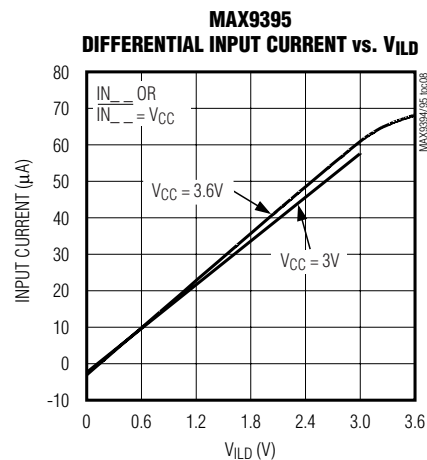
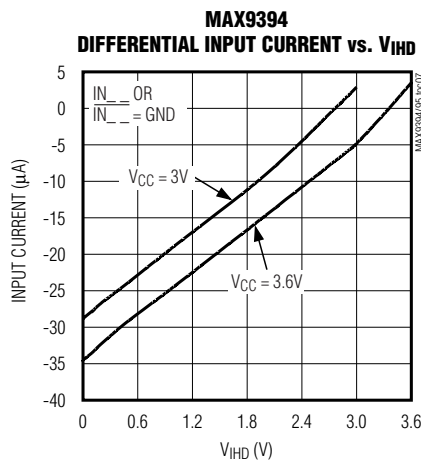
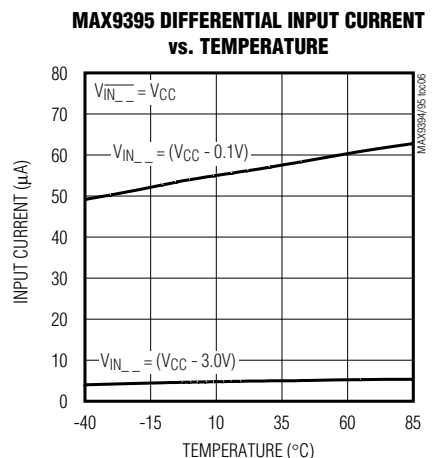
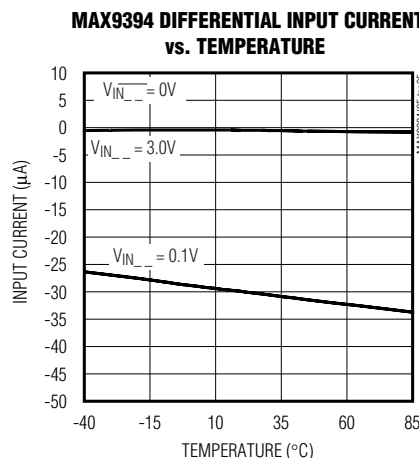
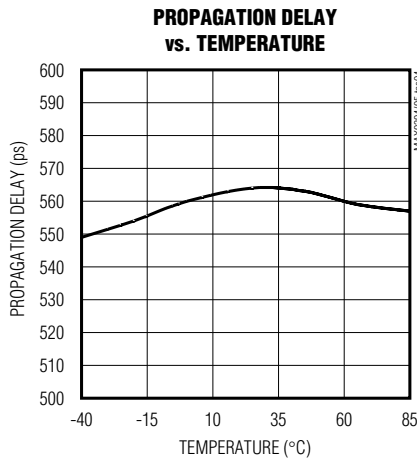
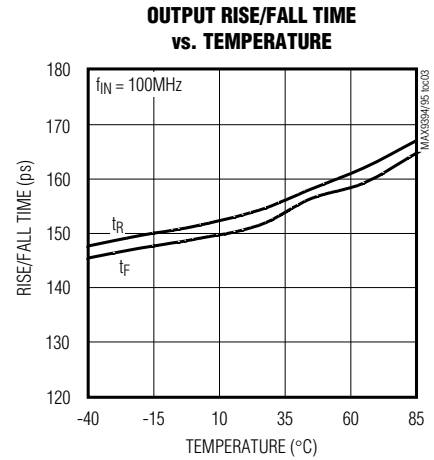
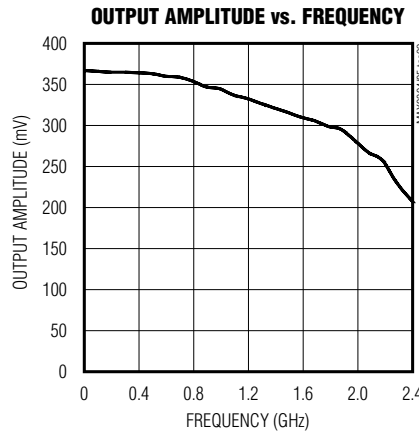
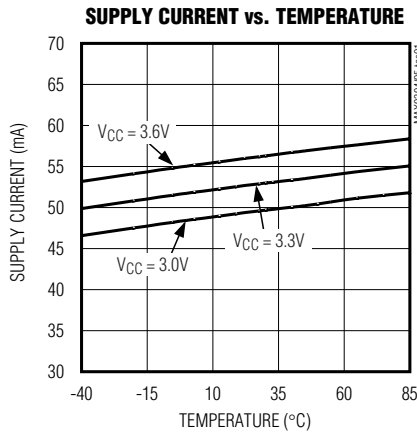
Note 7: Measured between outputs of the same device at the signal crossing points for a same-edge transition under the same conditions. Does not apply to loopback mode.

Note 8: Device jitter added to the differential input signal.

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Typical Operating Characteristics

($V_{CC} = 3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = +1.2V$, $T_A = +25^\circ C$, $f_{IN} = 1.34GHz$, Figure 5.)



2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 30, 31, 32	N.C.	No Connection. Not internally connected.
4, 9, 20, 25	GND	Ground
5	ENB	Channel B Output Enable. Drive ENB high to enable the LVDS outputs for channel B. An internal 435k Ω resistor to GND pulls ENB low when unconnected.
6	OUTB	Channel B LVDS Noninverting Output. Connect a 100 Ω termination resistor between OUTB and $\overline{\text{OUTB}}$ at the receiver inputs to ensure proper operation.
7	$\overline{\text{OUTB}}$	Channel B LVDS Inverting Output. Connect a 100 Ω termination resistor between OUTB and $\overline{\text{OUTB}}$ at the receiver inputs to ensure proper operation.
8, 13, 24, 29	V _{CC}	Power-Supply Input. Bypass each V _{CC} to GND with a 0.1 μ F and 0.01 μ F ceramic capacitor. Install both bypass capacitors as close to the device as possible, with the 0.01 μ F capacitor closest to the device.
10	$\overline{\text{INB0}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
11	INB0	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
12	LB_SELB	Loopback Select for Channel B Output. Connect LB_SELB to GND or leave unconnected to reproduce the INB_ ($\overline{\text{INB}}_+$) differential inputs at OUTB ($\overline{\text{OUTB}}$). Connect LB_SELB to V _{CC} to loop back the INA ($\overline{\text{INA}}$) differential inputs to OUTB ($\overline{\text{OUTB}}$). An internal 435k Ω resistor to GND pulls LB_SELB low when unconnected.
14	$\overline{\text{INB1}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
15	INB1	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
16	BSEL	Channel B Multiplexer Control Input. Selects the differential input to reproduce at the B channel differential output. Connect BSEL to GND or leave unconnected to select the INB0 ($\overline{\text{INB0}}$) set of inputs. Connect BSEL to V _{CC} to select the INB1 ($\overline{\text{INB1}}$) set of inputs. An internal 435k Ω resistor to GND pulls BSEL low when unconnected.
17	ENA1	Channel A1 Output Enable. Drive ENA1 high to enable the A1 LVDS outputs. An internal 435k Ω resistor to GND pulls the ENA1 low when unconnected.
18	$\overline{\text{OUTA1}}$	Channel A1 LVDS Inverting Output. Connect a 100 Ω termination resistor between OUTA1 and $\overline{\text{OUTA1}}$ at the receiver inputs to ensure proper operation.
19	OUTA1	Channel A1 LVDS Noninverting Output. Connect a 100 Ω termination resistor between OUTA1 and $\overline{\text{OUTA1}}$ at the receiver inputs to ensure proper operation.

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Pin Description (continued)

PIN	NAME	FUNCTION
21	ENA0	Channel A0 Output Enable. Drive ENA0 high to enable the A0 LVDS outputs. An internal 435k Ω resistor to GND pulls ENA0 low when unconnected.
22	$\overline{\text{OUTA0}}$	Channel A0 LVDS Inverting Output. Connect a 100 Ω termination resistor between OUTA0 and $\overline{\text{OUTA0}}$ at the receiver inputs to ensure proper operation.
23	OUTA0	Channel A0 LVDS Noninverting Output. Connect a 100 Ω termination resistor between OUTA0 and $\overline{\text{OUTA0}}$ at the receiver inputs to ensure proper operation.
26	INA	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
27	$\overline{\text{INA}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128k Ω pullup resistor to V _{CC} pulls the input high when unconnected (MAX9394). An internal 68k Ω resistor to GND pulls the input low when unconnected (MAX9395).
28	LB_SELA	Loopback Select for Channel A Output. Connect LB_SELA to GND or leave unconnected to reproduce the INA ($\overline{\text{INA}}$) differential inputs at OUTA_ ($\overline{\text{OUTA_}}$). Connect LB_SELA to V _{CC} to loop back the INB_ ($\overline{\text{INB_}}$) differential inputs to OUTA_ ($\overline{\text{OUTA_}}$). An internal 435k Ω resistor to GND pulls LB_SELA low when unconnected.

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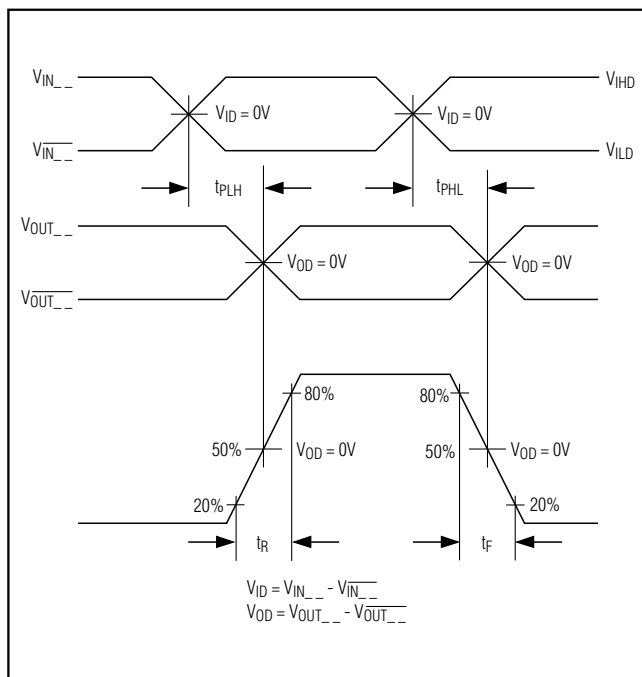


Figure 1. Output Transition Time and Propagation Delay Timing Diagram

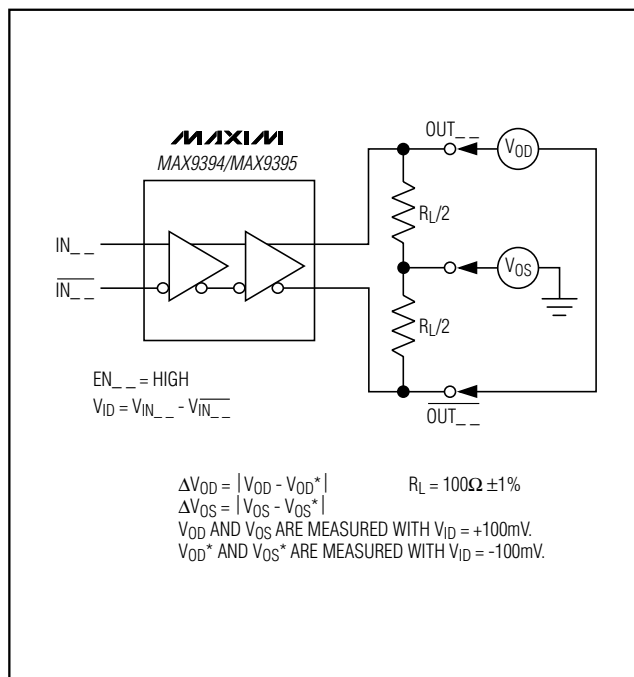


Figure 2. Test Circuit for V_{OD} and V_{OS}

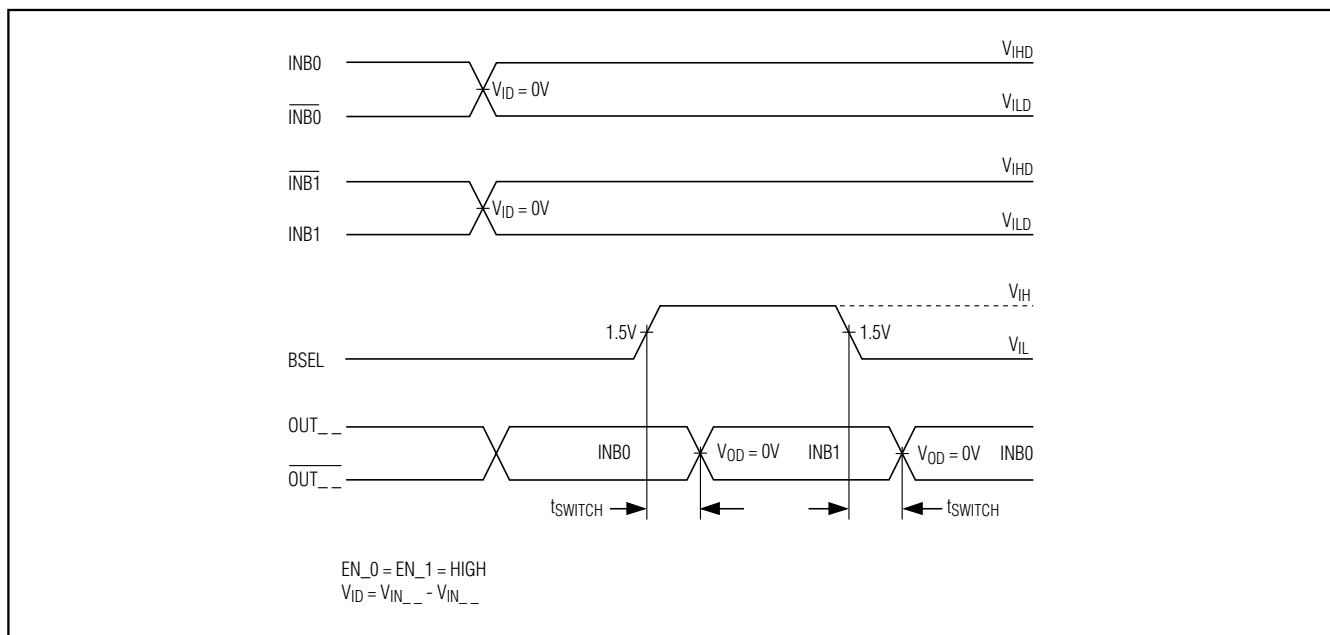


Figure 3. Input to Rising/Falling Edge Select and Mux Switch Timing Diagram

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

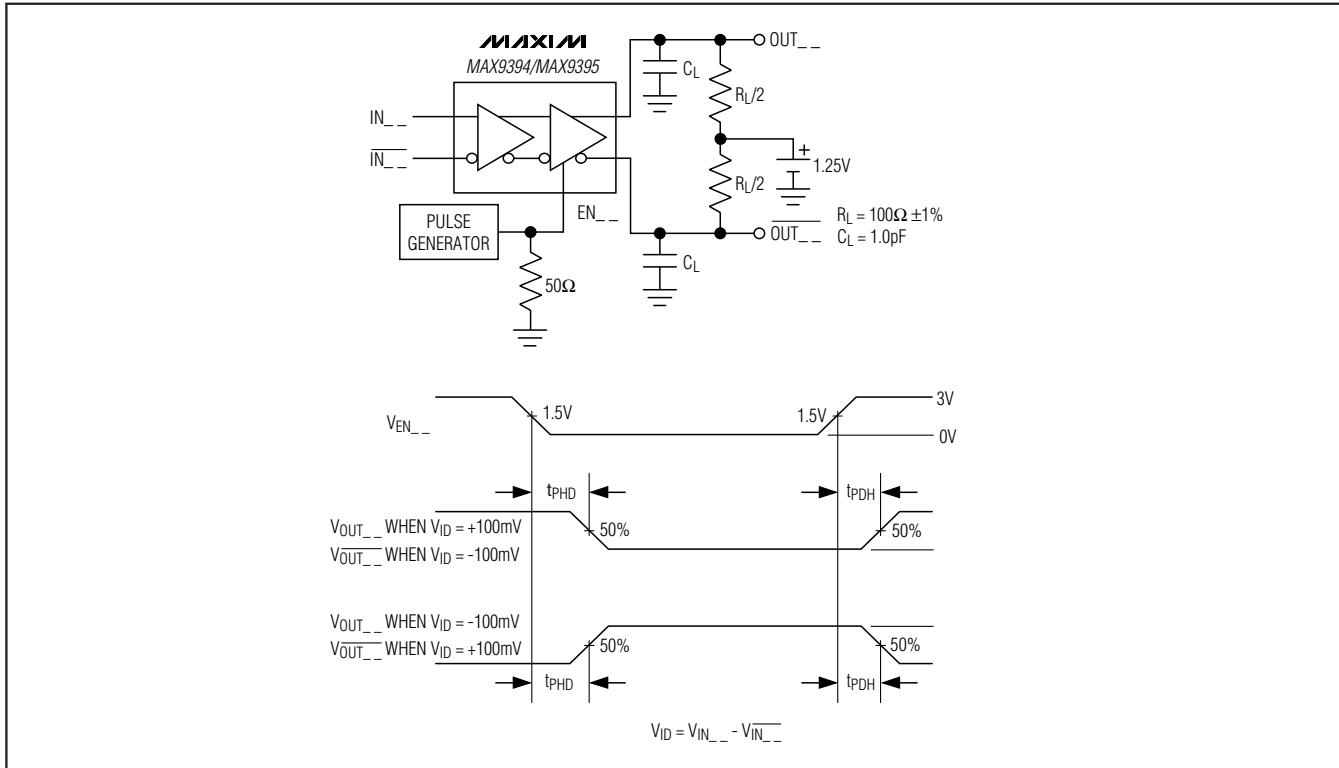


Figure 4. Output Active-to-Disable and Disable-to-Active Test Circuit and Timing Diagram

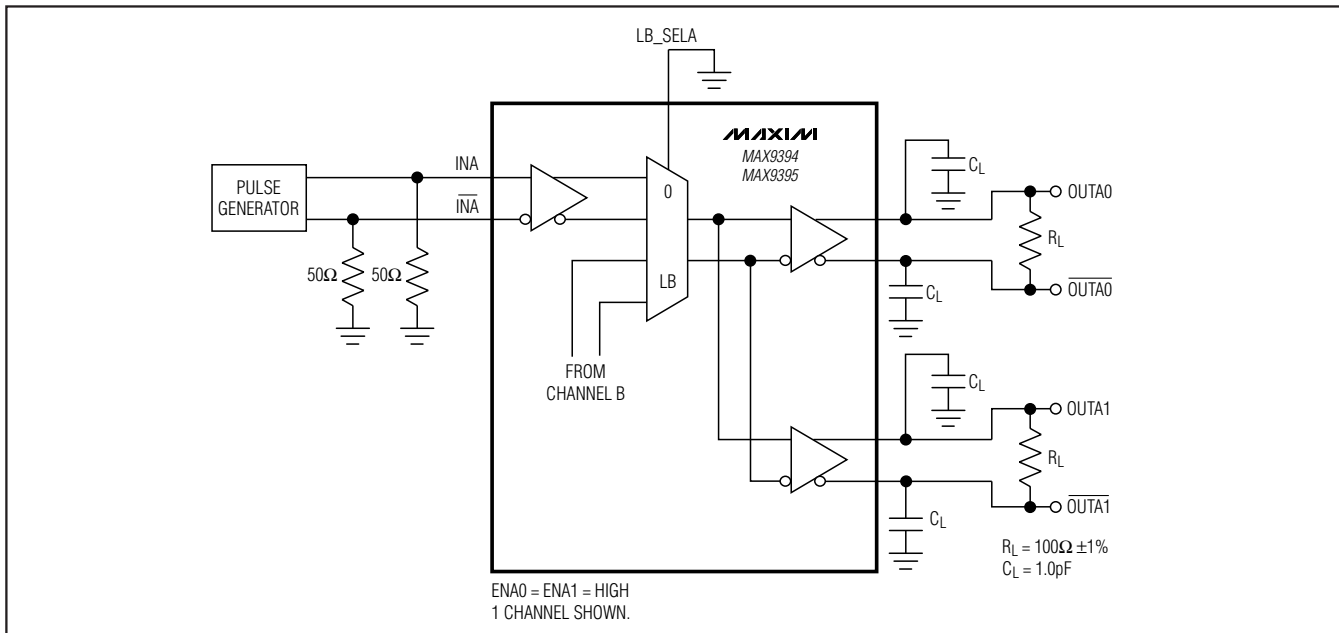


Figure 5. Output Transition Time, Propagation Delay, and Output Channel-to-Channel Skew Test Circuit

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

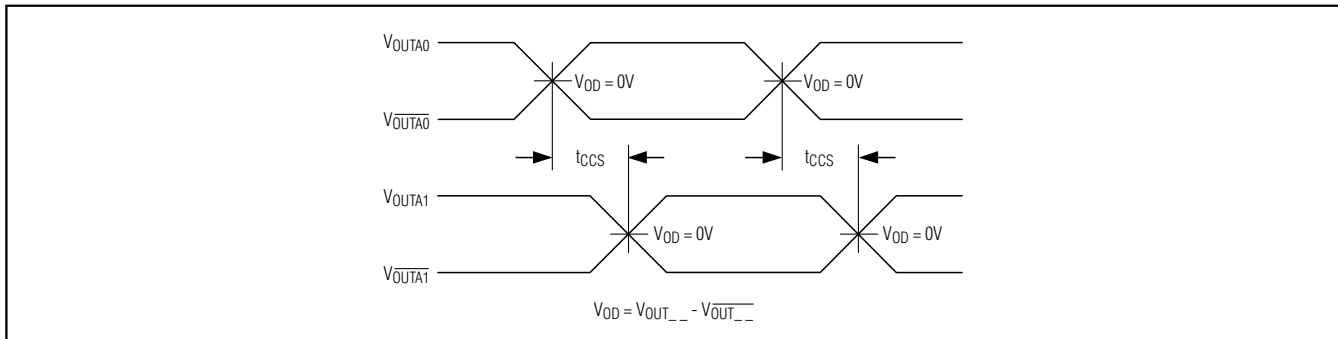


Figure 6. Output Channel-to-Channel Skew

Detailed Description

The LVDS interface standard provides a signaling method for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 standard. LVDS utilizes a lower voltage swing than other communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9394/MAX9395 high-speed, low-power 2:1 multiplexers and 1:2 demultiplexers with loopback provide signal redundancy switching in telecom and storage applications. These devices select one of two remote signal sources for local input and buffer a single local output signal to two remote receivers.

The multiplexer section (channel B) accepts two differential inputs and generates a single LVDS output. The demultiplexer section (channel A) accepts a single differential input and generates two parallel LVDS outputs. The MAX9394/MAX9395 feature a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A. LB_SELA and LB_SELB provide independent loopback control for each channel.

Three LVCMOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Input Fail-Safe

The differential inputs of the MAX9394/MAX9395 possess internal fail-safe protection. Fail-safe circuitry forces the outputs to a differential-low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9394 provides

high-level input fail-safe detection for LVDS, HSTL, and other GND-referenced differential inputs. The MAX9395 provides low-level input fail-safe detection for LVPECL, CML, and other VCC-referenced differential inputs.

Select Function

BSEL selects the differential input pair to transmit through OUTB ($\overline{\text{OUTB}}$) for LB_SELB = GND or through OUTA_ ($\overline{\text{OUTA_}}$) for LB_SELA = VCC. LB_SEL_ controls the loopback function for each channel. Connect LB_SEL_ to GND to select the normal inputs for each channel. Connect LB_SEL_ to VCC to enable the loopback function. The loopback function routes the input of channel A to the output of channel B, and the inputs of channel B to the outputs of channel A. See Tables 1 and 2 for a summary of the input/output routing between channels.

Enable Function

The EN_ logic inputs enable and disable each set of differential outputs. Connect EN_0 to VCC to enable the OUT_0/OUT_0 differential output pair. Connect EN_0 to GND to disable the OUT_0/OUT_0 differential output pair. The differential output pairs assert to a differential low condition when disabled.

Applications Information

Differential Inputs

The MAX9394/MAX9395 inputs accept any differential signaling standard within the specified common-mode voltage range. The fail-safe feature detects common-mode input signal levels and generates a differential output low condition for undriven inputs or when the common-mode voltage exceeds the specified range ($V_{CM} \geq V_{CC} - 0.6V$, MAX9394; $V_{CM} \leq 0.6V$, MAX9395). Leave unused inputs unconnected or connect to VCC for the MAX9394 or to GND for the MAX9395.

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Table 1. Input Select Truth Table

LOGIC INPUTS			DIFFERENTIAL OUTPUTS	
LB_SELA	LB_SELB	BSEL	OUTA_ / OUTA_	OUTB / OUTB
0	0	0	INA selected	INB0 selected
0	0	1	INA selected	INB1 selected
0	1	X	INA selected	INA selected
1	0	0	INB0 selected	INB0 selected
1	0	1	INB1 selected	INB1 selected
1	1	0	INB0 selected	INA selected
1	1	1	INB1 selected	INA selected

X = Don't care.

Differential Outputs

The output common-mode voltage is not properly established if the LVDS output is higher than 0.6V when the supply voltage is ramping up at power-on. This condition can occur when an LVDS output drives an LVDS input on the same chip. To avoid this situation for the MAX9394/MAX9395, connect a 10k Ω resistor from the noninverting output (OUT₊) to ground, and connect a 10k Ω resistor from the inverting output (OUT₋) to ground. These pull-down resistors keep the output below 0.6V when the supply is ramping up (Figure 7).

Power-Supply Bypassing

Bypass each VCC to GND with high-frequency surface-mount ceramic 0.1 μ F and 0.01 μ F capacitors in parallel as close to the device as possible. Install the 0.01 μ F capacitor closest to the device.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9394/MAX9395. Connect each input and output to a 50 Ω characteristic impedance trace. Maintain the distance between differential traces and eliminate sharp corners to avoid discontinuities in differential impedance and maximize common-mode noise immunity. Minimize the number of vias on the differential input and output traces to prevent impedance discontinuities. Reduce reflections by maintaining the 50 Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Output Termination

Terminate LVDS outputs with a 100 Ω resistor between the differential outputs at the receiver inputs. LVDS outputs require 100 Ω termination for proper operation.

Ensure that the output currents do not exceed the current limits specified in the *Absolute Maximum Ratings*.

Table 2. Loopback Select Truth Table

LB_SEL_	OUT_ _
GND or open	Normal inputs selected.
VCC	Loopback inputs selected.

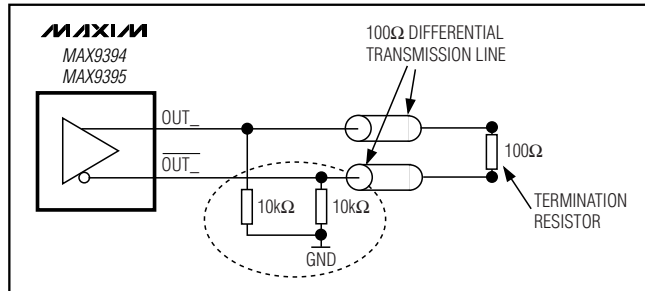


Figure 7. Pull-down Resistor Configuration for LVDS Outputs

Observe the total thermal limits of the MAX9394/MAX9395 under all operating conditions.

Cables and Connectors

Use matched differential impedance for transmission media. Use cables and connectors with matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables.

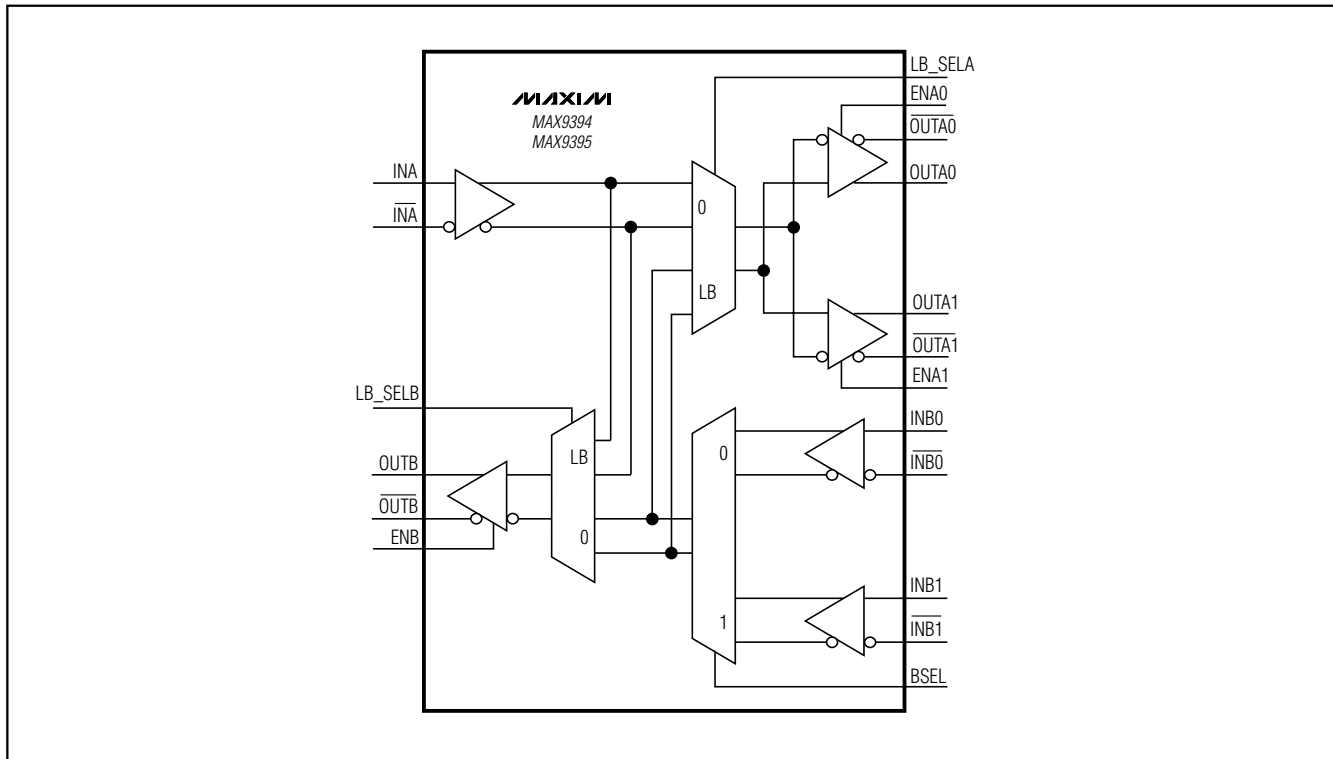
Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects.

Board Layout

Use a four-layer printed circuit (PC) board providing separate signal, power, and ground planes for high-speed signaling applications. Bypass VCC to GND as close to the device as possible. Install termination resistors as close to receiver inputs as possible. Match the electrical length of the differential traces to minimize signal skew.

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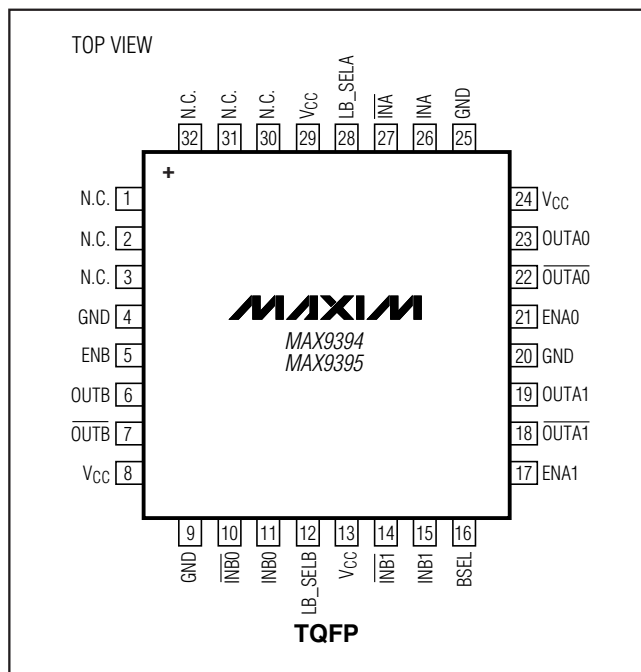
Functional Diagram



MAX9394/MAX9395

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Pin Configurations



Chip Information

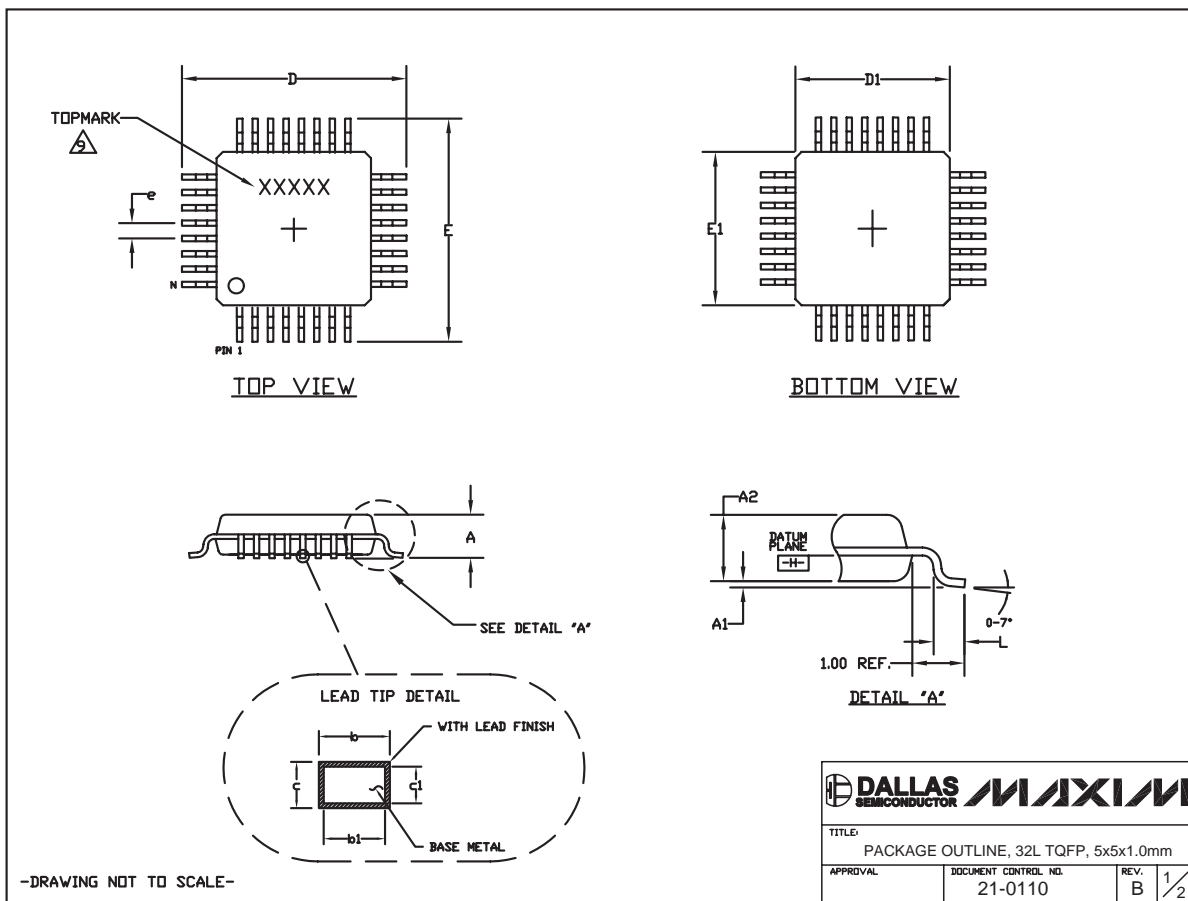
TRANSISTOR COUNT: 1565

PROCESS: BIPOLAR

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



MAX9394/MAX9395

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE \square IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. TOPMARK SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

JEDEC VARIATIONS		
DIMENSIONS IN MILLIMETERS		
AAA		
5x5x1.0 MM		
	MIN.	MAX.
A	\approx	1.20
A ₁	0.05	0.15
A ₂	0.95	1.05
D	6.80	7.20
D ₁	4.80	5.20
E	6.80	7.20
E ₁	4.80	5.20
L	0.45	0.75
N	32	
e	0.50 BSC.	
b	0.17	0.27
b ₁	0.17	0.23
c	0.09	0.20
c ₁	0.09	0.16

			
TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0110	B	2/2

-DRAWING NOT TO SCALE-

Revision History

All pages changed at Rev 1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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