

MAX7387/MAX7388

System Monitoring Oscillator with Watchdog and Power Fail

General Description

The MAX7387/MAX7388 replace ceramic resonators, crystals, and supervisory functions for microcontrollers in 3.3V and 5V applications.

The MAX7387/MAX7388 provide a clock source together with integrated reset, watchdog, and power-fail functions. The watchdog timer is pin programmable and provides watchdog timeout values in the 16ms to 2048ms range. The power-fail output provides early warning of power failure. The power-fail threshold on the MAX7388 is internally set. The MAX7387 also provides a separate watchdog output that is used as a status indicator or to control safety-critical system elements.

The MAX7387/MAX7388 clock outputs are factory programmed to a frequency in the 1MHz to 16MHz range. Four standard frequencies are available. Other frequencies are available upon request. The maximum operating supply current is 5.5mA (max) with a clock frequency of 12MHz.

Unlike typical crystal and ceramic resonator oscillator circuits, the MAX7387/MAX7388 are resistant to EMI and vibration, and operate reliably at high temperatures. The high-output drive current and absence of high-impedance nodes make the oscillator invulnerable to dirty or humid operating conditions.

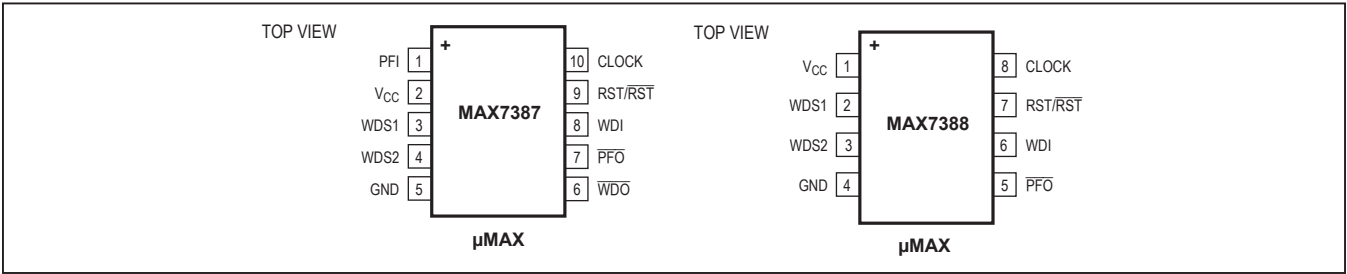
The MAX7387/MAX7388 are available in 10-pin and 8-pin μ MAX[®] packages, respectively. The MAX7387/MAX7388 standard operating temperature range is from -40°C to +125°C.

Applications

- White Goods
- Appliances and Controls
- Handheld Products
- Portable Equipment
- Microcontroller Systems

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Pin Configurations



Features

- Robust Microcontroller Clock and Supervisor in a Single Package
- Integrated Reset, Watchdog, and Power-Fail Functions
- Pin-Programmable Watchdog Timeout
- +2.7V to +5.5V Operation
- Factory-Trimmed Oscillator
- Reset Valid Down to 1.1V Supply Voltage
- ± 10 mA Clock-Output Drive Current
- $\pm 4\%$ Total Accuracy for -40°C to +125°C
- $\pm 2.75\%$ Total Accuracy for 0°C to +85°C
- -40°C to +125°C Temperature Range
- 8- and 10-Pin μ MAX Surface-Mount Packages
- 5.5mA Operating Current (12MHz)
- 1MHz to 16MHz Factory Preset Frequency

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7387srff	-40°C to +125°C	10 μ MAX
MAX7388srff	-40°C to +125°C	8 μ MAX

Note: “s” is a placeholder for the reset output type. Insert the symbol found in Table 3 in the place of “s.” “r” is a placeholder for the power-on reset (POR) voltage. Insert the symbol found in Table 2 in the place of “r.” “ff” is a placeholder for the nominal output frequency. Insert the symbol found in Table 4 in the place of “ff.” For example, MAX7387CMTP describes a device with 4.38V reset level, open-collector RST output, and a clock output frequency of 8MHz.

Typical Application Circuit, Functional Diagram, and Guide appear at end of data sheet.

Absolute Maximum Ratings

V_{CC} to GND -0.3V to +6.0V
 All Other Pins to GND -0.3V to (V_{CC} + 0.3V)
 CLOCK, $\overline{\text{PFO}}$ Output Current, RST/ $\overline{\text{RST}}$, WDO $\pm 50\text{mA}$
 Continuous Power Dissipation (T_A = +70°C)
 10-Pin μMAX (derate 5.6mW/°C over +70°C) 444mW
 8-Pin μMAX (derate 4.5mW/°C over +70°C) 362mW

Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Typical Application Circuit, V_{CC} = +2.7V to +5.5V, T_A = -40°C to +125°C, 1MHz to 16MHz output frequency range, typical values at V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Operating Supply Voltage	V _{CC}		2.7		5.5	V
Valid RST/ $\overline{\text{RST}}$ Supply Voltage	V _{CCR}	T _A = 0°C to +85°C			1.1	V
		T _A = -40°C to +125°C			1.18	
Operating Supply Current	I _{CC}	f _{CLOCK} = 12MHz			5.5	mA
		f _{CLOCK} = 8MHz			4.5	
TRI-LEVEL ANALOG INPUTS: WDS1, WDS2						
Input-High Voltage Level			V _{CC} - 0.55V			
Input-Middle Voltage Level			0.9	V _{CC} – 1.1V		
Input-Low Voltage Level					0.45	V
LOGIC INPUT: WDI						
Input Leakage Current	I _{LEAK}	Input high			0.5	μA
Logic-Input High Voltage	V _{IH}		0.7 x V _{CC}			V
Logic-Input Low Voltage	V _{IL}		0.3 x V _{CC}			V
PUSH-PULL LOGIC OUTPUTS: RST/ $\overline{\text{RST}}$						
Output High	V _{OH}	I _{SOURCE} = 1mA	V _{CC} – 1.5			V
Output Low	V _{OL}	I _{SINK} = 3mA		0.05	0.4	V
OPEN-DRAIN LOGIC OUTPUTS: $\overline{\text{RST}}$, $\overline{\text{PFO}}$, WDO						
Output Low	V _{OLO}	I _{SINK} = 3mA		0.05	0.4	V
OUTPUT: CLOCK						
Output High Voltage	V _{OH} C	I _{SOURCE} = 5mA	V _{CC} – 0.3			V
Output Low Voltage	V _{OL} C	I _{SINK} = 5mA			0.3	V
CLOCK Accuracy	f _{CLOCK}	T _A = 0°C to +85°C, V _{CC} = 5.0V	-2.75		+2.75	%
		T _A = -40°C to +125°C, V _{CC} = 5.0V	-4		+4	
Clock Frequency Temperature Coefficient		V _{CC} = 5.0V (Note 2)		140	400	ppm/°C
Clock Frequency Supply Voltage Coefficient		T _A = +25°C (Note 2)		0.67	1	%/V

Electrical Characteristics (continued)

(Typical Application Circuit, $V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, 1MHz to 16MHz output frequency range, typical values at $V_{CC} = +5.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

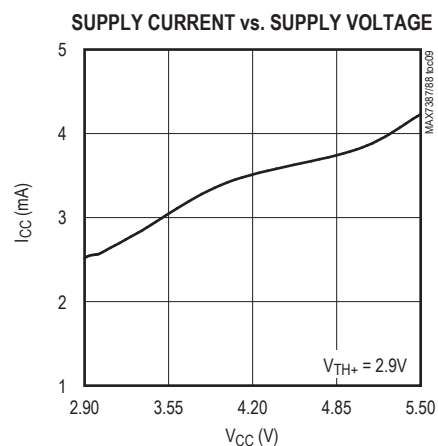
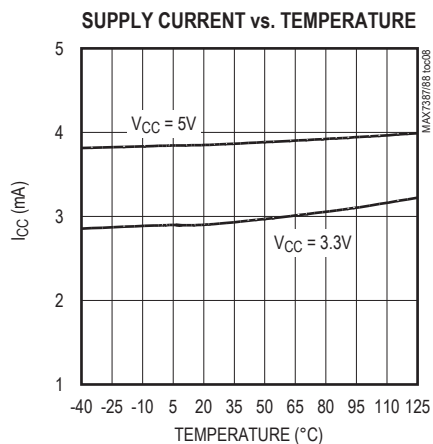
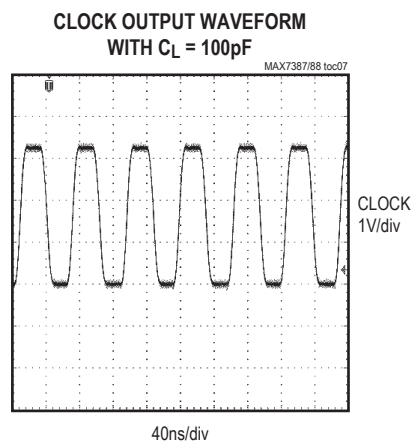
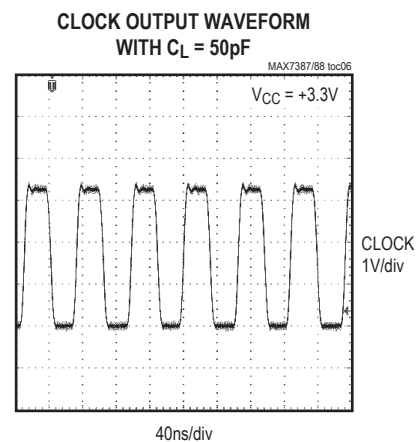
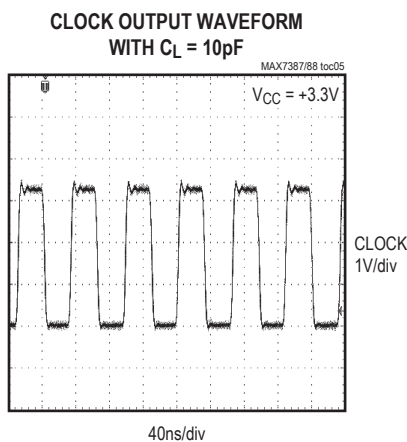
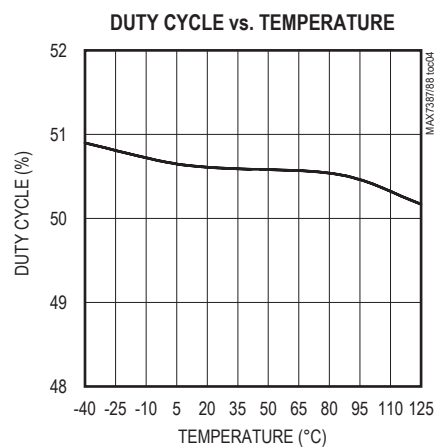
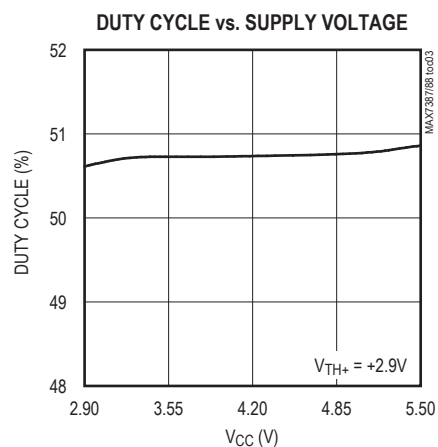
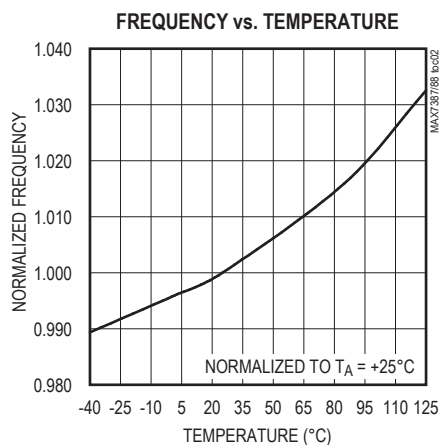
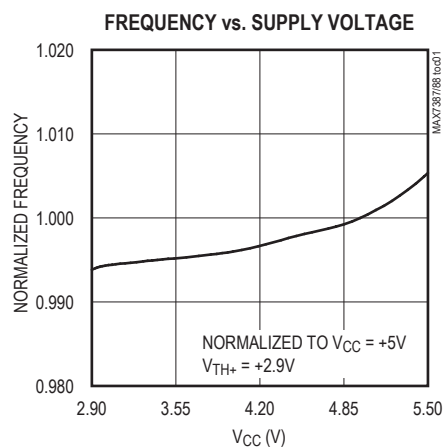
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK Duty Cycle		(Note 2)		45	50	55	%
CLOCK Output Jitter		Observation for 20s using a 500MHz oscilloscope		310			ps RMS
Output Rise Time	t _R	CLOAD = 10pF, 10% to 90% of full scale (Note 2)		2.5		7.0	ns
Output Fall Time	t _F	CLOAD = 10pF, 90% to 10% of full scale (Note 2)		2.8		7.5	ns
INTERNAL POWER-ON RESET							
Reset Voltage	V _{TH+}	V _{CC} rising, Table 2	T _A = +25°C	V _{TH} - 1.5%		V _{TH} + 1.5%	V
			T _A = -40°C to +125°C	V _{TH} - 2.5%		V _{TH} + 2.5%	
	V _{TH-}	V _{CC} falling		0.98 x V _{TH+}			
Reset Timeout Period	t _{RST}	Figures 1, 2		86	135	250	μs
WATCHDOG							
Watchdog Timeout Period (Figure 2)	t _{WDG}	WDS1 = GND, WDS2 = GND		11	16	22	ms
		WDS1 = open, WDS2 = GND		22	32	44	
		WDS1 = V _{CC} , WDS2 = GND		44	64	88	
		WDS1 = GND, WDS2 = open		88	128	177	
		WDS1 = open, WDS2 = open		177	256	354	
		WDS1 = V _{CC} , WDS2 = open		354	512	708	
		WDS1 = GND, WDS2 = V _{CC}		708	1024	1416	
		WDS1 = open, WDS2 = V _{CC}		1416	2048	2832	
		WDS1 = WDS2 = V _{CC} (watchdog disabled)					
POWER FAIL							
Power-Fail Select Threshold	V _{SEL}	PFI input		0.65 x V _{CC}		0.85 x V _{CC}	V
V _{CC} Monitoring Threshold (Internal Threshold)	V _{ITH}	V _{CC} rising		4.06	4.38	4.60	V
Internal Threshold Hysteresis	V _{IHYST}	V _{CC} falling		1.0	2	4.0	%V _{ITH}
PFI Monitoring Threshold (External Threshold)	V _{ETH}	PFI rising		0.9	1.1	1.4	V
External Threshold Hysteresis	V _{EHYST}	PFI falling		1.0	3.5	8.0	%V _{ETH}

Note 1: All parameters are tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design. Not production tested.

Typical Operating Characteristics

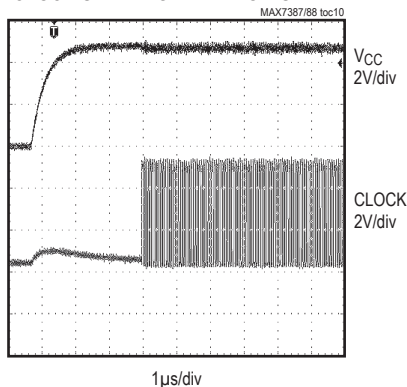
(Typical Application Circuit, $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)



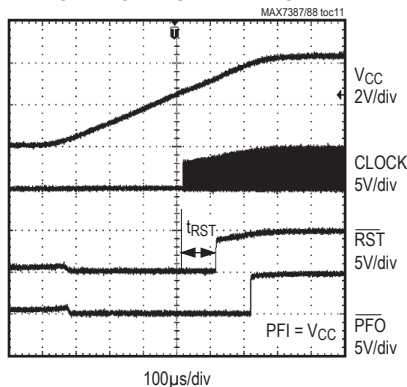
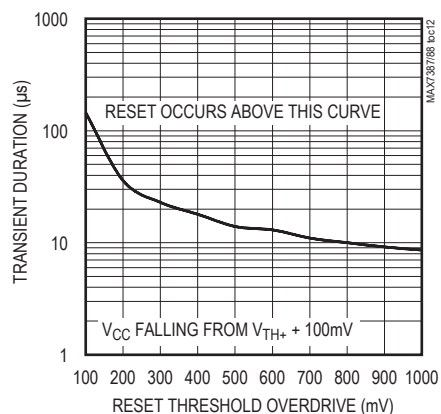
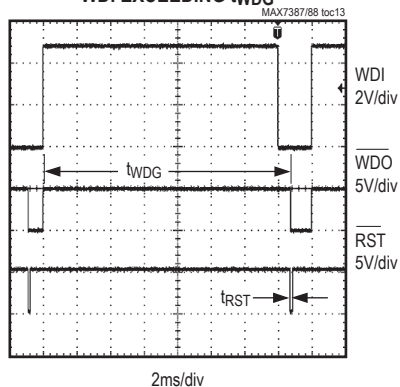
Typical Operating Characteristics (continued)

(Typical Application Circuit, $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

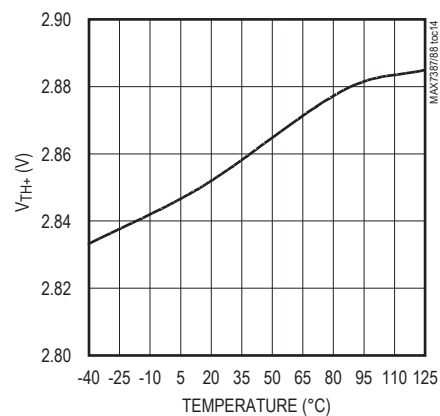
CLOCK SETTLING TIME FROM START



POWER-ON RESET BEHAVIOR

MAXIMUM V_{CC} TRANSIENT DURATION
vs. RESET THRESHOLD OVERDRIVERESPONSE OF \overline{RST} AND \overline{WDO}
WDI EXCEEDING t_{WDG} 

RISING THRESHOLD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX7387	MAX7388		
1	—	PFI	Power-Fail Input. PFI monitors the condition of either an external supplied voltage or V _{CC} . See the <i>Power Fail</i> section for more details.
2	1	V _{CC}	Power Input. Connect V _{CC} to the power supply. Bypass V _{CC} to GND with a 1μF capacitor. Install the bypass capacitor as close to the device as possible.
3	2	WDS1	Watchdog Timeout Select Input 1. Connect WDS1 and WDS2 to V _{CC} , GND, or V _{CC} /2, as shown in Table 1, to set the watchdog timeout period.
4	3	WDS2	Watchdog Timeout Select Input 2. Connect WDS2 and WDS1 to V _{CC} , GND, or V _{CC} /2, as shown in Table 1, to set the watchdog timeout period.
5	4	GND	Ground
6	—	$\overline{\text{WDO}}$	Watchdog Output. Open-drain watchdog output asserts low if WDI is not toggled within the watchdog timeout period.
7	5	$\overline{\text{PFO}}$	Power-Fail Output. Open-drain output asserts when the voltage being monitored drops below the power-fail threshold voltage.
8	6	WDI	Watchdog Input. A rising edge on WDI resets the watchdog timer. If WDI does not receive a rising edge within the watchdog timeout period (t _{WDG}), RST/ $\overline{\text{RST}}$ asserts. The watchdog timeout period is programmable through WDS1 and WDS2. Connect WDS1 and WDS2 to V _{CC} to disable watchdog timer.
9	7	RST/ $\overline{\text{RST}}$	Reset Output. Reset output is available in one of three configurations: push-pull RST, push-pull $\overline{\text{RST}}$, or open-drain $\overline{\text{RST}}$. The reset output occurs if any combination of the following conditions occurs: reset output is asserted during power-up and whenever V _{CC} is below the reset threshold level; for devices with WDI, reset output asserts when WDI does not receive a rising edge within the watchdog timeout period.
10	8	CLOCK	Clock Output

Detailed Description

The MAX7387/MAX7388 replace ceramic resonators, crystals, and supervisory functions for microcontrollers in 3.3V and 5V applications.

The MAX7387/MAX7388 provide a clock source together with integrated reset, watchdog, and power-fail functions. The watchdog timer is pin programmable and provides watchdog timeout values in the 16ms to 2048ms range. The power-fail output provides early warning of power failure. The power-fail threshold on the MAX7388 is internally set. The MAX7387 features a programmable power-fail threshold, which is configurable to detect either an external voltage or the V_{CC} supply voltage to the device. The MAX7387 also provides a separate watchdog output that is used as a status indicator or to control safety-critical system elements.

The integrated reset and watchdog functions provide the power-supply monitoring functions necessary to ensure correct microcontroller operation. The reset circuit has built-in power-supply transient immunity and provides both power-on reset and power-fail or brownout reset functionality. Two standard factorytrimmed reset levels are available. The watchdog timer is programmable to eight individual timeout values and may be disabled for test purposes.

A power-fail function is provided for power-supply voltage monitoring and can provide advance notice of an impending power failure. Parts with power-fail input (MAX7387) monitor external power-supply voltages through an external resistive divider. Connect PFI to V_{CC} to monitor V_{CC}.

Clock Output (CLOCK)

The push-pull clock output (CLOCK) drives a groundconnected 1k Ω load or a positive supply connected 500 Ω load to within 300mV of either supply rail. CLOCK remains stable over the full operating voltage range and does not generate short output cycles during either power-on or power-off. A typical startup characteristic is shown in the *Typical Operating Characteristics* section.

Reset

The reset function drives the microcontroller reset input to prevent operation in the cases of the initial power-on setting, low power-supply voltages, and the failed watchdog operations. Three reset output versions are available: push-pull RST, push-pull $\overline{\text{RST}}$, and open-drain $\overline{\text{RST}}$. The reset timeout period (t_{RST}) is nominally 135s.

Power-On Reset (POR)

The internal power-on reset (POR) circuit detects the power-supply voltage (V_{CC}) level at startup. The POR circuit starts the oscillator when V_{CC} exceeds the reset rising threshold level ($V_{\text{TH+}}$). The reset output remains asserted from the time V_{CC} crosses the $V_{\text{TH+}}$ and continues to be asserted for the reset timeout period (t_{RST}).

Upon completion of the reset timeout, the reset output is released. See Figure 1.

Low-Voltage Lockout

The reset output asserts whenever V_{CC} drops below the reset falling threshold, $V_{\text{TH-}}$. The difference between the reset rising and falling threshold values is $V_{\text{TH+}} - (V_{\text{TH-}})$. The nominal hysteresis value is 2% of the reset rising threshold value. The reset detection circuitry provides filtering to prevent triggering on negative voltage spikes. See the *Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive* typical operating circuit.

Figure 1 shows the reset output ($\text{RST}/\overline{\text{RST}}$) behavior during power-up and brownout.

Watchdog

The watchdog function provides microprocessor monitoring by requiring the microprocessor to toggle an output pin to indicate correct operation. The WDI input monitors the port signal and resets the watchdog timer on receipt of a rising edge. If an edge is not received within the required watchdog timeout period, the watchdog circuit initiates a reset cycle. The internal watchdog circuits are

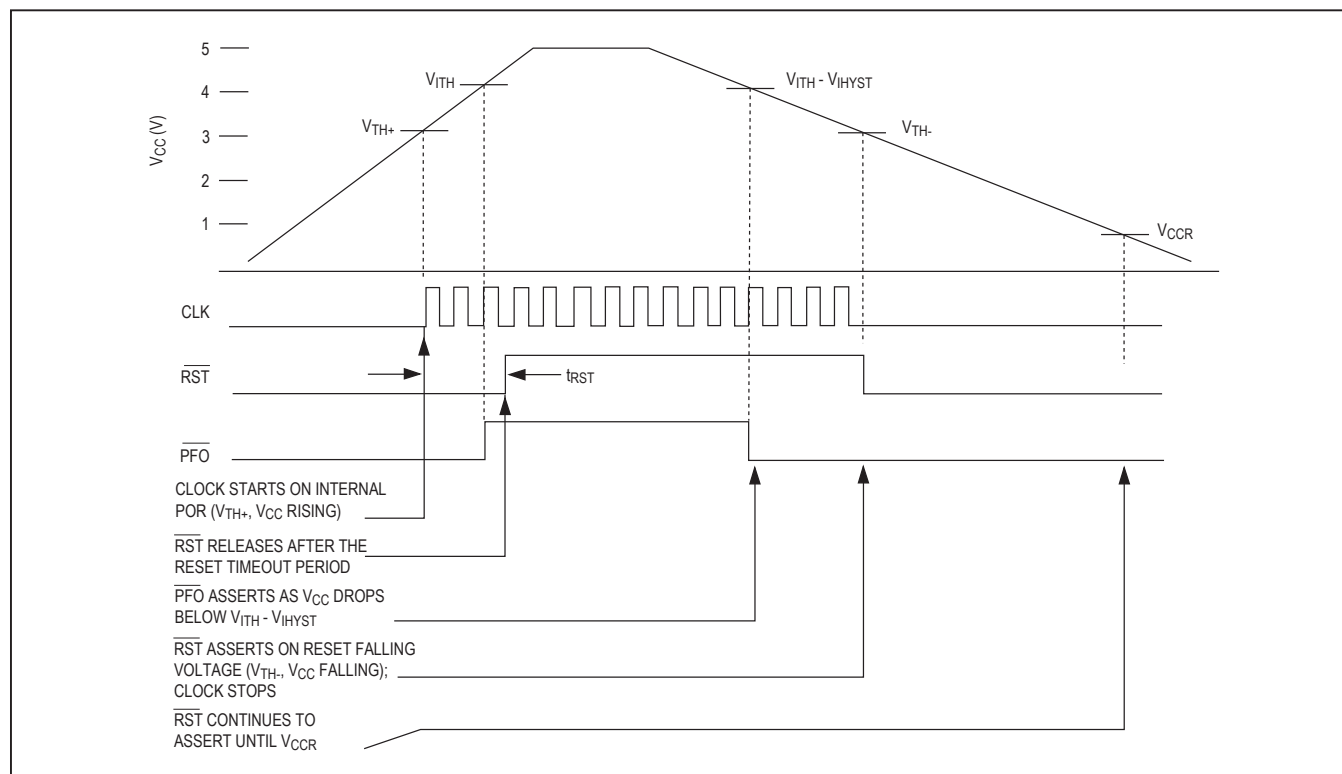


Figure 1. $\text{RST}/\overline{\text{RST}}$ and $\overline{\text{PFO}}$ Behavior During Power-Up and Brownout

reset and the watchdog timer restarts at the end of the reset cycle (RST/ $\overline{\text{RST}}$ output releases).

For the MAX7387, the $\overline{\text{WDO}}$ output asserts if the WDI input does not receive a rising edge within the watchdog timeout period. $\overline{\text{WDO}}$ output remains asserted until a valid edge is received on the WDI input, signifying correct microprocessor operation. The $\overline{\text{WDO}}$ output can be used as a status indicator either to the microprocessor or to an external device, such as a fault-indicating LED or sounder. The $\overline{\text{WDO}}$ output is an open-drain output. The power-up condition of the $\overline{\text{WDO}}$ output is high (not asserted).

The operation of the watchdog and reset function is illustrated in Figure 2.

The watchdog timeout period is set to one of nine possible values by pin strapping WDS1 and WDS2. Each control input has three possible values assigned by connection to GND, V_{CC} , or $V_{CC}/2$ (see Table 1). One of the assigned values disables the watchdog function and is intended for customer use during test. The watchdog timer is disabled while the RST/ $\overline{\text{RST}}$ output is asserted.

Power Fail

MAX7388 Power Fail

The power-fail function provides early warning of a power failure. The power-fail comparator threshold is internally set to 4.38V V_{CC} rising threshold (V_{ITH}). The open-drain $\overline{\text{PFO}}$ asserts low if the V_{CC} supply voltage drops below the V_{CC} falling threshold value. The V_{CC} falling threshold is nominally 2% below the V_{CC} rising threshold.

MAX7387 Power Fail

Internal (V_{CC}) detection is configured by connecting PFI to V_{CC} . The internal V_{CC} rising threshold (V_{ITH}) is set at 4.38V. The open-drain $\overline{\text{PFO}}$ asserts low if the V_{CC} supply voltage drops below the V_{CC} falling threshold value (V_{HYST}). The V_{CC} falling threshold is nominally 2% below the V_{CC} rising threshold.

Applications Information

Interfacing to a Microcontroller Clock Input

The CLOCK output is a push-pull, CMOS logic output, which directly drives any microprocessor (μP) or microcontroller (μC) clock input. There are no impedance-

Table 1. Watchdog Timeout Periods

WDS1	WDS2	WATCHDOG TIMEOUT PERIOD (ms)		
		MIN	TYP	MAX
GND	GND	11	16	22
$V_{CC}/2$ = open	GND	22	32	44
V_{CC}	GND	44	64	88
GND	$V_{CC}/2$ = open	88	128	177
$V_{CC}/2$ = open	$V_{CC}/2$ = open	177	256	354
V_{CC}	$V_{CC}/2$ = open	354	512	708
GND	V_{CC}	708	1024	1416
$V_{CC}/2$ = open	V_{CC}	1416	2048	2832
V_{CC}	V_{CC}	Disabled		

Note: WDS1 or WDS2 is pulled to open if left floating.

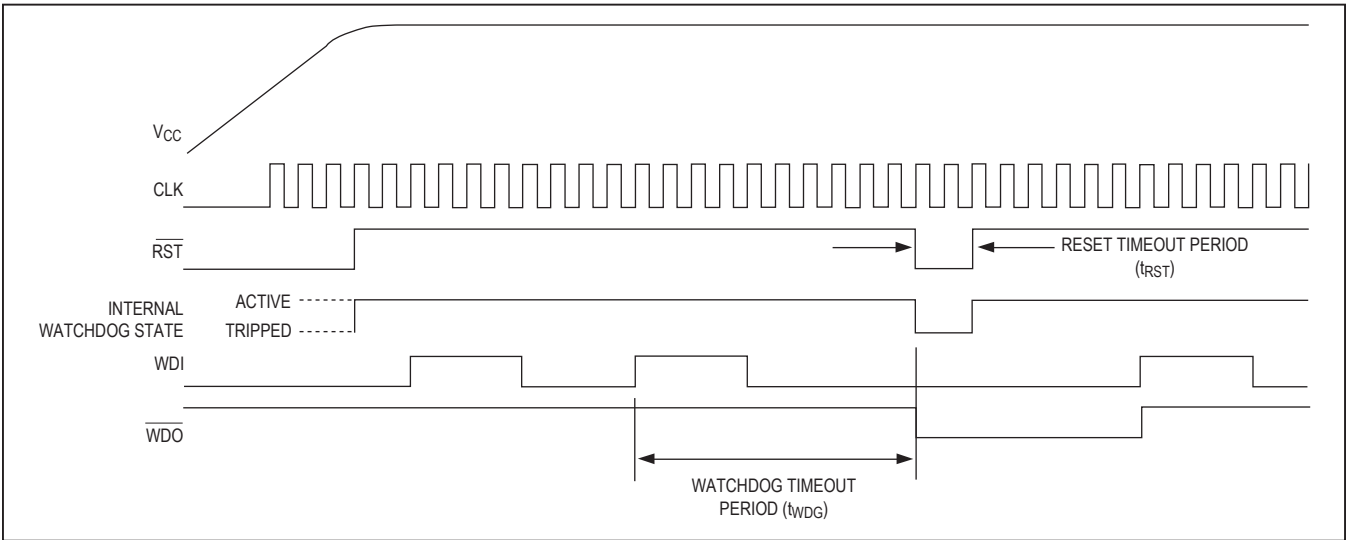


Figure 2. Watchdog Timing Diagram

matching issues when using the MAX7387/MAX7388. Operate the MAX7387/MAX7388 and microcontroller (or other clock input device) from the same supply voltage level. Refer to the microcontroller data sheet for clock-input compatibility with external clock signals.

The MAX7387/MAX7388 require no biasing components or load capacitance. When using the MAX7387/MAX7388 to retrofit a crystal oscillator, remove all biasing components from the oscillator input.

Power-Supply Consideration

The MAX7387/MAX7388 operate with power-supply voltages in the 2.7V to 5.5V range. Power-supply decoupling is needed to maintain the power-supply rejection performance of the MAX7387/MAX7388. Bypass V_{CC} to GND with a 0.1 μ F surface-mount ceramic capacitor. Mount the bypass capacitor as close to the device as possible. If possible, mount the MAX7387 /MAX7388 close to the microcontroller's decoupling capacitor so that additional decoupling is not required.

A larger-value bypass capacitor is recommended if the MAX7387/MAX7388 are to operate with a large capaci-

tive load. Use a bypass capacitor value of at least 1000 times that of the output load capacitance.

Output Jitter

The MAX7387/MAX7388s' jitter performance is given in the *Electrical Characteristics* table as a peak-to-peak value obtained by observing the output of the device for 20s with a 500MHz oscilloscope. Jitter measurements are approximately proportional to the period of the output frequency of the device. Thus, a 4MHz part has approximately twice the jitter value of an 8MHz part.

The jitter performance of all clock sources degrades in the presence of mechanical and electrical interference. The MAX7387/MAX7388 are immune to vibration, shock, and EMI influences, and thus provide a considerably more robust clock source than crystal- or ceramic-resonator-based oscillator circuits.

Table 2. POR Voltage

POWER-ON RESET VOLTAGE (V_{TH})	r
4.38	M
3.96	J
3.44	N
3.34	P
3.13	Q
2.89	S
2.82	V
2.5	X

Note: Standard values are shown in bold. Contact factory for other POR voltages.

Table 3. Reset Output Type

OUTPUT TYPE	s
Push-pull \overline{RST}	A
Push-pull \overline{RST}	B
Open-drain \overline{RST}	C

Note: Standard values are shown in bold. Contact factory for other output types.

Table 4. Clock Output Frequency

CLOCK FREQUENCY (f_{CLOCK}) (MHz)	ff
4	RD
8	TP
12	VB
16	WB

Note: Contact factory for other frequencies.

Selector Guide

PART	FREQUENCY RANGE (MHz)	RESET FUNCTION	WATCHDOG INPUT (WDI)/ WATCHDOG OUTPUT (\overline{WDO})	POWER-FAIL INPUT (PFI)/ POWER-FAIL OUTPUT (\overline{PFO})	SPEED	PIN-PACKAGE
MAX7387	1 to 16	Yes	Yes/yes	Yes/yes	—	10 μ MAX
MAX7388	1 to 16	Yes	Yes/no	No/yes	—	8 μ MAX
MAX7389	1 to 16	Yes	Yes/yes	—	—	8 μ MAX
MAX7390	1 to 16	Yes	Yes/no	—	Yes	8 μ MAX
MAX7391	1 to 16	Yes	—	Yes/yes	Yes	8 μ MAX

Note: Other versions with different features are available. Refer to the MAX7389/MAX7390 and MAX7391 data sheets.

**MAX7387
MAX7388**

The block diagram illustrates the internal architecture of the MAX7387 and MAX7388. Key components include:

- POWER-ON RESET**: Receives the **WDI** input and provides a reset signal to the **WATCHDOG TIMER** and the **OSCILLATOR**.
- OSCILLATOR**: Provides a **CLOCK** signal to the **WATCHDOG TIMER** and the **RESET TIMER**.
- PRESCALER**: Receives the **CLOCK** signal and provides input to the **WATCHDOG TIMER** and the **RESET TIMER**.
- WATCHDOG TIMER**: Receives **WDS1** and **WDS2** inputs. Its output is connected to an N-channel MOSFET, which drives the **PFO** pin.
- RESET TIMER**: Receives the **CLOCK** signal and provides input to the **WATCHDOG TIMER** and the **RESET** pin.
- RESET**: Receives the output of an AND gate (which combines the **WATCHDOG TIMER** output and the **RESET TIMER** output) and provides a reset signal to the **WATCHDOG TIMER**.
- INTERNAL (V_{CC} DETECTION)**: Provides input to a comparator.
- Comparator**: Receives the output of the **INTERNAL (V_{CC} DETECTION)** block and the **V_{TH}** threshold voltage. Its output is connected to an N-channel MOSFET, which drives the **PFO** pin.
- PFI***: Provides input to the **WATCHDOG TIMER** and the **INTERNAL (V_{CC} DETECTION)** block.
- GND**: Ground connection.

*MAX7387 ONLY

POWER SUPPLY

DC-DC

5V

R1

R2

WDS1

WDS2

PFI*

MAX7387

MAX7388

VCC

GND

RST/RST

PFO

WDI

WDO*

CLOCK

RST/RST

INT

I/O PORT

I/O PORT

OSC1

uC

*MAX7387 ONLY

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 μ max	U10-2	21-0061	90-0330
8 μ max	U8-1	21-0036	90-0092

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/14	No /V OPNs; removed Automotive reference from <i>Applications</i> section	1

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