MAX2837

2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

General Description

The MAX2837 direct-conversion zero-IF RF transceiver is designed specifically for 2.3GHz to 2.7GHz wireless broadband systems. The MAX2837 completely integrates all circuitry required to implement the RF transceiver function, providing RF-to-baseband receive path; and baseband-to-RF transmit path, VCO, frequency synthesizer, crystal oscillator, and baseband/control interface. The device includes a fast-settling sigma-delta RF synthesizer with smaller than 20Hz frequency steps and a crystal oscillator, which allows the use of a low-cost crystal in place of a TCXO. The transceiver IC also integrates circuits for on-chip DC offset cancellation, I/Q error, and carrier-leakage detection circuits. Only an RF bandpass filter (BPF), crystal, RF switch, PA, and a small number of passive components are needed to form a complete wireless broadband RF radio solution.

The MAX2837 completely eliminates the need for an external SAW filter by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filters along with the Rx and Tx signal paths are optimized to meet stringent noise figure and linearity specifications. The device supports up to 2048 FFT OFDM and implements programmable channel filters for 1.75MHz to 28MHz RF channel bandwidths. The transceiver requires only 2µs Tx-Rx switching time, which includes frequency transient settling. The IC is available in a small, 48-pin thin QFN package measuring only 6mm x 6mm x 0.8mm.

Applications

- 802.16-2004 Fixed WiMAX®
- Korea Wibro and 802.16e Mobile WiMAX
- Dual Mode™ WiMAX/802.11b/g Wi-Fi
- Proprietary Wireless Broadband Systems
- 4G/LTE Systems

Features

- 2.3GHz to 2.7GHz Wideband Operation
- Complete RF Transceiver, PA Driver, and Crystal Oscillator
  - 0dBm Linear OFDM Transmit Power
  - -70dBr Tx Spectral Emission Mask
  - 2.3dB Rx Noise Figure
  - Tx/Rx I/Q Error and LO Leakage Detection
  - Monolithic Low-Noise VCO with -39dBc Integrated Phase Noise
  - Programmable Tx I/Q Lowpass Anti-Aliasing Filter
  - Sigma-Delta Fractional-N PLL with 20Hz Step Size
  - 45dB Tx Gain-Control Range
  - 94dB Receive Gain-Control Range
  - 60dB Analog RSSI Instantaneous Dynamic Range
  - 4-Wire SPI Digital Interface
  - I/Q Analog Baseband Interface
  - Digitally Tuned Crystal Oscillator
  - On-Chip Digital Temperature Sensor Read-Out
- +2.7V to +3.6V Transceiver Supply
- Low-Power Shutdown Current
- Small 48-Pin Thin QFN Package (6mm x 6mm x 0.8mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2837ETM+TD	-40°C to +85°C	48 TQFN-EP*

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

***Pin Configuration* appears at end of data sheet.**

19-0806; Rev 2; 7/15

maxim integrated™

Absolute Maximum Ratings

V_{CCLNA}, V_{CCTXMX}, $V_{CCTXPAD}$, V_{CCDIG}, V_{CCCP}, V_{CCXTAL}, V_{CCVCO}, $V_{CCRXVGA}$, V_{CCRXFL} and V_{CCRXMX} to GND .....-0.3V to +3.9V

B1–B7, TXRF_, $\overline{CS}$, SCLK, DIN, DOUT, TXBBI_, TXBBQ_, RXHP, RXBBI_, RXBBQ_, RSSI, ENABLE, BYPASS, CPOUT_, CLOCKOUT, XTAL1, XTAL2, RXRF_,RXENABLE, TXENABLE to GND..... -0.3V to (Operating V_{CC} + 0.3V)

RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT_, DOUT, CLOCKOUT, PABIAS Short-Circuit Duration..... 10s

RF Input Power .....+10dBm

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derates 37mW/°C above +70°C) 2.96W

Operating Temperature Range..... -40°C to +85°C

Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +160°C

Lead Temperature (soldering, 10s) .....+260°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.7V to 3.6V, Rx set to the maximum gain; $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open; 90mV_{RMS} differential I and Q signals applied to I, Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, registers set to recommended settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$	2.7		3.6	V
Supply Current	Shutdown mode, T_A = +25°C		10		µA
	Standby mode		35	45	mA
	Rx mode		91	110	
	Tx mode, T_A = +25°C		145	170	
	Rx calibration mode		135	160	
	Tx calibration mode		110	135	
Rx I/Q Output Common-Mode Voltage	D9:D8 = 00 in A4:A0 = 00100	0.85	1.0	1.20	V
	D9:D8 = 01 in A4:A0 = 00100		1.1		
	D9:D8 = 10 in A4:A0 = 00100		1.2		
	D9:D8 = 11 in A4:A0 = 00100		1.35		
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled	0.5		1.2	V
Tx Baseband Input Bias Current	Source current		10	20	µA
LOGIC INPUTS: ENABLE, TXENABLE, RXENABLE, SCLK, DIN, $\overline{CS}$, B7:B1, RXHP					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA

DC Electrical Characteristics (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.7V to 3.6V, Rx set to the maximum gain; $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open; 90mV_{RMS} differential I and Q signals applied to I, Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, registers set to recommended settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS: DOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC Electrical Characteristics—Rx MODE

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at 90mV_{RMS} (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT TO BASEBAND I/Q OUTPUTS						
RF Input Frequency Range			2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Input Frequency Range	Tested at band edges and band center			0.8		dB
RF Input Return Loss	All LNA gain settings			13		dB
Total Voltage Gain	T_A = -40°C to +85°C	Maximum gain, B7:B1 = 0000000	90	99		dB
		Minimum gain, B7:B1 = 1111111		5	13	
RF Gain Steps	From max RF gain to max RF gain - 8dB			8		dB
	From max RF gain to max RF gain - 16dB			16		
	From max RF gain to max RF gain - 32dB			32		
Gain Change Settling Time	Any RF or baseband gain change; gain settling to within P1dB of steady state; RXHP = 1			0.2		µs
	Any RF or baseband gain change; gain settling to within P0.1dB of steady state; RXHP = 1			2		
Baseband Gain Range	From maximum baseband gain (B5:B1 = 00000) to minimum baseband gain (B5:B1 = 11111), T_A = -40°C to +85°C		58	62	66	dB
Baseband Gain Minimum Step Size				2		dB
DSB Noise Figure	Voltage gain R 65dB with max RF gain (B7:B6 = 00)			2.3		dB
	Voltage gain = 50dB with max RF gain - 8dB (B7:B6 = 01)			5.5		
	Voltage gain = 45dB with max RF gain - 16dB (B7:B6 = 10)			17		
	Voltage gain = 15dB with max RF gain - 32dB (B7:B6 = 11)			27		

AC Electrical Characteristics—Rx MODE (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at 90mV_{RMS} (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
In-Band Input P-1dB	Max RF gain (B7:B6 = 00)			-37		dBm
	Max RF gain - 8dB (B7:B6 = 01)			-29		
	Max RF gain - 16dB (B7:B6 = 10)			-21		
	Max RF gain - 32dB (B7:B6 = 11)			-4		
Maximum Output Signal Level	Over passband frequency range; at any gain setting; 1dB compression point			2.5		V_{P-P}
Out-of-Band Input IP3 (Note 2)	Max RF gain (B7:B6 = 00), AGC set for -65dBm wanted signal			-11		dBm
	Max RF gain - 8dB (B7:B6 = 01), AGC set for -55dBm wanted signal			-8		
	Max RF gain - 16dB (B7:B6 = 10), AGC set for -40dBm wanted signal			-6		
	Max RF gain - 32dB (B7:B6 = 11), AGC set for -30dBm wanted signal			+16		
I/Q Phase Error	50kHz baseband output; 1σ variation			0.15		Degrees
I/Q Gain Imbalance	50kHz baseband output; 1σ variation			0.1		dB
Rx I/Q Output Load Impedance (R ‖ C)	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			5		pF
I/Q Output DC Droop	After switching RXHP to 0; average over 1µs after any gain change, or 2µs after receive enabled with 100Hz interval AC-coupling, 1σ variation			±1		mV/ms
I/Q Static DC Offset	No RF input signal; measure at 3µs after receive enable; RXHP = 1 for 0 to 2µs and set to 0 after 2µs, 1σ variation			±1		mV
Loopback Gain (for Receiver I/Q Calibration)	Transmitter I/Q input to receiver I/Q output; transmitter B6:B1 = 000011, receiver B5:B1 = 10100 programmed through SPI		-4.5	0	+4.5	dB
RECEIVER BASEBAND FILTERS						
Baseband Filter Rejection	At 15MHz			57		dB
	At 20MHz			75		
	At > 40MHz			90		
Baseband Highpass Filter Corner Frequency	RXHP = 1 (used before AGC completion)			650		kHz
	RXHP = 0 (used after AGC completion) address A4:A0 = 01110	D5:D4 = 00		0.1		
		D5:D4 = 01		1		
		D5:D4 = 10		30		
		D5:D4 = 11		100		

AC Electrical Characteristics—Rx MODE (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at 90mV$_{RMS}$ (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Channel BW Supported by Baseband Filter	A4:A0 = 00010 serial bits D7:D4 = 0000			1.75		MHz
	A4:A0 = 00010 serial bits D7:D4 = 0001			2.25		
	A4:A0 = 00010 serial bits D7:D4 = 0010			3.5		
	A4:A0 = 00010 serial bits D7:D4 = 0011			5.0		
	A4:A0 = 00010 serial bits D7:D4 = 0100			5.5		
	A4:A0 = 00010 serial bits D7:D4 = 0101			6.0		
	A4:A0 = 00010 serial bits D7:D4 = 0110			7.0		
	A4:A0 = 00010 serial bits D7:D4 = 0111			8.0		
	A4:A0 = 00010 serial bits D7:D4 = 1000			9.0		
	A4:A0 = 00010 serial bits D7:D4 = 1001			10.0		
	A4:A0 = 00010 serial bits D7:D4 = 1010			12.0		
	A4:A0 = 00010 serial bits D7:D4 = 1011			14.0		
	A4:A0 = 00010 serial bits D7:D4 = 1100			15.0		
	A4:A0 = 00010 serial bits D7:D4 = 1101			20.0		
	A4:A0 = 00010 serial bits D7:D4 = 1110			24.0		
	A4:A0 = 00010 serial bits D7:D4 = 1111			28.0		
Baseband Gain Ripple	0 to 2.3MHz for BW = 5MHz			1.3		dB_{P-P}
	0 to 4.6MHz for BW = 10MHz			1.3		
Baseband Group Delay Ripple	0 to 2.3MHz for BW = 5MHz			90		ns_{P-P}
	0 to 4.6MHz for BW = 10MHz			50		
Baseband Filter Rejection for 5MHz RF Channel BW	At 3.3MHz			7		dB
	At > 21MHz			85		
Baseband Filter Rejection for 10MHz RF Channel BW	At 6.7MHz			7		dB
	At > 41.6MHz			85		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} ≥ 10kΩ			0.4		V
RSSI Maximum Output Voltage	R_{LOAD} ≥ 10kΩ			2.2		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		800		

AC Electrical Characteristics—Tx MODE

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; f_{REF} = 40MHz, ENABLE = TXENABLE = $\overline{CS}$ = high, and RXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit*. Lowpass filter is set to 10MHz RF channel BW, 90mV_{RMS} sine and cosine signal (or 90mV_{RMS} 64QAM 1024-FFT OFDMA FUSC I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled).) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS					
RF Output Frequency Range		2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Band	Output optimally matched over 200MHz RF BW		2.5		dB
Total Voltage Gain	Max gain; at unbalanced 50Ω balun output		12		dB
Maximum Output Power over Frequency for Any Given 200MHz Band	OFDM signal conforming to spectral emission mask and -36dB EVM after I/Q imbalance calibration by modem (Note 3)		0		dBm
RF Output Return Loss	Given 200MHz band in the 2.3GHz to 2.7GHz range, for which the matching has been optimized		8		dB
RF Gain Control Range			45		dB
Unwanted Sideband Suppression	Without calibration by modem, and excludes modem I/Q imbalance; P_{OUT} = 0dBm		45		dBc
RF Gain-Control Binary Weights	B1		1		dB
	B2		2		
	B3		4		
	B4		8		
	B5		16		
	B6		16		
Carrier Leakage	Relative to 0dBm output power; without calibration by modem		-35		dBc
Tx I/Q Input Impedance (R ‖ C)	Minimum differential resistance		100		kΩ
	Maximum differential capacitance		0.5		pF
Baseband Frequency Response for 5MHz RF Channel BW	0 to 2.3MHz		0.2		dB
	At > 25MHz		80		
Baseband Frequency Response for 10MHz RF Channel BW	0 to 4.6MHz		0.2		dB
	At > 17MHz		80		
Baseband Group Delay Ripple	0 to 2.3MHz (BW = 5MHz)		20		ns
	0 to 4.6MHz (BW = 10MHz)		12		

AC Electrical Characteristics—Frequency Synthesis

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
RF Channel Center Frequency		2.3		2.7	GHz
Channel Center Frequency Programming Minimum Step Size			20		Hz
Charge-Pump Comparison Frequency		11	40		MHz
Reference Frequency Range		11	40	80	MHz
Reference Frequency Input Levels	AC-coupled to XTAL2 pin	800			mV_{P-P}
Reference Frequency Input Impedance (R ‖ C)	Resistance (XTAL2 pin)		10		kΩ
	Capacitance (XTAL2 pin)		1		pF
Programmable Reference Divider Values		1	2	4	
Closed-Loop Integrated Phase Noise	Loop BW = 120kHz; integrate phase noise from 200Hz to 5MHz, charge-pump comparison frequency = 40MHz		-39		dBc
Charge-Pump Output Current	On each differential side		1.6		mA
Close-In Spur Level	f_{OFFSET} = 0 to 1.8MHz		-40		dBc
	f_{OFFSET} = 1.8MHz to 7MHz		-70		
	f_{OFFSET} > 7MHz		-80		
Reference Spur Level			-85		dBc
Turnaround LO Frequency Error	Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes		±50		Hz
Temperature Range over Which VCO Maintains Lock	Relative to the ambient temperature T_A, as long as the VCO lock temperature range is within operating temperature range		T_A ±40		°C
Reference Output Clock Divider Values		1		2	
Output Clock Drive Level	20MHz output, 1x drive setting		1.5		V_{P-P}
Output Clock Minimum Load Impedance (R ‖ C)	Resistance		10		kΩ
	Capacitance		2		pF

AC Electrical Characteristics—Miscellaneous Blocks

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PA BIAS DAC: CURRENT MODE					
Numbers of Bits			6		Bits
Minimum Output Sink Current	D5:D0 = 000000 in A4:A0 = 11100		0		µA
Maximum Output Sink Current	D5:D0 = 111111 in A4:A0 = 11100		310		µA
Compliance Voltage Range		0.8		2.0	V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs		200		ns
DNL			1		LSB
PA BIAS DAC: VOLTAGE MODE					
Output High Level	10mA source current		V_{CC} -0.2		V
Output Low Level	10mA sink current		0.1		V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs		200		ns
CRYSTAL OSCILLATOR					
On-Chip Tuning Capacitance Range	Maximum capacitance, A4:A0 = 11000, D6:D0 =1111111		15.5		pF
	Minimum capacitance, A4:A0 = 11000, D6:D0 =0000000		0.5		
On-Chip Tuning Capacitance Step Size			0.12		pF
ON-CHIP TEMPERATURE SENSOR					
Digital Output Code	Read-out at DOUT pin through SPI A4:A0 = 00111, D4:D0; T_A = +25°C		01111		
	T_A = +85°C		11101		
	T_A = -40°C		00001		

AC Electrical Characteristics—Timing

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING						
Turnaround Time		Measured from Tx or Rx enable rising edge; signal settling to within 0.5dB of steady state; Rx to Tx		2		µs
		Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)		Measured from Tx enable rising edge; signal settling to within 0.5dB of steady state		2		µs

AC Electrical Characteristics—Timing (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx Turn-Off Time (to Standby Mode)		From Tx enable falling edge		0.1		µs
Rx Turn-On Time (from Standby Mode)		Measured from Rx enable rising edge; signal settling to within 0.5dB of steady state		2		µs
Rx Turn-Off Time (to Standby Mode)		From Rx enable falling edge		0.1		µs
4-WIRE SERIAL-INTERFACE TIMING (See Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of CS or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20		ns
Time Between Rising Edge of CS and the Next Rising Edge of SCLK	t_{CS1}			6		ns
Clock Frequency	f_{CLK}				45	MHz
Rise Time	t_R			f_{CLK} / 10		ns
Fall Time	t_F			f_{CLK} / 10		ns
SCLK Falling Edge to Valid DOUT	t_D			12.5		ns

Note 1: Min and max limits guaranteed by test above T_A = +25°C and guaranteed by design and characterization at T_A = -40°C. The power-on register settings are not production tested. Recommended register setting must be loaded after V_{CC} is supplied.

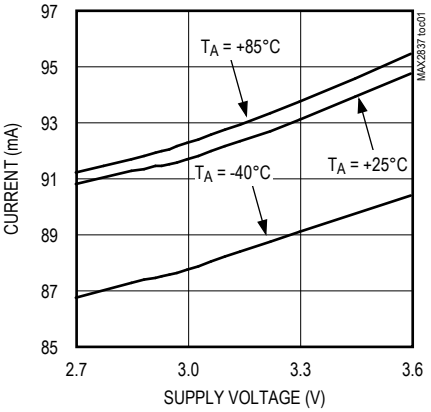
Note 2: Two tones at +25MHz and +39MHz offset with -35dBm/tone. Measure IM3 at 1MHz.

Note 3: Gain adjusted over max gain and max gain - 3dB. Optimally matched over given 200MHz band.

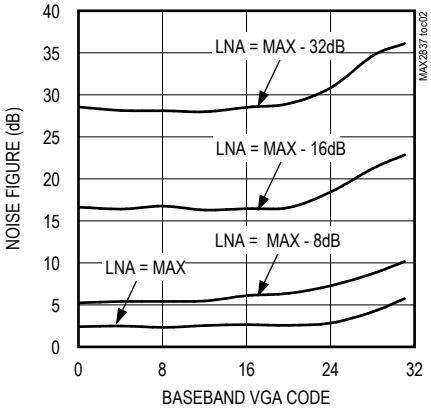
Typical Operating Characteristics

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

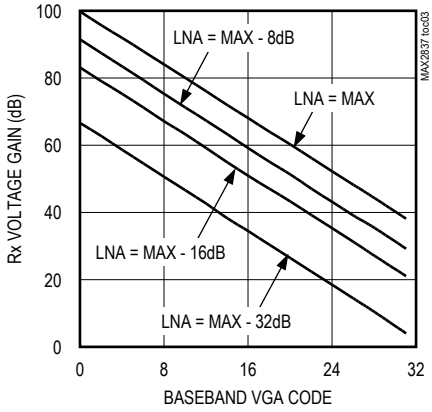
Rx CURRENT vs. SUPPLY VOLTAGE



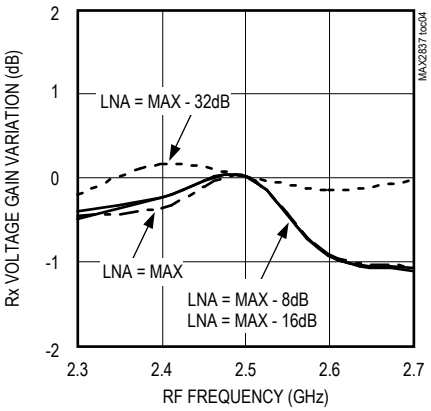
NOISE FIGURE vs. BASEBAND VGA GAIN SETTING



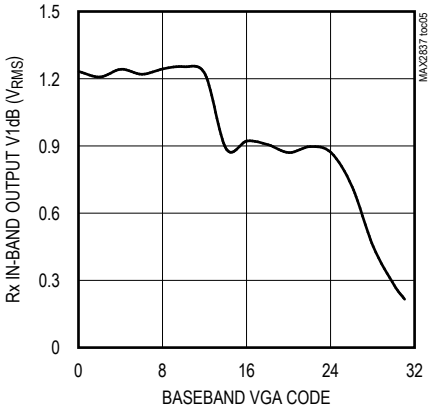
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



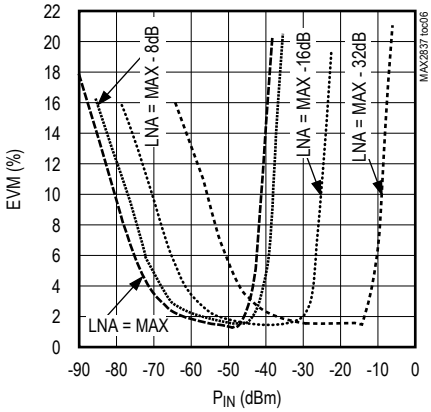
Rx VOLTAGE GAIN VARIATION vs. RF FREQUENCY



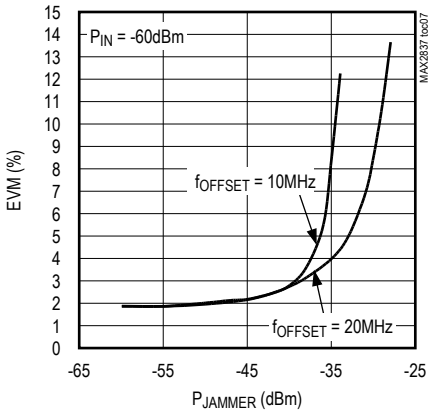
Rx IN-BAND OUTPUT V1dB vs. BASEBAND GAIN SETTING



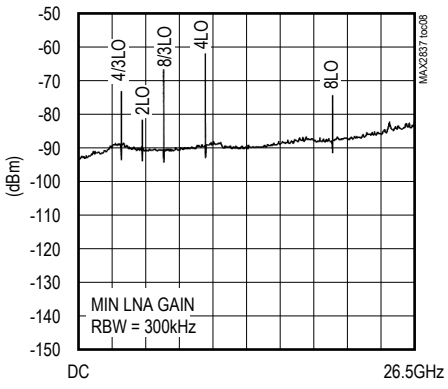
Rx EVM vs. P_{IN}



WiMAX EVM WITH OFDM JAMMER vs. OFFSET FREQUENCY



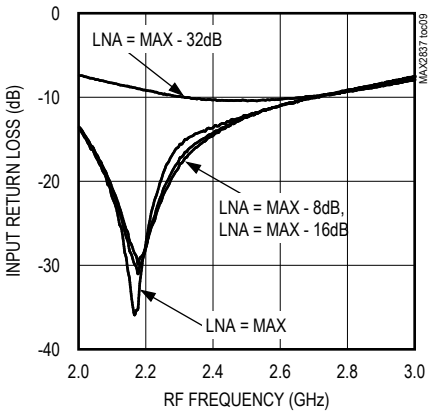
Rx EMISSION SPECTRUM AT LNA INPUT



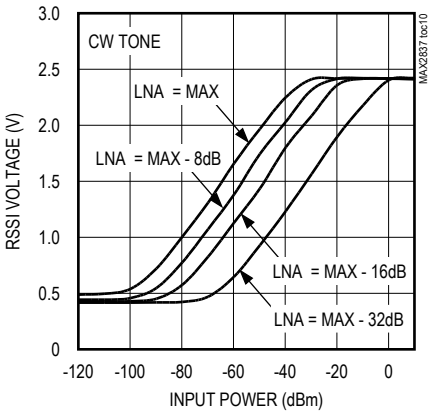
Typical Operating Characteristics (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

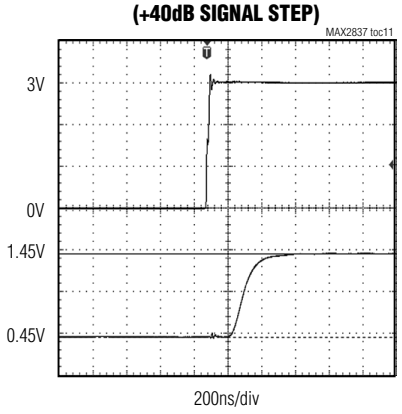
INPUT RETURN LOSS vs. RF FREQUENCY



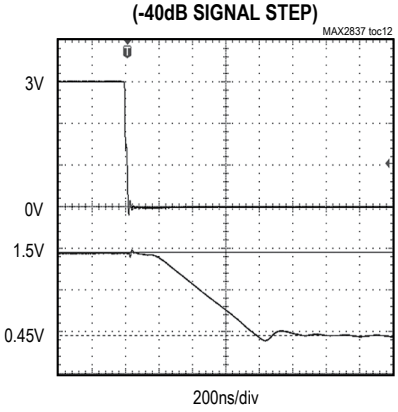
RSSI VOLTAGE vs. INPUT POWER



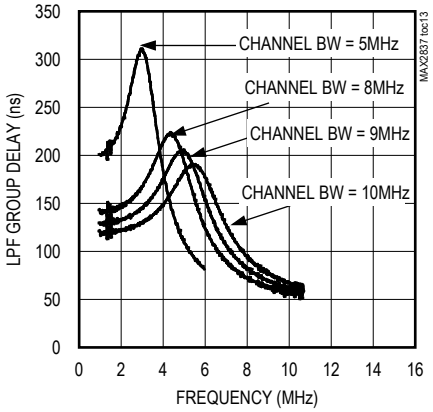
Rx RSSI STEP RESPONSE (+40dB SIGNAL STEP)



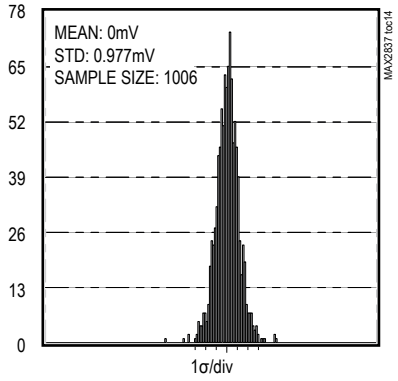
Rx RSSI STEP RESPONSE (-40dB SIGNAL STEP)



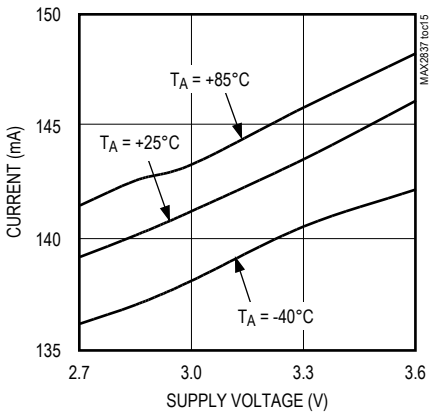
Rx LPF GROUP DELAY vs. FREQUENCY



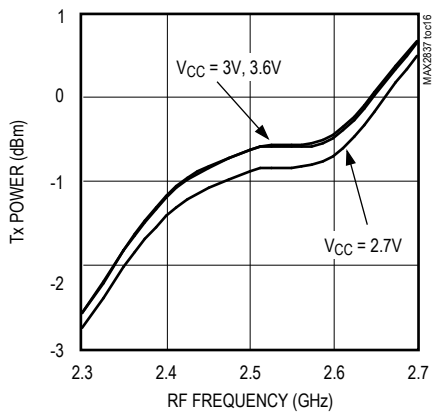
HISTOGRAM: Rx STATIC DC OFFSET



Tx CURRENT vs. SUPPLY VOLTAGE



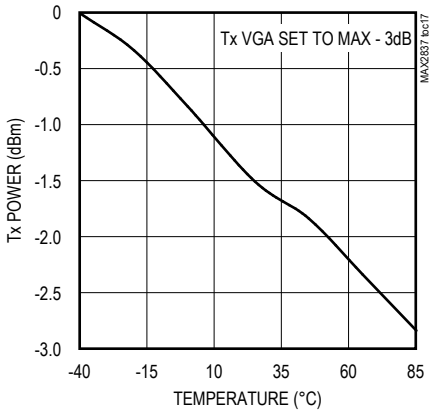
Tx OUTPUT POWER vs. RF FREQUENCY



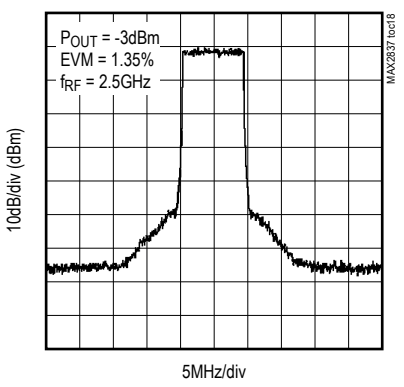
Typical Operating Characteristics (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

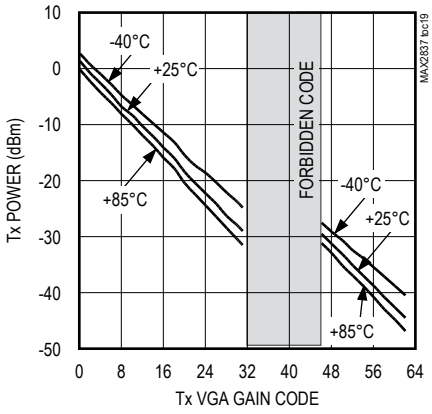
Tx OUTPUT POWER vs. TEMPERATURE



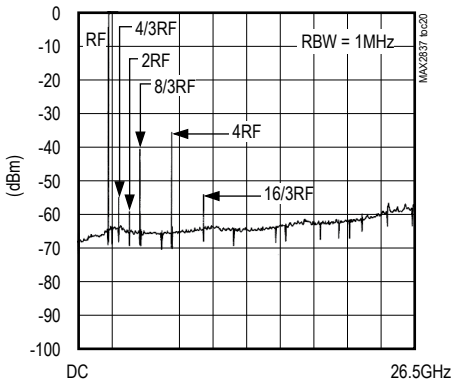
Tx OUTPUT SPECTRUM



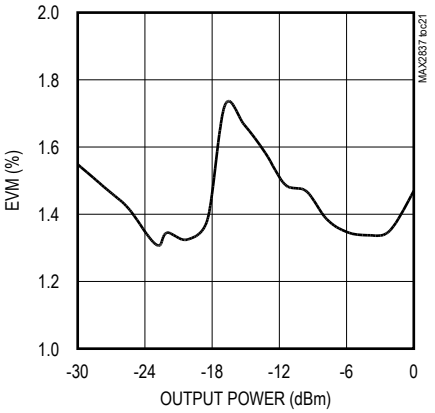
Tx POUT vs. GAIN SETTING



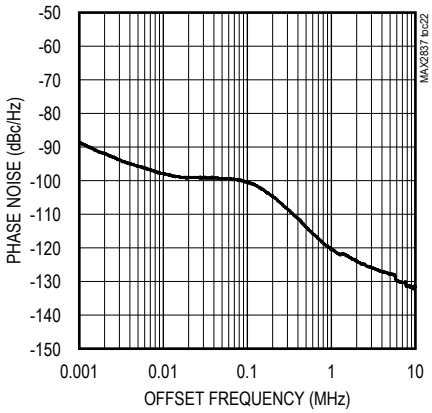
Tx TRANSMIT SPECTRUM FROM DC TO 26.5GHz



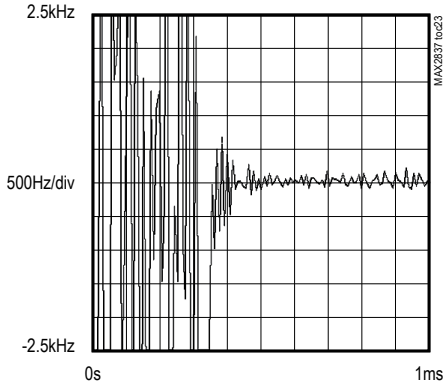
EVM vs. Tx OUTPUT POWER



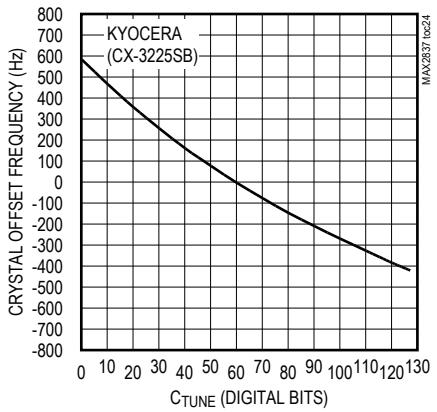
PHASE NOISE vs. OFFSET FREQUENCY



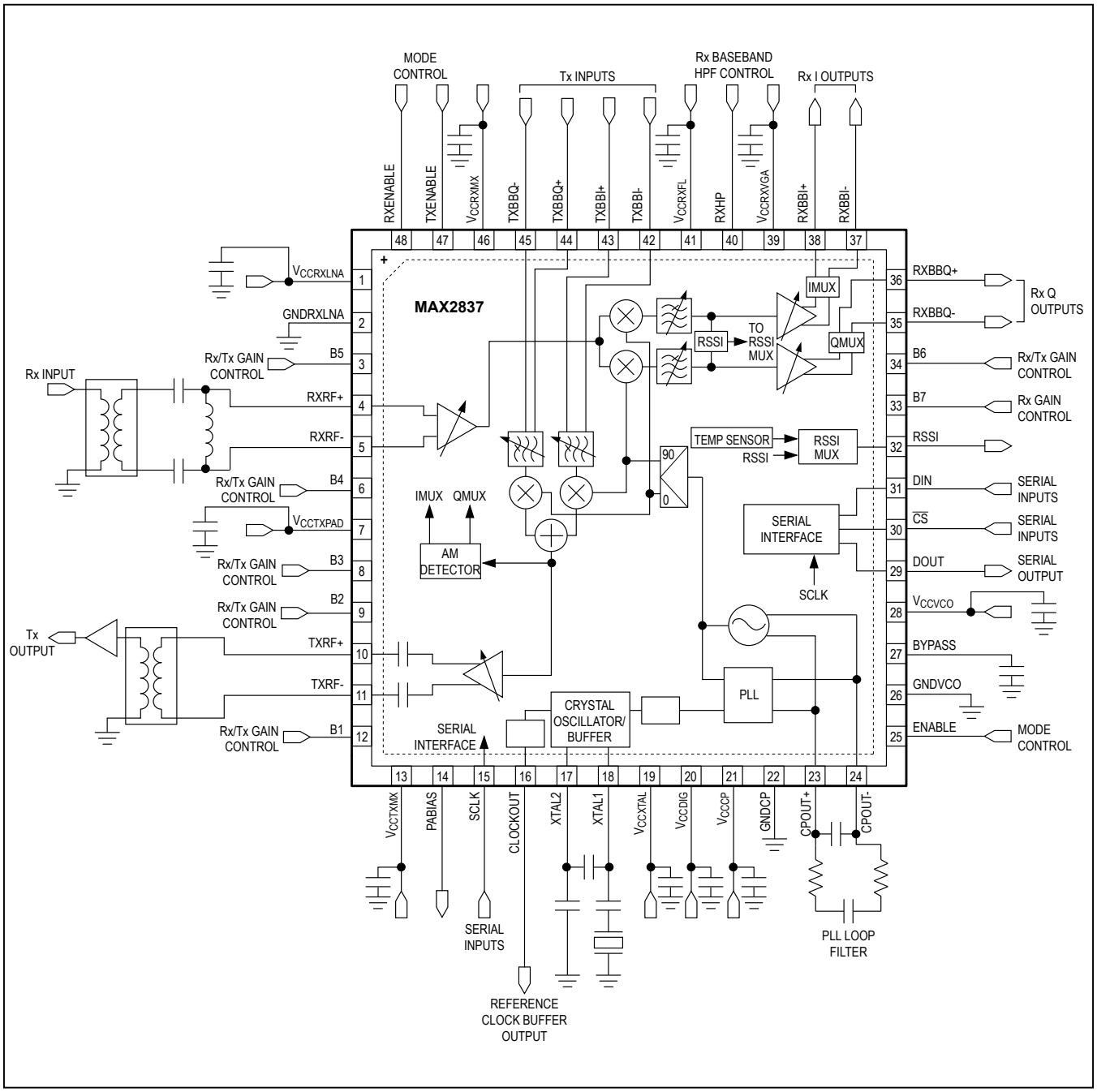
PLL SETTLING TIME FROM SHUTDOWN



CRYSTAL OFFSET FREQUENCY vs. C_{TUNE} BITS



Block Diagram/Typical Operating Circuit



Pin Description

PIN	NAME	FUNCTION
1	$V_{CCRXLNA}$	LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
2	GNDRXLNA	LNA Ground
3	B5	Receiver and Transmitter Gain-Control Logic Input Bit 5
4	RXRF+	LNA Differential Inputs. Inputs are internally DC-coupled. An external shunt inductor and series capacitors match the inputs to 100Ω differential.
5	RXRF-	
6	B4	Receiver and Transmitter Gain-Control Logic Input Bit 4
7	$V_{CCTXPAD}$	Supply Voltage for Power-Amplifier Driver. Bypass with a capacitor as close as possible to the pin.
8	B3	Receiver and Transmitter Gain-Control Logic Input Bit 3
9	B2	Receiver and Transmitter Gain-Control Logic Input Bit 2
10	TXRF+	Power-Amplifier Driver Differential Output. PA driver output is internally matched to a 100I differential. The pins have internal DC-blocking capacitors.
11	TXRF-	
12	B1	Receiver and Transmitter Gain-Control Logic Input Bit 1
13	V_{CCTXMX}	Transmitter Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
14	PABIAS	Transmit PA Bias DAC Output
15	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface (See Figure 1)
16	CLOCKOUT	Reference Clock Buffer Output
17	XTAL2	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
18	XTAL1	Connection for Crystal-Oscillator Off-Chip Capacitors. When using an external reference clock input, leave XTAL1 unconnected.
19	V_{CCXTAL}	Crystal-Oscillator Supply Voltage. Bypass with a capacitor as close as possible to the pin.
20	V_{CCDIG}	Digital Circuit Supply Voltage. Bypass with a capacitor as close as possible to the pin.
21	V_{CCCP}	PLL Charge-Pump Supply Voltage. Bypass with a capacitor as close as possible to the pin.
22	GNDCP	Charge-Pump Circuit Ground
23	CPOUT+	Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT-. (See the Typical Operating Circuit.)
24	CPOUT-	
25	ENABLE	Operation Mode Logic Input. See Table 1 for operating modes.
26	GNDVCO	VCO Ground
27	BYPASS	On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this point.
28	V_{CCVCO}	VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin.
29	DOUT	Data Logic Output of 4-Wire Serial Interface (See Figure 1)
30	$\overline{CS}$	Chip-Select Logic Input of 4-Wire Serial Interface (See Figure 1)
31	DIN	Data Logic Input of 4-Wire Serial Interface (See Figure 1)
32	RSSI	RSSI or Temperature Sensor Multiplexed Analog Output
33	B7	Receiver Gain-Control Logic Input Bit 7
34	B6	Receiver and Transmitter Gain-Control Logic Input Bit 6
35	RXBBQ-	Receiver Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
36	RXBBQ+	
37	RXBBI-	Receiver Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
38	RXBBI+	
39	$V_{CCRXVGA}$	Receiver VGA Supply Voltage
40	RXHP	Receiver Baseband AC-Coupling Highpass Corner Frequency Control Logic Input
41	V_{CCRXFL}	Receiver Baseband Filter Supply Voltage

Pin Description (continued)

PIN	NAME	FUNCTION
42	TXBBI-	Transmitter Baseband I-Channel Differential Inputs
43	TXBBI+	
44	TXBBQ+	Transmitter Baseband Q-Channel Differential Inputs
45	TXBBQ-	
46	V_{CCRXMX}	Receiver Downconverters Supply Voltage. Bypass with a capacitor as close as possible to the pin.
47	TXENABLE	Tx Mode Control Logic Input. See Table 1 for operating modes.
48	RXENABLE	Rx Mode Control Logic Input. See Table 1 for operating modes.
EP	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Table 1. Operating Mode Table

MODE	LOGIC PINS			REGISTER SETTING		CIRCUIT BLOCK STATES				
	ENABLE	RXENABLE	TXENABLE	D1:D0 A4:A0 = 10000		Rx PATH	Tx PATH	PLL, VCO, LO GEN	CALIBRATION SECTIONS ON	CLOCK OUT
Clock-Out	1	0	0	0	0	Off	Off	Off	None	On
Shutdown	0	0	0	0	X	Off	Off	Off	None	Off
Standby	1	0	0	0	1	Off*	Off*	On	None	On
Rx	1	1	0	0	1	On	Off	On	None	On
Tx	1	0	1	0	1	Off	On	On	None	On
Rx Calibration	1	1	0	1	1	On (Except LNA)	Off (Except Upconverters)	On	Tx Baseband Buffer	On
Tx Calibration	1	0	1	1	1	Off	On (Except PA Driver)	On	AM Detector, Rx I/Q Buffers	On

**Blocks of the transceiver can be selectively enabled through SPI.*

Detailed Description

Modes of Operation

The modes of operation for the MAX2837 are clock-out, shutdown, transmit, receive, transmitter calibration, and receiver calibration. See Table 1 for a summary of the modes of operation. The logic input pins—ENABLE (pin 25), TXENABLE (pin 47), and RXENABLE (pin 48)—control the various modes. When the parts are active, various blocks can be shut down individually through SPI.

Shutdown Mode

The MAX2837 features a low-power shutdown mode. Current drain is the minimum possible with the supply voltages applied. In shutdown mode, all circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers. If the supply voltage is applied, the registers are loaded and retained.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, PLL, VCO, and LO generator are on, so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks can be selectively enabled in this mode.

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx BB I and Q outputs. The slow-charging Tx circuits are in a precharged "idle-off" state for fast Rx-to-Tx turnaround time.

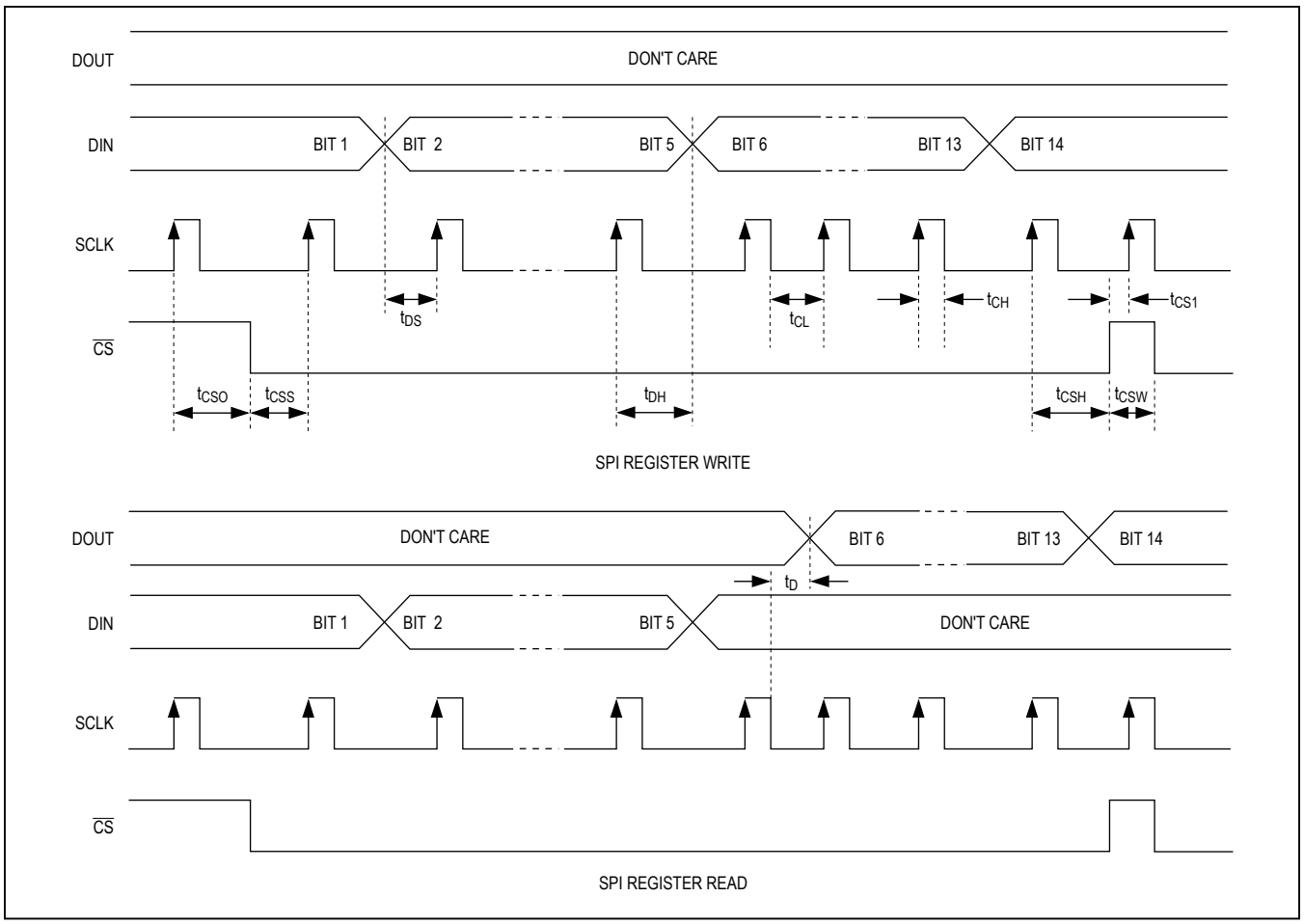


Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

Transmit (Tx) Mode

In transmit mode, all Tx circuit blocks are powered on. The external PA is powered on after a programmable delay using the on-chip PA bias DAC. The slow-charging Rx circuits are in a precharged “idle-off” state for fast Tx-to-Rx turnaround time.

Clock-Out Only

In clock-out mode, the entire transceiver is off except the divided reference clock output on the CLKOUT pin and the clock divider, which remains on.

Temperature Sensor Readout Through DOUT Pin

To estimate chip temperature, on-chip temperature sensor is enabled by programming Address 9 D<1> = 1. The procedure is as follows:

1) Enable temp-sensor by setting Address 9 D<1> = 1. Roughly 100µs to 1ms time is needed to let the temperature sensor output settle to within 5 to 1 degrees.
2) To trigger temperature sensor ADC, program Address 9 D<0> from “0” to “1”. The ADC will acquire the 5-bit logic output in 2µs, temperature sensor needs to be ON (Address 9 D<1> = 1) to maintain the ADC logic output. Note that the ADC trigger should happen AFTER the temp sensor is enabled to get the correct result. Therefore, step 1 and step 2 of this procedure should be carried out on two separate SPI programming events separated by the temp sensor settling time.
3) Note that after the ADC latches its output and you desire to retake another temp sensor temperature reading value, the ADC has to be retriggered to reacquire a new temp sensor value (assuming the temp sensor is already enabled). To do so, program Address 9 D<0> from “1” to “0” then from “0” to “1”. After the ADC latches it digital output in 2µs it shuts off.
4) To read the 5-bit logic output through DOUT pin, apply 4-wire SPI readout programming sequence to Address 7.

VAS Operating Procedure

After power-up, program Address 22 D<1> = 0 such that VAS frequency acquisition starts from VCO band 15, it reduces the worst-case acquisition time by half. VAS acquisition starts after Address 17 is programmed (i.e. rising edge of CSB), it takes the worst-case 896µs to acquire lock.

Wireless LAN or MAN systems do not switch channel frequency often, die temperature may change quite a bit over time and makes PLL out of lock. To relock PLL as soon as possible, the user can program Address 22 D<1> = 1 after the first power-up frequency acquisition. VAS starts from the previous frequency subband and should relock PLL within 112µs.

VAS Readout

The selected VCO subband, Vtune ADC output and VAS accomplished (VASA) signal can be read out through DOUT pin by programming Address 9 D<7:5> = 010 and corresponding Address 26 D<9:6>.

VCO Subband Selection Through SPI

For very fast band selection operation, the user can characterize the mapping between VCO frequencies and corresponding subbands during factory calibration. After programming Address 22 D<0> = 0, the VCO subband can be selected by Address 23 D<4:0>.

Programmable Registers and 4-Wire SPI Interface

The MAX2837 includes 32 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit. The next 5 bits are register address. The 10 least significant bits (LSBs) are register data. Register data is loaded through the 4-wire SPI/MICROWIRE®-compatible serial interface. Data at DIN is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock. During the read mode, register data selected by address bits is shifted out to DOUT at the falling edges of the clock. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. However, every time the power-supply voltage is turned on, the registers are reset to the default values. Note that default register states are not guaranteed, and the user should always reprogram all registers after power-up.

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Table 2. Recommended Register Settings

ADDRESS	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	1	0	1	0	1	0	0	0	0	150
1	0	0	0	0	0	0	0	0	1	0	002
2	0	1	1	1	1	1	0	1	0	0	1F4
3	0	1	1	0	1	1	1	0	0	1	1B9
4	0	0	0	0	0	0	1	0	1	0	00A
5	0	0	1	0	0	0	0	0	0	0	080
6	0	0	0	0	0	0	0	1	1	0	006
7	0	0	0	0	0	0	0	0	0	0	000
8	0	0	1	0	0	0	0	0	0	0	080
9	0	0	0	0	0	1	1	0	0	0	018
10	0	0	0	1	0	1	1	0	0	0	058
11	0	0	0	0	0	1	0	1	1	0	016
12	1	0	0	1	0	0	1	1	1	1	24F
13	0	1	0	1	0	1	0	0	0	0	150
14	0	1	1	1	0	0	0	1	0	1	1C5
15	0	0	1	0	0	0	0	0	0	1	081
16	0	0	0	0	0	1	1	1	0	0	01C
17	0	1	0	1	0	1	0	1	0	1	155
18	0	1	0	1	0	1	0	1	0	1	155
19	0	1	0	1	0	1	0	0	1	1	153
20	1	0	0	1	0	0	0	0	0	1	241
21	0	0	0	0	1	0	1	1	0	1	02D
22	0	1	1	0	1	0	1	0	0	1	1A9
23	1	0	0	1	0	0	1	1	1	1	24F
24	0	1	1	0	0	0	0	0	0	0	180
25	0	1	0	0	0	0	0	0	0	0	100
26	1	1	1	1	0	0	1	0	1	0	3CA
27	1	1	1	1	1	0	0	0	1	1	3E3
28	0	0	1	1	0	0	0	0	0	0	0C0
29	1	1	1	1	1	1	0	0	0	0	3F0
30	0	0	1	0	0	0	0	0	0	0	080
31	0	0	0	0	0	0	0	0	0	0	000

Table 3. Address 0, RXRF Register 1 (Default = 150_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	0	Sets the center frequency of LNA output LC tank. 0 = Band 2.3~2.5GHz 1 = Band 2.5~2.7GHz
D8:D3	101010	Set to recommended value.
D2	0	Enables RX quadrature generation, except for shut down mode. 1 = Enable 0 = Disabled
D1	0	Enables RX Mixer, except for shut down mode. 1 = Enable 0 = Disabled
D0	0	Enables LNA, except for shut down mode. 1 = Enable 0 = Disabled

Table 4. Address 1, RXRF Register 2 (Default = 002_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D5	00000	RX LO IQ calibration SPI control. Active when Address 8 D<9> = 1. Serves as trim word of fuse links independent of Address 8 D<9>. 00000 = +4.0° phase error (default) (Q lags I signal by 94°). … 01111 = 0.0° phase error. … 11111 = -4.0° deg phase error (Q lags I signal by 86°).
D4:D2	000	Adjusts the LNA gain by SPI. Active when Address 8 D<0> = 1. 000 = MAX gain (default) 100 = MAX-8dB 010 = MAX-16dB 110 = MAX-24dB 011 = MAX-32dB 111 = MAX-40dB
D1	1	LNA output tank de_Q resistance tuning in ‘Down’ process. 0 = Nominal 1 = Increase ~2dB gain in down process (default)
D0	0	LNA output LC tank center frequency tuning in ‘Down’ process. 0 = Nominal (default) 1 = Down process

Table 5. Address 2, LPF Register 1 (Default = $1F4_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	Fine-tune the LPF cutoff frequency. 00 = -10% 01 = Nominal (default) 10 = Nominal 11 = +10%
D7:D4	1111	Sets the LPF RF Bandwidth. 0000 = 1.75MHz 0001 = 2.5MHz 0010 = 3.5MHz 0011 = 5.0MHz 0100 = 5.5MHz 0101 = 6.0MHz 0110 = 7.0MHz 0111 = 8.0MHz 1000 = 9.0MHz 1001 = 10.0MHz 1010 = 12.0MHz 1011 = 14.0MHz 1100 = 15.0MHz 1101 = 20.0MHz 1110 = 24.0MHz 1111 = 28.0MHz (default)
D3:D2	01	Sets the mode of the lowpass filter block. Active when Address 6 D<9> = 1. 00 = Rx Calibration 01 = Rx LPF (default) 10 = Tx LPF 11 = LPF Trim
D1	0	Enables the TX input buffer, except for shutdown mode. 1 = Enabled 0 = Disabled
D0	0	Enables the lowpass filter, except for shutdown mode. 1 = Enabled 0 = Disabled

Table 6. Address 3, LPF Register 2 (Default = $1B9_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	011	Tx output (real pole) common-mode voltage adjustment. 000 = 1.00 V 001 = 1.05 010 = 1.10 011 = 1.15 (default) 100 = 1.20 101 = 1.25 110 = 1.30 111 = Not allowed
D6:D0	0111001	Set to recommended value.

Table 7. Address 4, LPF Register 3 and VGA Register 1 (Default = $00A_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	Sets the RX VGA output common-mode voltage. 00 = 0.9V (default) 01 = 1.0V 10 = 1.1V 11 = 1.25V
D7:D6	00	Set to recommended value.
D5	0	RXVGA output MUX and buffer enable, except for shutdown mode. 1 = Enable 0 = Disabled
D4	0	Enables RxVGA, except for shutdown mode. 1 = Enable 0 = Disabled
D3:D0	1010	Set to recommended value.

Table 8. Address 5, VGA Register 2 (Default = 080_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0010	Set to recommended value.
D5	0	RX baseband output select. Used to select RX mode and TX calibration mode output. 0 = RXVGA (default) 1 = TX AM detector for TX calibration mode.
D4:D0	00000	Sets attenuation in the RxVGA. Active when Address 8 D<1 > = 1. 00000 = MAX gain (default) 00001 = MAX - 2dB … 11111 = MIN gain

Table 9. Address 6, VGA Register 3 and RX_TOP SPI bits (Default = 006_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	0	LPF mode mux, LPF_MODE_SEL = 1. 0 = Normal operation 1 = Operating mode is programmed Address 2 D3:D2
D8	0	RSSI operating mode during RX mode. 0 = Off when RXHP = 0 1 = Independent of RXHP
D7	0	RSSI pin output MUX. 0 = Select RSSI 1 = Select Temperature sensor.
D6	0	RSSI enable, except in shutdown mode. 0 = Disable RSSI 1 = Enable RSSI.
D5:D0	000110	Set to recommended value.

Table 10. Address 7, Temperature Sensor 5 bit ADC outputs (Default = 000_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D5	00000	Set to Zeros
D4:D0	00000	Directly connected to Temp Sensor ADC's 5 bit outputs, can be read out by selecting RD_ ENABLE for this register. See the Temperature Sensor Readout Through DOUT Pin section in the Detailed Description.

Table 11. Address 8, RX_TOP SPI bits and RX_BIAS SPI (Default = 080_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	0	RX IQ calibration DAC MUX between trim word and SPI. 0 = Select mux trim word 1 = Select mux SPI
D8:D2	0100000	**Set to recommended value.**
D1	0	Mux VGA gain control bits from SPI. 0 = VGA gain to be controlled by external pins. 1= VGA gain to be controlled by SPI.
D0	0	Mux LNA gain control bits from SPI. 0 = LNA gain to be controlled by external pins. 1 = LNA gain to be controlled by SPI

Table 12. Address 9, RX_TOP SPI bits (Default = 018_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	**Set to recommended value.**
D7:D5	00	DOUT pin output MUX select. 000 = SPI output (default) 001 = PLL lock detect and test output by Address 21 D9:D7. Set Address 21 D9:D7 = 000 for lock detect output.
D4	1	DOUT pin pullup enable. 0 = Open drain 1 = CMOS (default)
D3	1	DOUT pin output drive select. 0 = 1x (dly<4.4ns) 1 = 4x (dly<3.1ns, default)
D2	0	**Set to recommended value.**
D1	0	Temp sensor comparator and clock enable. 0 = Disable (default) 1 = Enable
D0	0	Temp sensor ADC trigger. 0 = Not trigger ADC readout 1 = Trigger ADC readout, ADC is disabled automatically after readout finishes. See the *Temperature Sensor Readout Through DOUT Pin* section in the Detailed Description.

Table 13. Address 10, TX_TOP SPI register 1 (Default = 058_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0001	**Set to recommended value.**
D5:D3	011	Adjust the bandwidth of TX AM detector baseband filter. 000 = Default +12% … 011 = Default bandwidth … 111 = Default – 16%
D2:D1	00	TX AM detector baseband gain control. 00 = Default minimum gain 01 = +10dB 10 = +20dB 11 = +30dB
D0	0	**Set to recommended value.**

Table 14. Address 11, TX_TOP SPI register 2 (Default = 016_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D0	0	**AM detector SPI enable.** **0 = Disable AM detector** **1 = Enable AM detector in all modes except shutdown.**
D4:D1	1011	Sets the TX mixer V2I gain. 0000 = MAX gain 0001 = MAX gain – 0.5dB … 1011 = MAX gain – 5.5dB (default) … 1111 = MAX gain – 7.5dB
D0	0	**Set to recommended value.**

Table 15. Address 12, HPFSM register 1 bits (Default = $24F_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	100	Sets the RXVGA 600kHz highpass corner duration triggered by B7 and B6 switching. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D6:D4	100	Sets the RXVGA 600kHz highpass corner duration triggered by RXEN rising edge. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D3:D2	11	Sets the RXVGA 10MHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)
D1:D0	11	Sets the RXVGA 10MHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)

Table 16. Address 13, HPFSM register 2 bits (Default = 150_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	100	Sets the RXVGA 600kHz highpass corner duration triggered by B7 and B6 switching. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D6:D4	100	Sets the RXVGA 600kHz highpass corner duration triggered by RXEN rising edge. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D3:D2	11	Sets the RXVGA 10MHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)
D1:D0	11	Sets the RXVGA 10MHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)

Table 17. Address 14, HPFSM register 3 bits (Default = $1C5_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9	0	**Selects the RXVGA HPFSM operating mode.** **0 = Mode #1** **1 = Mode #2 which makes use of pin RXHP.**
D8	1	RXVGA HPFSM retriggered by B7 and B6. 0 = Disable 1 = Enable (default)
D7:D6	11	RXVGA highpass corner on-hold selection only during MODE2 when RXHP = 1. 00 = 1kHz 01 = 30kHz 10 = 100kHz 11 = 600kHz (default)
D5:D4	00	Selects the RXVGA final highpass corner. 00 = 100Hz (default) 01 = 1kHz 10 = 30kHz 11 = 100kHz
D3:D2	01	Sets the RXVGA HPCa and HPCd rising edge delay for 100kHz/30kHz/1kHz/100Hz highpass corner. 00 = 0µs 01 = 0.2µs (default) 10 = 0.4µs 11 = 0.6µs
D1:D0	01	RXVGA 1kHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 3.2µs (default) 10 = 6.4µs 11 = 9.6µs

Table 18. Address 15, HPFSM Register 4 Bits (Default = 081_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	**Set to recommended value.**
D7	1	Controls DOUT three-state to be dependent on CSB. 1 = Dout is three-state when CSB is Hi (default) 0 = Dout is not three-state and is independent on CSB
D6	0	Sequence bypass during RXHP 1-->0 transition. 0 = Switch from HPC_STOP_M2<1:0> and programmed sequence (default) 1 = Switch from HPC_STOP_M2<1:0> directly to HPC_STOP<1:0>
D5:D0	000001	Set to recommended value.

Table 19. Address 16, Building Block SPI Enable Control (Default = $01C_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9	0	TX LO I/Q Divider Enable. Enable TX LO divide-by-2 divider except for shutdown. 0 = Disable 1 = Enable
D8	0	TX Mixer SPI Enable. Enable TX Mixer in all modes except shutdown. 0 = Disable 1 = Enable
D7	0	PA Bias DAC TX Mode Enable. Enable PA Bias DAC only in TX mode. Turn-on delay is controlled by Address 27 D9:D6. 0 = Disable (default) 1 = Enable when pin TXENABLE = 1
D6	0	PA Bias DAC SPI Enable. Enable PA Bias DAC in all modes except for shutdown. The turn-on delay is controlled by Address 27 D9:D6. 0 = Disable (default) 1 = Enable except during shutdown mode
D5	0	PA Driver SPI Enable. Enable PA Driver in all modes except shutdown. 0 = Enable by pin combination (default) 1 = Enable except shutdown mode
D3	1	Synthesizer SPI Enable. Enable and disable PLL in all modes except shutdown. Independent of RXEN and TXEN pins. 0 = Disable 1 = Enable except shutdown mode (default)
D2	1	LOGEN SPI Enable. Enable LOGEN in all modes except for shutdown. 0 = Enable by pin combination 1 = Enable except shutdown mode (default)
D1	0	RX/TX Calibration Mode Enable. RX or TX mode is selected by pin RXEN or TXEN. 0 = Normal operation (default) 1 = Calibration mode
D0	0	Chip Enable Bit. Logic AND with pin ENABLE to enable/disable the whole chip except crystal oscillator and CLKOUT pin buffer. 0 = Disable (default) 1 = Enable

Table 20. Address 17, Synthesizer Fractional Divide Ratio #1 (Default = 155_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D9	0101010101	Synthesizer 20-bit Fractional Divide Ratio Bit<9:0>, combine with Address 18 D9:D0 to form the whole fractional word. Default = 0101010101

Table 21. Address 18, Synthesizer Fractional Divide Ratio #2 (Default = 155_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D9	0101010101	Synthesizer 20-bit Fractional Divide Ratio Bit<19:10>, combine with Address 17 D<9:0> to form the whole fractional word. Default = 0101010101

Table 22. Address 19, Synthesizer Integer Divide Ratio (Default = 153_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	Sets the LO Generation Band Switch Control for Optimal TX Spur. 00 = 2300~2399.99MHz 01 = 2400~2499.99MHz (default) 10 = 2500~2599.99MHz 11 = 2600~2700MHz
D7:D0	1010011	Synthesizer 8-Bit Integer Divide Ratio. Default = 01010011

Table 23. Address 20, Synthesizer Configuration#1 (Default = 241_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	100	Set to recommended value.
D6	1	Synthesizer Turbo Mode Enable. 0 = Disable 1 = Enable.
D5	0	CLOCKOUT Buffer Drive. 0 = 1x drive (default) 1 = 4x drive
D4:D3	00	Selects the Charge-Pump Current. 00 = 3.2mA diff. CP (default) 01 = 1.6mA diff. CP 10 = 1.6mA single-ended CP 11 = 0.8mA single-ended CP
D2:D1	00	Sets the Reference Divider Ratio. 00 = Divide-by-1 (default) 01 = Divide-by-2 10 = Divide-by-4 11 = Divide-by-8
D0	1	Fractional-N PLL Mode Enable. 1 = Enable the fractional-N PLL 0 = Enable the integer-N PLL.

Table 24. Address 21, Synthesizer Configuration#2 (Default = $02D_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	000	Synthesizer Test Output Select. D<9> = 1 programs charge pump into test mode. D<8:7> decide which PLL test signal is delivered to DOUT MUX and finally selected by Address 9 D<7:5>. 000 = Lock detect (default) 001 = Sigma-delta modulator TVM output 010 = Reference-divider output 011 = Main divider output 100 = CP in low-Z mode and select lock detect 101 = CP in source mode and select sigma-delta modulator 110 = CP in sink mode and select reference-divider output 111 = CP in high-Z mode and select main divider output (used for VCO frequency estimation)
D6:D5	01	Charge-Pump Linearity Current Select. 00 = Disable 01 = +3% (default) 10 = +9% 11 = +12%
D4:D0	01101	Set to recommended value.

Table 25. Address 22, VCO Auto-Select (VAS) Configuration (Default = $1A9_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	Set to recommended value.
D7	1	VAS Triggering by Address 17 Enable. See Address 17 definitions for details. 0 = Disable for small frequency adjustment (i.e.~100kHz). 1 = Enable for channel switching (default)
D6:D2	01010	Set to recommended value.
D1	0	VAS Relock Mode Select. 0 = Relock starting at sub-band selected by Address 23 D4:D0 (default) 1 = Relock starting at present acquired sub-band.
D0	1	VAS Operating Mode Select. 0 = Select VCO subband by SPI Address 23 D<4:0> (VAS_SPI<4:0>) 1 = Select VCO subband by VAS (default)

Table 26. Address 23, LO Miscellaneous Configuration (Default = $24F_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9	1	VCO SPI Enable. Enable VCO except shutdown mode. 0 = Disable 1 = Enable
D8:D5	0010	Set to recommended value.
D4:D0	01111	VAS Sub-band SPI Overwrite. Active when Address 22 D0 (VAS_MODE) = 0. 00000 = Minimum frequency … 01111 = 15 (default) … 11111 = Maximum frequency

Table 27. Address 24, Crystal Oscillator Configuration (Default = 180_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	0	Crystal Oscillator Core Enable. Enable except shutdown mode. 0 = Disable (default) 1 = Enable
D8	1	Sets the CLKOUT Divide Ratio. 0 = Divide-by-1 1 = Divide-by-2 (default)
D7	1	CLKOUT Pin Enable. 0 = Disable 1 = Enable (default)
D6:D0	0000000	Crystal Oscillator Frequency Tuning. 000000 = Maximum frequency (default) … 111111 = Minimum frequency

Table 28. Address 25, Voltage Controlled Oscillator (VCO) Configuration (Default = 100_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	VCO Buffer Bias Control. 00 = 800µA 01 = 1200µA (default) 10 = 1600µA 11 = 2000µA
D7:D5	000	Set to recommended value.
D4:D1	0000	VCO Bias Trim SPI Code. Active when Address 25 D<0> (VCO_BIAS_SPI_EN) = 1. Trim word for VCO bias trim. 0000 = Minimum bias (default) … 1000 = Nominal process … 1111 = Maximum bias
D0	0	VCO Bias Trim SPI Overwrite Enable. 0 = By trim block (default) 1 = By SPI

Table 29. Address 26, LO Generation (LOGEN) Configuration (Default = $3CA_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	1111001010	Set to recommended value.

Table 30. Address 27, PA Driver and PA Bias DAC (PADRV and PADAC) Configuration (Default = $3E3_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9	1	TX DC Offset Correction. 0 = Disable 1 = Enable
D8	1	PA DRV/DAC On/Off Gating by VAS TXOOL and PLL LD. 0 = Independent of TXOOL and LD 1 = Relock when TXOOL = 1 or LD = 0 (default)
D7	1	Set to recommended value.
D6	1	PA DAC Voltage-Mode Output Select. Active when Address 27 D5 (PADAC_IV) = 0. 0 = Logic “0” output 1 = Logic “1” output (default)
D5	1	PA DAC I/V Output Select. 0 = Select voltage output 1 = Select current output.
D4:D3	10	Set to recommended value.
D2:D0	011	PA Driver Bias Control. 000 = Minimum … 011 = Default … 111 = Maximum

Table 31. Address 28, PA Bias DAC (PADAC) Configuration (Default = $0C0_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0011	PADAC Turn-On Delay Control. 0000 = 0µs 0001 = 0µs 0010 = 0.5µs … 0011 = 1.0µs (default) … 1111 = 7.0µs
D5:D0	000000	PADAC Output Current Control. Active when Address 27 D5 = 1 (PADAC_IV). 000000 = 0µA (default) 000001 = 5µA … 111111 = 315µA

Table 32. Address 29, TX Gain Configuration (Default = $3F0_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D4	111111	TX VGA SPI Gain Control. Active when Address 29 D0 (TXVGA_GAIN_SPI_EN) = 1 000000 = MIN attenuation … 111111 = MAX attenuation (default)
D3	0	Set to recommended value.
D2	0	TX DC Offset SPI Adjust Enable. 0 = By fuse (default) 1 = By SPI
D1	0	Pin TR6 SPI TX VGA Control Enable. 0 = By pin (default) 1 = By SPI Address 29 D9
D0	0	TX VGA Gain SPI Control Enable. 0 = By pin (default) 1 = By SPI Address 29 D9:D4

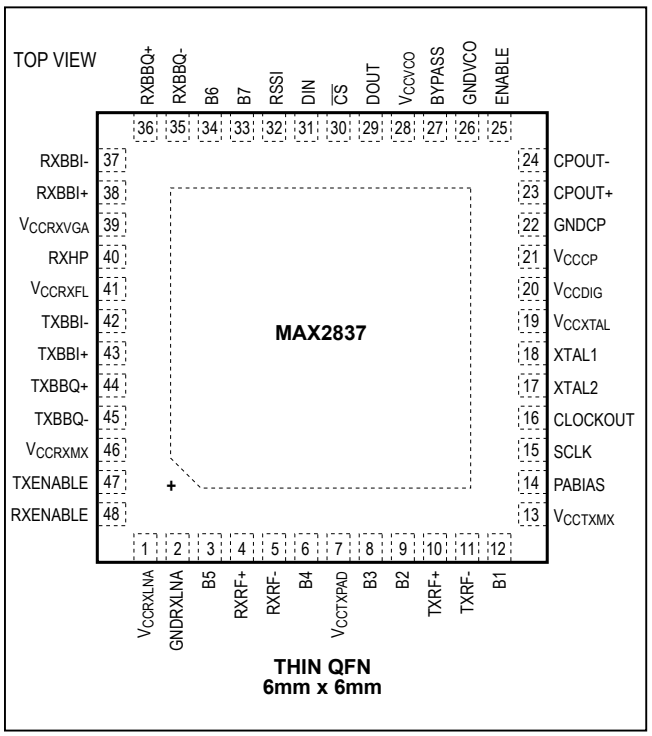
Table 33. Address 30, TX LO I/Q Configuration (Default = 080_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0010	Set to recommended value.
D5	0	TX LO I/Q Phase SPI Adjust Enable. 0 = By trim (default) 1 = By Address 30 D4:D0
D4:D0	00000	TX LO I/Q Phase SPI Adjust. Active when Address 30 D5 (TXLO_IQ_SPI_EN) = 1. As trim word for fuse trim. 00000 = +4deg (Q lags I by 94degs, default) … 01111 = +0deg … 11111 = -4deg (Q lags I by 86degs)

Table 34. Address 31, TX DC Correction Configuration (Default = 000_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D5	00000	TX DC Offset Correction for Q-Channel. Active when Address 29 D2 (TX_DCCORR_SPI_EN) = 1. As trim word for fuse trim. 00000 = 992/0µA (+/-ve offset current, default) 00001 = 960/32µA 00010 = 928/64µA … 01111 = 512/480µA … 11111 = 0/992µA
D4:D0	00000	TX DC Offset Correction for I-Channel. Active when Address 29 D2 (TX_DCCORR_SPI_EN) = 1.As trim word for fuse trim. 00000 = 992/0µA (+/-ve offset current, default) 00001 = 960/32µA 00010 = 928/64µA … 01111 = 512/480µA … 11111 = 0/992µA

Pin Configuration



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
48 TQFN-EP	T4866+2	21-0141	90-0007

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/07	Initial release	—
1	11/08	Corrected SPI description in *Programmable Registers and 4-Wire SPI-Interface* section	16
2	7/15	Added new *Temperature Sensor Readout Through DOUT Pin*, *VAS Operating Procedure*, *VAS Readout*, and *VCO Subband Selection Through SPI* sections. Added Register and Bit Descriptions.	16–33

