MAX17061A

8-String White LED Driver with SMBus for LCD Panel Applications

General Description

The MAX17061A is a high-efficiency driver for white lightemitting diodes (LEDs). It is designed for large liquid-crystal displays (LCDs) that employ an array of LEDs as the light source. An internal switch current-mode step-up controller drives the LED array, which can be configured for up to eight strings in parallel and 10 LEDs per string. Each string is terminated with ballast that achieves ±1.5% current-regulation accuracy between strings, ensuring even LED brightness. The MAX17061A has a wide input voltage range from 7.5V to 26V, and provides a fixed 25mA or adjustable 15mA to 30mA full-scale LED current.

The MAX17061A internally generates a DPWM signal for accurate WLED dimming control. The DPWM frequency is resistor programmable, while DPWM duty cycle is co trolled directly from an external PWM signal or through a control word through the MAX17061A's SMBus™ interface. This DPWM control provides a dimming range with 8-bit resolution and supports Intel display-power-saving technology (DPST) to maximize battery life.

The MAX17061A has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage under any circumstance, ensuring safe operation. Once an open string is detected, the string is disabled while other strings operate normally. The MAX17061A also features short LED detection. The shorted strings are also disabled after a 2ms fault blanking interval. The controller features cycle-by-cycle current limit to provide stable operation and soft-start capability. If the MAX17061A is in current-limit condition, the step-up converter is latched off after an internal timer expires. A thermal-shutdown circuit provides another level of protection.

The MAX17061A's step-up controller features an internal 150mΩ (typ), 45V (max) power MOSFET with local current-sense amplifier for accurate cycle-by-cycle current limit. This architecture greatly simplifies the external circuitry and saves PCB space. Low-feedback voltage at each LED string 625mV (typ) at 25mA LED current helps reduce power loss and improve efficiency. The MAX17061A features selectable switching frequency (500kHz, 750kHz, or 1MHz), which enables a wide variety of applications that can trade off component size for operating frequency.

The MAX17061A is available in a thermally enhanced 28-pin, 4mm x 4mm Thin QFN package.

SMBus is a trademark of Intel Corp.

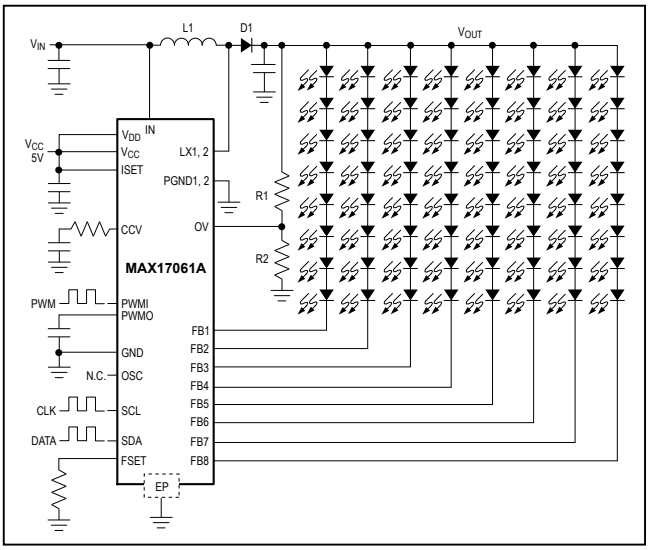
Features

- Accurate Dimming Control Using SMBus, PWM Interface
- Dimming Range with 8-Bit Resolution
- Adjustable DPWM Frequency with 1.5% Accuracy
- Up to Eight Parallel Strings Multiple Series-Connected LEDs
- ±1.5% Current Regulation Accuracy Between Strings
- Low String Feedback Voltage: 625mV at 25mA LED Current
- Full-Scale LED Current Adjustable from 15mA to 30mA, or Preset 25mA
- Open and Short LED Protections
- Output Overvoltage Protection
- 0.15Ω Internal HV Power MOSFET (45V max)
- Wide Input-Voltage Range from 4.5V to 26V
- 500kHz/750kHz/1MHz Selectable Switching Frequency
- Small 28-Pin, 4mm x 4mm, Thin QFN package

Applications

- Notebook, Subnotebook, and Tablet Computer Displays
- Handy Terminals

Simplified Operating Circuit



***Ordering Information* and *Pin Description* appear at end of data sheet.**

maxim integrated™

Absolute Maximum Ratings

IN to GND .....-0.3V to +28V
FB_, LX_ to GND .....-0.3V to +45V
PGND_ to GND .....-0.3V to +0.3V
V_{CC}, V_{DD}, PWMI, SDA, SCL to GND .....-0.3V to +6V
ISET, CCV, PWMO, FSET, OSC,
OV to GND .....-0.3V to V_{CC} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 16.9mW/°C above +70°C)...1667mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Circuit of Figure 1. V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC} = 5V, R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Input Voltage Range			7.5		26	V
IN UVLO Threshold	Rising edge		7.08	7.2	7.32	V
	Falling edge		6.86	6.98	7.1	
IN Input Current	V_{IN} = 26V	MAX17061A is enabled		70	110	µA
		MAX17061A is disabled, T_A = +25°C	+1		+1	
V_{CC} Input Voltage			4.5	5	5.5	V
V_{CC} UVLO Threshold	Rising edge, typical hysteresis = 10mV		4.00	4.25	4.45	V
V_{CC} Quiescent Current	MAX17061A is enabled			1.24	2	mA
V_{CC} Shutdown Current	MAX17061A is disabled				10	µA
BOOST CONVERTER						
LX On-Resistance	20mA from LX_ to PGND			0.15	0.3	Ω
LX Leakage Current	45V on LX_, T_A = +25°C				1	µA
Operating Frequency	V_{OSC} = V_{CC}		0.9	1.0	1.1	MHz
	V_{OSC} = open		675	750	825	kHz
	V_{OSC} = GND		450	500	550	
OSC High-Level Threshold			V_{CC} - 0.4			V
OSC Midlevel Threshold			1.5		V_{CC} - 2.0	V
OSC Low-Level Threshold					0.4	V
Minimum Duty Cycle	PWM mode (Note 1)			10		%
Maximum Duty Cycle			94	95.5	97	%
LX Current Limit	Duty cycle = 75% (Note 1)		1.6			A
CONTRL INPUT						
SDA, SCL Logic Input High Level			2.1			
SDA, SCL Logic Input Low Level					0.8	V
PWMI Logic Input High Level			2.1			V
PWMI Logic Input Low Level					0.8	V

Electrical Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC} = 5V, R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT LEAKAGE					
PWMI Leakage Current	T_A = +25°C	-0.3		+0.3	µA
ISET, FSET Leakage Current	ISET, FSET to V_{CC}, T_A = +25°C			+1	µA
OV Leakage Current	T_A = +25°C	-0.1		+0.1	µA
SDA, SCL Input Bias Current	T_A = +25°C	-1		+1	µA
SDA Output Low Sink Current	V_{SDA} = 0.4V	4			mA
OSC Leakage Current	T_A = +25°C	3		+3	µA
LED CURRENT					
Full-Scale FB_ Output Current	ISET = V_{CC}	24.5	25.0	25.5	mA
	R_{ISET} = 133kΩ	28.8	30.0	31.2	
	R_{ISET} = 200kΩ	19.3	20.0	20.7	
	R_{ISET} = 266kΩ	14.4	15.0	15.6	
ISET High-Level Threshold	Default setting	V_{CC} - 0.4			V
ISET Output Voltage		1.166,	1.236	1.306	V
Current Regulation Between Strings	ISET = V_{CC}	-1.5		+1.5	%
Minimum FB_ Regulation Voltage	$I_{FB\_}$ = 25mA	475	625	910	mV
	$I_{FB\_}$ = 30mA	575	750	1100	
	$I_{FB\_}$ = 20mA	380	500	740	
	$I_{FB\_}$ = 15mA	285	375	560	
Maximum FB_ Ripple	$I_{FB\_}$ = 20mA (C_{OUT} = 1µF, OSC = V_{CC}) (Note 1)		120	200	mV_{P-P}
FB_ On-Resistance	$V_{FB\_}$ = 50mV (includes 10Ω sense resistor)		17.5	28.4	Ω
FB_ Leakage Current	$V_{FB\_}$ = 26V, T_A = +25°C			1	µA
	$V_{FB\_}$ = 45V, T_A = +25°C		2.5	4	
FAULT PROTECTION					
OV Threshold Voltage	Rising edge, typical hysteresis = 60mV	1.166	1.236	1.306	V
FB_ Overvoltage Threshold		5.2	5.6	6.0	V
FB_ Undervoltage Threshold		130	175	220	mV
Boost Global Fail		48	84	120	mV
Thermal-Shutdown Threshold	(Note 1)		160		°C
Overcurrent Fault Shutdown Timer	I_{PEAK} > 3.3A at duty = 0% or 1.8A at duty = 90% (typ)	88	128	168	µs
FB_ Overvoltage-Fault Timer		1.7	2	2.3	ms

Electrical Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC} = 5V, R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWM FILTER					
PWM Output Impedance		20	40	60	kΩ
DPWM Oscillator Frequency	R_{FSET} = 464kΩ	197	200	203	Hz
	R_{FSET} = 113kΩ	750	785	820	
	R_{FSET} = 65kΩ	1.270	1.335	1.400	kHz
	R_{FSET} = 42kΩ		2		
PWMI Input Frequency Range		5	10	100	kHz
PWMI Full-Range Accuracy				5	LSB
PWMI Brightness Setting	PWMI duty cycle = 100%	98	100		%
	PWMI duty cycle = 50%	48	50	52	
	PWMI duty cycle = 0%	2.6	2.7	2.8	
SMBus TIMING SPECIFICATION					
SMBus Frequency	FSMB	10		100	kHz
Bus Free Time	TBUF	4.7			µs
START Condition Hold Time from SCL	THD:STA	4			µs
START Condition Setup Time from SCL	TSU:STA	4.7			µs
STOP Condition Setup Time from SCL	TSU:STO	4			µs
SDA Hold Time from SCL	THD:DAT	300			µs
SDA Setup Time from SCL	TSU:DAT	250			µs
SCL Low Period	T_{LOW}	4.7			µs
SCL High Period	T_{HIGH}	4			µs

Electrical Characteristics

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, 5V = R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Input Voltage Range			7.5		26	V
IN UVLO Threshold	Rising edge		7.08		7.32	V
	Falling edge		6.86		7.1	
IN Input Current	V_{IN} = 26V	MAX17061A is enabled			110	µA
V_{CC} Input Voltage			4.5		5.5	V
V_{CC} UVLO Threshold	Rising edge, typical hysteresis = 10mV		4.00		4.45	V
V_{CC} Quiescent Current	MAX17061A is enabled				2	mA

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, 5V = R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Shutdown Current	MAX17061A is disabled			10	µA
BOOST CONVERTER					
LX On-Resistance	20mA from LX_ to PGND			0.3	Ω
Operating Frequency	V_{OSC} = V_{CC}	0.89		1.10	MHz
	V_{OSC} = open	675		825	kHz
	V_{OSC} = GND	450		560	
OSC High-Level Threshold		V_{CC} - 0.4			V
OSC Midlevel Threshold		1.5		V_{CC} - 2.0	V
OSC Low-Level Threshold				0.4	V
Minimum Duty Cycle		94			%
LX Current Limit	Duty cycle = 75% (Note 1)	1.6			A
CONTRL INPUT					
SDA, SCL Logic Input High Level		2.1			
SDA, SCL Logic Input Low Level				0.8	V
PWMI Logic Input High Level		2.1			V
PWMI Logic Input Low Level				0.8	V
INPUT LEAKAGE					
SDA Output Low Sink Current	V_{SDA} = 0.4V	4			mA
LED CURRENT					
Full-Scale FB_ Output Current	ISET = V_{CC}	24.5		25.5	mA
	R_{ISET} = 133kΩ	28.6		31.4	
	R_{ISET} = 200kΩ	19.0		21.0	
	R_{ISET} = 266kΩ	14.4		15.6	
ISET High-Level Threshold	Default setting	V_{CC} - 0.4			V
ISET Output Voltage		1.166		1.306	V
Current Regulation Between Strings	ISET = V_{CC}	-1.5		+1.5	%
Minimum FB_ Regulation Voltage	$I_{FB\_}$ = 25mA	425		910	mV
	$I_{FB\_}$ = 30mA	575		1100	
	$I_{FB\_}$ = 20mA	380		740	
	$I_{FB\_}$ = 15mA	285		560	
Maximum FB_ Ripple	$I_{FB\_}$ = 20mA (C_{OUT} = 1µF, OSC = V_{CC}) (Note 1)			200	mV_{P-P}
FB_ On-Resistance	$V_{FB\_}$ = 50mV (includes 10Ω sense resistor)			28.4	Ω

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, 5V = R_{FSET} = 464kΩ, V_{PWMI} = GND, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

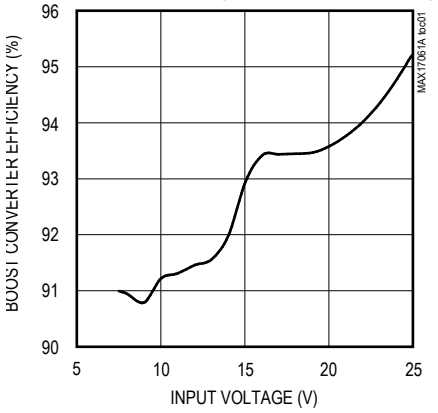
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT PROTECTION					
OV Threshold Voltage	Rising edge, typical hysteresis = 60mV	1.166		1.306	V
FB_ Overvoltage Threshold		5.2		6.0	V
FB_ Undervoltage Threshold		130		220	mV
Boost Global Fail		48		120	mV
Overcurrent FAULT Shutdown Timer	I_{PEAK} > 3.3A at duty = 0% or 1.8A at duty = 90% (typical)	88		168	µs
FB_ Overvoltage Fault Timer		1.6		2.4	ms
PWM FILTER					
PWM Output Impedance		20		60	kΩ
DPWM Oscillator Frequency	R_{FSET} = 464kΩ	197		203	Hz
	R_{FSET} = 113kΩ	750		820	
	R_{FSET} = 65kΩ	1.27		1.40	kHz
PWMI Input Frequency Range		5		100	kHz
PWMI Full-Range Accuracy				5	LSB
PWMI Brightness Setting	PWMI duty cycle = 100%	98			%
	PWMI duty cycle = 50%	48		52	
	PWMI duty cycle = 0%	2.6		2.8	
SMBus TIMING SPECIFICATION					
SMBus Frequency	FSMB	10		100	kHz
Bus Free Time	TBUF	4.7			µs
START Condition Hold Time from SCL	THD:STA	4			µs
START Condition Setup Time from SCL	TSU:STA	4.7			µs
STOP Condition Setup Time from SCL	TSU:STO	4			µs
SDA Hold Time from SCL	THD:DAT	300			µs
SDA Setup Time from SCL	TSU:DAT	250			µs
SCL Low Period	T_{LOW}	4.7			µs
SCL High Period	T_{HIGH}	4			µs

Note 1: Specifications are guaranteed by design, not production tested.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

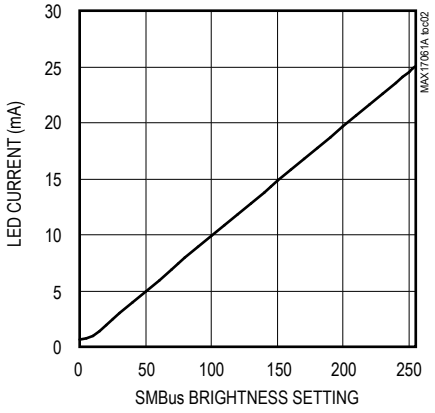
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, R_{FSET} = 464kΩ, V_{PWMI} = GND, LEDs = 10 series x 4 parallel strings, T_A = +25°C, unless otherwise noted.)

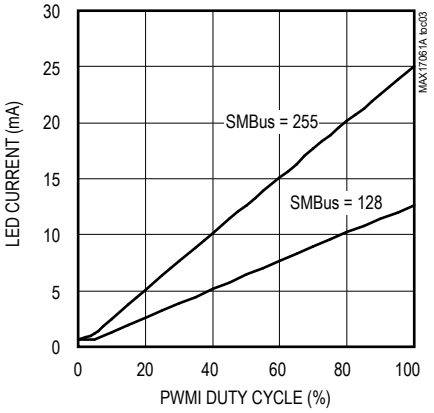
BOOST CONVERTER EFFICIENCY vs. INPUT VOLTAGE (BRIGHTNESS = 100%)



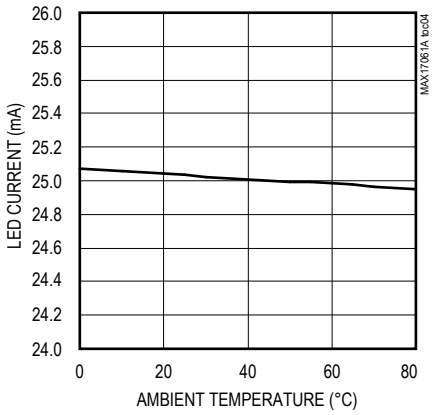
LED CURRENT vs. SMBus BRIGHTNESS SETTING



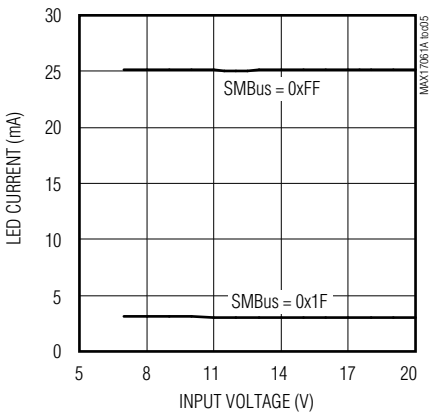
LED CURRENT vs. PWMI DUTY CYCLE



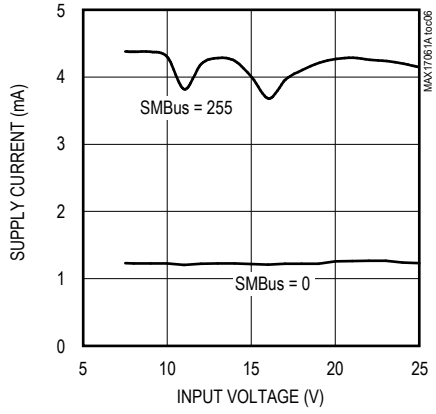
LED CURRENT vs. AMBIENT TEMPERATURE (BRIGHTNESS = 100%)



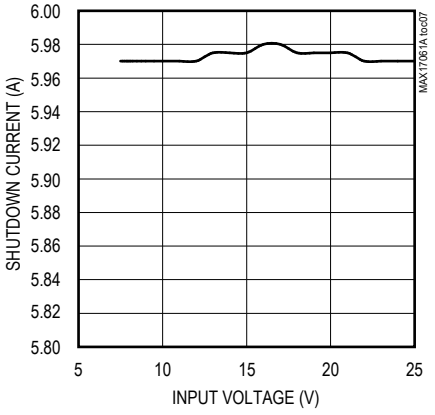
LED CURRENT vs. INPUT VOLTAGE



V_{CC} SUPPLY CURRENT vs. INPUT VOLTAGE



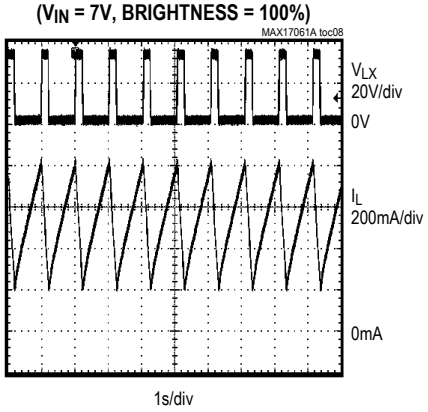
V_{CC} SHUTDOWN CURRENT vs. INPUT VOLTAGE



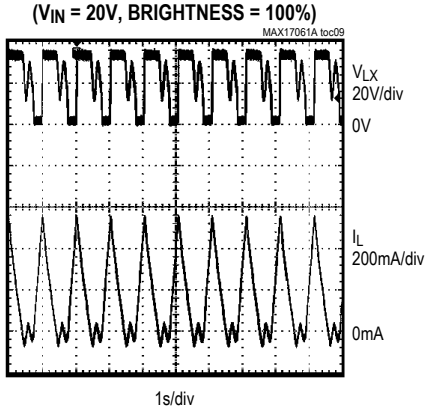
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, R_{FSET} = 464kΩ, V_{PWMI} = GND, LEDs = 10 series x 4 parallel strings, T_A = +25°C, unless otherwise noted.)

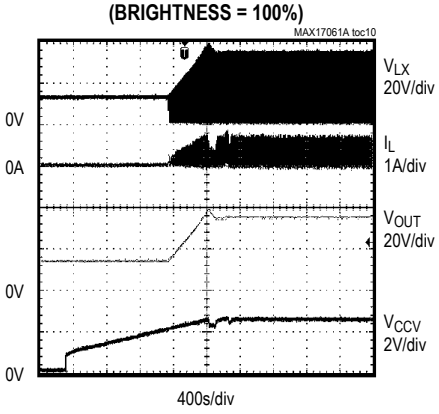
SWITCHING WAVEFORMS (V_{IN} = 7V, BRIGHTNESS = 100%)



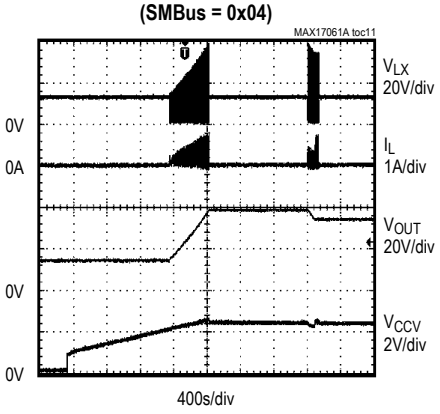
SWITCHING WAVEFORMS (V_{IN} = 20V, BRIGHTNESS = 100%)



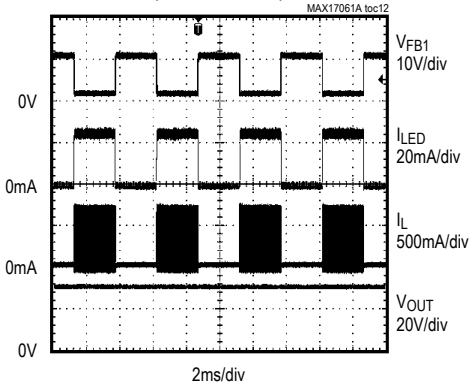
STARTUP WAVEFORMS (BRIGHTNESS = 100%)



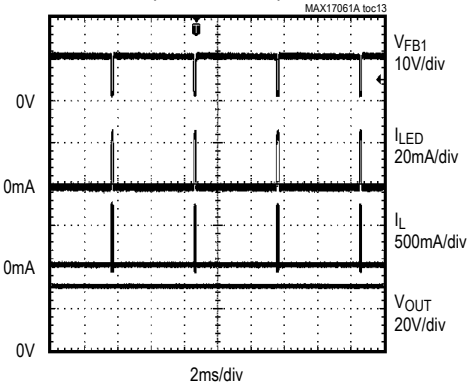
STARTUP WAVEFORMS (SMBus = 0x04)



LED CURRENT WAVEFORMS (SMBus = 0x80)



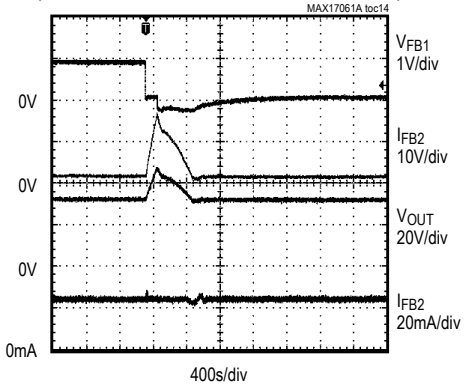
LED CURRENT WAVEFORMS (SMBus = 0x04)



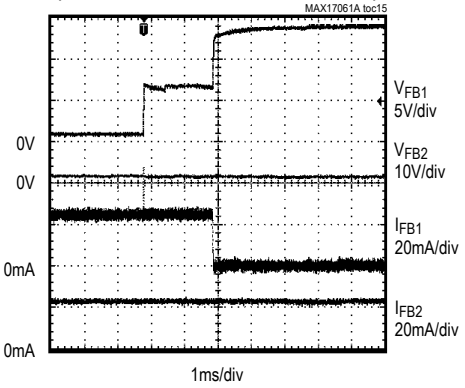
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, C_{CCV} = 0.022µF, R_{CCV} = 5.1kΩ, V_{ISET} = V_{OSC} = V_{DD} = V_{CC}, R_{FSET} = 464kΩ, V_{PWMI} = GND, LEDs = 10 series x 4 parallel strings, T_A = +25°C, unless otherwise noted.)

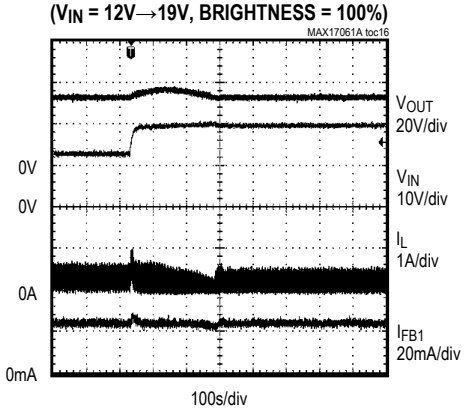
LED-OPEN FAULT PROTECTION
(BRIGHTNESS = 100%, LED OPEN ON FB1)



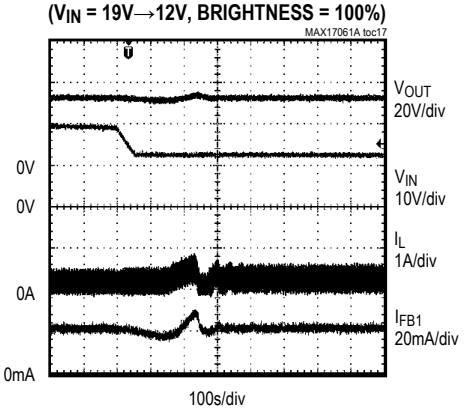
LED-SHORT FAULT PROTECTION
(BRT = 100%, 2 LEDs SHORT ON FB1)



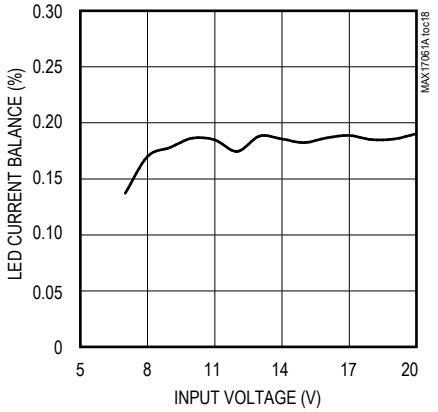
LINE TRANSIENT RESPONSE
(V_{IN} = 12V→19V, BRIGHTNESS = 100%)



LINE TRANSIENT RESPONSE
(V_{IN} = 19V→12V, BRIGHTNESS = 100%)



LED CURRENT BALANCE
vs. INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	FB3	LED String 3 Cathode Connection. FB3 is the open-drain output of an internal regulator, which controls current through FB3. FB3 can sink up to 30mA. If unused, connect FB3 to V_{CC}.
2	FB4	LED String 4 Cathode Connection. FB4 is the open-drain output of an internal regulator, which controls current through FB4. FB4 can sink up to 30mA. If unused, connect FB4 to V_{CC}.
3	GND	Analog Ground
4, 6, 18	N.C.	No Connection
5	FB5	LED String 5 Cathode Connection. FB5 is the open-drain output of an internal regulator, which controls current through FB5. FB5 can sink up to 30mA. If unused, connect FB5 to V_{CC}.
7	FB6	LED String 6 Cathode Connection. FB6 is the open-drain output of an internal regulator, which controls current through FB6. FB6 can sink up to 30mA. If unused, connect FB6 to V_{CC}.
8	FB7	LED String 7 Cathode Connection. FB7 is the open-drain output of an internal regulator, which controls current through FB7. FB7 can sink up to 30mA. If unused, connect FB7 to V_{CC}.
9	FB8	LED String 8 Cathode Connection. FB8 is the open-drain output of an internal regulator, which controls current through FB8. FB8 can sink up to 30mA. If unused, connect FB8 to V_{CC}.
10	OSC	Oscillator Frequency-Selection Pin. Connect OSC to V_{CC} to set the step-up converter's oscillator frequency to 1MHz. Connect OSC to GND to set the frequency to 500kHz. Float OSC to set the frequency to 750kHz.
11	PWMI	PWM Signal Input. This PWM signal is used for brightness control in PWM mode or DPST mode. This signal is filtered and its duty cycle is converted into a digital signal to calculate DPWM duty cycle. In PWM mode, the DPWM duty cycle equals the input PWM duty cycle. In DPST mode, the DPWM duty cycle is the input PWM duty cycle multiplied by the SMBus brightness command.
12	PWMO	Filtered PWM Signal Output. Connect a capacitor between PWMO and GND. The capacitor forms a lowpass filter with an internal 40kΩ (typ) resistor to filter the PWM signal into an analog signal whose level represents the duty-cycle information of the input PWM signal.
13	FSET	DPWM Frequency Adjustment Pin. Connect a resistor from FSET to GND to set the internal DPWM frequency: $$f_{DPWM} = \frac{10^9}{\alpha \times R[\Omega] + \gamma}$$ where: α = 10.638, γ = 58509. This DPWM signal directly chops WLED current with the calculated duty cycle for brightness control.
14	SDA	SMBus Serial-Data Input
15	SCL	SMBus Serial-Clock Input
16	LX2	Boost Regulator Internal MOSFET Drain. Connect the inductor and the Schottky diode to LX2 node. LX2 should always be shorted to LX1 externally.
17	LX1	Boost Regulator Internal MOSFET Drain. Connect the inductor and the Schottky diode to LX1 node. LX1 should always be shorted to LX2 externally.
19	PGND2	Boost Regulator Power Ground
20	PGND1	Boost Regulator Power Ground
21	IN	Supply Input, 7.5V to 26V. Bypass IN to GND directly at the pin with a 0.1µF or greater ceramic capacitor. When IN voltage is below its UVLO threshold, the MAX17061A turns off the output.

Pin Description (continued)

PIN	NAME	FUNCTION
22	V_{DD}	Boost Regulator MOSFET Gate Drive Supply. Bypass V_{DD} to GND with a ceramic capacitor of 1µF or greater.
23	V_{CC}	5V Control Supply Input. V_{CC} provides power to the MAX17061A. Bypass V_{CC} to GND with a ceramic capacitor of 1µF or greater.
24	CCV	Step-Up Converter Compensation Pin. Connect a 0.022µF ceramic capacitor and 5.1kΩ resistor from CCV to GND. When the MAX17061A shuts down, CCV is discharged to 0V through an internal 20kΩ resistor.
25	OV	Overvoltage Sense. Connect OV to the center tap of a resistive voltage-divider from V_{OUT} to ground. The detection threshold for voltage limiting at OV is 1.236V (typ).
26	ISET	Full-Scale LED Current Adjustment Pin. The resistance from ISET to GND controls the full-scale current in each LED string: $I_{LEDMAX} = 20mA \times 200k\Omega/R_{ISET}$ The acceptable resistance range is $133k\Omega < R_{ISET} < 266k\Omega$, which corresponds to full-scale LED current of $30mA > I_{LEDMAX} > 15mA$. Connect ISET to V_{CC} for a default full-scale LED current of 25mA.
27	FB1	LED String 1 Cathode Connection. FB1 is the open-drain output of an internal regulator, which controls current through FB1. FB1 can sink up to 30mA. If unused, connect FB1 to V_{CC}.
28	FB2	LED String 2 Cathode Connection. FB2 is the open-drain output of an internal regulator, which controls current through FB2. FB2 can sink up to 30mA. If unused, connect FB2 to V_{CC}.
—	EP	Exposed Backside Pad. Solder to the circuit board ground plane with sufficient copper connection to ensure low thermal resistance. See the *PCB Layout Guidelines* section.

Detailed Description

The MAX17061A is a high-efficiency driver for arrays of white LEDs. It contains a fixed-frequency current-mode PWM step-up controller, dimming control circuit, SMBus interface, internal power MOSFET, and eight regulated current sources (see Figure 2). When enabled, the step-up controller boosts the output voltage to provide sufficient headroom for the current sources to regulate their respective string currents. The MAX17061A features selectable switching frequency (500kHz, 750kHz, or 1MHz), which allows trade-offs between external component size and operating efficiency.

WLED brightness is controlled by turning the WLEDs on and off with a DPWM signal. The DPWM frequency can be accurately adjusted with a resistor. The brightness of the LEDs is proportional to the duty cycle of the DPWM signal, which is controlled externally through either a PWM or 2-wire SMBus-compatible interface, or both. When both interfaces are used at the same time, the product of the PWM duty cycle and SMBus command value is used for the dimming control. This DPWM control scheme provides a full dimming range with 8-bit resolution.

The MAX17061A has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage in all circumstances. The MAX17061A checks each FB_ voltage during the operation. If one or more strings are open, the corresponding FB_ voltages are pulled below 175mV (typ), and opencircuit fault is detected. As a result, the respective current sources are disabled. When one or more LEDs are shorted and the FB_ voltage exceeds 1.1 x V_{CC}, short fault is detected and the respective current source is disabled. In either LED open or short conditions, the fault strings are disabled while other strings can still operate normally. The controller features cycle-by-cycle current limit to provide stable operation and soft-start protection. In a current-limit condition, the controller shuts down after a 128µs overcurrent-fault timer expires. A thermal-shutdown circuit provides another level of protection.

The MAX17061A requires an external 5V supply to provide the internal bias and gate drive for the step-up controller.

Fixed-Frequency Step-Up Controller

The MAX17061A's fixed-frequency, current-mode, step-up controller automatically chooses the lowest active FB_ voltage to regulate the output voltage. Specifically, the difference between the lowest FB_ voltage and the current-source control signal plus an offset (V_{SAT}) is integrated at the CCV output. The resulting error signal is compared to the external switch current plus slope compensation to determine the switch on-time. As the load changes, the error amplifier sources or sinks current to the CCV output to deliver the required peak-inductor current. The slope-compensation signal is added to the current-sense signal to improve stability at high duty cycles.

At high input voltages when the on-time is pushed to be lower than the minimum on-time (90ns typ), the boost converter runs with minimum on-time, boosting the output voltage higher than the input voltage.

5V Supply V_{CC} and UVLO

The MAX17061A requires an external 5V V_{CC} supply for internal control voltage.

The MAX17061A includes power-on-reset (POR) and undervoltage-lockout (UVLO) features. POR resets the fault latch and sets all the SMBus registers to their POR values. POR occurs when V_{CC} rises above 2.8V (typ). The controller is disabled until V_{CC} exceeds the UVLO threshold of 4.25V (typ). Hysteresis on UVLO is approximately 85mV.

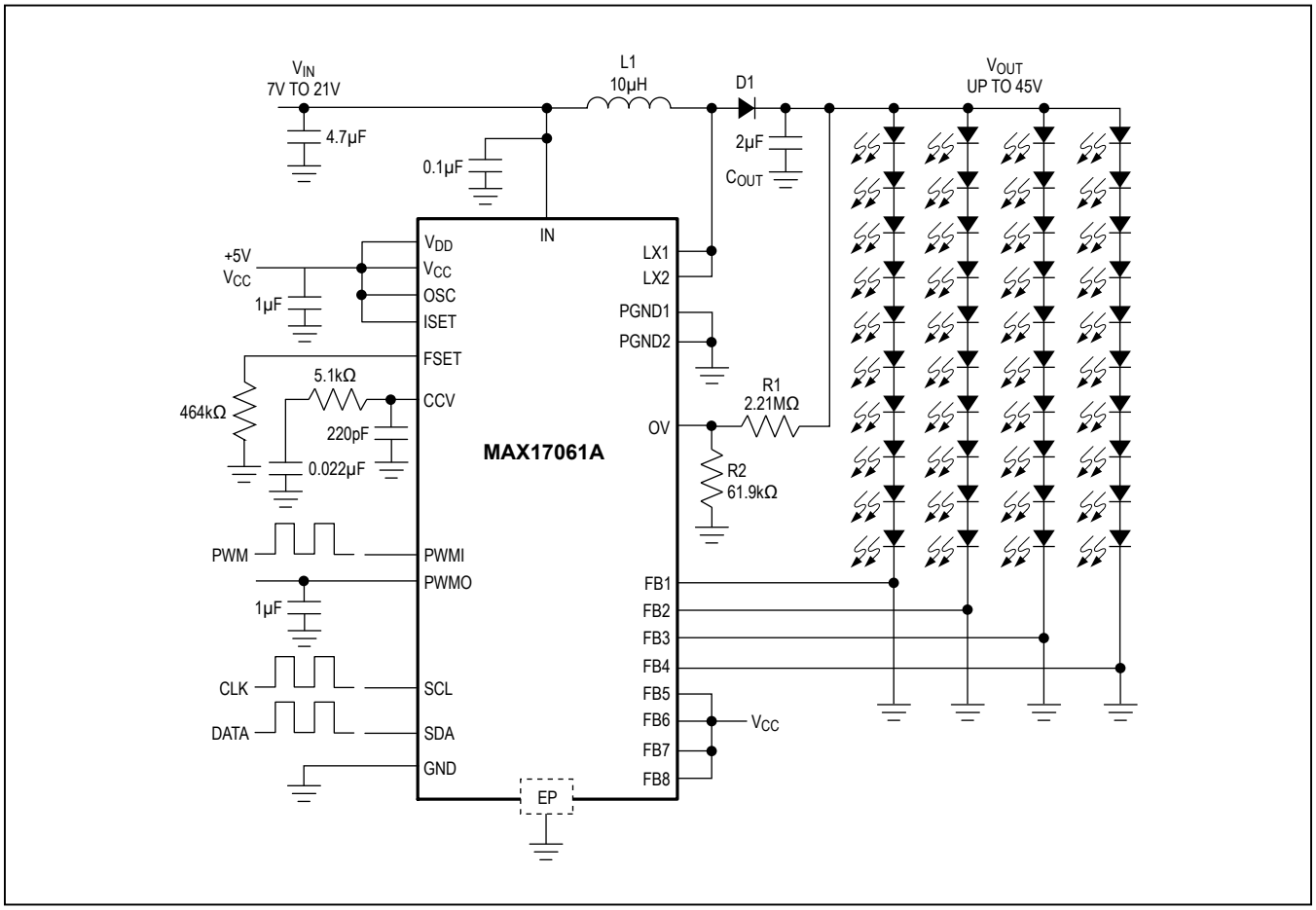


Figure 1. Typical Operating Circuit

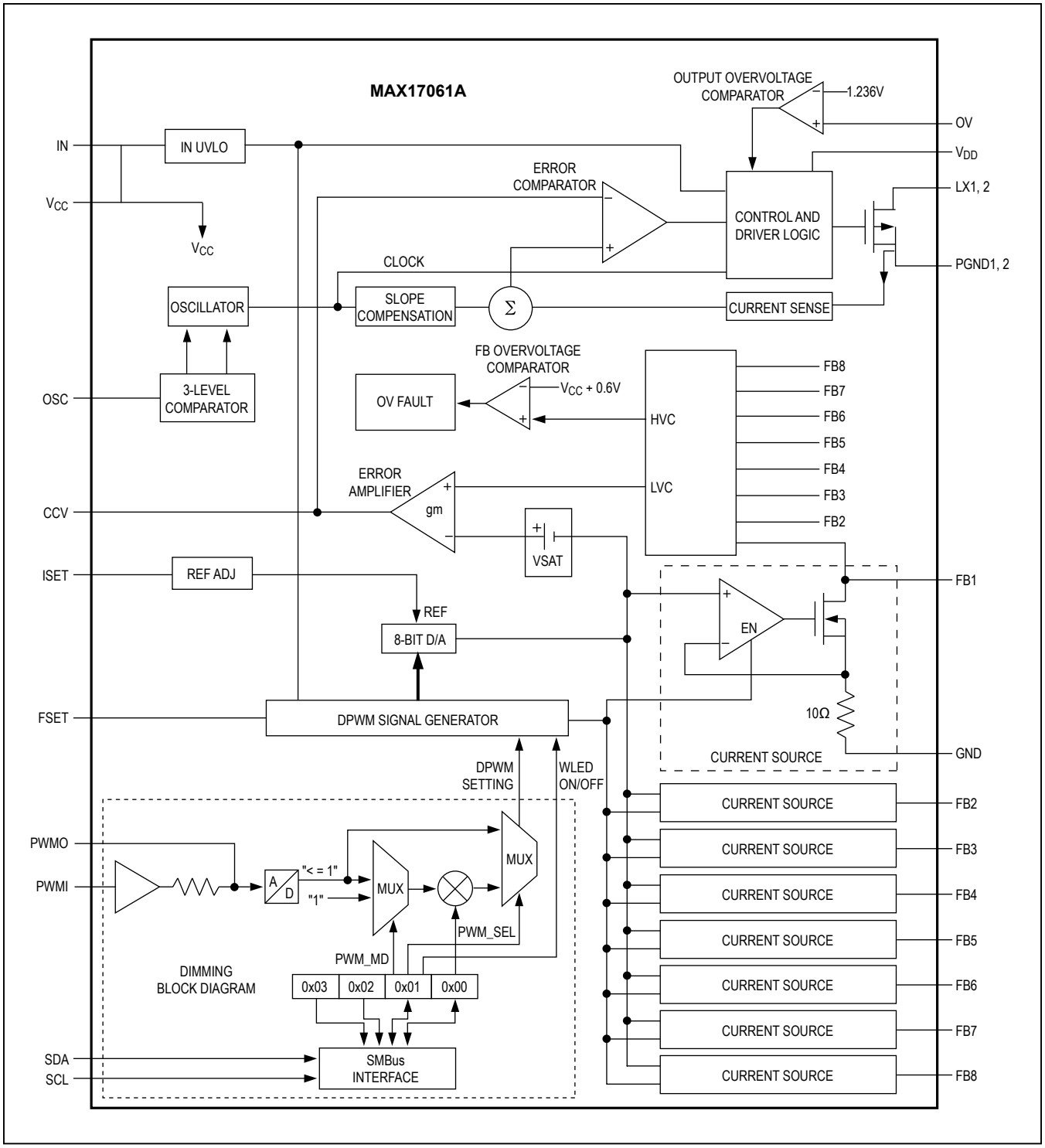


Figure 2. Control Circuit Block Diagram

The V_{CC} and V_{DD} pins should be bypassed to GND with a minimum 1µF ceramic capacitor.

IN UVLO

The MAX17061A implements an IN UVLO function to safeguard the operation in the specified range. When IN pin voltage drops below its UVLO threshold (6.98V typ), the converter is shut off and the BL_Stat bit of the fault/status register is cleared. The BL_CTL bit of control register is not altered. When IN pin voltage rises above the UVLO rising edge threshold (7.2V typ) the backlight resumes automatically if the BL_CTL bit is set to 1.

Startup

At startup, the MAX17061A checks the OV pin to see if the Schottky diode is open. If the OV voltage is lower than 84mV (typ), the boost converter does not start. After the OV test is done, the MAX17061A performs a diagnostic test of the LED array. The test is divided to two phases; each phase takes approximately 1.024ms. In the first test phase, all FB_ inputs are quickly discharged down to 5.6V (typ) and then continuously discharged by 800µA (typ) current sources. If a given FB_ voltage remains higher than 5.6V (typ), the string is considered to be shorted. Otherwise, if a given FB_ voltage is higher than 3V (typ), the string is considered to be unused. Unused strings should be tied to V_{CC}. In the second phase, each FB_ is precharged by an internal 400µA (typ) current source. If a given FB_ voltage remains lower than 1V (typ), the FB_ is considered to be a short to GND and the device is disabled. After the LED string diagnostic phases are finished, the boost converter starts. The total startup time is less than 10ms, including 4.2ms (typ) soft-start.

Shutdown

The MAX17061A can be placed into shutdown by clearing bit 0 of the device control register (0x01). When a critical failure is detected, the IC also enters shutdown mode. In shutdown mode, all functions of the IC are turned off. The fault/status register is set accordingly in shutdown. When bit 0 of the device control register (0x01) is recycled to 1, the MAX17061A exits shutdown mode and starts. The fault/status register is reset at startup.

Frequency Selection

A tri-level OSC input sets the internal oscillator frequency for step-up converter, as shown in Table 1. High-frequency (1MHz) operation optimizes the regulator for the smallest component size, at the expense of efficiency due to increased switching losses. Low-frequency (500kHz) operation offers the best overall efficiency, but requires larger components and PCB area.

Table 1. Frequency Selection

OSC PIN CONNECTION	SWITCHING FREQUENCY (kHz)
GND	500
Open	750
V_{CC}	1000

Overvoltage Protection

To protect the step-up converter when the load is open, or the output voltage becomes excessive for any reason, the MAX17061A features a dedicated overvoltage feedback input (OV). The OV pin is tied to the center tap of a resistive voltage-divider from the high-voltage output. When the OV pin voltage (V_{OV}) exceeds 1.236V, a comparator turns off the internal power MOSFET. This step-up converter switch is reenabled after the V_{OV} drops 60mV (typ) hysteresis below the protection threshold. This overvoltage-protection feature ensures the step-up converter fail-safe operation when the LED strings are disconnected from the output.

LED Current Sources

Maintaining uniform LED brightness and dimming capability are critical for LCD backlight applications. The MAX17061A is equipped with a bank of eight matched current sources. These specialized current sources are accurate to within ±1.5% between strings and can be switched on and off within 15µs, enabling PWM frequencies of up to 2kHz. All LED full-scale currents are identical and are set through the ISET pin (15mA < I_{LED} < 30mA). When ISET is connected to V_{CC}, the LED full-scale current is set at the 25mA default value.

The minimum voltage drop across each current source is approximately 625mV when the LED current is 25mA. The low-voltage drop helps reduce dissipation while maintaining sufficient compliance to control the LED current within the required tolerances.

The LED current sources can be disabled by tying the respective FB_ pin to V_{CC} at startup. When the IC is powered up, the controller scans settings for all FB_ pins. If a FB_ pin is not tied to V_{CC}, an internal circuit pulls this pin low, and the controller enables the corresponding current source to regulate the string current. If the FB_ pin is tied to V_{CC}, the controller disables the corresponding current regulator. The current regulator cannot be disabled by connecting the respective FB_pin to V_{CC} after the IC is powered up.

All FB_ pins in use are combined to extract a lowest FB_ voltage (LVC) (see Figure 2). LVC is fed into the step-up converter's error amplifier and is used to set the output voltage.

Current-Source Fault Protection

The MAX17061A performs a diagnostic test at startup. Open/short strings are disabled. LED fault open/short is also detected after startup. When one or more strings fails after startup, the corresponding current sources are disabled. The remaining LED strings still operate normally. When a fault is detected, bit 4 or/and bit 5, as well as bit 0 of the fault/status resister are set (see the *Fault/Status Register* section).

Open-Current Source Protection

The MAX17061A step-up converter output voltage is regulated according to the minimum FB_ voltages on all the strings in use. If one or more strings are open, the respective FB_ pins are pulled to ground. For any FB_ lower than 175mV, the corresponding current source is disabled. The unaffected LED strings still operate normally. If all strings in use are open, the MAX17061A shuts down the step-up converter.

The MAX17061A can tolerate A slight mismatch (4.4V) between LED strings. When severe mismatches (> 4.4V) or WLED shorts occur, the FB_ voltages will be uneven because mismatched voltage drops across strings. If a given FB_ voltage is higher than 5.6V (typ) after 24µs blanking time when LEDs are turned on, an LED short condition is detected on the respective string. When the short continues for greater than 2ms, the string is disabled. The controller allows the unaffected LED strings to operate normally. When only one string is in operation and there are shorts on some LEDs, then the converter does not shut down. Instead, the output voltage is adjusted accordingly.

The LED short-protection feature is disabled during the soft-start phase of the step-up converter.

Dimming Control

The MAX17061A internally generates a DPWM signal for accurate WLED brightness dimming control. The DPWM frequency is adjustable through an external setting resistor and has 1.5% accuracy for R_{FSET} = 464kΩ. The duty cycle of this DPWM signal can be controlled externally through two interfaces: PWM and SMBus. The ISET pin sets the amplitude of the current sources for each LED string (Figure 3). The internal DPWM signal directly controls the duty cycle of these current sources. The resulting current is chopped and synchronized to the DPWM signal. When filtered by the slow response time of the human eye, the overall brightness is modulated in a consistent flicker-free manner.

Full-Scale LED Brightness in DPWM Dimming Control

The full-scale LED current in the DPWM dimming is determined by resistance from the ISET pin to ground:

$$I_{LEDMAX} = \frac{20mA \times 200k\Omega}{R_{ISET}}$$

The acceptable resistance range is 133kΩ < R_{ISET} < 266kΩ, which corresponds to full-scale LED current of 30mA > I_{LEDMAX} > 15mA. Connect ISET to V_{CC} for a default full-scale LED current of 25mA.

The current source output is pulse-width modulated and synchronized with a DPWM signal to reduce jitter and flicker noise in the display.

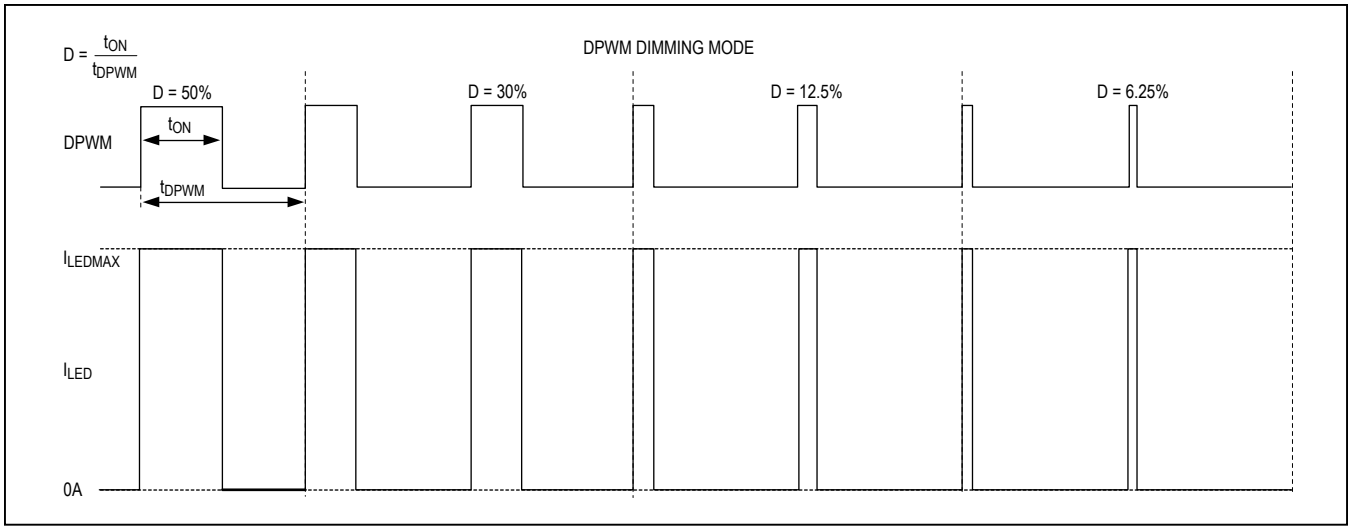


Figure 3. LED Current Control by DPWM Signal in Dimming

DPWM Frequency Setting

The MAX17061A uses an internal DPWM signal to perform dimming control. The DPWM frequency is specified by an external resistor connected from FSET pin to GND:

$$f_{DPWM} = \frac{10^9}{\alpha \times R[\Omega] + \gamma}$$

where: α = 10.638

γ = 58509

The adjustable range for the FSET resistor, R_{FSET}, is from 42kΩ to 464kΩ, corresponding to the DPWM frequency of 200Hz to 2kHz.

Dimming Control Interfaces

The MAX17061A's dimming control circuit consists of two interfaces: PWM and SMBus. The block diagram of these two input interfaces is shown in Figure 4. The dimming can be performed in three modes: PWM, SMBus, or DPST. In PWM mode, the brightness is adjusted by the PWM signal applied to the PWMI pin. In SMBus mode, the brightness is adjusted by a command from uplink processor through the 2-wire SMBus. In DPST mode, the brightness is adjusted by the product of the PWM duty cycle and SMBus command value. This DPWM control provides a dimming range with 8-bit resolution down to 2.7% and supports Intel DPST to maximize battery life.

The SMBus interface can be used to adjust the dimming, as well as shut down the MAX17061A. Before the MAX17061A receives a turn-on command from the SMBus, it automatically remains off. In this low-power state, most of the control circuits are turned off. Even in PWM dimming mode, only the PWMI interface is used for brightness control; the MAX17061A cannot run without the SMBus interface. For sister products without the SMBus interface, contact Maxim Integrated Products, Inc.

Dimming Control Register Descriptions

The MAX17061A includes four registers to monitor and control brightness, fault status, identification, and operating mode. The slave address is 0b0101100. The MAX17061A uses two multiplexers internally to direct the dimming signal processing (Figure 4). These two multiplexers are controlled by 2 bits of the device control register, PWM_SEL, and PWM_MD, respectively. The PWM_SEL bit selects either the SMBus or the PWM input to control the brightness. The PWM_MD bit selects the mode in which the PWM input is to be interpreted. Table 2 provides a complete setting of the three dimming modes (X means don't care).

In PWM mode, the output LED brightness is solely controlled by the percentage duty cycle of the input signal to PWMI. In SMBus mode, the input of PWMI has no effect on the dimming control, and only the SMBus command to brightness control register adjusts the output brightness. In DPST mode, the overall brightness level is the normalized product of the SMBus command setting and PWM input duty cycle. The PWM signal starts from 100% when operating in DPST mode.

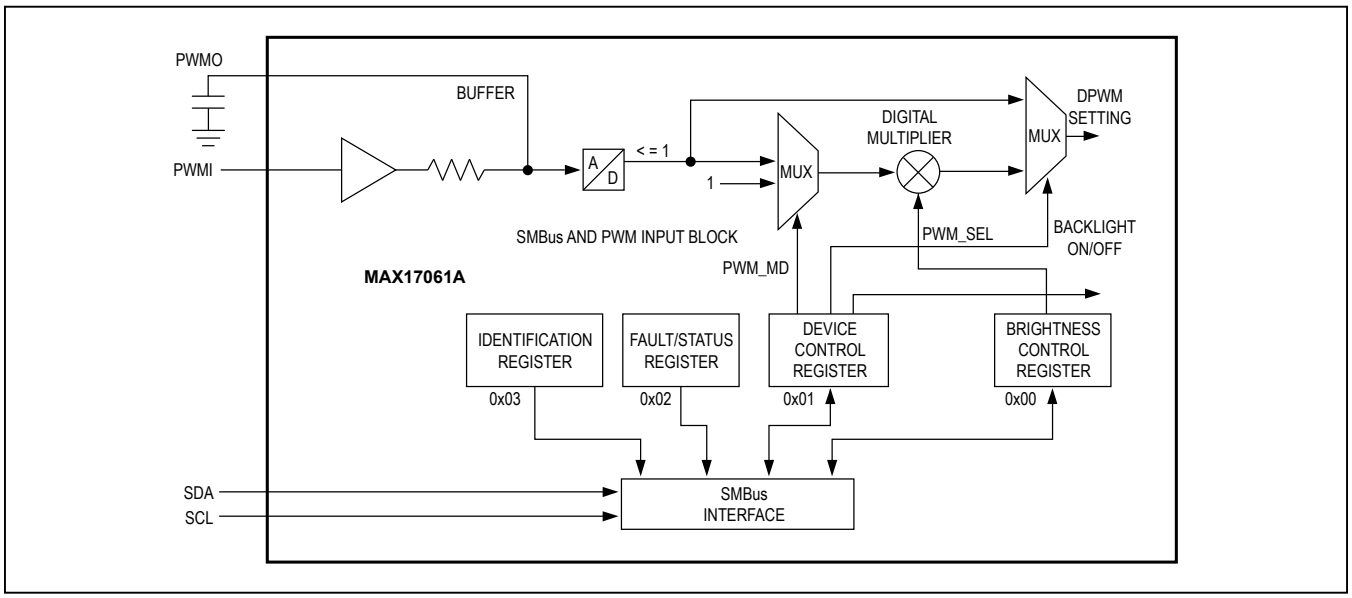


Figure 4. LED Current Control by DPWM Signal in Dimming

Brightness control register: Address is 0x00. This register is both readable and writable for all 8 bits, BRT0–BRT7, which are used to control the LED brightness level. In SMBus dimming mode, an SMBus write byte cycle to register 0x00 sets the output brightness level. The SMBus setting of 0xFF for this register sets the backlight controller to the maximum brightness output, and 0x00 sets the minimum backlight brightness (about 2.7%). The default value for register 0x00 is 0xFF. A write byte cycle to register 0x00 has no effect when the backlight controller is in PWM mode. The SMBus read byte cycle to register 0x00 returns the current brightness level, regardless of the dimming mode.

REGISTER 0x00		BRIGHTNESS CONTROL REGISTER			DEFAULT VALUE 0xFF		
BRT7	**BRT6**	**BRT5**	**BRT4**	**BRT3**	**BRT2**	**BRT1**	**BRT0**
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0

Bit field definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit [7..0]	BRT [7..0]	8-bit brightness setting, adjusting brightness levels in 256 steps, default value are 0xFF.

Device control register: Address is 0x01. This register is both readable and writable for Bit 0 to Bit 2. Bit 0, also named BL_CTL, is used as ON/OFF control for the output LEDs. Bit 1 and Bit 2, named PWM_SEL and PWM_MD, respectively, control the operating mode of the backlight controller. Bit 3 through Bit 7 are reserved bits. All reserved bits, return zero when read, and are ignored by the controller when written. A value of 1 written to BL_CTL turns on the backlight in 10ms or less after the write cycle completes. A value of zero written to BL_CTL immediately turns off the backlight.

REGISTER 0x01		DEVICE CONTROL REGISTER			DEFAULT VALUE 0x00		
RESERVED	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**PWM_MD**	**PWM_SEL**	**BL_CTL**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

Bit field definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 2	PWM_MD	PWM mode select (1 = absolute brightness, 0 = % change), default = 0
Bit 1	PWM_SEL	Brightness MUX select (1 = PWM pin, 0 = SMBus value), default = 0
Bit 0	BL_CTL	BL on/off control (1 = on, 0 = off), default = 0

Table 2. Operating Modes Selected by Device Control Register Bits 1 and 2

PWM_MD	PWM_SEL	MODE	DPWM DUTY-CYCLE SETTING
X	1	PWM mode	PWMI input duty cycle
1	0	SMBus mode	SMBus command
0	0	DPST mode	Product of PWMI input duty cycle and SMBus command

Fault/Status Register: Address is 0x02. This register has 6 status bits that allow monitoring the backlight controller's operating state. Bit 6 and Bit 7 are reserved bits, and Bit 3 is the status indicator or backlight. The other 5 bits are fault indicators. Bit 0 is a logical OR of all fault codes including LED open/short to simplify error detection. All the bits in this register are read only. The reserved bits return a zero when read.

REGISTER 0x02		FAULT STATUS REGISTER			DEFAULT VALUE 0x00		
RESERVED	**RESERVED**	**2_CH_SD**	**1_CH_SD**	**BL_STAT**	**OV_CURR**	**THRM_SHDN**	**FAULT**
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Bit field definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 5	2_CH_SD	Two or more LED output channels are faulted (1 = faulted, 0 = OK)
Bit 4	1_CH_SD	At least one LED output channel is faulted (1 = faulted, 0 = OK)
Bit 3	BL_STAT	Backlight status (1 = BL on, 0 = BL off)
Bit 2	OV_CURR	Input overcurrent (1 = overcurrent condition, 0 = current OK)
Bit 1	THRM_SHD	Thermal shutdown (1 = thermal fault, 0 = thermal OK)
Bit 0	FAULT	Any fault, logic OR of all fault conditions (1 = fault condition, 0 = no fault)

Identification Register: Address is 0x03. The ID register contains two bit fields to denote the manufacturer and the silicon revision of the controller IC. The bit field widths were chosen to allow up to 32 vendors with up to eight silicon revisions each. This register is read only. The value for the MAX17061A is 0x81.

REGISTER 0x03		ID REGISTER			DEFAULT VALUE 0x81		
LED PANEL	**MFG3**	**MFG2**	**MFG1**	**MFG0**	**REV2**	**REV1**	**REV0**
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Bit field definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 7	LED panel	Display panel using LED backlight, bit 7 = 1
Bit [6..3]	MFG[3..0]	Manufacturer ID; see Table 3, default = 0
Bit [2..0]	REV[2..0]	Silicon rev (revs 0–7 allowed for silicon spins), default = 1

The list of ID values for vendors is shown in Table 3.

Thermal Shutdown

The MAX17061A includes a thermal-protection circuit. When the local IC temperature exceeds +160°C (typ), the controller and current sources shut down and do not restart until the die temperature drops by 15°C. When thermal shutdown occurs, Bit 0 and Bit 1 of fault/status register is set to 1.

Table 3. Vendor IDs

ID	VENDOR
0	Maxim
1	Micro Semi
2	MPS
3	O2 Micro
4	TI
5	ST
6	Analog Devices
7-14	Reserved
15	Vendor ID register not implemented

Design Procedure

All MAX17061A designs should be prototyped and tested prior to production. Table 4 provides a list of power components for the typical applications circuit. Table 5 lists component suppliers.

External component value choice is primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once L is known, choose the diode and capacitors.

Step-Up Converter Current Calculation

To ensure the stable operation, the MAX17061A includes slope compensation, which sets the minimum inductor value. In continuous-conduction mode (CCM), the minimum inductor value is calculated with the following equation:

$$L_{CCM(MIN)} = \frac{\left(V_{OUT(MAX)} + V_{DIODE} - 2 \times V_{IN(MIN)}\right) \times R_S}{2 \times 24.7mV \times f_{OSC(MIN)}}$$

where 24.7mV is a scale factor from the slope compensation, the $L_{CCM(MIN)}$ is the minimum inductor value for stable operation in CCM, and R_S =12mΩ (typ) is the equivalent sensing scale factor from the controller's internal current-sense circuit.

The controller can also operate in discontinuous conduction mode (DCM). In this mode, the inductor value can be lower, but the peak inductor current is higher than in CCM. In DCM, the maximum inductor value is calculated with the following equation:

$$L_{DCM(MAX)} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)} + V_{DIODE}}\right) \times \frac{V_{IN(MIN)}^2 \times \eta}{2 \times f_{OSC(MAX)} \times V_{OUT(MAX)} \times I_{OUT(MAX)}}$$

where the $L_{DCM(MAX)}$ is the maximum inductor value for DCM, η is the nominal regulator efficiency (85%), and $I_{OUT(MAX)}$ is the maximum output current.

Table 4. Component List

SWITCHING FREQUENCY	1MHz	1MHz
White LED	Nichia NSSW008C 3.2V (typ), 3.5V (max) at 20mA	Nichia NSSW008C 3.2V (typ), 3.5V (max) at 20mA
Number of WLEDs	10 pcs x 4 strings, 25mA (max)	10 pcs x 8 strings, 25mA (max)
Input Voltage	7V to 21V	7V to 21V
Inductor	10µH, 1.2A power inductor TDK VLP6810T-100M1R2; Sumida CR6D09HPNP-100MC	10µH, 2.5A power inductor TDK SLF10145T-100M2R5-PF
Input Capacitors	4.7µF ±10%, 25V X5R ceramic capacitor (1206) Murata GRM319R61E475KA12D	10µF ±10%, 25V X5R ceramic capacitor (1206) Murata GRM31CR61E106KA
Output Capacitor C_{OUT}	0.33µF ±10%, 50V X7R ceramic capacitor (1206) (6x) Murata GRM319R71H334K TDK C3216JB1H334K	1µF ±10%, 50V X7R ceramic capacitor (1206) (4x) Murata GRM31MR71H105KA TDK C3216X7R1H105K
Diode Rectifier	0.7A, 60V Schottky diode (US-flat) Toshiba CUS04	3A, 60V Schottky diode Nihon EC31QS06

Table 5. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Nichia Corp.	248-352-6575	www.nichia.com
Sumida Corp.	847-545-6700	www.sumida.com
Toshiba America Electronic Components, Inc.	949-455-2000	www.toshiba.com/taec
Vishay	203-268-6261	www.vishay.com

The output current capability of the step-up converter is a function of current limit, input voltage, operating frequency, and inductor value. Because the slope compensation is used to stabilize the feedback loop, the inductor current limit depends on the duty cycle, and is determined with the following equation:

$$I_{LIM} = 1.9A + \frac{24.7mV \times (0.75 - D)}{R_S}$$

where 24.7mV is the scale factor from the slope compensation, 1.9A is a typical current limit at 75% duty cycle, and D is the duty cycle.

The output current capability depends on the currentlimit value and operating mode. The maximum output current in CCM is governed by the following equation:

$$I_{OUT\_CCM(MAX)} = \left(I_{LIM} - \frac{0.5 \times D \times V_{IN}}{f_{OSC} \times L} \right)$$

where I_{LIM} is the current limit calculated above, η is the nominal regulator efficiency (85%), and D is the duty cycle. The corresponding duty cycle for this current is:

$$D = \frac{V_{OUT} - V_{IN} + V_{DIODE}}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

where V_{DIODE} is the forward voltage of the rectifier diode and R_{ON} is the internal MOSFET's on-resistance (0.15Ω typ).

The maximum output current in DCM is governed by the following equation:

$$I_{OUT\_DCM(MAX)} = \frac{L \times I_{LIM}^2 \times f_{OSC} \times \eta}{2 \times (V_{OUT} + V_{DIODE} - V_{IN})}$$

Inductor Selection

The inductance, peak current rating, series resistance, and physical size should all be considered when selecting an inductor. These factors affect the converter's operating mode, efficiency, maximum output load capability, transient response time, output voltage ripple, and cost.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance minimizes the current ripple, and therefore reduces the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increases physical size and I^2R copper losses. Low inductor values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves the compromises among circuit efficiency, inductor size, and cost.

In choosing an inductor, the first step is to determine the operating mode: continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The MAX17061A has a fixed internal slope compensation that requires minimum inductor value. When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-size inductor is required, DCM mode can be chosen. In DCM mode, the inductor value and size can be minimized, but the inductor ripple current and peak current are higher than those in CCM. The controller can be stable, independent of the internal slope compensation mode, but there is a maximum inductor value requirement to ensure the DCM operating mode.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The controller operates in DCM mode when LIR is higher than 2.0, and it works in CCM mode when LIR is lower than 2.0. The best trade-off between inductor size and converter efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripples can be accepted to reduce the number of required turns and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can reduce losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, LIR higher than 2.0 can be chosen for DCM operating mode.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions. The detail design procedure for CCM can be described as follows:

Inductor Selection in CCM Operation

1) Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{OUT(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN\_MIN}}{V_{OUT}} \right)^2 \left(\frac{V_{OUT} - V_{IN\_MIN}}{I_{OUT(MAX)} \times f_{OSC}} \right) \left(\frac{\eta_{TYP}}{LIR} \right)$$

The MAX17061A has a minimum inductor value limitation for a stable operation in CCM mode at low input voltage because of the internal fixed-slope compensation. The minimum inductor value for stability is calculated with the following equation:

$$L_{CCM(MIN)} = \frac{\left(V_{OUT(MAX)} + V_{DIODE} - 2 \times V_{IN(MIN)}\right) \times R_S}{2 \times 24.7mV \times f_{OSC(MIN)}}$$

where 24.7mV is a scale factor from slope compensation, and the R_S is the equivalent current-sensing scale factor (12mΩ typ):

1) Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$, using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*.

$$I_{IN(DC,MAX)} = \frac{I_{OUT(MAX)} \times V_{OUT}}{V_{IN(MIN)} \times \eta_{MIN}}$$

2) Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{OUT(MAX)} - V_{IN(MIN)}\right)}{L \times V_{OUT(MAX)} \times f_{OSC}}$$

Inductor Selection in DCM Operation

When DCM operating mode is chosen to minimize the inductor value, the calculations are different from those above in CCM mode. The maximum inductor value for DCM mode is calculated with the following equation:

The peak-inductor current in DCM is calculated with fo lowing equation:

$$L_{DCM(MAX)} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)} + V_{DIODE}}\right) \times \frac{V_{IN(MIN)}^2 \times \eta}{2 \times f_{OSC(MAX)} \times V_{OUT(MAX)} \times I_{OUT(MAX)}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Inductor Selection Design

Examples:

Considering the *Figure 1. Typical Operating Circuit* with four 10-LED strings and 25mA LED full-scale current, the maximum load current ($I_{OUT(MAX)}$) is 100mA with a 35.9V output and a minimal input voltage of 7V.

Choosing a CCM operating mode with LIR = 1 at 1MHz and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{7V}{35.9V}\right)^2 \left(\frac{35.9V - 7V}{100mA \times 1MHz}\right)\left(\frac{0.85}{1}\right) = 9.44\mu H$$

In CCM, the inductor has to be higher than $L_{CCM(MIN)}$:

$$L_{CCM(MIN)} = \frac{\left(35.9V + 0.4V - 2 \times 7V\right) \times 12m\Omega}{2 \times 24.7mV \times 0.9MHz} = 6.0\mu H$$

A10µH inductor is chosen, which is higher than the minimum L that guarantees stability in CCM.

The peak-inductor current at minimum input voltage is calculated as follows:

$$I_{PEAK} = \frac{100mA \times 35.9V}{7V \times 0.85} + \frac{7V \times \left(35.9V - 7V\right)}{2 \times 10\mu H \times 35.9V \times 0.9MHz} = 0.92A$$

Alternatively, choosing a DCM operating mode at 750kHz and estimating efficiency of 85% at this operating point:

$$L_{DCM(MAX)} = \left(1 - \frac{7V}{35.9V + 0.4V}\right) \times \frac{(7V)^2 \times 0.85}{2 \times 0.825MHz \times 35.9V \times 100mA} = 5.6\mu H$$

A 4.7µH inductor is chosen. The peak inductor current at minimum input voltage is calculated as follows:

$$I_{PEAK} = \sqrt{\frac{100mA \times 2 \times 35.9V \times \left(35.9V + 0.4V - 7V\right)}{4.7uH \times 0.675MHz \times 0.85 \times \left(35.9V + 0.4V\right)}} = 1.47A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging on the output capacitor, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{OUT(MAX)}}{C_{OUT}} \left(\frac{V_{OUT(MAX)} - V_{IN(MIN)}}{V_{OUT(MAX)} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK}R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section).

The output voltage ripple should be low enough for the FB_ current-source regulation. The ripple voltage should be less than $200mV_{P-P}$. For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. The actual capacitance of a ceramic capacitor is reduced by DC voltage biasing. Ensure the selected capacitor has enough capacitance at actual DC biasing.

Rectifier Diode Selection

The MAX17061A's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PEAK} calculated in the *Inductor Selection* section and that its breakdown voltage exceeds the output voltage.

Overvoltage Protection Determination

The OV protection circuit should ensure the circuit safe operation; therefore, the controller should limit the output voltage within the ratings of all MOSFET, diode, and output capacitor components, while providing sufficient output voltage for LED current regulation. The OV pin is tied to the center tap of a resistive voltage-divider (R1 and R2 in Figure 1) from the high-voltage output. When the controller detects the OV pin voltage reaching the threshold V_{OV_TH}, typically 1.23V, OV protection is activated. Hence, the step-up converter output overvoltage protection point is:

$$V_{OUT(OVP)} = V_{OV\_TH} \times \left(1 + \frac{R1}{R2}\right)$$

In Figure 1, the output OVP voltage is set to:

$$V_{OUT(OVP)} = 1.236V \times (1 + \frac{2.21M\Omega}{61.9k\Omega}) \approx 45V$$

Input Capacitor Selection

The input capacitor (C_{IN}) filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the *Figure 1. Typical Operating Circuit* (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. In some applications, C_{IN} can be reduced below the values used in the *Figure 1. Typical Operating Circuit* (Figure 1). Ensure a low-noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter.

LED Selection and Bias

The series/parallel configuration of the LED load and the full-scale bias current have a significant effect or regulator performance. LED characteristics vary significantly from manufacturer to manufacturer. Consult the respective LED data sheets to determine the range of output voltages for a given brightness and LED current. In general, brightness increases as a function of bias current. This suggests that the number of LEDs could be decreased if higher bias current is chosen; however, high current increases LED temperature and reduces operating life. Improvements in LED technology are resulting in devices with lower forward voltage and while increasing the bias current and light output.

LED manufacturers specify LED color at a given LED current. With lower LED current, the color of the emitted light tends to shift toward the blue range of the spectrum. A blue bias is often acceptable for business applications but not for high-image-quality applications such as DVD players. Direct DPWM dimming is a viable solution for reducing power dissipation while maintaining LED color integrity. Careful attention should be paid to switching noise to avoid other display quality problems.

Using fewer LEDs in a string improves step-up converter efficiency, and lowers breakdown voltage requirements of the external MOSFET and diode. The minimum number of LEDs in series should always be greater than maximum input voltage. If the diode voltage drop is lower than maximum input voltage, the voltage drop across the current-sense inputs (FB_) increases and causes excess heating in the IC. Between 8 and 12 LEDs in series are ideal for input voltages up to 20V.

Applications Information

LED $V_{FB\_}$ Variation

The MAX17061A has accurate (±1.5%) matching for each current source. However, the forward voltage of each white LED can vary up to 25% from part to part. The accumulated voltage difference in each string equates to additional power loss within the IC. For the best efficiency, the voltage difference between strings should be minimized. The difference between lowest voltage string and highest voltage string should be less than 4.8V (typ). Otherwise, the internal LED shortprotection circuit disables the high FB string.

FB Pin Maximum Voltage

The current through each FB_ pin is controlled only during the step-up converter's on-time. During the converter's off-time, the current sources are turned off. The output voltage does not discharge and stays high. The MAX17061A disables the FB current source to which the string is shorted. In this case, the step-up converter's output voltage is always applied to the disabled FB pin. The FB_ pin can withstand 45V.

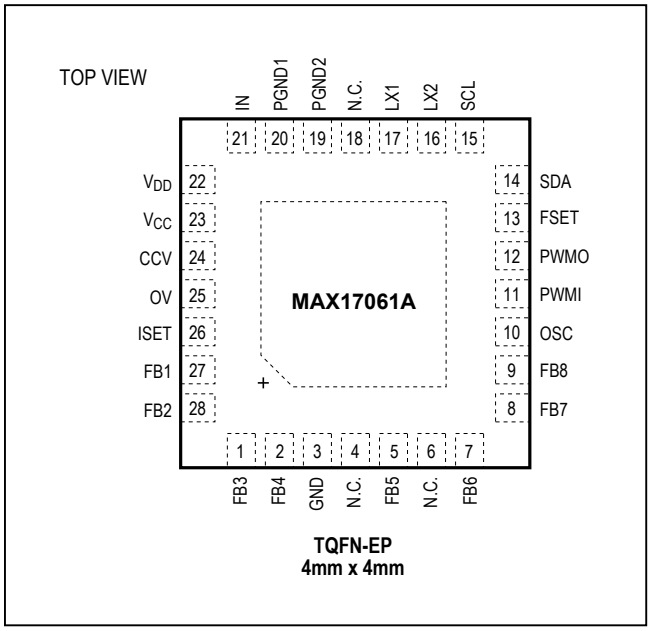
PCB Layout Guidelines

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high current switching loop of rectifier diode, internal MOSFET, and output capacitor to avoid excessive switching noise.
2) Connect high-current input and output components with short and wide connections. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the internal MOSFET, then to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode, to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.
3) Create a ground island (PGND) consisting of the input and output capacitor ground and negative terminal of the current-sense resistor. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the powerground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground island (AGND) consisting of the overvoltage detection divider ground connection, the ISET and FSET resistor connections, CCV capacitor connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the GND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
4) Place the overvoltage detection divider resistors as close as possible to the OV pin. The divider's center trace should be kept short. Placing the resistors far away causes the sensing trace to become antennas that can pick up switching noise. Avoidrunning the sensing traces near LX.
5) Place IN pin bypass capacitor as close as possible to the device. The ground connection of the IN bypass capacitor should be connected directly to GND pins with a wide trace.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and ground. If possible, avoid running the LX node from one side of the PCB to the other. Use DC traces as shield if necessary.

Refer to the MAX17061A evaluation kit for an example of proper board layout.

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T-2844+1	21-0139	90-0035

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17061AETI+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/09	Initial release	—
1	11/14	No /V OPNs; deleted “Automotive Systems” from *Applications* section; moved *Ordering Information* to end of data sheet; updated *Package Information*	1, 24

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