MAX14781E

Half-Duplex RS-485 Transceiver with Polarity Correction

General Description

The MAX14781E +5V, half-duplex ±25kV ESD-protected RS-485 transceiver features integrated automatic polarity correction to ensure that miswired A and B lines are autonomously corrected, simplifying equipment and network installation.

The MAX14781E includes slew-rate limited drivers that minimize EMI, allowing for error-free data transmission up to 370kbps.

This device includes fail-safe circuitry, guaranteeing a logic-high receiver output when the receiver inputs are shorted or open. Hot-swap functionality on the receiver and driver enable inputs also eliminates false transitions on the bus during power-up or live insertion.

The MAX14781E features a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. All driver outputs are protected up to ±25kV ESD using the Human Body Model. The MAX14781E is available in an 8-pin SO package and operates over the extended -40°C to +85°C temperature range.

Applications

- Power Meter Networks
- HVAC Networks
- Control Systems

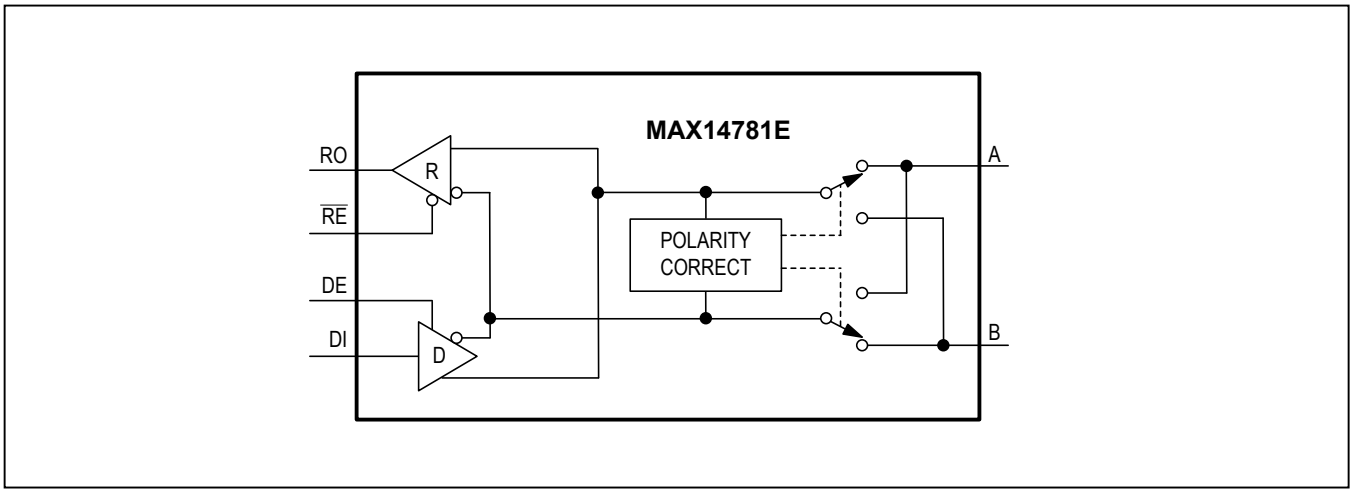
Benefits and Features

- Automatic Polarity Correction
- Integrated Protection Increases Robustness
  - High ESD Protection
    - ±25kV HBM ESD
    - ±15kV IEC 61000-4-2 Air Gap Discharge ESD
    - ±9kV IEC 61000-4-2 Contact Discharge ESD
  - True Fail-Safe Receiver
  - Hot-Swap Functionality
- +5V Operation
- Low 10µA (max) Shutdown Current
- Extended -40°C to +85°C Operating Temperature

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14781E.related.

Functional Diagram



19-6859; Rev 0; 12/13

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND)
V_{CC} ..... -0.3V to +6.0V
$\overline{RE}$, RO ..... -0.3V to (V_{CC} + 0.3V)
DE, DI ..... -0.3V to +6.0V
A, B ..... -8.0V to +13V
Short-Circuit Duration (RO, A, B) to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate at 7.6mW/°C above +70°C) 606mW
Operating Temperature Range ..... -40ºC to +85ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150°C
Lead Temperature (soldering 10 sec) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 132°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 38°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 5V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.)(Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Supply Voltage	V_{CC}			4.5		5.5	V
Differential Driver Output	V_{OD}	R_L = 100Ω, Figure 1		3		V_{CC}	V
		R_L = 54Ω, Figure 1		2		V_{CC}	
		No load, Figure 1				V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 4)			V_{CC} /2	3	V
Change in Magnitude of Common-Mode Otput Voltage	ΔV_{OC}	R_L = 54Ω, Figure 1 (Note 4)				0.2	V
Input Voltage High	V_{IH}	DE, DI, $\overline{RE}$		3.0			V
Input Voltage Low	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN}	DE, $\overline{RE}$		-1		+1	µA
Input Impedance Until First Transition at Power-Up (DE, $\overline{RE}$)	R_{FTPU}	Until the first DE/$\overline{RE}$ transition occurs, Figure 9 (Note 7)		3.65		8.8	kΩ
Input Impedance Until First Transition After POR Delay (DE, $\overline{RE}$)	R_{FTPOR}	Until the first DE/$\overline{RE}$ transition occurs, Figure 9		7		60	kΩ
Driver Short-Circuit Output Current	I_{OSD}	Driver is in short circuit (Note 5)	Output low, 0V ≤ V_{OUT} ≤ 12V	+40		+250	mA
			Output high, -7V ≤ V_{OUT} ≤ V_{CC}	-250		-40	

Electrical Characteristics (continued)

(V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.)(Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Short-Circuit Foldback Ouptut Current	I_{OSDF}	Driver is in short circuit (Note 5)	Output low, (V_{CC} -1V) ≤ V_{OUT} ≤ 12V	20			mA
			Output high, -7V ≤ V_{OUT} ≤ +1V			-20	
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising			+175		°C
Thermal Shutdown Hysteresis	T_{HYST}				15		°C
Input Current (A and B)	$I_{A,B}$	DE = low, V_{CC} = 0V or 5V	V_{IN} = 12V			125	µA
			V_{IN} = -7V	-100			
RECEIVER							
Receiver Differential Threshold Voltages	V_{TH1}	-7V ≤ V_{CM} ≤ +12V	Normal/ noninverted mode	-200	-125	-50	mV
	V_{TH2}		Inverted mode	+50	+125	+200	
Receiver Input Hysteresis	ΔV_{TH}	V_A + V_B = 0V			15		mV
Receiver Output Voltage High	V_{OH}	$\overline{RE}$ = low, I_{SOURCE} = -1mA		V_{CC} - 0.6			V
Receiver Output Voltage Low	V_{OL}	$\overline{RE}$ = low, I_{SINK} = 1mA				0.4	V
Receiver Three-State Output Current	I_{OZR}	$\overline{RE}$ = high, 0V ≤ V_{RO} ≤ V_{CC}		-1		+1	µA
Receiver Output Short Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}		-110		+110	mA
POLARITY DETECTION							
Maximum A-B Voltage Difference for Inverted Polarity	V_{PI}	(V_A - V_B) for at least t_{PM}				-200	mV
Minimum A-B Voltage Difference for Normal Polarity	V_{PN}	(V_A - V_B) for at least t_{PM}		+200			mV
Polarity Monitoring Interval	t_{PM}	(Note 6)		8.3		20	ms
SUPPLY CURRENT							
Supply Current	I_{CC}	DE = high, $\overline{RE}$ = low, no load			1.2	1.8	mA
Shutdown Supply Current	I_{SHDN}	DE = low, $\overline{RE}$ = high				10	µA
PROTECTION							
ESD Protection (A and B Pins)		Human Body Model			±25		kV
		IEC 61000-4-2 Air Gap Discharge to GND			±15		
		IEC 61000-4-2- Contact Discharge to GND			±9		
ESD Protection (All Other Pins)		Human Body Model			±2		kV

Switching Characteristics

(V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.)(Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay	t_{DPLH}	R_L = 54Ω, C_L = 50pF, Figures 2, 3	200		1000	ns
	t_{DPHL}		200		1000	
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figures 2, 3			140	ns
Driver Differential Output Rise or Fall Time	t_R, t_F	R_L = 54Ω, C_L = 50pF, Figures 2, 3	250		900	ns
Maximum Data Rate	DR_{MAX}		370			kbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF, Figures 4, 5 (Note 9)			2500	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF, Figures 4, 5 (Note 9)			2500	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF, Figures 4, 5 (Note 9)			100	ns
Driver Disable Time from High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figures 4, 5 (Note 9)			100	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figures 4, 5 (Note 9)			5.5	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figures 4, 5 (Note 9)			5.5	µs
Time to Shutdown	t_{SHDN}	(Note 10)	50	340	700	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}	C_L = 15pF, Figures 6, 7			200	ns
	t_{RPLH}				200	
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figures 6, 7			30	ns
Maximum Data Rate	DR_{MAX}		0.125		500	kbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			50	ns

Switching Characteristics (continued)

(V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.)(Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			50	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			50	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			5.5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8 (Note 9)			5.5	µs
Time to Shutdown	t_{SHDN}	(Note 10)	50	340	700	ns

Note 2: All devices are 100% production tested at T_A = +25°C. Spefications over temperature are guaranteed by design.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to ground, unless otherwise noted.

Note 4: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 5: The short-circuit output current applies to the peak current just prior to foldback current limiting. The short-circuit foldback output current applies during current limiting to allow recovery from a bus contention.

Note 6: t_{PM} is the interval, with no A/B switching activity, after which the internal logic circuitry records the polarity. t_{PM} includes the correction delay, after which the polarity is changed.

Note 7: Not production tested. Guaranteed by design.

Note 8: Capacitive loads include test probe and fixture capacitance.

Note 9: This parameter refers to the driver/receiver enable delay when the device has exited the initial hot-swap state and is in normal operating mode.

Note 10: Shutdown is enabled by driving $\overline{RE}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.

Test Circuits and Waveforms

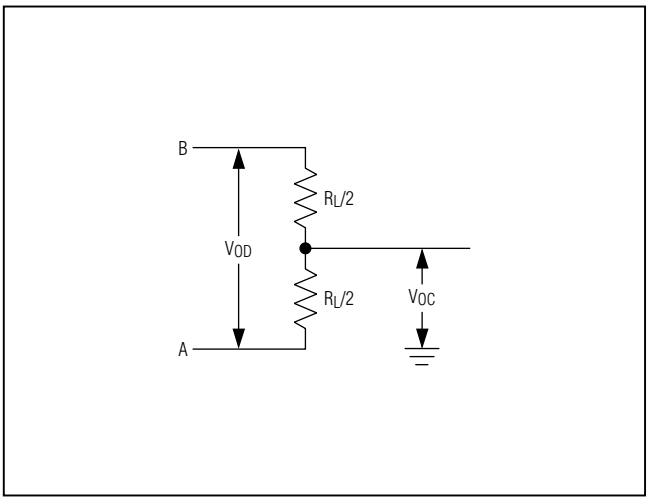


Figure 1. Driver DC Test Load

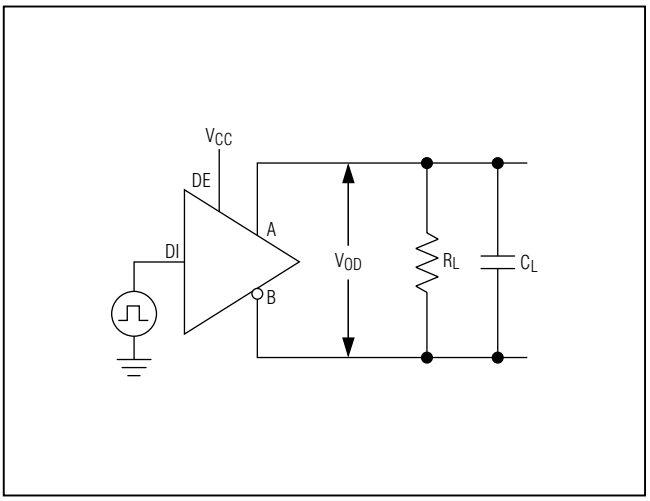


Figure 2. Driver Timing Test Circuit

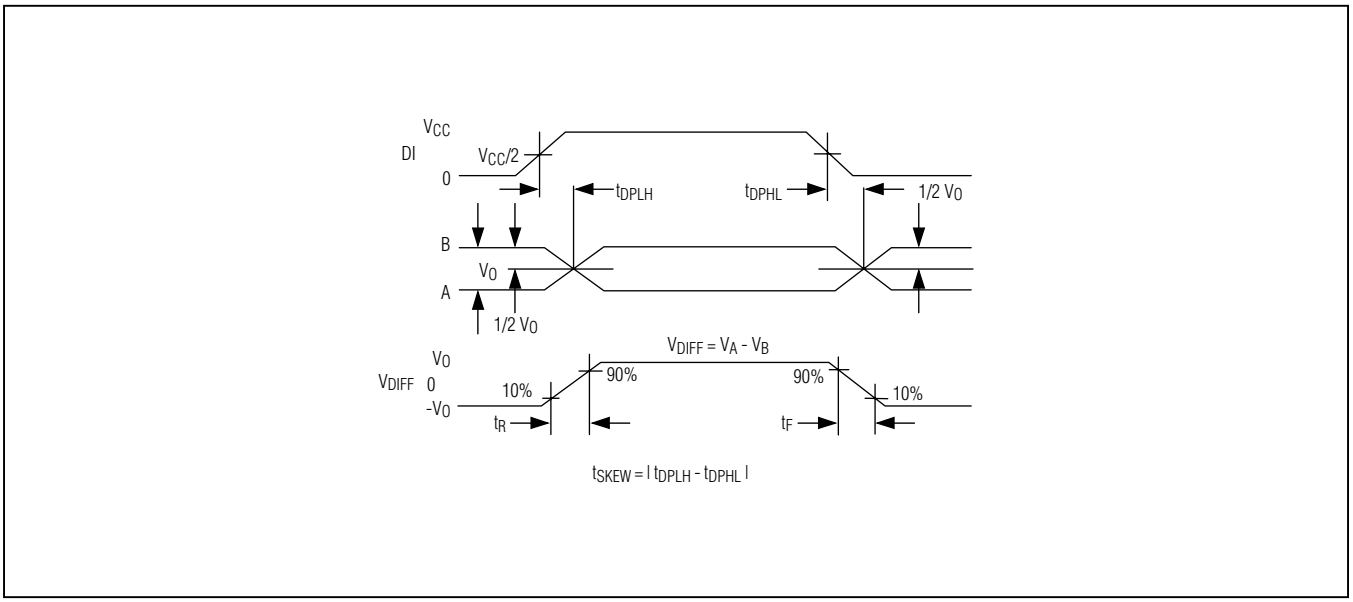


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

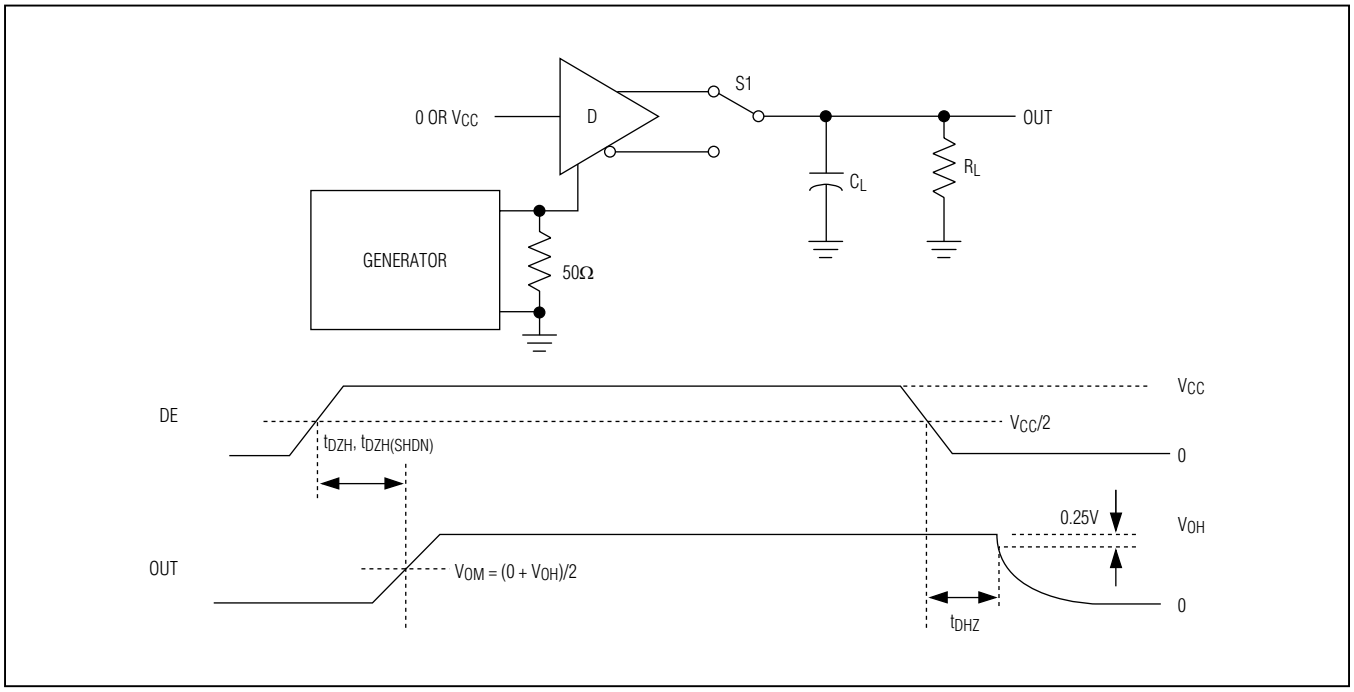


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

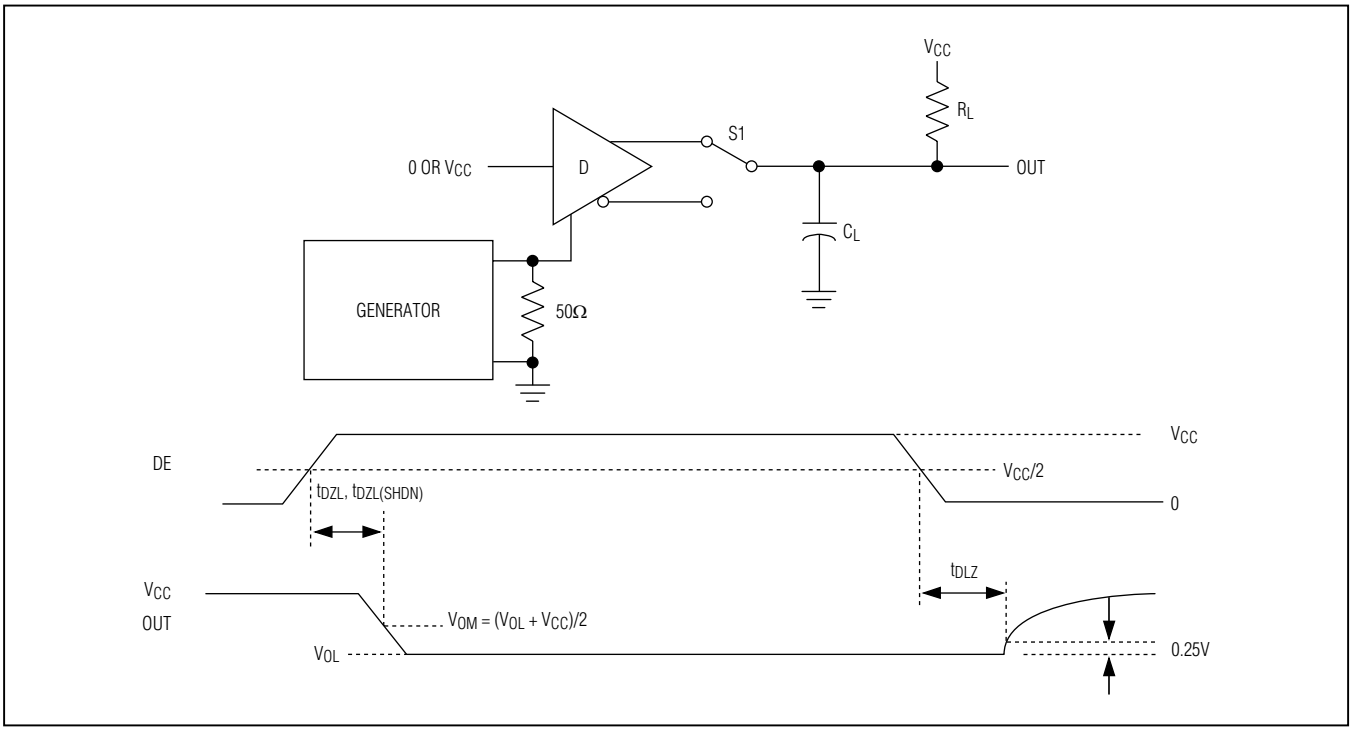


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ}, $t_{DLZ(SHDN)}$)

Test Circuits and Waveforms (continued)

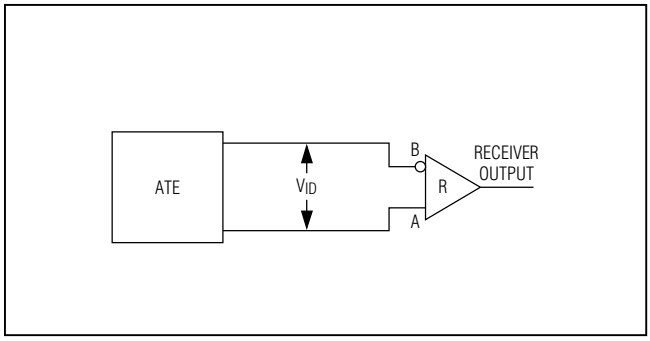


Figure 6. Receiver Propagation Delay Test Circuit

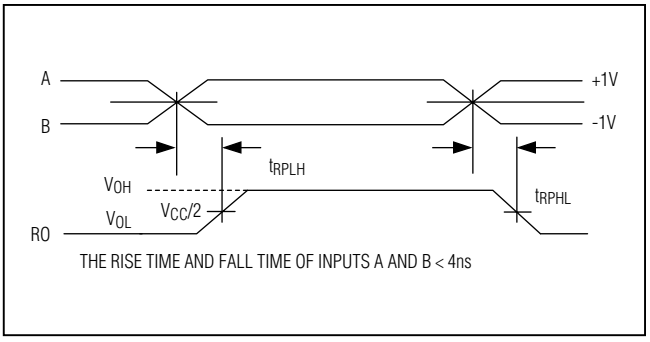


Figure 7. Receiver Propagation Delays

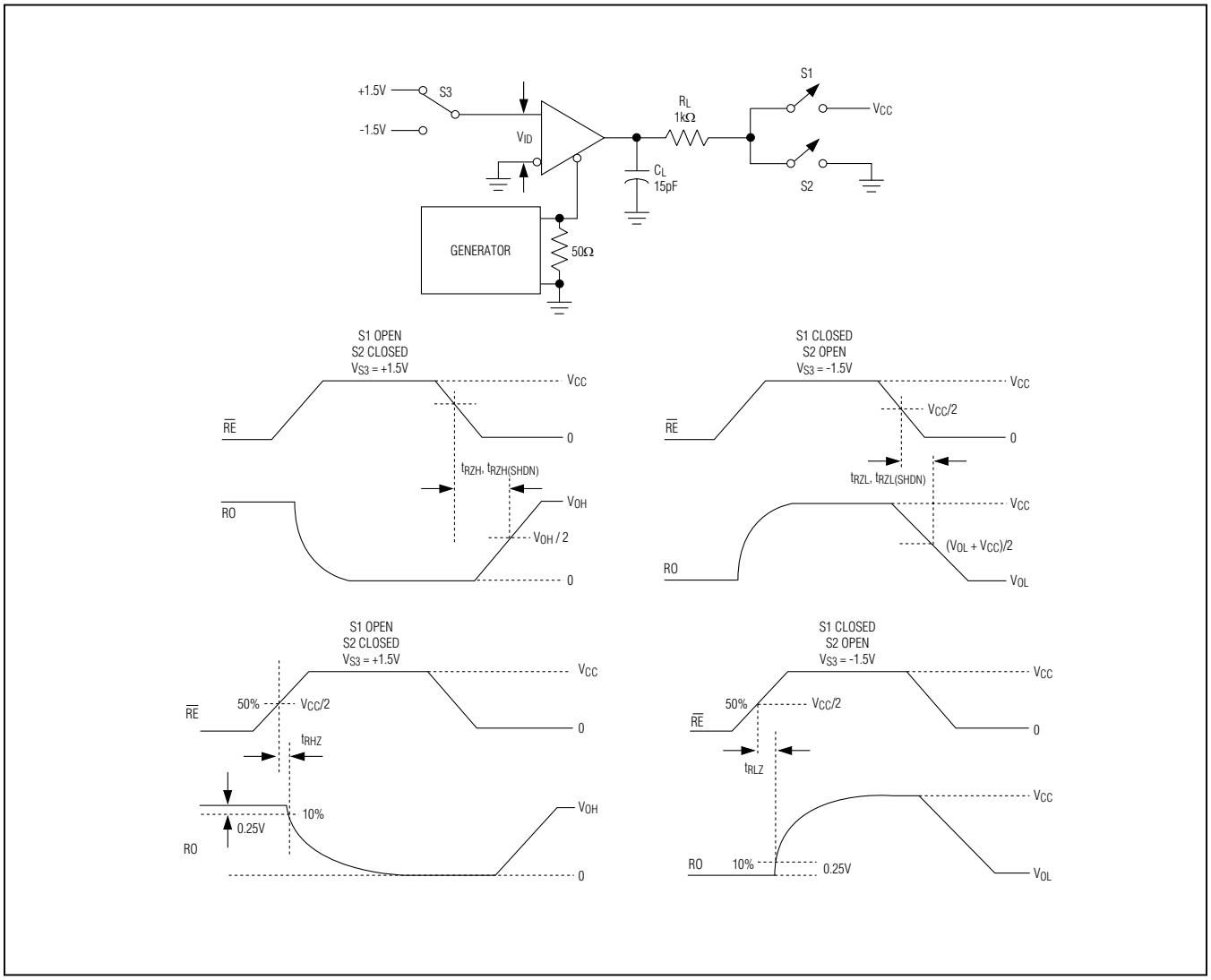
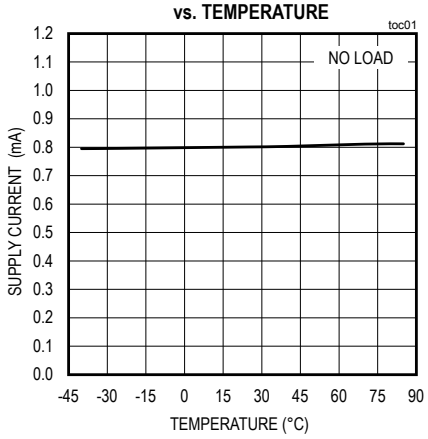


Figure 8. Receiver Enable and Disable Times

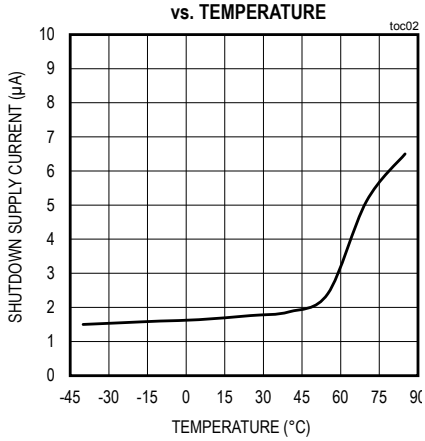
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

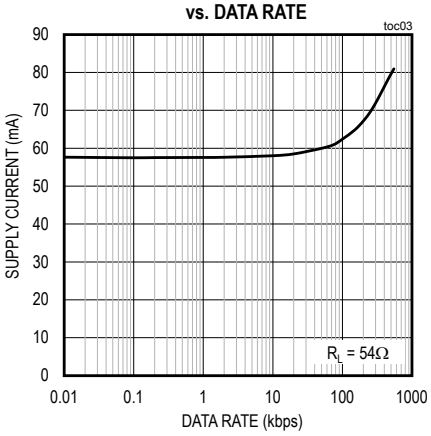
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



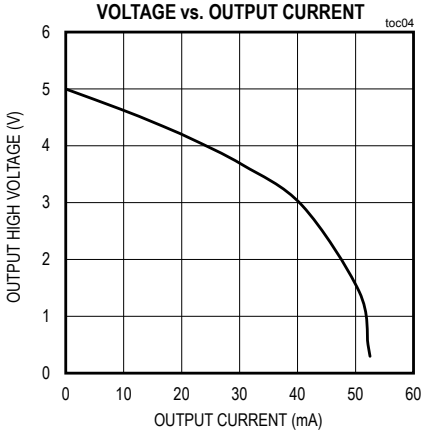
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



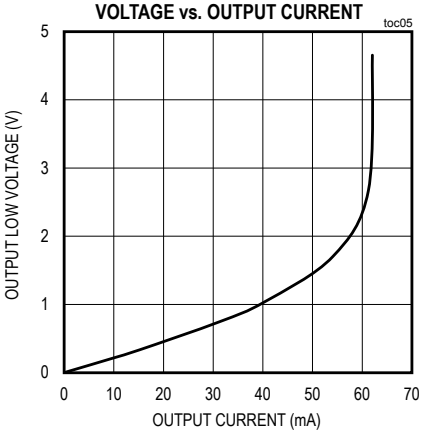
SUPPLY CURRENT vs. DATA RATE



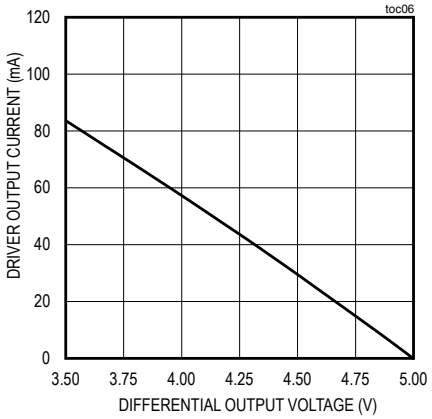
RECEIVER OUTPUT HIGH VOLTAGE vs. OUTPUT CURRENT



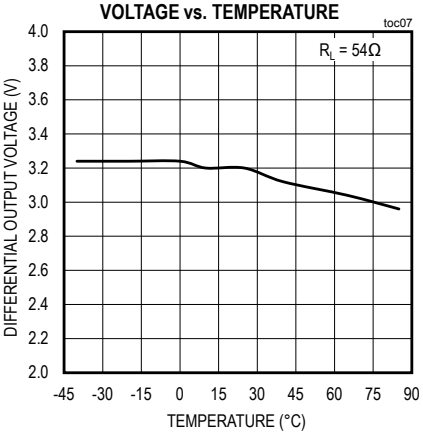
RECEIVER OUTPUT LOW VOLTAGE vs. OUTPUT CURRENT



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



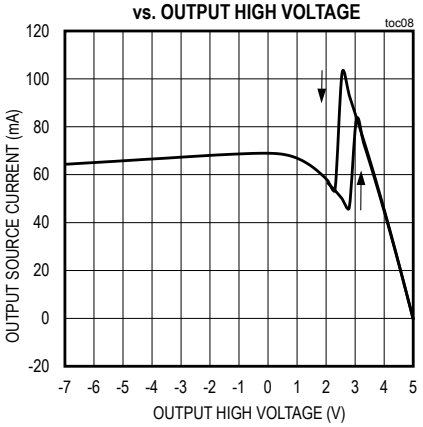
DIFFERENTIAL DRIVER OUTPUT VOLTAGE vs. TEMPERATURE



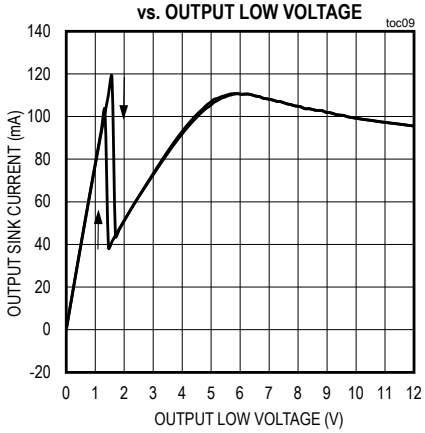
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

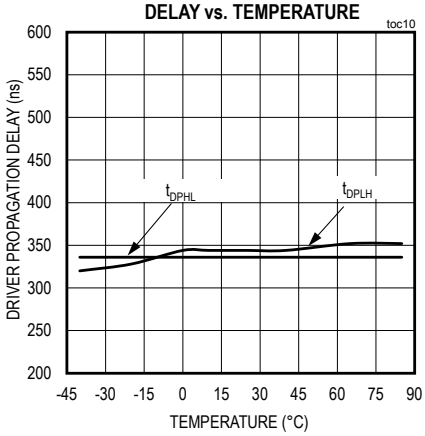
DRIVER OUTPUT SOURCE CURRENT vs. OUTPUT HIGH VOLTAGE



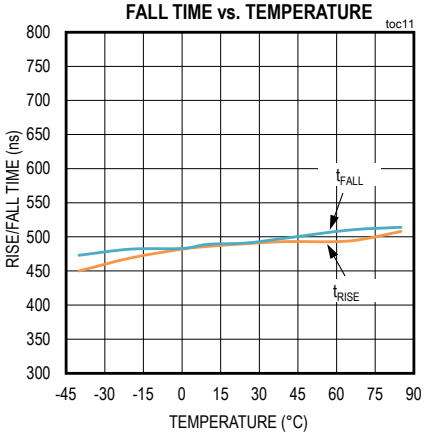
DRIVER OUTPUT SINK CURRENT vs. OUTPUT LOW VOLTAGE



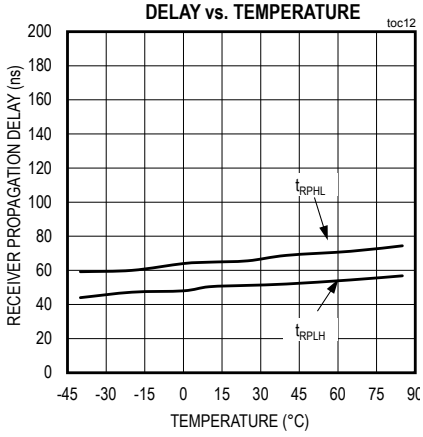
DRIVER PROPAGATION DELAY vs. TEMPERATURE



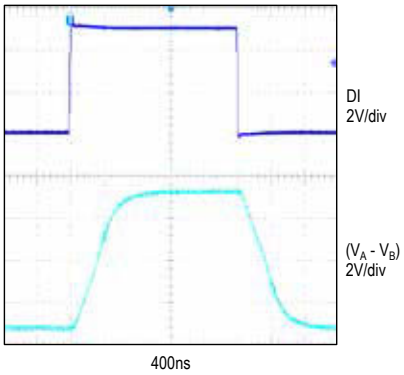
DIFFERENTIAL DRIVER OUTPUT RISE AND FALL TIME vs. TEMPERATURE



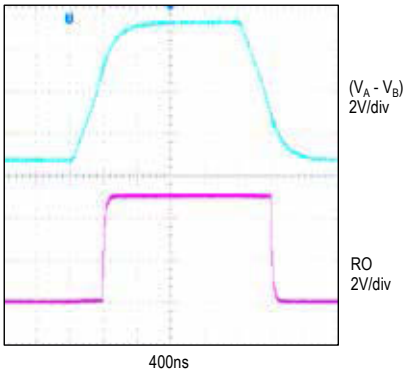
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



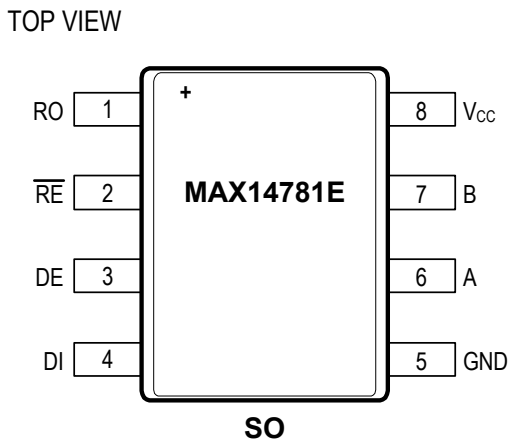
DRIVER PROPAGATION DELAY



RECEIVER PROPAGATION DELAY



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. See the *Receiving Functional Table* for details. RO is high impedance when $\overline{RE}$ is high.
2	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low to enable RO. RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the *Hot Swap Capability* section for details).
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for details).
4	DI	Driver Input. See the *Transmitting Functional Table* for details.
5	GND	Ground
6	A	Noninverting Receiver Input/Driver Output*
7	B	Inverting Receiver Input/Driver Output*
8	V_{CC}	Positive Supply. Bypass V_{CC} to GND with a 0.1µF capacitor.

**This is the default polarity at power-up. In case of polarity correction, A becomes the inverting receiver input/driver output and the B is the noninverting receiver input/driver output.*

Function Tables

TRANSMITTING					
INPUTS			DETECTED POLARITY	OUTPUTS	
$\overline{RE}$	DE	DI		A	B
X	1	1	Normal	1	0
		0	Normal	0	1
		1	Inverted	0	1
		0	Inverted	1	0
0	0	X	X	High-Z	High-Z
1	0	X	X	Shutdown	

X = Don't care

RECEIVING				
INPUTS				OUTPUTS
$\overline{RE}$	DE	DETECTED POLARITY	$(V_A - V_B)$ for TIME < t_{PM}	RO
0	X	Normal	≥ -50mV	1
		Inverted	< 50mV	1
		X	Open/Shorted	1
		Normal	< -200mV	0
		Inverted	≥ 200mV	0
1	1	X	X	High-Z
1	0	X	X	Shutdown

X = Don't care

Detailed Description

The MAX14781E half-duplex RS-485 transceiver features automatic polarity correction on the RS-485 bus lines. This device also includes fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when connected to a terminated transmission line with all drivers disabled. Hot-swap capability on the enable inputs allows line insertion without erroneous data transfer and controlled slew-rate drivers minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 370kbps.

The MAX14781E features short-circuit current limits on the driver and receiver outputs and thermal shutdown circuitry to protect against excessive power dissipation.

Fail-Safe

The MAX14781E receiver input threshold is between -50mV and -200mV, guaranteeing a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. If the differential receiver input voltage is less than or equal to -200mV for less than the idle period, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by termination. With the receiver threshold of the MAX14781E, this results in a logic-high with a 50mV minimum noise margin. The -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of these devices to defined logic level. Leakage currents up to ±10µA from the high-impedance state of the processor's logic driver could cause standard CMOS enable inputs of a transceiver to drive to an incorrect logic level.

Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerating input.

Hot-Swap Input Circuitry

The enable inputs feature hot-swap capability. At the input, there are two nMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal 10µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 500µA current sink, and M1, a 100µA current sink, pull DE to GND through a 5kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$ there is a complementary circuit employing two pMOS devices that pull $\overline{RE}$ to V_{CC}.

Automatic Polarity Detection

The MAX14781E is designed to detect and correct installation-based connections on RS-485 lines. With the driver disabled, internal detection circuitry samples the voltages at the A and B inputs during an idle period (20ms, min) and configures the driver and receiver for the detected polarity. Polarity is swapped only when $|V_A - V_B| > 200mV$ for the idle period (Table 1 and 2). The A/B line polarity can be defined by a pullup and pulldown resistor pair on the A/B lines, for example, in the RS-485 half-duplex master terminal (see the *Typical Operating Circuit*).

When the polarity is normal, A is the noninverting receiver input/driver output and B is the inverting input/output. When the polarity is inverted, A is the inverting input/output and B is the noninverting input/output.

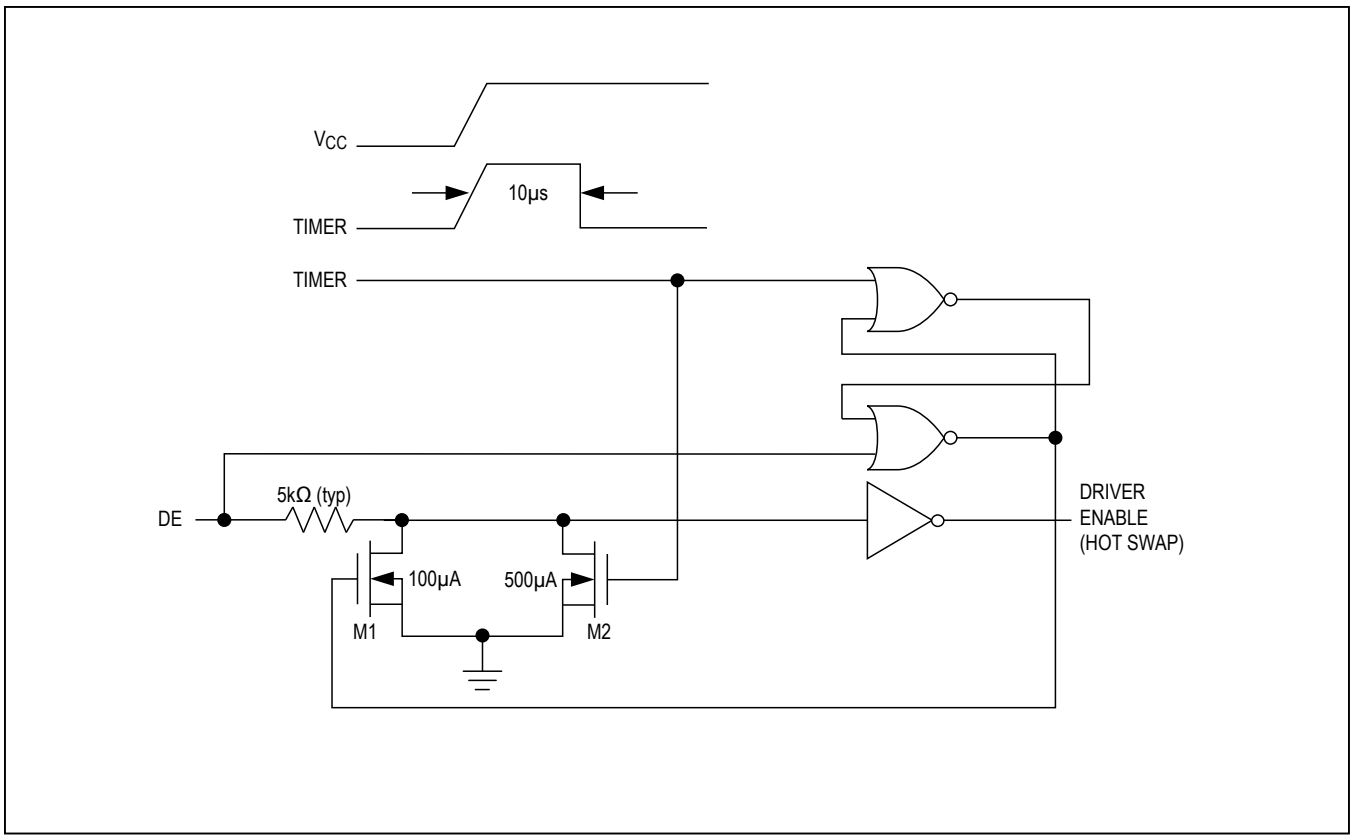


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

Table 1. Polarity Detection Starting from Normal Polarity

INPUTS			POLARITY DETECTION	POLARITY AFTER t_{PM} TIME
DE	$\overline{RE}$	(V_A - V_B) FOR TIME > t_{PM}		
0	0	Open/Shorted	ON	Normal/ Previous Detection Polarity
		> -50mV	ON	Normal/ Previous Detection Polarity
		< -200mV	ON	Inverted
1	1	X	OFF	Previous Detection Polarity
1	0	X	OFF	Previous Detection Polarity
0	1	X	OFF	Previous Detection Polarity

X = Don't care

Table 2. Polarity Detection Starting from Inverted Polarity

INPUTS			POLARITY DETECTION	POLARITY AFTER t_{PM} TIME
DE	$\overline{RE}$	(V_B - V_A) FOR TIME > t_{PM}		
0	0	Open/Shorted	ON	Inverted/ Previous Detection Polarity
		> -50mV	ON	Inverted/ Previous Detection Polarity
		< -200mV	ON	Normal
1	1	X	OFF	Previous Detection Polarity
1	0	X	OFF	Previous Detection Polarity
0	1	X	OFF	Previous Detection Polarity

X = Don't care

The polarity detection circuitry is disabled when the driver is enabled or when the transceiver is in low-power shutdown mode.

±25kV ESD (HBM) Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver input of the MAX14781E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±25kV (HBM) without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX14781E keeps working without latch-up or damage.

The transmitter output and receiver input of the MAX14781E are characterized for protection to the following limits:

- ±25kV using the Human Body Model
- ±9kV using the Contact Discharge method specified in IEC 61000-4-2
- ±15kV using the Air-Gap Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

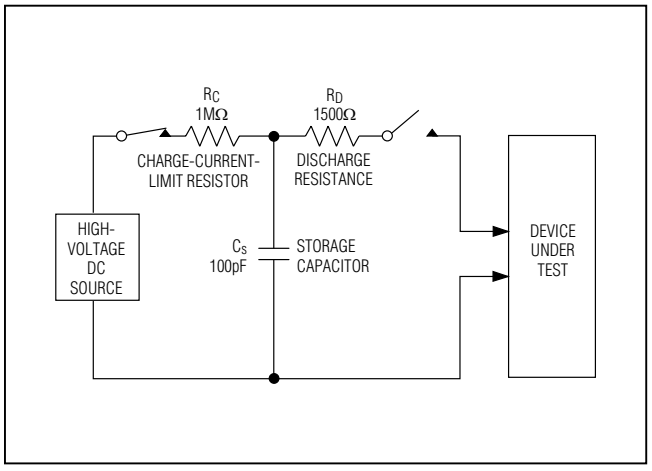


Figure 10a. Human Body ESD Test Model

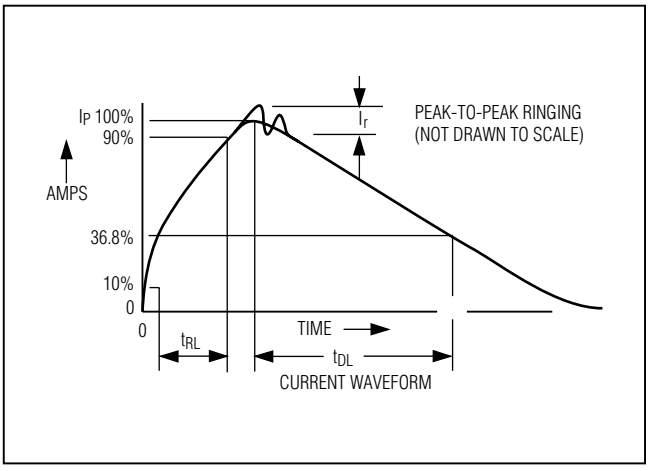


Figure 10b. Human Body Current Waveform

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14781E helps in designing equipment to meet IEC 61000-4-2, without the need for additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Applications Information

Reduced EMI and Reflections

The MAX14781E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 375kbps.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. In shutdown, the device typically draws less than 10µA (max) of supply current.

$\overline{RE}$ and DE can be driven simultaneously, the device is guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 700ns, the device is guaranteed to enter shutdown.

Enable times t_{ZH} and t_{ZL} (see the *Switching Characteristics* section) assume the devices were not in the low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the devices were in shutdown state. It takes driver and receivers longer to become enabled from low-power shutdown mode ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature exceeds +175°C.

Typical Applications

The MAX14781E transceiver is designed for bidirectional data communications on half-duplex multipoint bus transmission lines.

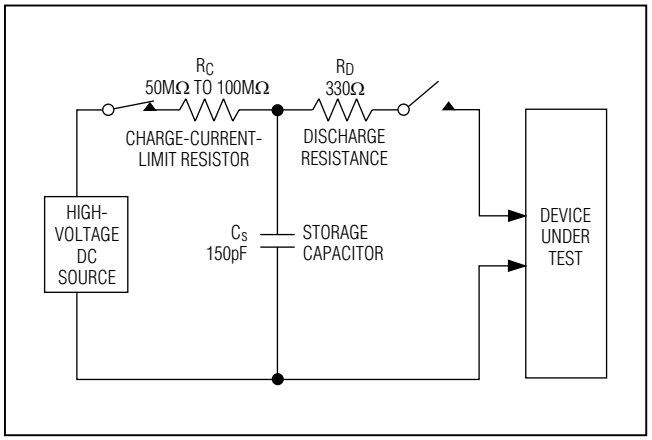


Figure 10c. IEC 61000-4-2 Test Model

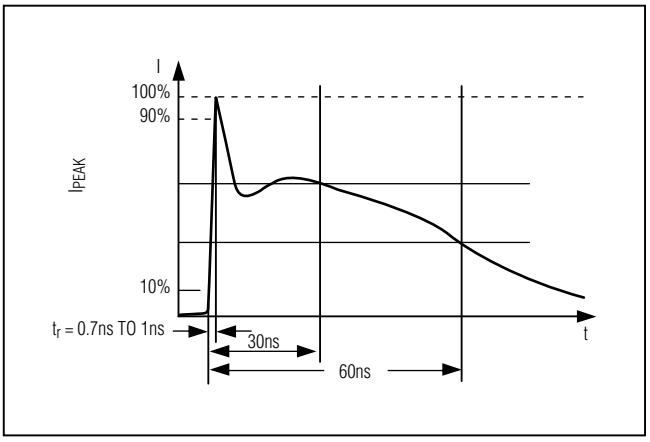


Figure 10d. IEC 61000-4-2 ESD Generator Current Waveform

Automatic polarity detection and correction in the MAX14781E is based on having non-changing voltages on the A/B bus signals for longer than 20ms that define the reference polarity. Fixing the A/B voltages can be achieved during the idle intervals in master/slave communication.

Passive Polarity Definition

To allow the bus to define A/B polarity, connect one pullup/pulldown resistor pair to the bus to set the bus status during the idle periods. It is preferable to locate the resistor pair in the bus master, as shown in Figure 11.

Active Polarity Definition

Alternatively, the bus polarity can be defined actively by the bus master. For this technique, connect differential termination resistors on the bus, preferably in the bus master module, as shown in Figure 12. The termination resistor ensures that the differential (V_A – V_B) voltage during bus idle times is zero. The MAX14781E fail-safe feature ensures that the receiver outputs are logic high and that the detected polarity is not changed during the idle time. This active technique requires the bus master to the A/B signals to a constant DC condition for over 20ms. The master can do this by driving its DE high for longer than 20ms while DI is logic high.

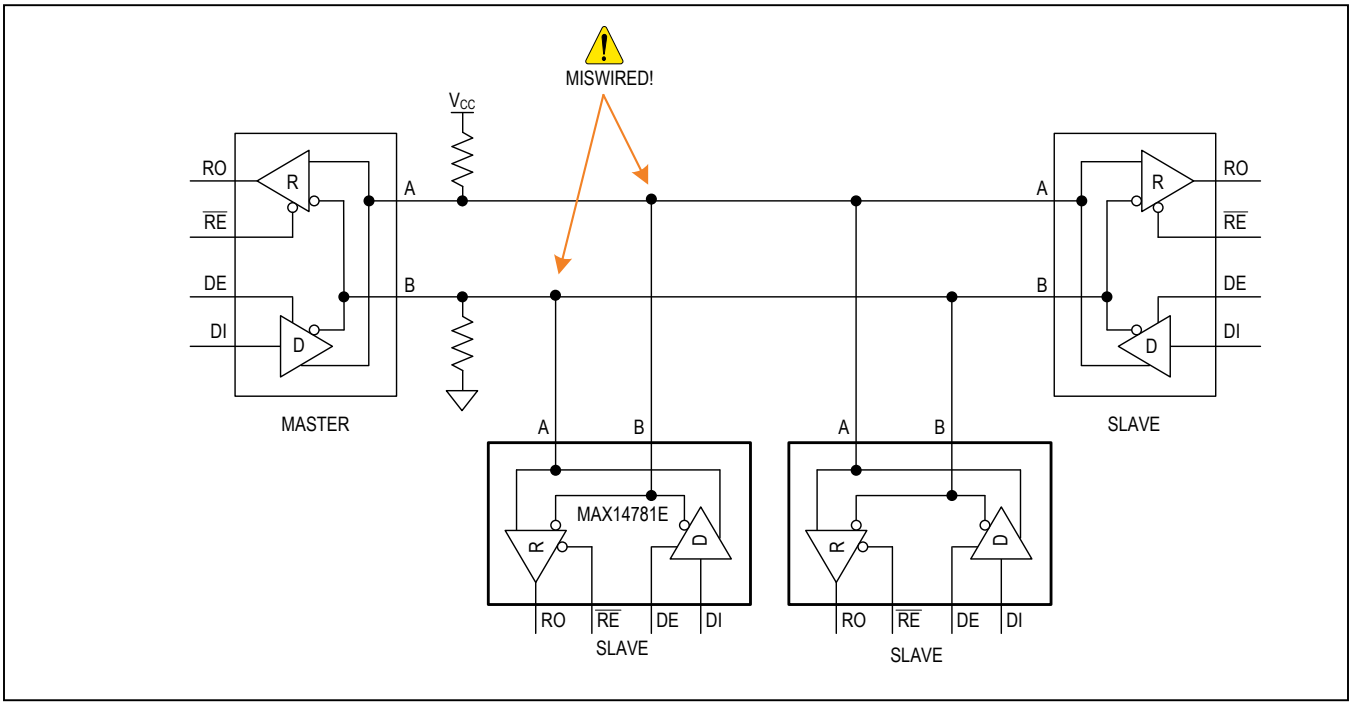


Figure 11. Passive Polarity Definition

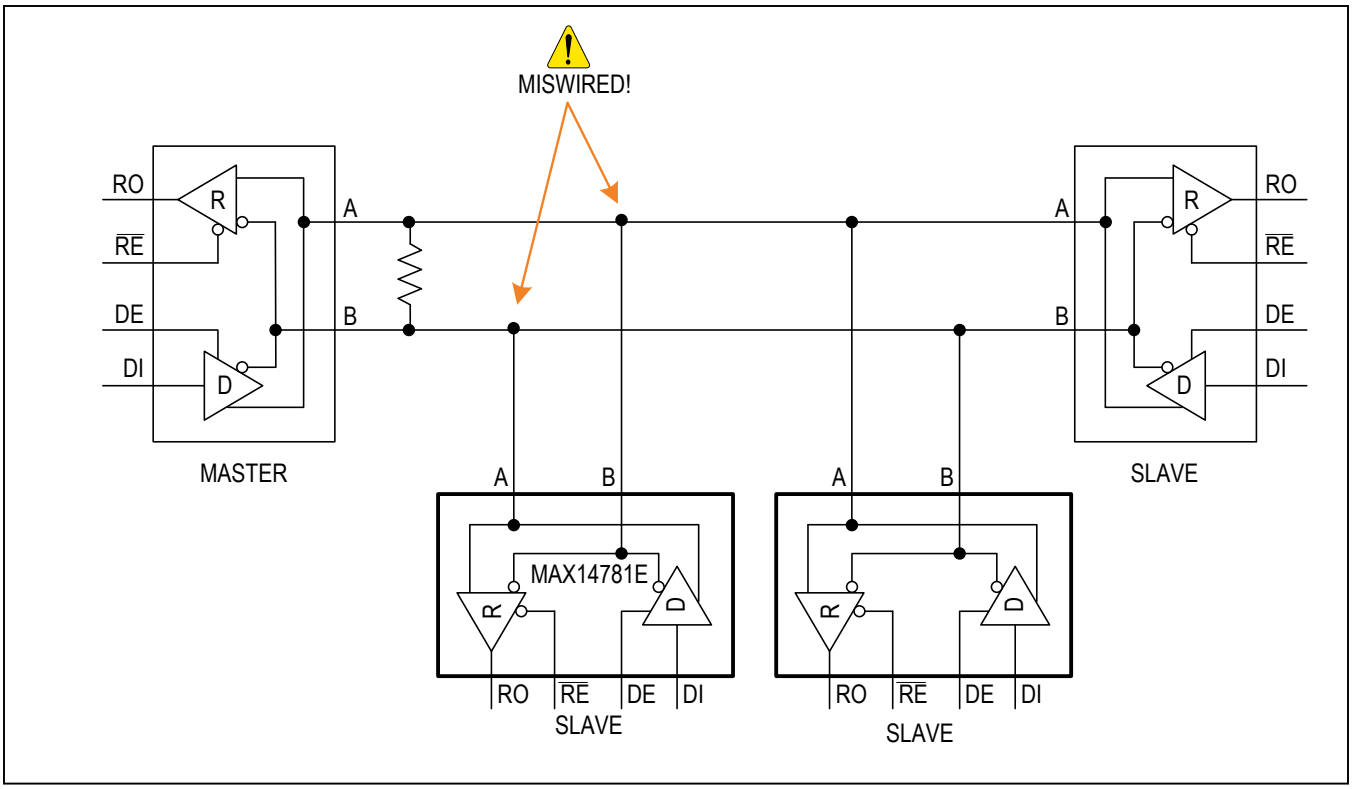


Figure 12. Differential Termination with Active Polarity Definition

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14781EESA+	-40°C to +85°C	8 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+4	21-0041	90-0096

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—

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