Datasheet – MAP7154

6MHz, 800mA Buck Converter for RFPA

General Description

The MAP7154 is synchronous buck converter for 3G, 3.5G and 4G RFPA (RF Power Amplifier).
The MAP7154 can operate at 6MHz switching frequency and has 2.7V to 5.5V input voltage range, 800mA output current capability.
The MAP7154 has three output modes. In Seep mode, output regulation is not required and MAP7154 may be entering in Sleep mode by setting V_{REF} nominally to 100mV, also very low I_Q operation. In Buck mode, output voltage can be programmed from 0.4V to 3.50V in proportion to V_{REF} input voltage ranged from 0.16V to 1.40V. Output voltage is the same with input voltage in bypass mode. Bypass mode reduces the voltage drop to less than 60mV. These features enable RFPA to operate at higher power efficiency saving its output power.
The MAP7154 has the protections, input under voltage lockout, thermal shutdown and over current limit.
The MAP7154 is available in 1.32mm x 1.27mm 0.40mm pitch, 9 bumps WLCSP package

Features

- 2.7V to 5.5V input voltage range
- 0.4V to 3.50V output voltage in Buck mode
- Low drop output voltage in Bypass mode
- 800mA output current
- 6MHz switching frequency
- Up to efficiency : 96%
- Soft-Start : 50us
- Quiescent current in sleep mode :Typ.70uA
- Shutdown current : Typ. 1uA
- 100% max duty
- Fast load transient
- Protections : Current limit, Thermal Shutdown
- Package : 1.32mm x 1.27mm, 0.40mm-pitch, 9 bumps, WLCSP package

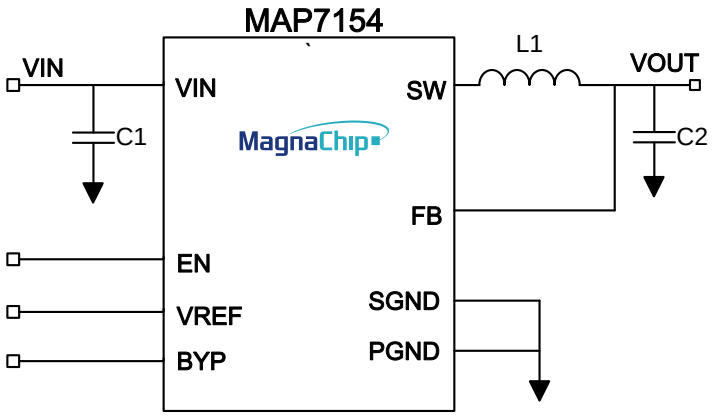
Applications

- Mobile phones
- Digital cameras
- USB devices

Ordering Information

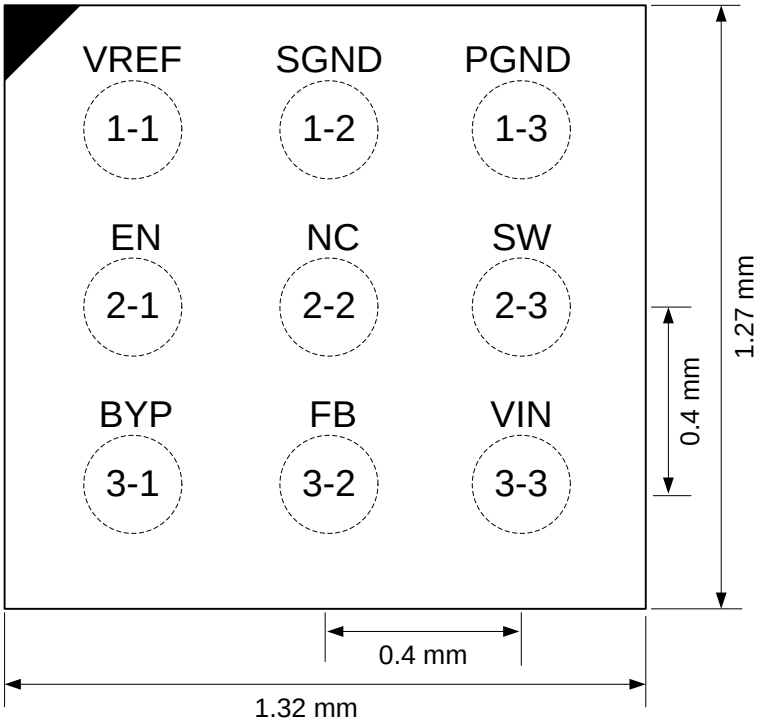
Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP7154WCRH	54LLL	-40℃ to +85℃	1.32mmX1.27mm, 0.40mm pitch, 9 bumps WLCSP	Halogen Free

Typical Application



Pin Configuration

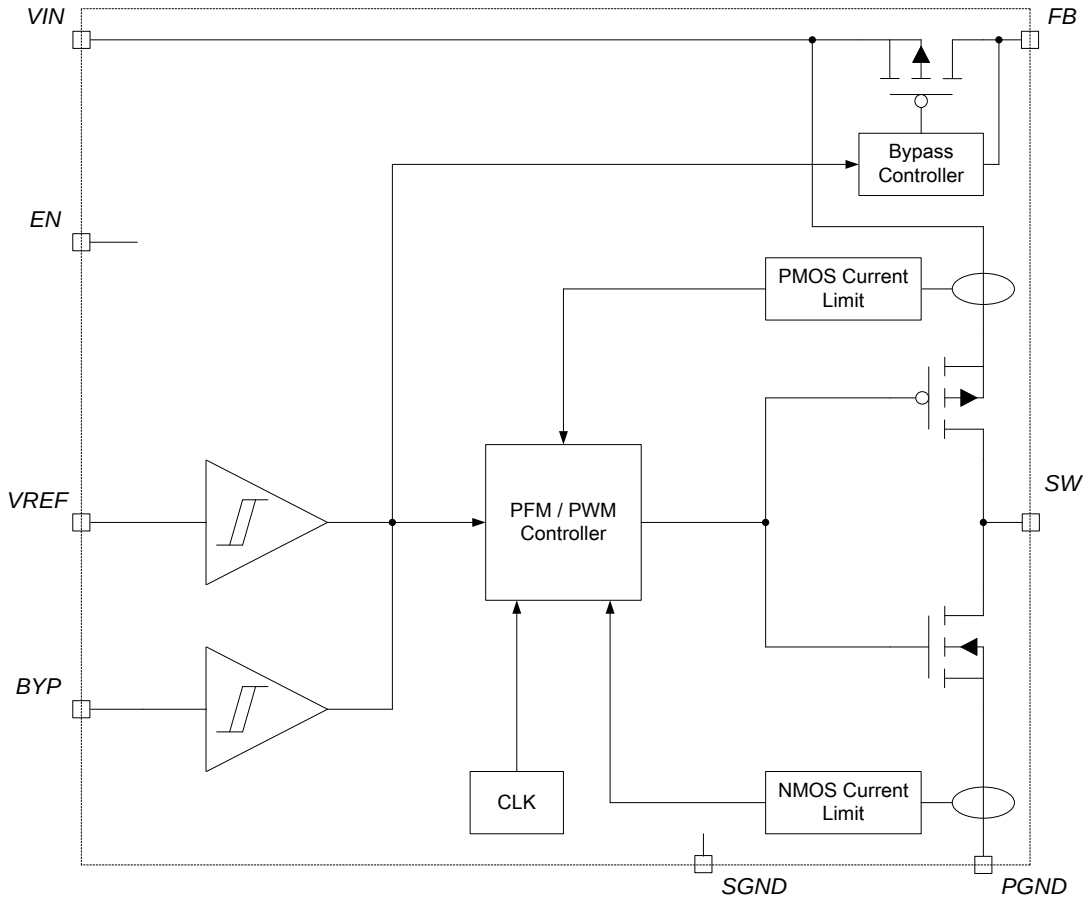
Top View



Pin Description

1.32mmX1.27mm 9 bumps WLCSP	**Name**	**Description**
1-1	VREF	Voltage control analog input for output voltage setting, $2.5 \times V_{REF}=V_{OUT}$
1-2	SGND	Signal ground. Reference ground for the IC
1-3	PGND	Power ground. Power ground of the internal Power MOSFET switches.
2-1	EN	Enable, Normal operation when EN High, Shut down when EN Low. This pin must not be left floating.
2-2	NC	
2-3	SW	Switch node. Connect to external inductor.
3-1	BYP	When BYP is high, MAP7154 enters into the forced Bypass mode. When BYP is low, MAP7154 enter into the auto Bypass mode. This pin must not be left floating.
3-2	FB	Output voltage feedback sense
3-3	VIN	IC supply input.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VIN}	Supply Voltage on VIN pin	-0.3	6	V
V_{SW}, V_{EN}, V_{FB}, V_{VREF}, V_{BYP}	SW, EN, FB, VREF, BYP Pin Voltage to GND	-0.3	V_{IN} + 0.3	V
T_{PAD}	Soldering Lead / Pad Temperature, 10sec		+260	°C
T_J	Junction Temperature	-40	+125	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{VIN}	Supply Input Voltage	2.7	5.5	V
$I_{OUT\_Buck\ Mode}$	Output current in Buck Mode	0	0.8	A
$I_{OUT\_Bypass\ Mode}$	Output current in Bypass Mode	0	2.4	A
V_{OUT}	Output voltage	0.4	≤Vin	V
T_A	Ambient Temperature (Note 2)	-40	+85	°C
T_J	Junction Temperature	-40	+125	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Electrical Characteristics

V_{IN} = 3.7V, I_{OUT}=200mA, C_{IN} = 4.7µF, EN=V_{IN}, T_A=-40℃ to 85℃, unless otherwise noted. Typical values are at T_A=+25℃

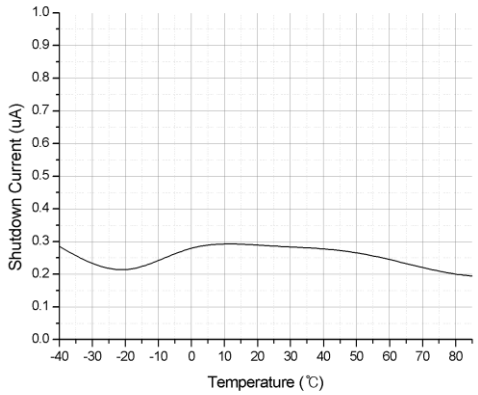
Parameter		Test Condition	Min	Typ.	Max	Unit
General Input Output Specifications						
V_{VIN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	I_{OUT} = 0mA, Sleep Mode		70		uA
$I_{SHUTDOWN}$	Shutdown Current	EN = Low		1	3	uA
V_{EN}	Logic Input Level on EN pin	V_{EN_L} : Logic Low			0.5	V
		V_{EN_H} : Logic High	1.2			
I_{EN}	Enable Input Current	EN=VIN or GND			1.0	uA
V_{UVLO}	V_{IN} Rising	Input High Threshold		2.3	2.6	V
	Vin hysteresis			200		mV
Oscillator						
F_{SW}	Internal Oscillator Frequency		5.7	6.0	6.3	MHz
D_{MAX}	Maximum Duty Cycle (1)				100	%
Output Regulation						
V_{OUT_ACC}	V_{OUT} Accuracy (2)	Ideal = 2.5 x V_{REF} (0.16V ≤ V_{REF} ≤ 1.4V)	-3		+3	%
			-50		+50	mV
V_{LINE_REG}	Line Regulation (1)			±5		mV
V_{LOAD_REG}	Load Regulation (1)			±25		mV
$V_{VREF\_SL\_IN}$	V_{REF} Sleep Mode Enter	V_{REF} voltage that force MAP7154 into Sleep mode	50			mV
$V_{VREF\_SL\_OUT}$	V_{REF} Sleep Mode Exit	V_{REF} voltage that exit MAP7154 from Sleep mode			135	mV
$V_{VREF\_BYP\_IN}$	V_{REF} Bypass Mode Enter	V_{REF} voltage that force MAP7154 into Bypass mode	1.6			V
$V_{VREF\_BYP\_OUT}$	V_{REF} Bypass Mode Exit	V_{REF} voltage that exit MAP7154 from Bypass mode			1.4	V
$V_{VREF\_TH\_IN}$	Threshold voltage to enter Bypass Mode	V_{IN} - V_{OUT}	140	200	260	mV
$V_{VREF\_TH\_OUT}$	Threshold voltage to exit Bypass Mode	V_{IN} - V_{OUT}	265	380	495	mV
T_{SL_IN}	Sleep mode enter time (1)	V_{REF} < 50mV		40		us
T_{SL_OUT}	Sleep mode exit time (1)	V_{REF} > 135mV		11		us
T_{BUCK_TR}	Output voltage step response rise time (1)	V_{IN} = 3.7V, V_{OUT} from 5% to 95% (V_{OUT} =1.4V ~ 3.4V), Rout=7Ω			10	us
T_{BUCK_TF}	Output voltage step response fall time (1)	V_{IN} = 3.7V, V_{OUT} from 5% to 95% (V_{OUT} =3.4V ~ 1.4V), Rout=7Ω			10	us
Internal Switches						
$R_{DS(ON)\_H}$	High-side Switch On Resistance –PMOS (1)	V_{IN} = V_{GS} =3.7V		0.23		Ω
$R_{DS(ON)\_L}$	Low-side Switch On Resistance – NMOS (1)	V_{IN} = V_{GS} =3.7V		0.15		Ω
$R_{DS(ON)\_BYP}$	Bypass FET Resistance (1)	V_{IN} = V_{GS} =3.7V		0.21		Ω
Protection						
T_{SD}	Thermal Shutdown Temperature	Shutdown Temperature		150		°C
		Hysteresis, ΔT_{SD}		25		
T_{SS}	Soft-Start time (1)	EN=Low to High; V_{IN} =4.2V, V_{OUT} =3.4V , C_{OUT} =4.7uF			50	us

Note 1: Guaranteed by design; not test in production.
Note 2: Test condition: Open Loop test (only internal test setup), Linearity limits are ±3% or 50mV, whichever is larger.

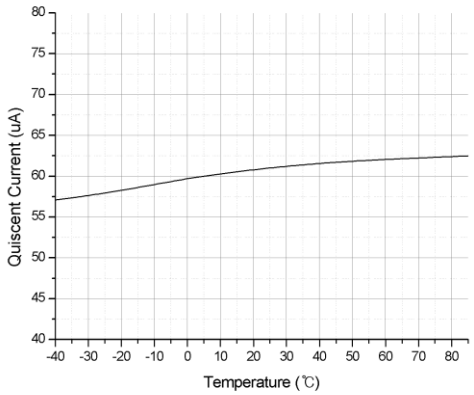
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7V, L1 = 0.47uH, C_{OUT} = 4.7uF, and T_A = 25°C.

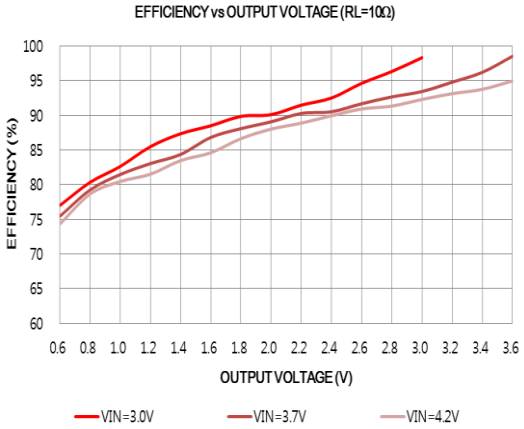
Shutdown Current vs Temperature



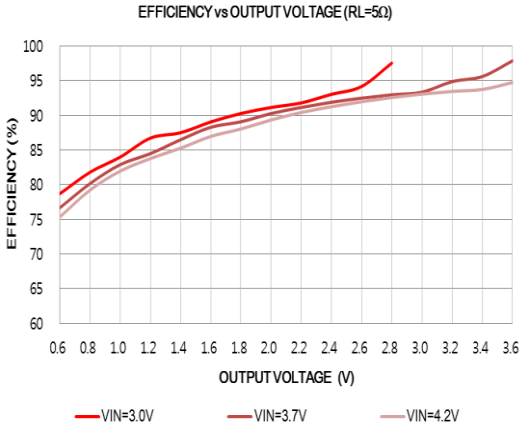
Quiescent Current vs Temperature



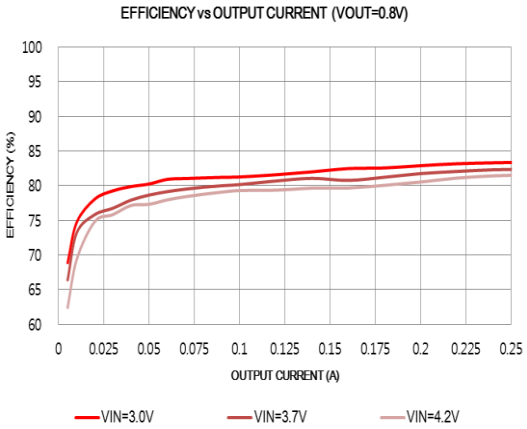
Efficiency vs Output Voltage vs Input Voltage, R_{PA}=10Ω



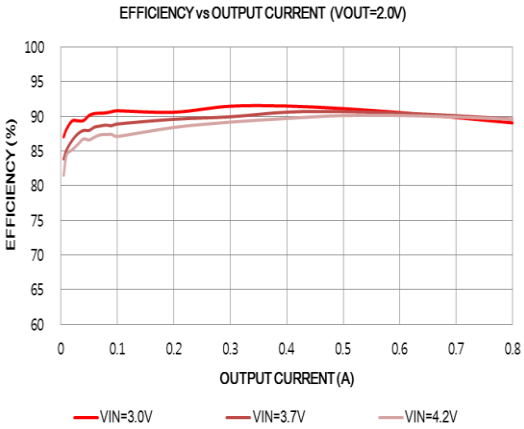
Efficiency vs Output Voltage vs Input Voltage, R_{PA}=5Ω



Efficiency vs Output Current vs Input Voltage



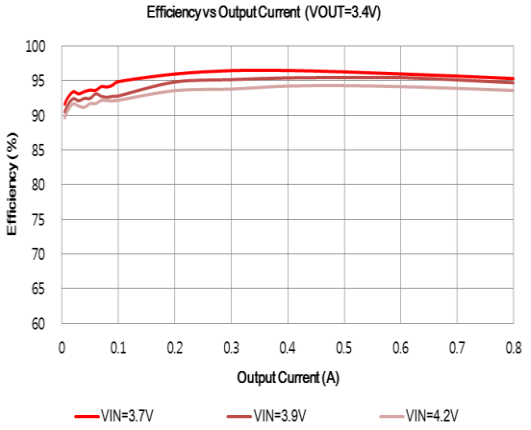
Efficiency vs Output Current vs Input Voltage



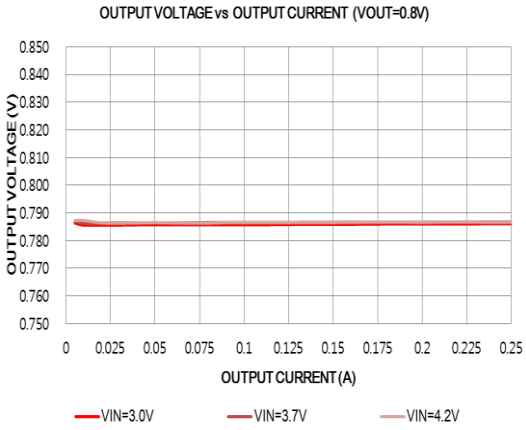
Typical Operating Characteristics - Continued

Unless otherwise noted, V_{IN} = EN = 3.7V, L1 = 0.47uH, C_{OUT} = 4.7uF and T_A = 25°C.

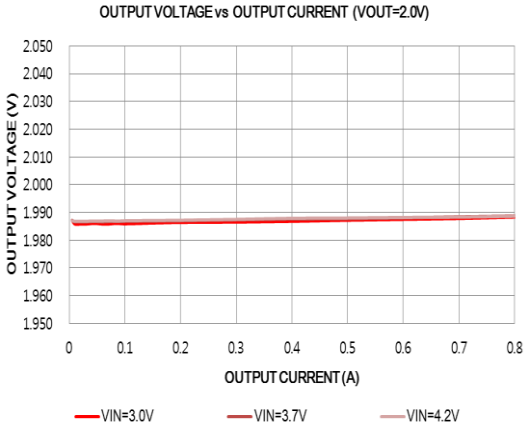
Efficiency vs Output Current vs Input Voltage



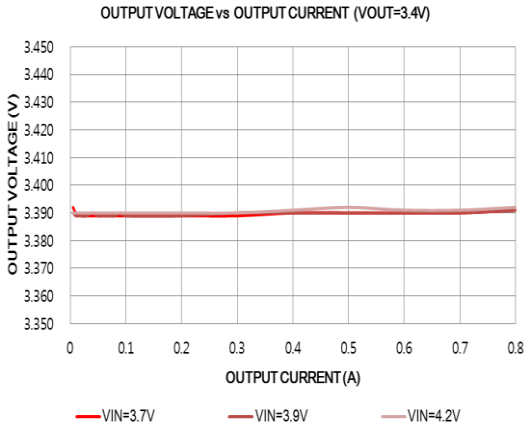
Load Regulation vs Output Current vs Input Voltage



Load Regulation vs Output Current vs Input Voltage

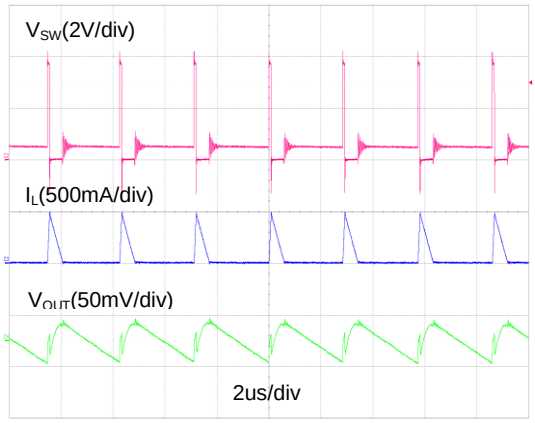


Load Regulation vs Output Current vs Input Voltage



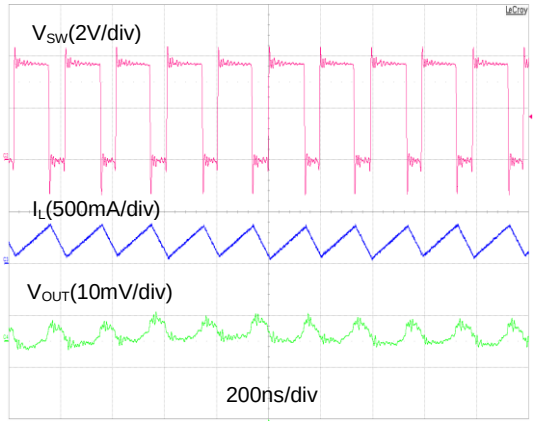
Output Voltage Ripple and Switching Waveform

V_{OUT}=0.5V, R_{AP}=10Ω



Output Voltage Ripple and Switching Waveform

V_{OUT}=2.5V, R_{AP}=10Ω

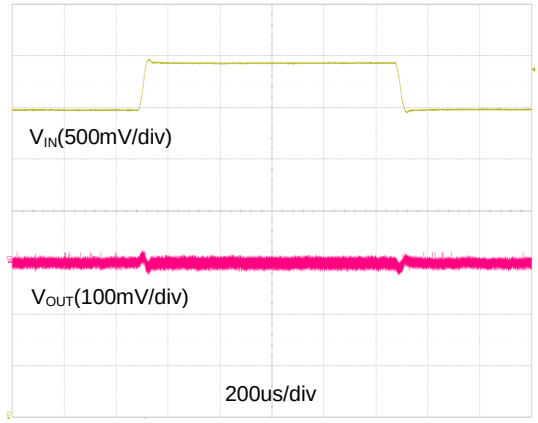


Typical Operating Characteristics - Continued

Unless otherwise noted, V_{IN} = EN = 3.7V, L1 = 0.47uH, C_{OUT} = 4.7uF and T_A = 25°C.

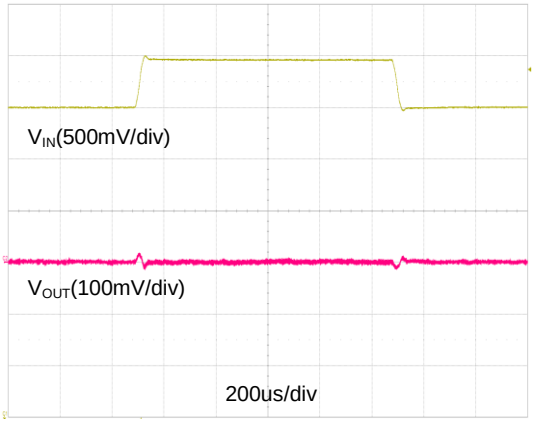
Line Transient Response

V_{IN}=3.6V to 4.2V, V_{OUT}=1.0V, R_{AP}=10Ω



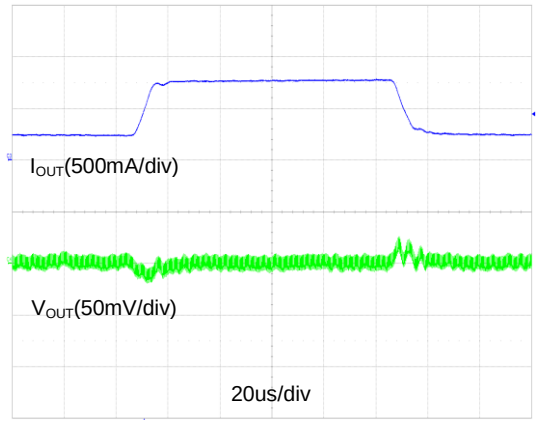
Line Transient Response

V_{IN}=3.6V to 4.2V, V_{OUT}=2.5V, R_{AP}=10Ω



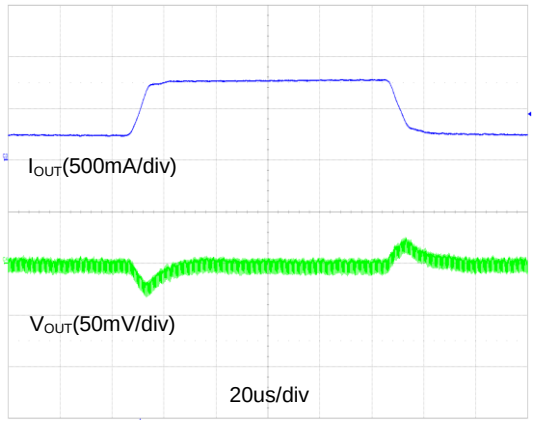
Load Transient Response

V_{OUT}=1.0V, I_{OUT}=200mA to 800mA



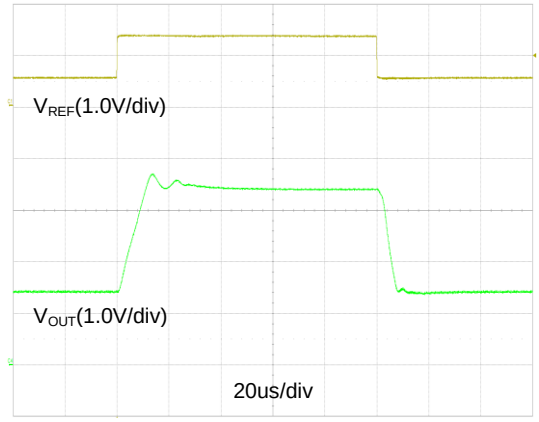
Load Transient Response

V_{OUT}=2.5V, I_{OUT}=200mA to 800mA



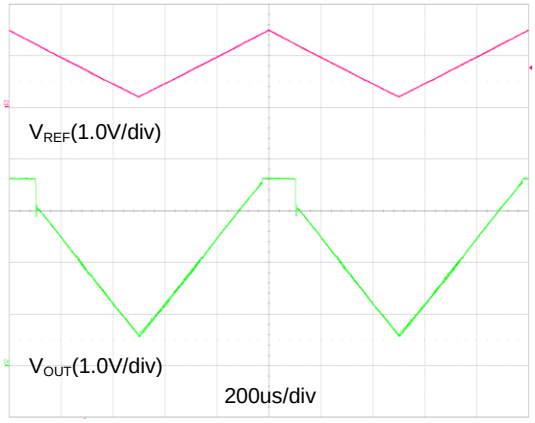
Output Voltage Transient Response

V_{OUT}=1.4V to 3.4V (ΔV_{OUT}=2.0V), R_{AP}=10Ω



Output Voltage Transient and BYP Response

V_{REF}=0.2V to 1.5V (ΔV_{REF}=1.3V), R_{AP}=10Ω



Operation Description

Device Information

The MAP7154 is a simple, a high efficiency synchronous step-down DC-DC converter optimized for powering RF power amplifiers (PA) with a single Li-Ion battery. It adjusts the output voltage by an external DAC. Regulated Vout is set to 2.5×Vref.

The DC-DC operates in PWM mode or PFM mode, depending on the output voltage and load current. Bypass mode is supported where the output voltage is shorted to the input voltage via a low on-state resistance bypass FET.

The MAP7154 supports a wide range of load currents. High-current applications up to a DC output of 800mA, mandated by enabling the DC-DC to run at either a 6MHz switching rate.

Sleep mode

The MAP7154 offers a sleep mode to minimize current, while also enabling a rapid return to regulation. Sleep mode is entered when Vref is held below 50mV for at least 40us. In this mode, current consumption is reduced to under 70uA. Sleep mode is exited after approximately 11us when Vref is set above 135mV.

PFM (Pulse Frequency Modulation) Mode

The MAP7154 automatically transitions to from PWM into PFM operation. At low output voltages and light load currents, typically less than 100mA; the DC-DC operates in a constant on-time mode. In the on-state, the P-MOS switch is turned on during a well-defined on time before switching to the off state, whereby the N-MOS switch is turned on and the inductor current is decreased to 0A. The switcher output is put into high-resistance state until the new regulation cycle starts.

PFM mode realizes high efficiency while maintaining RF power amplifiers system performance down to low load currents.

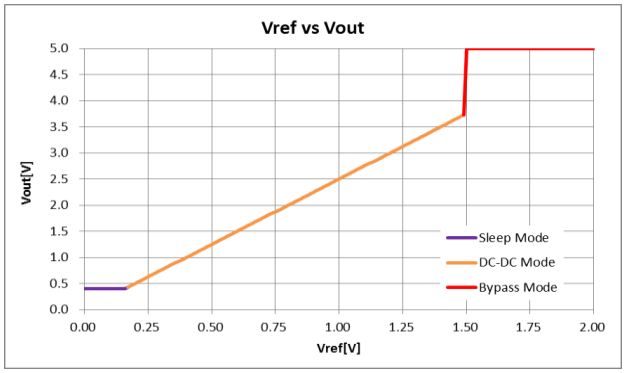
PWM (Pulse Width Modulation) Mode

The MAP7154 operation in PWM mode, regulation starts with an on state where a P-MOS switch is turn on and inductor current is ramped up until the off state begins. In the off state, the P MOS switch is off and a N-MOS switch is turned on. The inductor current decreases to maintain an average value equal to the DC output load current.

The inductor current is continuously monitored. A current sense flags when the P-MOS switch current exceeds the current limit and the switcher is turned off to decrease the inductor current sense flags when the N-MOS switch current exceeds the current limit and redirects discharging current through the inductor back to the battery.

The output voltage of the DC-DC is determined by Vref, provided by an external DAC or voltage reference

$$2.5 \times V_{REF} = V_{OUT} \quad (1)$$



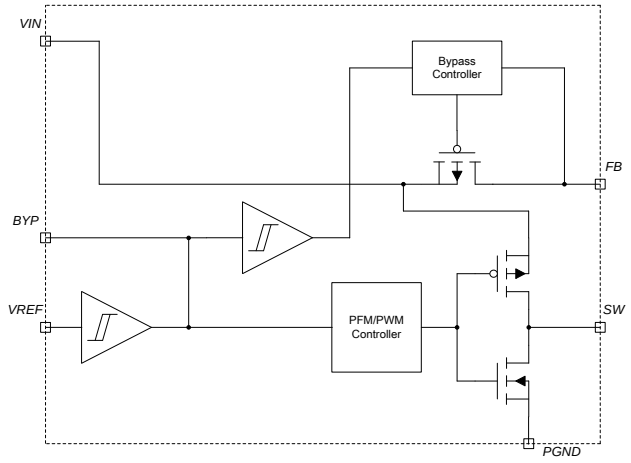
The DC-DC is able to provide a regulated Vout

Bypass Mode

The MAP7154 operates at 100% duty cycle with the bypass P-MOS switch turned on. This enables a very low voltage dropout with up to 2.4A DC output load current. In applications with 3G, 3.5G and 4G Pas, the Bypass mode typically handles 800mA.

The trigger to enter bypass mode is based on the voltage difference between the battery voltage and the internally generated reference voltage, reference voltage, as depiction in below Figure. The DC-DC enters bypass mode when Vin=Vout+200mV. It then turns into 100% duty cycle and the low Rds(on) bypass P-MOS switch is turn on with switching P-MOS switcher. So In the bypass mode, enables a very low voltage dropout (=60mV) with up to 2.4A. As Vout approaches Vin the DC-DC operates in a constant off time mode, the frequency is decreased to achieve a high duty cycle and the system continues to run in a regulated mode until the bypass condition is satisfied.

As noted above, bypass mode is also entered when Vref exceeds 1.5V.



The bypass P-MOS switch is turned on progressively using a slew rate controller to limit the inrush current. The inrush current is expressed as a function of the specified slew rate as follow;

$$I_{INRUSH} \approx C_{OUT} \frac{\Delta V_{OUT}}{\Delta t} = C_{OUT} \times V_{BP\_SLEW} \quad (2)$$

The slew rate controller is not used when releasing the bypass mode.

Dynamic Adjustment Output Voltage

The output of the MAP7154 can be dynamically adjusted by changing the voltage on the Vref pin.

The MAP7154 realizes less than 10us transition times with a large output capacitor and output voltage ranges.

ΔVout Positive Step and ΔVout Negative Step after a Vref positive step and Vref negative step, the DC-DC enters a current limit mode, where Vout ramps with a constant slew rate dictated by the output capacitor and the current limit.

The Vout dynamic to or from bypass mode requires the bypass conditions be met. The MAP7154 performs detection of the bypass conditions after Vref dynamic and enables the required charging or discharging circuit to realize a transition time of 10us.

Vout dynamic at start up, after EN rising edge is detected, the system requires 50us to enable all internal voltage references and amplifiers before enabling the DC-DC function.

Vout dynamic after Bypass EN, when BYP enters high, the controller dismisses the internal bypass flags and sensors and enables BYP. However, the dynamic is managed with the same current limit

Thermal Protection

If the junction temperature exceeds the maximum specified junction temperature, the MAP7154 enters Power Down Mode (Except the thermal detection circuit).

Table 1. Mode Operation Descriptions

NO	Mode	Operation Description	Conditions	
			BYP	EN
1	Shutdown Mode	IC is disabled	X	X
2	Sleep Mode	IC is disabled	X	H
3	DCDC Mode	IC is enable	X	H
4	Bypass Mode	Bypass FET is forced ON, DCDC is set to 100% Duty Cycle	H	H

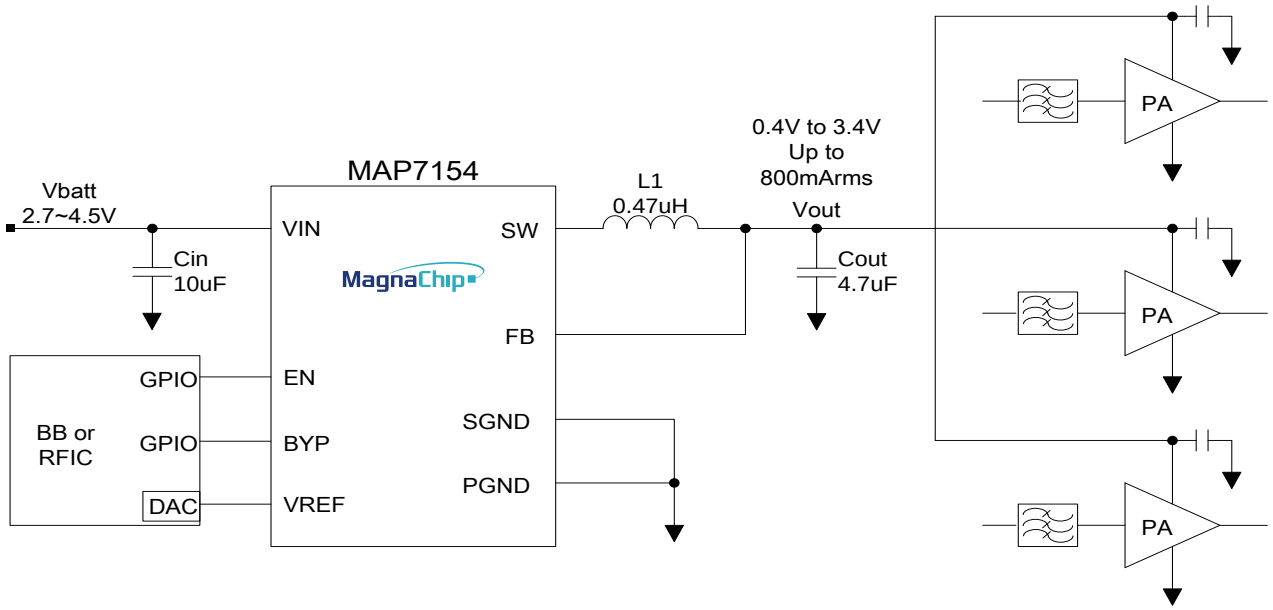
When Vout exceeds Vin-200mV, the bypass P-MOS is enabled and the DC-DC operate by 100% duty cycle. When Vout$\leq$Vin-380mV, the bypass P-MOS is disabled and the DC-DC operates by Auto Mode.

Application Information

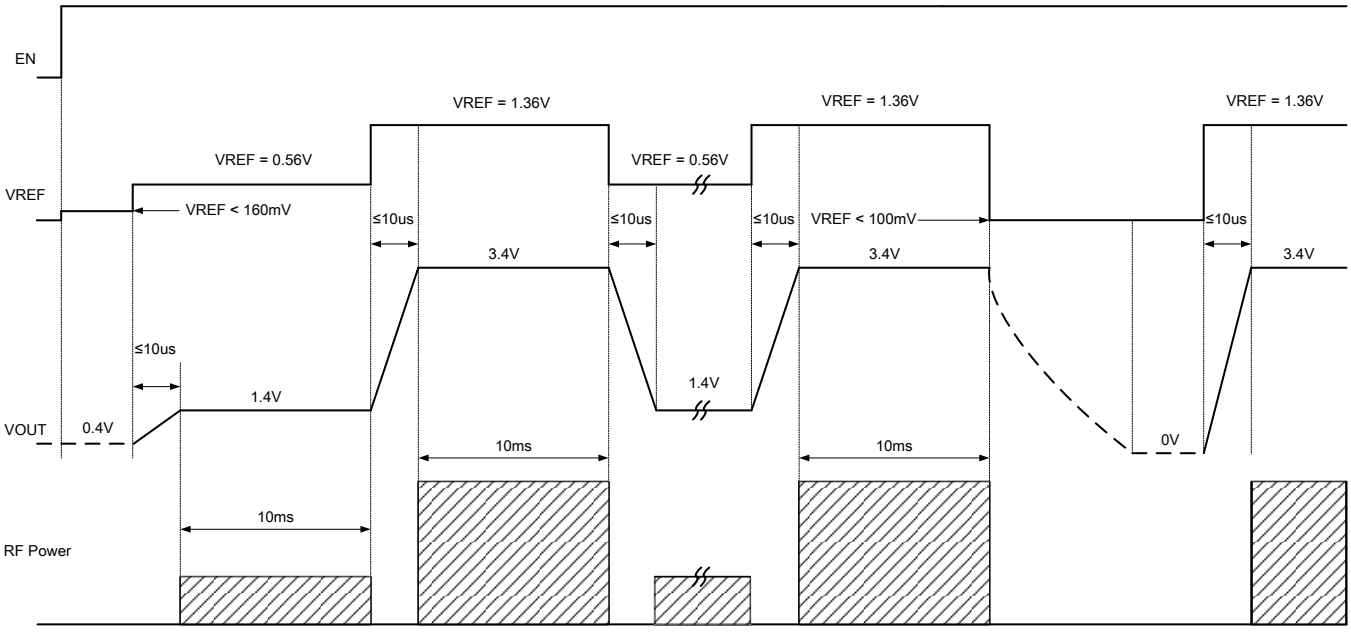
The below Figure illustrates an application of the MAP7154 in 3G, 3.5G, 4G transmitter. The MAP7154 is designed for driving multiple Pas.

DAC (VREF) Control

An analog voltage to the VREF pin can dynamically program the output voltage from 0.4V to 3.5V in both PFM and PWM modes of operation, without the need for external resistors. The output voltage is governed by $V_{OUT} = V_{REF} * 2.5$ (V_{REF} = 0.16V to 1.4V)



[Typical Application Diagram Supplying 3G, 3.5G, 4G Pas]



[Dynamic Timing Adjustment of Output Voltage and 3G ~ 4G Transmitters]

Inductor Selection
The MAP7154 is operating at 6MHz switching frequency, which allows for the use of a 0.47uH inductor.

Table 2. Recommended Inductors

Inductor	Fsw	Description
L1	6MHz	0.47uH, ± 20%,3.1A 2520 TOKO:DFE252010C
		0.47uH, ± 20%,3.1A 2520 Murata:LQM2HPNR47MG0

Capacitor Selection
The minimum required output capacitor Cout is 4.7uF, 6.3V, X5R with an ESR of 10mΩ or lower and an ESL of 0.3nH or lower. Larger case sizes result in increased loop parasitic inductance and higher noise.

Table3. Recommended Capacitors

Capacitor	Description
CVin	10uF, ± 20%, X5R, 10V
CVout	4.7uF, ± 20%, X5R, 6.3V
CVref	470pF, ± 20%, X5R

Vref Filter
Vref is the analog control pin of the DC-DC and should be connected to an external Digital to Analog Converter (DAC). It is recommended to place up to 470pF decoupling capacitance between Vref and AGND to filter the DAC from the DC-DC high frequency switching noise coupled through the Vref pin.

Any noise on the Vref input is transferred to Vout with a gain of two and a half(2.5). If the DAC output is noisy, a series resistor may be inserted the DAC output and the capacitor to form an RC filter.

Follow these guidelines:

- ✓ Use a low noise source or a driver with good PSRR to generate Vref.
- ✓ The Vref driver must be referenced to AGND.
- ✓ Vcon routing must be protected against VIN, SW, PGND signals, and other noisy signals. Use AGND shielding for better isolation.
- ✓ Be sure the DAC output can drive the 470pF capacitor on Vref. It may be necessary to insert a low value resistor to ensure DAC stability without slowing Vref fast transition times.

No Floating Inputs
The MAP7154 does not have internal pull down resistors on its inputs. Therefore, unused inputs should not be left floating and should be pulled High or Low.

PCB Layout and Component Placement

- ✓ Make the power ground PGND connection shared between U1, C1 and C2 compact. This minimizes the parasitic inductance of the switching loop paths.
- ✓ Place PGND on the top layer and connect it to the AGND ground plane next to Cout using several vias.
- ✓ Ensure that the routing loop, VIN PGND VOUT is the very shortest possible.
- ✓ Place the inductor away from the feedback pins to prevent unpredictable loop behavior.
- ✓ Use the application circuit layout from the datasheet whenever possible. Its performance has been verified.
- ✓ VIN and PGND must rout with the widest and shortest traces possible. It is acceptable for the traces connecting the inductor to be long rather than having long VIN or PGND traces. The SW node is a source of electrical switching noise. Do not route it near sensitive analog signals.
- ✓ Two small vias are used to connect the SW node to the inductor L1. Use solders filled vias if available.
- ✓ The connection from Cout to FB should be wide to minimize the Bypass mode voltage drop and the series inductance. Even if the current in Bypass Mode is small, keep this trace short and at least 5mm wide.

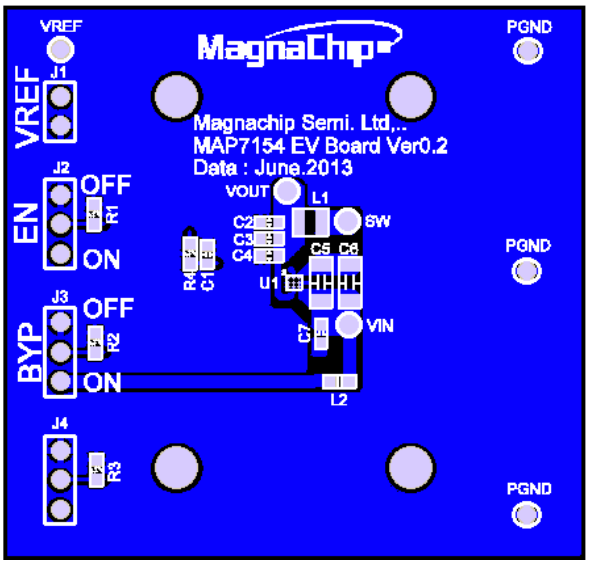
- ✓ The ground plane should be not be broken into pieces. Ground currents must have a direct, wide path from input to output.
- ✓ Each capacitor should have at least two dedicated ground vias. Place vias within 0.1mm of the capacitors.
- ✓ Ensure the traces are wide enough to handle the maximum current value, especially in Bypass Mode.
- ✓ Ensure the vias are able to handle the current density. Use metal filled vias if available.

Assembly

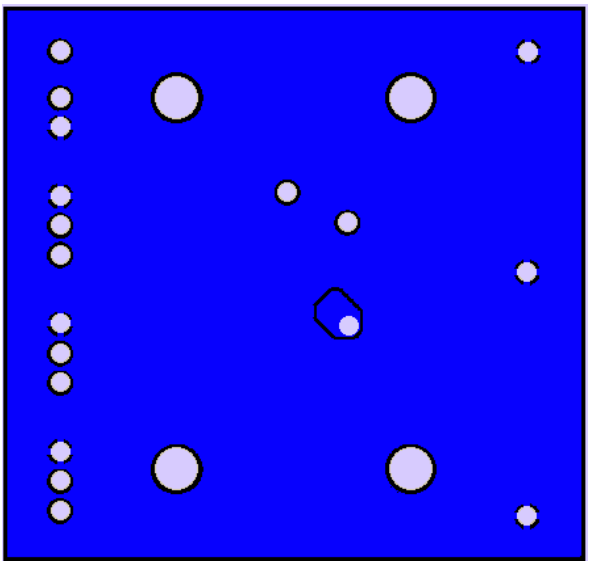
- ✓ Use metal-filled or solder-filled vias if available.
- ✓ Poor soldering can cause low DC-DC conversion efficiency. If the efficiency is low, X-ray the solder connections to verify their integrity.

PCB Layout Example

[PCB Top Side]

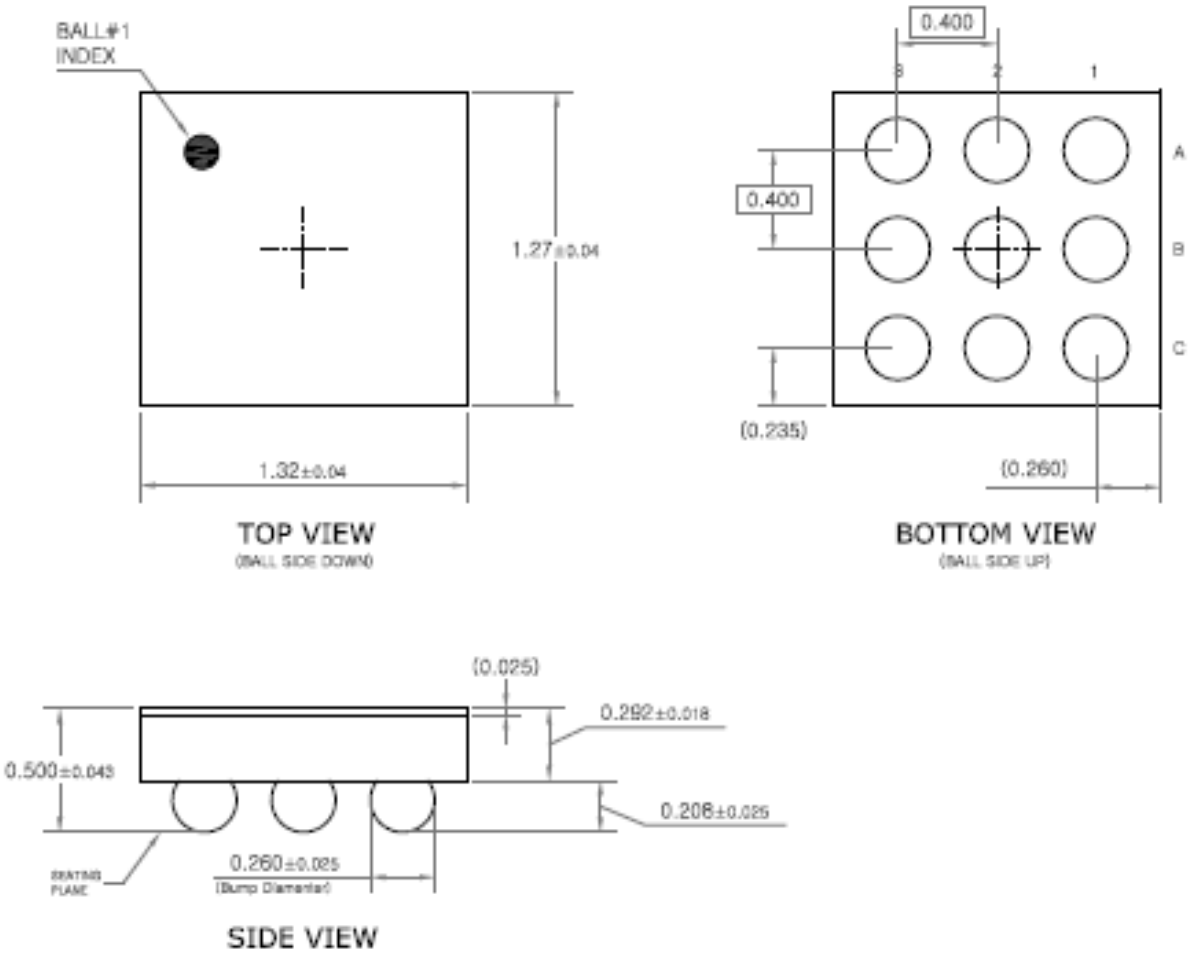


[PCB Bottom Side]



Physical Dimensions

- **1.32mmX1.27mm, 0.40mm pitch, 9 bumps WLCSP**



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