

1 FEATURES

MERUS™ multilevel switching technology

- 5-level voltage modulation for ultra-low idle power consumption: 155 mW @ 24 PVDD without the need of complex dynamic rail-tracking systems
- Inductor-less application for reduced system cost without output power limitations
- Reduced EMI emissions compared to traditional 2 and 3 level class D audio amplifiers for fast time to market without compromises in audio performance or efficiency
- High efficiency at low output power: 80 %, 2×1.5 W, 8 Ω for extended battery life and easy thermal management in multichannel products even in idle state

Flexible configuration and application

- BTL rated output: 2×63 W, 24 V, 4 Ω, 10% THD
- PBTL rated output: 1×125 W, 24 V, 2 Ω, 10% THD
- PVDD voltage range (audio playback): 13.5 V to 26 V
- PVDD voltage range (communication): 6.65 V to 26 V
- High efficiency at low output power: 80 %, 2×1.5 W, 8 Ω
- Short circuit protection: 8 A peak (BTL) / 16 A peak (PBTL)
- External closed-loop feedback for improved THD
- Integrated DSP with configurable biquads, limiters, volume control and more
- Easy configuration over I2C-bus with up to 64 devices
- 8-bit auxiliary ADC for internal temp. / PVDD monitoring or sampling from external sources
- Configurable switching edge steepness and inter-chip PWM sync for multi-device systems
- No external heatsink required

Audio performance

- Output noise: 64 µVrms (A-weighted)
- Dynamic range: 106 dB (A-weighted)
- THD+N: 0.045%, 1 W, 1 kHz

Audio I/O

- 3-wire digital audio interface (no MCLK required)
- 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz sample rates
- I2S and TDM formats supported
- Low input-to-output latency for echo cancellation
- Post-DSP I2S output for chaining / echo cancellation

2 TARGET APPLICATIONS

- Battery powered speakers
- Bluetooth/wireless/smart speakers and soundbars
- Conference speakers
- Multichannel/multi-room audio systems

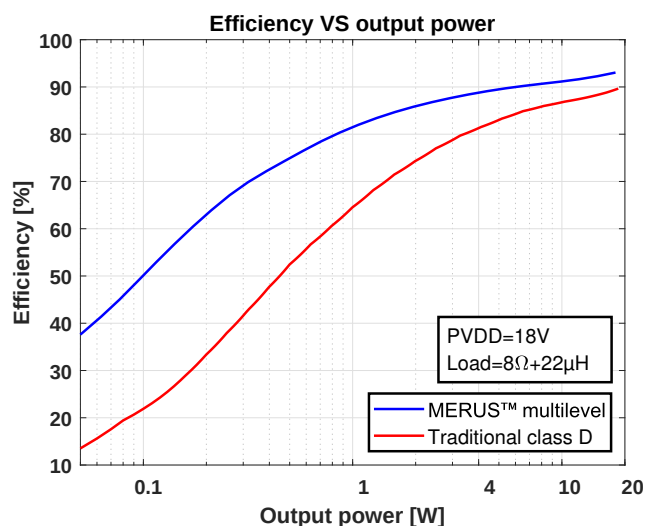
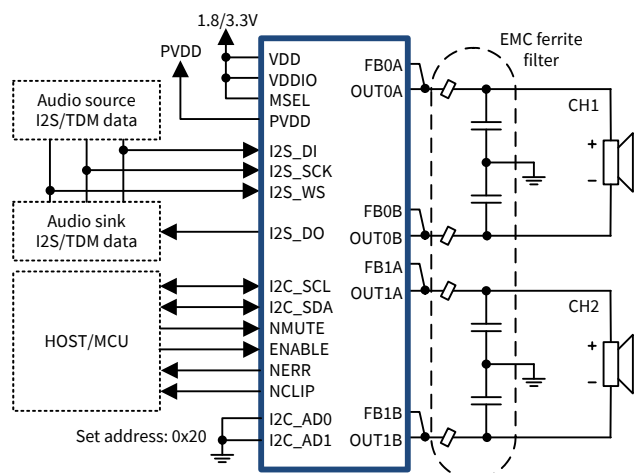
3 DESCRIPTION

The MA2306DNS is a 2×63 W audio amplifier with integrated audio DSP and I2S/TDM audio interface. It features the MERUS™ multilevel switching amplifier technology enabling unmatched power efficiency at both low and high output power. Multilevel switching also relaxes EMI and enables inductor-less applications with lower cost and no compromise in audio performance or efficiency. A high order internal feedback loop ensures low THD for excellent audio performance. The integrated DSP offers a configurable processing flow and can be used to correct and tune real speaker applications with equalization, limiting and more. The ultra-low idle power consumption is at least five times lower than the traditional class D audio amplifiers, making MA2306DNS ideal for battery powered speaker applications with extended battery life and reduced battery cell cost. In mains-powered applications, the reduced and scalable EMI performance, enables otherwise impossible industrial designs, without the necessity for a heatsink or an LC filter.

4 PRODUCT VALIDATION

Qualification standard: Standard

5 TYPICAL APPLICATION



6 Functional Application Block Diagram

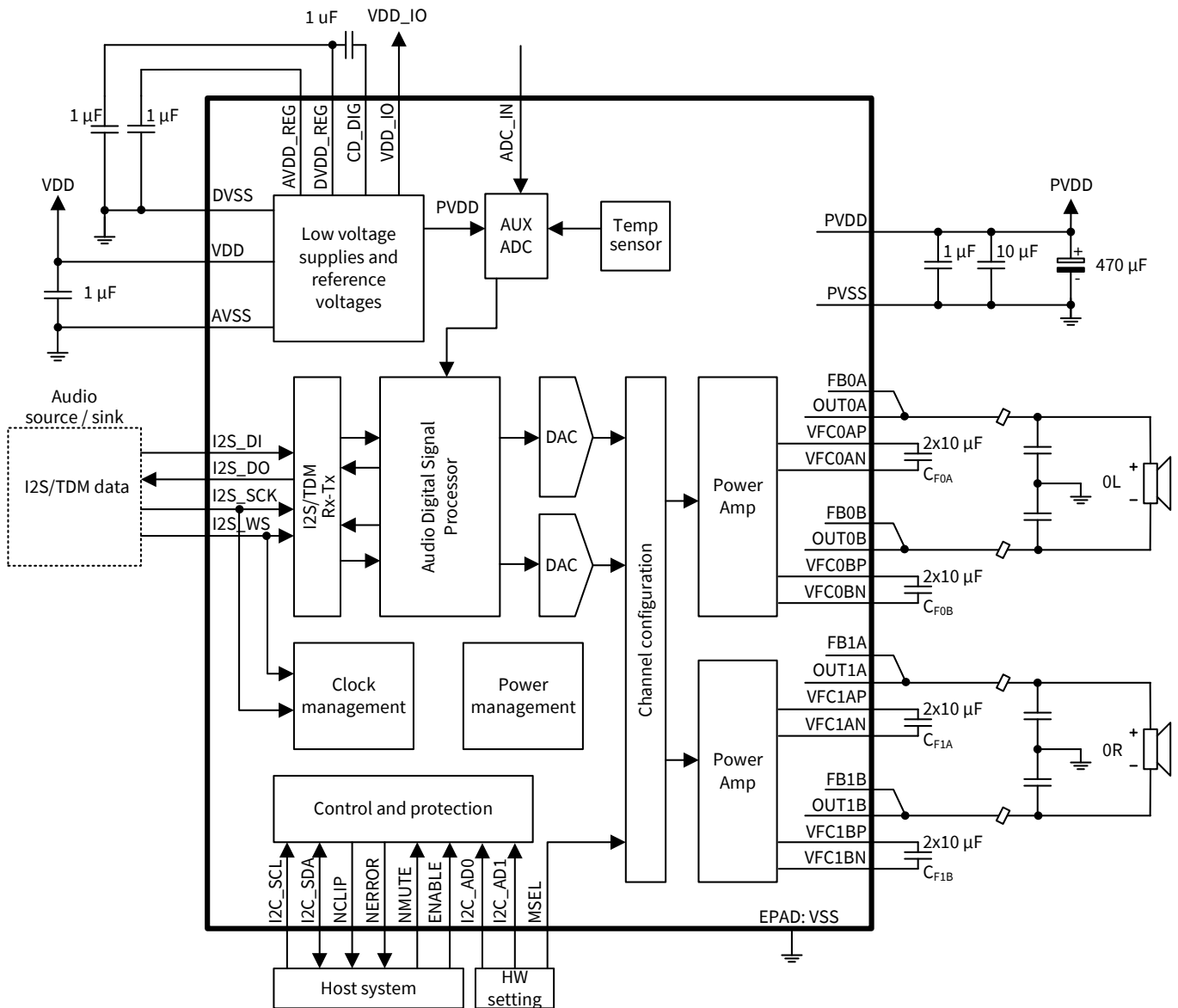


Figure 6.1: Functional Application Block Diagram

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7 Device Comparison Table

Table 1: Device comparison

Device name	Functional variance
MA2306DNS	Fully configurable dual-core DSP, 13.5-26 V
MA2306PNS	Audio limiter and volume control only, 13.5-26 V
MA2304DNS	Fully configurable single-core DSP, 10-20 V
MA2304PNS	Audio limiter and volume control only, 10-20 V

8 Pin Configuration

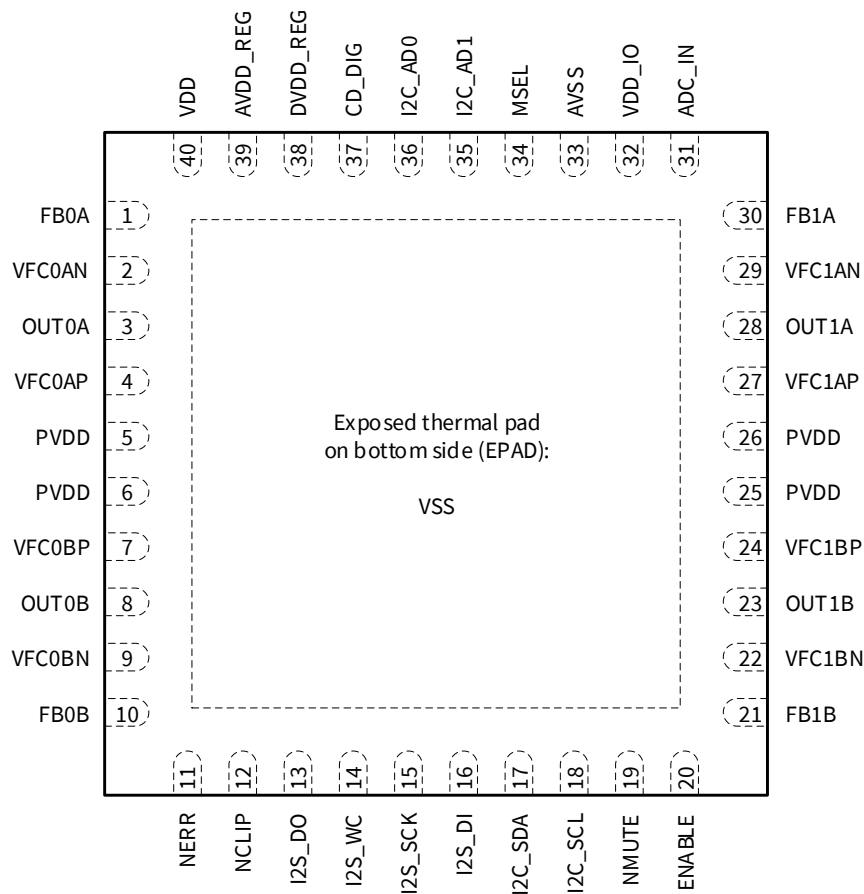


Figure 8.1: Package Overview - 6x6 mm QFN-40 pins

9 Pin List

Table 2: Pin List MA2306DNS

Pin Nr.	Name	Type	Description
1	FB0A	I	Output channel 0A post-ferrite feedback
2	VFC0AN	P	Negative side flying capacitor for channel 0A
3	OUT0A	O	Audio output channel 0A
4	VFC0AP	P	Positive side flying capacitor for channel 0A
5	PVDD	P	Power supply for power stage
6	PVDD	P	Power supply for power stage

7	VFC0BP	P	Positive side flying capacitor for channel 0B
8	OUT0B	O	Audio output channel 0B
9	VFC0BN	P	Negative side flying capacitor for channel 0B
10	FB0B	I	Output channel 0B post-ferrite feedback
11	NERR	O	Error indicator – open drain output. Use this pin as interrupt for host microcontroller to read error register.
12	NCLIP	I/O	Clipping indicator output (default) or PWM synchronization I/O
13	I2S_DO	O	I2S/TDM digital audio data output
14	I2S_WC	I	I2S/TDM digital audio word clock
15	I2S_SCK	I	I2S/TDM digital audio bit clock
16	I2S_DI	I	I2S/TDM digital audio data input
17	I2C_SDA	I/O	I2C bus serial clock
18	I2C_SCL	I/O	I2C bus serial data
19	NMUTE	I	Mutes audio output when pulled low
20	ENABLE	I	Enables device when pulled high. Pulling this pin low shuts down the device.
21	FB1B	I	Output channel 1B post-ferrite feedback
22	VFC1BN	P	Negative side flying capacitor for channel 1B
23	OUT1B	O	Audio output channel 1B
24	VFC1BP	P	Positive side flying capacitor for channel 1B
25	PVDD	P	Power supply for power stage
26	PVDD	P	Power supply for power stage
27	VFC1AP	P	Positive side flying capacitor for channel 1A
28	OUT1A	O	Audio output channel 1A
29	VFC1AN	P	Negative side flying capacitor for channel 1A
30	FB1A	I	Output channel 1a post-ferrite feedback
31	ADC_IN	I	Auxiliary ADC input
32	VDD_IO	P	Digital I/O supply. Used for external resistor pull-ups, e.g. for I2C bus.
33	AVSS	P	Ground for internal analog circuitry
34	MSEL	I	Hardware select for BTL (pull high) or PBTL (pull low)
35	I2C_AD1	I	I2C bus address pin 1. Use I2C_AD1 and I2C_AD0 to set I2C address: 00:0x20, 01:0x21, 10:0x22, 11:0x23.
36	I2C_AD0	I	I2C bus address pin 0
37	CD_DIG	P	Internal digital core supply charge-pump. Connect 1 μ F between this pin and DVDD_REG.
38	DVDD_REG	P	Internal regulated supply decoupling. Connect 1 μ F between this pin and ground.
39	AVDD_REG	P	Internal regulated supply decoupling. Connect 1 μ F between this pin and ground.
40	VDD	P	External low voltage supply.
EPAD	VSS	P	Ground for internal digital circuitry and PVDD

10 Specifications

10.1 Absolute Maximum Ratings

NOTE: Usage outside the specifications stated in this table may cause permanent damage to the device and/or compromise reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VDD	Low voltage supply	-0.3	5.5	V
PVDD	Power amp supply	-0.3	28	V
VDD_IO	Digital I/O supply	-0.3	5.5	V
V _{speak}	Speaker node output pins	-0.3	PVDD+2	V
V _{PIO}	IO and hardware setting pins (NERR, NCLIP, I2S_DO, I2S_WC, I2S_SCK, I2S_DI, I2C_SDA, I2C_SCL, NMUTE, ENABLE, MSEL, I2C_AD0, I2C_AD1)	-0.3	VDD_IO	V
V _{ADC}	ADC_IN pin	-0.3	1.5	V
T _{AMB}	Ambient operating temperature	-25.0	85	°C
T _J	Junction temperature	-25.0	150	°C
T _{STORE}	Storage temperature	-55.0	150	°C

10.2 ESD and Thermal Characteristics

Table 4: ESD and Thermal Characteristics

Parameter	Description	Min	Typ	Max	Unit
V _{ESD,HB}	ESD Human Body Model	-2500		+2500	V
V _{ESD,CD}	ESD Charged Device Model	-1000		+1000	V
T _{θJA}	Thermal resistance, Junction-to-Ambient, 4-layer PCB (EVAL_MA23xx)		14.7		°C/W
T _{θJC}	Thermal resistance, Junction-to-Case (EPAD)		1.3		°C/W

10.3 Recommended Operating Conditions

NOTE: Usage outside the recommended operating conditions stated in this table may cause the device to not behave properly. This can lead to interrupted audio playback, protection features being triggered etc. This applies to DC+AC values outside the min/max values.

Table 5: Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD	Low voltage supply (DC+AC ripple)	1.62	1.8 / 3.3	3.65	V
VDD_IO	Digital I/O supply (DC+AC ripple)	1.62	1.8 / 3.3	3.65	V
PVDD	Power amp supply (DC+AC ripple)	13.5	24	26	V
ILEQ	Minimum required equivalent load inductance per output pin for short circuit protection	0.5			μH

Refer to sections 11.5 and 11.5.4 for more details on supply voltages and their protection mechanisms.

10.4 Electrical Characteristics

Conditions (unless specified otherwise): PVDD=24 V, VDD/VDD_IO=1.8 V, Fsw-fet=256 kHz, Fsw-load=1024 kHz, T_{AMB}=25 °C, Load: 4 ohm + 22 µH, PCB: EVAL_AUD_MA2306xNS_DUO, (no input or output filter)

Table 6: Electrical characteristics.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
BTL Output Power						
P _{COUT,BTL}	Continuous Output Power p/ch (no heatsink)	Load=4Ω+22μH, Thermal Error triggered		17		W
		Load=8Ω+22μH, THD+N=1%		31		W
		Load=8Ω+22μH, THD+N=10%		39		W
P _{COUTH,BTL}	Continuous Output Power p/ch (with heatsink) ³	Load=4Ω+22μH, Thermal Error triggered		40		W
P _{RMSOUT,BTL}	RMS Output Power p/ch	Load=4Ω+22μH, THD+N=1%		50		W
		Load=4Ω+22μH, THD+N=10%		63		W
I _{OUT,BTL}	Maximum Output Current p/ch		8			A
PBTL Output Power						
P _{COUT,PBTL}	Continuous Output Power p/ch (no heatsink)	Load=2Ω+22μH, Thermal Error triggered		34		W
		Load=4Ω+22μH, THD+N=1%		50		W
		Load=4Ω+22μH, THD+N=10%		63		W
P _{COUTH,PBTL}	Continuous Output Power p/ch (with heatsink) ³	Load=2Ω+22μH, Thermal Error triggered		80		W
P _{RMSOUT,PBTL}	RMS Output Power p/ch	Load=2Ω+22μH, THD+N=1%		100		W
		Load=2Ω+22μH, THD+N=10%		125		W
I _{OUT,PBTL}	Maximum Output Current p/ch		16			A
Power stage						
η _{BTL}	Efficiency (BTL) ²	POUT=2x1.5W, Load=8Ω+22μH		80		%
		POUT=2x33W, Load=8Ω+22μH		93		%
		POUT=2x1.5W, Load=6Ω+22μH		78		%
		POUT=2x42W, Load=6Ω+22μH		91		%
		POUT=2x1.5W, Load=4Ω+22μH		74		%
		POUT=2x58W, Load=4Ω+22μH		85		%
R _{ON,BTL}	On-resistance of the internal power stage (BTL) ¹	BTL on-resistance: 2x MOSFETS in series		167		mΩ
R _{ON,PBTL}	On-resistance of the internal power stage (PBTL) ¹	PBTL on-resistance: 2x BTL power stages in parallel		84		mΩ
f _{SW,FET}	Internal MOSFET switching frequency ¹			256		kHz
f _{SW,LOAD}	Switching frequency seen differentially by the load ¹			1024		kHz
BTL Power Consumption						
P _{IDLE,BTL}	Total idle power consumption for VDD+PVDD+VDD_IO	PVDD=24V, (device enabled and unmuted)		155		mW
I _{PVDD,IDLE,BTL}	Quiescent/idle current, PVDD	PVDD=24V, (device enabled and unmuted)		6.1		mA
I _{VDD,IDLE,BTL}	Quiescent/idle current, VDD	VDD=1.8 V, (device enabled and unmuted)		4.3		mA
I _{VDD_IO,IDLE,BTL}	Quiescent/idle current, VDD_IO	VDD_IO = 1.8 V, I2S_DO unloaded		3.9		μA
ΔP _{DSP}	Power consumption difference between ROM code and max DSP program (dual-core) ¹	VDD=3.3 V		11.9		mW
		VDD=1.8 V		7.4		mW
PBTL Power Consumption						
P _{IDLE,PBTL}	Total idle power consumption for VDD+PVDD+VDD_IO	PVDD=24V, Load=2Ω+22μH, (device enabled and unmuted)		108		mW

I _{PVDD,IDLE,PBTL}	Quiescent/idle current, PVDD	PVDD=24V, (device enabled and unmuted)		4.2		mA
I _{VDD,IDLE,PBTL}	Quiescent/idle current, VDD	VDD=1.8 V, (device enabled and unmuted)		3.7		mA
Audio Performance/IO						
V _{NOISE}	Output integrated noise level	20-20kHz, A-weighted, pvdd_scale=11, PVDD = 24 V		64		μV
		20-20kHz, A-weighted, pvdd_scale=10, PVDD = 20.5 V		58		μV
DNR	Dynamic Range	-60dBFS method		106		dB
THD+N	Total Harmonic Distortion + Noise	POUT=1W, sig=1kHz, Load=4Ω+22μH		0.045		%
V _{OS}	Output offset voltage, PVDD=24 V, pvdd_scale=11		-6		6	mV
f _S	Supported I2S/TDM input sampling rates ¹			32 44.1 48 88.2 96 176.4 196		kHz
t _{PD}	Propagation delay from audio input to amplifier ¹	Sample rate = 48 kHz, DSP enabled running ROM code		146		μs
I2S_SCK _{MAX}	Maximum supported bit clock on I2S_SCK pin ¹			25		MHz
N _{CH,MAX,IN}	Maximum supported input I2S/TDM channels ¹			16		
N _{CH,MAX,OUT}	Maximum supported output I2S/TDM channels ¹			2		
G	Amplifier gain in dB (Vrms/FS) ¹	pvdd_scale=11, PVDD = 24 V		25.9		dB
		pvdd_scale=10, PVDD = 20.5 V		24.6		dB
		pvdd_scale=01, PVDD = 16 V		22.4		dB
Enable/Mute						
T _{ENABLE}	Time from ENABLE=high until ready for I2C communication ¹			15		ms
T _{UNMUTE}	Unmute time delay until audio output ¹			30		ms
I2C serial control interface						
f _{SCL}	I2C clock frequency ¹	Standard Mode		100		kHz
		Fast Mode		400		kHz
t _r	SDA and SCL rise time ¹	Standard Mode			1000	ns
t _f	SDA and SCL fall time ¹	Standard Mode			300	ns
t _{HIGH}	SCL clock high ¹	Standard Mode	4			μs
t _{LOW}	SCL clock low ¹	Standard Mode	4.7			μs
t _{SU;DAT}	Data, setup ¹	Standard Mode	250			ns
t _{HD;DAT}	Data, hold ¹	Standard Mode	5			ns
t _{BUF}	Min. stop to start condition ¹	Standard Mode	4.7			μs
R _{PU,FM}	Pull-up resistor for SDA/SCL ¹	Fast Mode	1		4.7	kΩ
R _{PU,SM}	Pull-up resistor for SDA/SCL ¹	Standard Mode	1		5.6	kΩ
Protection						
UVLO _{PVDD,CLR}	PVDD undervoltage lock-out clear (I2C interface functional)	PVDD rising	6.4			V
UVLO _{PVDD}	PVDD undervoltage lock-out threshold (I2C interface non functional)	PVDD falling			6.65	V

OVP _{PVDD}	PVDD over-voltage error threshold	PVDD rising		26.5		V
OVP _{PVDD,CLR}	PVDD over-voltage error clear	PVDD falling while OVP error triggered		26.25		V
OTE _{TRIG}	Over-temperature error trigger	Temperature rising		145		°C
OTE _{CLR}	Over-temperature error clear	Temperature falling		140		°C
OTW _{TRIG}	Over-temperature warning trigger	Temperature rising		115		°C
OTW _{CLR}	Over-temperature warning clear	Temperature falling		110		°C

¹Guaranteed by design simulation.

²Measured on evaluation kit PCB. Parameter may depend on application/layout/board stackup, etc.

³Heatsink: 527-45AB, thermal interface: A17653-03. Duration may depend on application/layout/board stackup, etc.

11 Functional description

11.1 MERUS™ Multilevel Switching

MERUS™ multilevel switching features several benefits in class D audio amplification compared to conventional 2-level switching:

- Ultra low power consumption
- Unmatched power efficiency
- Low electromagnetic emission
- Reduced system cost

This chapter aims to explain these benefits in more detail.

11.1.1 Multilevel Topology

The integrated power stage of the MA2306DNS is a MERUS™ multilevel switching topology. It consists of two half-bridges with each four power MOSFETs and a flying capacitor. An intermediate voltage supply is generated over the flying capacitor's terminals, which together with the switching scheme of the MOSFETs result in a 2-phase PWM output with three voltage levels (0V, $\frac{1}{2}PVDD$ and $PVDD$) rather than the conventional two. This doubles the effective switching frequency seen at the PWM output.

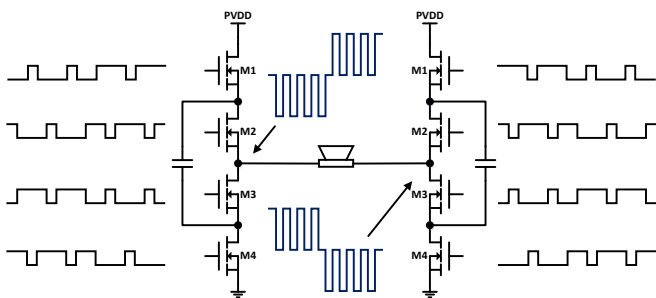


Figure 11.1: BTL/PBTL configuration of two 3-level half bridges

In MA2306DNS, two half-bridges are combined in a BTL/PBTL configuration (Figure 11.1) with a relative phase shift of 270° achieving a 5-level switching scheme across the load, effectively quadrupling the switching frequency seen at the load. This allows the internal MOSFETs to be driven with lower switching frequency, thus reducing power losses related to switching. Switching waveforms are shown in Figure 11.2.

11.1.2 Reduced Inductor Ripple Current

The multilevel topology reduces the voltage magnitude over the output filter inductor during switching, which in turn reduces the ripple current and relaxes filter inductor requirements. At idle operation where the output signal level is low, the MOSFETs are switched at 50 % duty cycle, resulting in near-zero ripple current. Hysteresis losses in the

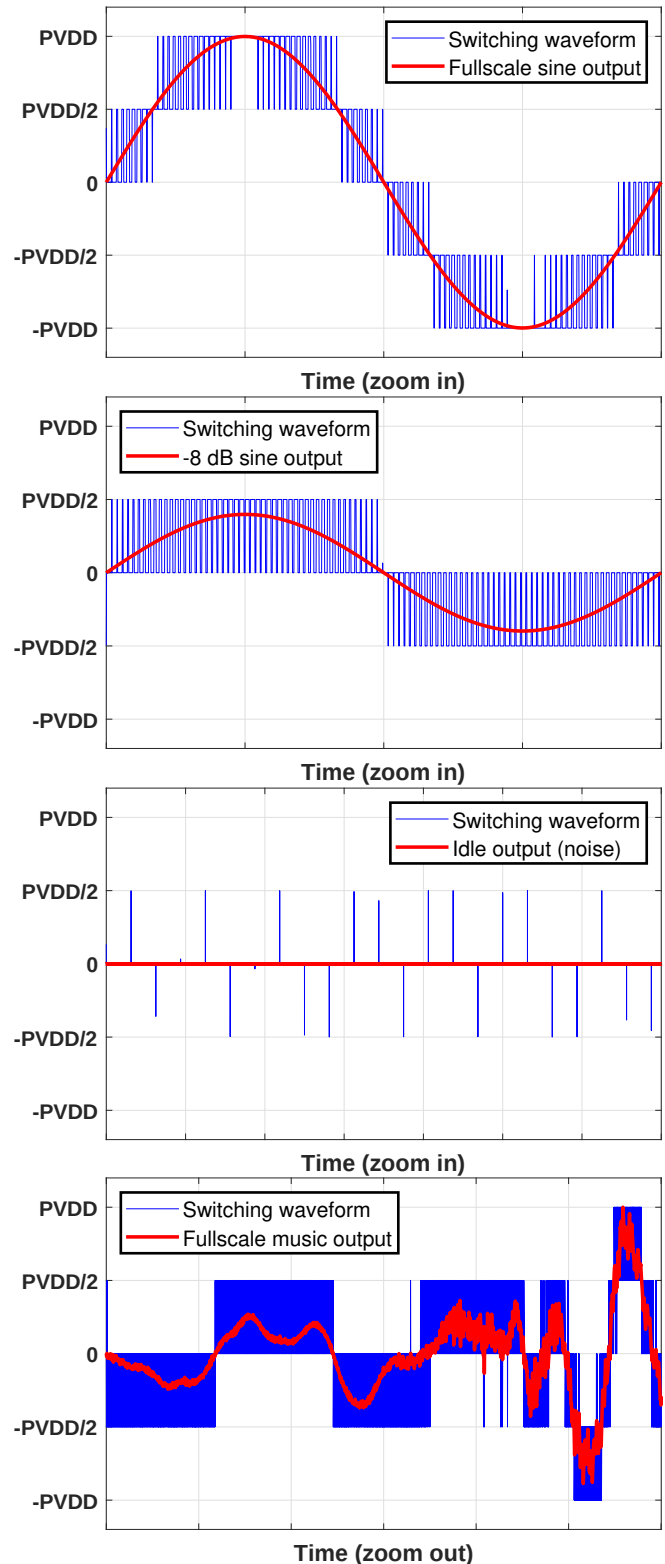


Figure 11.2: Multilevel switching with various signals.

inductor core material are therefore also greatly reduced which improves overall power efficiency. From Figure 11.3 it is clear that 5-level switching provides greatly reduced ripple current over the entire duty cycle range compared to conventional 2-level switching. In fact, it is not even necessary to use a standard LC filter for electromagnetic inter-

ference (EMI) suppression. The MA2306DNS can even operate with a simple ferrite filter reducing both application cost and size. See Section 11.1.4 for more information.

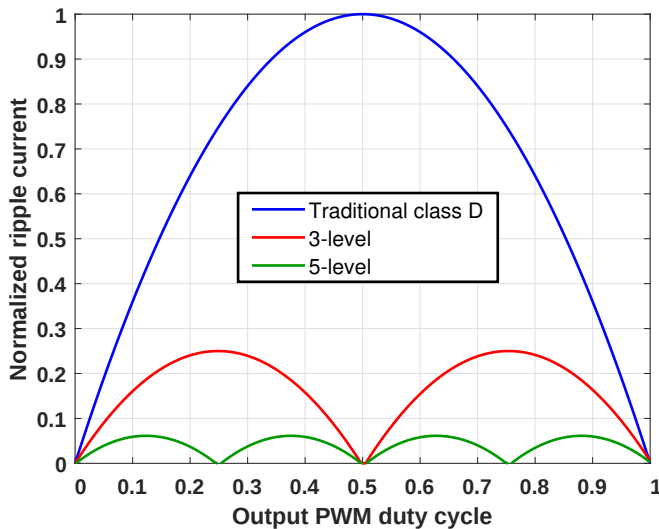


Figure 11.3: Ripple current comparison

11.1.3 Ultra Low Power Consumption with Music

MA2306DNS exhibits ultra low power consumption at low and mid output power, which is ensured by low MOSFET switching frequency, smaller voltage transitions when switching and near zero-ripple current. The low idle power consumption can make battery-powered applications last significantly longer or reduce the amount of battery cells required for a particular application.

Because of the low power consumption at lower output power levels, the MA2306DNS is ideal for real applications with dynamic signals like music/noise that exhibit a high signal peak-to-RMS ratio (crest factor). Power efficiency can be as high as 80 % at 1 W output power per channel, and because of the low power losses MA2306DNS may run without external heatsink in most applications. Figure 11.4 shows the difference in power efficiency between multilevel and traditional class D. From the figure it is clear that multilevel operation yields superior results for lower playback levels, which is the normal usage in common speaker products.

11.1.4 EMI Reduction

Complying with EMC regulations is a typical challenge with class D amplifiers due to the high power square wave output waveform. Traditional class D amplifiers have maximum current ripple in the output filter inductor at 50 % duty cycle (idle operation) which gives rise to high amount of common mode frequency content. However, MERUS™ multilevel operation exhibits minimal switching at idle which ensures minimal common mode emission at idle operation. The differential mode content at higher playback levels, when switching activity is stronger, is also significantly reduced as the transition between voltage levels is relatively small

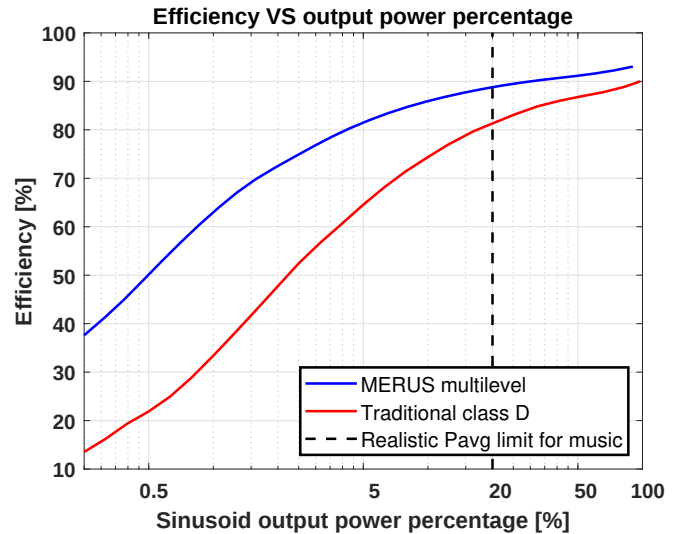


Figure 11.4: MERUS™ multilevel modulation efficiency compared to traditional 2-level modulation

for multilevel compared to traditional class D. In addition, MA2306DNS makes it possible to address EMC issues from a software perspective with its [PWM synchronization](#) feature as well as [configurable switching edge](#) steepness (slew rate), all to reduce EMI in applications with many devices, e.g. multi-channel amplifiers.

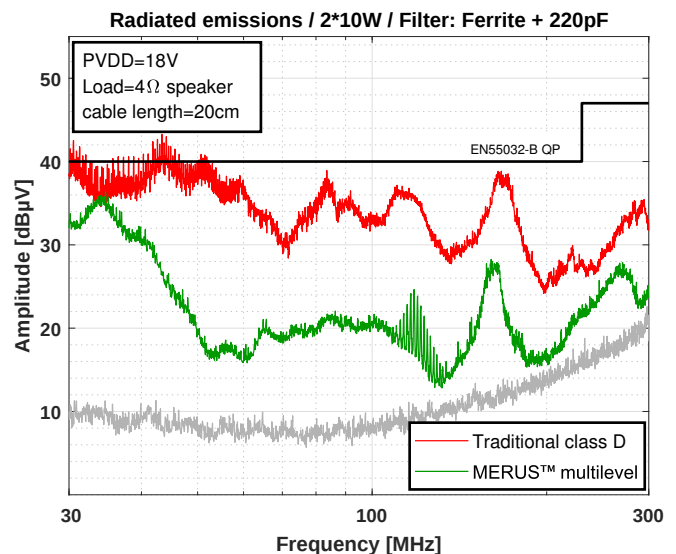


Figure 11.5: MERUS™ multilevel emissions compared to traditional modulation

11.2 Modes of Operation

11.2.1 Normal Operation / Shutdown (ENABLE pin)

The ENABLE pin (20) controls the shutdown state of MA2306DNS. When ENABLE is low, the device is in shutdown mode. When ENABLE becomes high, the device exits shutdown state, boots up and enters normal operation. Refer to [specifications](#) for ENABLE timing.

11.2.2 Mute / Unmute (NMUTE pin)

NMUTE (19) controls muting of the amplifier output and is an active-low pin, i.e. if NMUTE=high the output will be unmuted. Muting is instantaneous, but unmuting is a timed function with a delay (refer to [NMUTE timing](#))
Muting can also be performed with the [mute_ch0/1](#) register for individual channels. Use [mute_source](#) to choose the source of muting: NMUTE pin or register setting.

In muted state, no audio content is present at the amplifier output, but there will be some switching activity to balance and pre-charge the flying capacitors. If no switching activity is desired the individual amplifier channels can be disabled with the [disable_ch0/1](#) registers.

Optionally, the NMUTE pin can be used to enable and disable the standby mode described in section 11.2.3. The pin functionality is modified with the [nmute_action](#) register.

11.2.3 Standby

The device can be put in standby mode for the lowest possible power consumption while still maintaining a functional I2C interface (to wake the device at a later point). In this mode, it is still possible to have communication with the device while the output stage and related functional blocks remain disabled. The standby mode is controlled with the [standby](#) register or optionally with the [NMUTE](#) pin.

11.3 BTL/PBTL Output Configurations

The amplifier output can be configured to operate in

- Bridge Tied Load (BTL)
- Parallel Bridge Tied Load (PBTL)

Table 7: BTL/PBTL properties

Parameter	PBTL	BTL
Min. current limit	16 A	8 A
Recommended load	2-4 Ω	4-8 Ω
MSEL pin tie-off	Ground	VDD_IO

The MSEL pin (34) controls the output configuration and must be set before the device powers up (when ENABLE=1). Alternatively, the [mode_pbtl](#) register can be used to configure the output after the device has powered up. The [msel_reg_ctrl](#) register must also be set for the mode_pbtl register to take effect and override the hardware setting of the MSEL pin.

BTL is best suited for standard current, two-channel applications, e.g. stereo speaker pairs and 2-way systems. PTBL is a 1-channel configuration but with twice the output power/current capability, which can be useful for sub-woofers and/or low impedance speakers. Refer to Figure 11.6 and 11.7 for configuration diagrams.

PBTL mode dynamically enables the second output based on the signal level so that idle power consumption can be as low as possible when high output power is not needed.

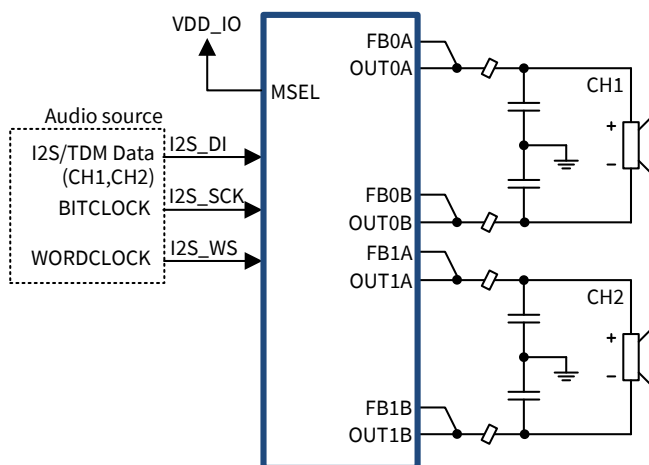


Figure 11.6: Bridge Tied Load (BTL) configuration

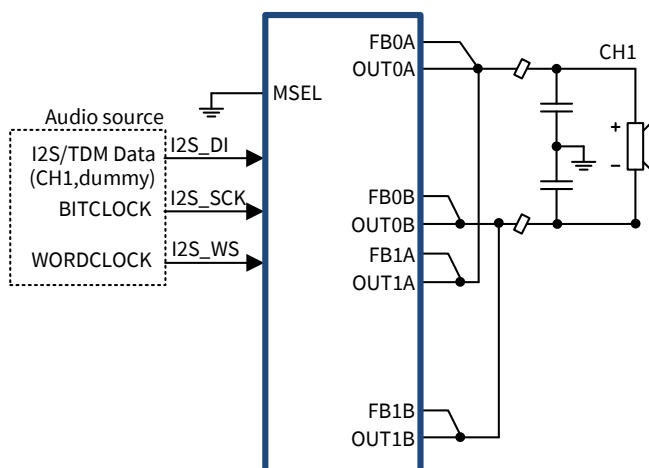


Figure 11.7: Bridge Tied Load (PBTL) configuration

11.4 Gain Configuration

MA2306DNS offers different gain configurations for matching full scale output with the desired PVDD voltage in an application. The gain is controlled with the [pvdd_scale](#) register. Reducing the amplifier gain to a lower value also reduces output noise. Changing gain settings while the power stage is unmuted can result in significant pop/click and should be avoided. Each gain setting can only be used up to a specific supply voltage (PVDD). Table 8 shows the recommended pvdd scale setting for each different maximum PVDD supply level and the maximum peak output voltage.

11.5 Protection

MA2306DNS offers a range of protection features to avoid damage to the device itself or attached speakers.

Table 8: Gain options for recommended (guideline) PVDD voltages.

pvdd_scale	Maximum PVDD	Maximum peak output voltage - 4 Ω + 22 μ H
01	18 V	15.2 V
10	22 V	18.4 V
11 (default)	26 V	22 V

11.5.1 Errors and Error Handling (NERR pin)

The protection system in MA2306DNS monitors a range of parameters to check if min/max thresholds are exceeded. Exceeding the thresholds will trigger an error event in the protection system and the NERR pin (pin 11) will change from high to low. The NERR pin will only report errors correctly after the first PLL lock which requires clocks present on I2S_SCK and I2S_WC pins.

The NERR pin can be used as an interrupt flag for an external host control device, e.g. a system microcontroller. Alternatively, the [err_pin](#) register can be used to monitor the NERR pin as well. Once an error has been detected by the host, the error type can be identified by reading the error registers. Connect a 51 k Ω resistor from NERR to VDD_IO as shown in Figure 11.8.

General device errors:

- Low temperature warning
- I2S input error
- PLL error
- PVDD over-voltage
- PVDD under-voltage
- Over-temperature error
- Over-temperature warning

The errors above can be read as individual bits in the following registers:

- [errVect_now.errVector_all__0](#) (instantaneous)
- [errVect_acc.errVector_all__0](#) (accumulated/sticky)

Individual channel errors:

- DC error
- Flying capacitor error
- Over-current error

The errors above can be read as individual bits in the following registers:

- [errVect_acc.errVector_ch0](#) (Channel 0 accumulated / sticky errors)
- [errVect_acc.errVector_ch1](#) (Channel 1 accumulated / sticky errors)

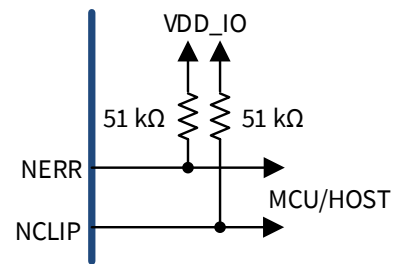


Figure 11.8: NERR/NCLIP schematic

Clearing errors

Errors can be cleared by toggling the [reg.errTrig_reset](#) register from 0 to 1 and then back to 0.

Error handling:

It is generally recommended to use the accumulated error registers for error detection and handling. Normal error handling procedure:

- I2S clocks must be enabled at least once so the device can properly register the PLL and I2S error.
- Disregard errors during start-up of the device defined by [T_ENABLE](#). (Flying capacitor error will appear accumulated for both channels when enabling the device).
- Clear errors immediately after start-up.
- Monitor accumulated error registers (general + channel) and take appropriate action if an error occurs. Optionally, use the NERR pin to detect if an error was triggered.
- Clear error register(s) after action has been taken to again monitor for new errors.
- Note that flying capacitor errors are expected to trigger while a temperature error occurs. Table 9 shows how to handle errors in these specific conditions.

Error handling during standby mode:

Special consideration needs to be given to the error mechanisms when the device is set into standby mode:

- During standby, the device will pull the NERR pin low and the I2S input and PLL errors will be triggered in the error registers. (PLL error will not be registered in the accumulated register).
- When the device is set to exit standby mode (stand by mode disabled) the NERR pin will be pulled high again and only the I2S input error will remain in the accumulated register which at this point can be cleared.
- Table 9 shows how to handle errors in these specific conditions.

Table 9: Error handling exceptions

Error type	Disregard during start-up	Triggered during standby	Triggered with over-temp. err.
I2S input		✓	
PLL		✓	
Flying cap.	✓		✓

11.5.2 Output DC Protection (DCP)

The amplifier output can detect if a DC voltage is present at the output terminals. If the output voltage stays above the DCP threshold for too long, corresponding to a 1 Hz sinusoid, the power stage will shut down, a DC error will be reported to the [channel error register](#) and the power stage will attempt to restart and resume operation. Each output channel is monitored separately.

11.5.3 Over-Current Protection (OCP)

Over-current (OC) events can be triggered by e.g. driving low impedance loads with high PVDD and shorting speaker terminals to each other or to ground. The current flowing in each internal MOSFET in the output stage is monitored. If the threshold is exceeded (refer to [BTL threshold](#) and [PBTL threshold](#)) the power stage will shut down, an OCP error will be reported to the error register and the power stage will attempt to restart and resume operation.

11.5.4 PVDD Over/Under-Voltage Protection

PVDD features over-voltage (OVP) and under-voltage (UVP) protection as well as under-voltage lockout (UVLO). Threshold voltages can be found in [specifications](#). Refer to Figure 11.9 for an overview of the voltage protection on PVDD.

PVDD voltage range	Functionality
Above absolute maximum	Device breakdown
OVP area	Output muted
Recommended operating conditions	Normal operation
UVP area	Output muted
UVLO area	Device in reset

Figure 11.9: PVDD voltage protection overview

OVP protects the MOSFETs in the output power stage against permanent damage due to over-voltage. If PVDD voltage rises above OVP_{PVDD} the power stage will stop switching and the output will effectively be muted (overriding NMUTE pin). PVDD voltage must fall below $OVP_{PVDD,CLR}$

voltage before the device exits muted state. OVP will not protect the device against PVDD voltages rising above the [absolute maximum value](#).

UVP behaves similarly and also mutes the output (without audio artifacts) by stopping all switching in the output power stage if PVDD voltage drops below the [recommended operating conditions](#). In UVP state it is still possible to communicate with the device but mute is sustained. UVP should be considered a warning for low and/or unstable PVDD.

If PVDD is reduced further, falling below the $UVLO_{PVDD}$ threshold, the device shuts down. Power-on reset is applied when raising PVDD above the rising threshold again. When shut down, the device is not functional.

11.5.5 Over Temperature Protection (OTP)

An internal temperature sensor effectively safeguards the device against a thermally induced failure due to overloading and/or insufficient cooling. A high die temperature initially causes an Over Temperature Warning (OTW). During an OTW event, the device will continue to operate normally but if the temperature rises further, the device will reach Over Temperature Error (OTE). An OTE event will cause the device to stop all output switching activity in order to avoid permanent damage. The device will resume switching when the temperature has dropped sufficiently. Both OTW and OTE will report to the NERR pin and the error registers. Refer to [specifications](#) for OTE and OTW trigger and clear temperatures.

11.5.6 PLL Error and I2S Input Error

PLL error will occur in case of lost clock signals on the I2S_SCK and I2S_WC. The MA2306DNS relies on these clock signals to operate properly and if they are not present or faulty, the core will come to a halt state, reporting to the error system that the PLL is not locked. When the clock signals return, operation is resumed. In the event of bad audio input an error will also be reported to the error register on a separate bit.

11.5.7 Flying Capacitor Over/Under-Voltage Protection

The flying capacitors connected to the VFCxxx pins are essential for MERUS™ multilevel switching to function properly. During normal operation an internal voltage balancing circuit will generate a virtual PVDD/2 supply across the external flying capacitor. To protect the internal MOSFETs against permanent damage the MA2306DNS features over/under-voltage protection (OVP/UVP) in case of loop instability or flying capacitor balancing errors. The flying capacitor voltage is monitored and OVP/UVP is triggered if the voltage over the flying capacitors is deviating too far from PVDD/2. In this event, the output stage stops switching (output muted). When the flying

capacitor voltage has again been balanced the device starts switching automatically (output unmuted).

Note that flying capacitor over/under-voltage protection will not trigger if the PVDD voltage is below 13 V. The reason is that the feature is designed to protect the internal MOSFETs against over-voltage conditions that could cause permanent damage to the IC, and at lower PVDD voltages the MOSFETs are no longer prone to this condition.

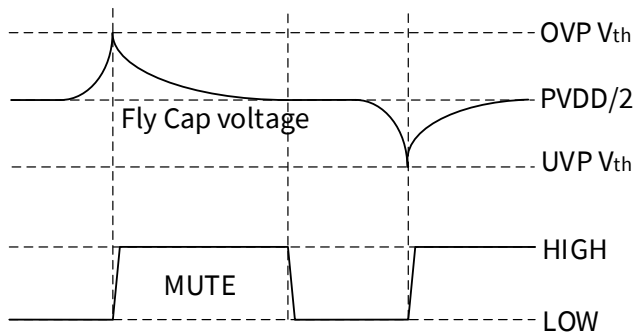


Figure 11.10: Flying capacitor protection behaviour

11.5.8 NCLIP Pin

The NCLIP works as a clipping indicator and starts pulsing from high to low at higher levels and becomes constant low when near clipping. A system microcontroller can use this pin as an indicator to decrease volume/gain if desired when clipping occurs. Alternatively, the integrated DSP features a configurable output limiter that can be used to prevent clipping. Triggering NCLIP does not register as an error, but the `clip_pin` register can be used monitor the state of NCLIP. Connect a 51 kΩ resistor from NCLIP to VDD_IO as shown in Figure 11.8.

11.6 Power Supplies

11.6.1 Supplies for Internal Analog/Digital Circuitry (VDD/VDD_IO)

MA2306DNS generates its own internal analog/digital supplies from VDD with the use of external capacitors and the AVDD_REG, DVDD_REG and CD_DIG pins. AVSS is the ground reference pin for the internal analog circuitry. MA2306DNS is designed to work with common power supply voltages, 1.8 V / 3.3 V, which are typically found in applications powering the host device already. When VDD is power cycled, the MA2306DNS register settings are reset to default. All VDD decoupling capacitors should be placed as close as possible to the supply pins. The recommended capacitor specifications are shown in Figure 11.11.

VDD_IO is used for pull-up resistors to I/O pins on the south side of MA2306DNS (pins 11-18). These are NERR (11), NCLIP (12), I2S_DO (13), I2S_WC (14), I2S_SCK (15), I2S_DI (16), I2C_SDA (17), I2C_SCL (18), NMUTE (19) and ENABLE (20). Note that the serial audio data output pin I2S_DO is

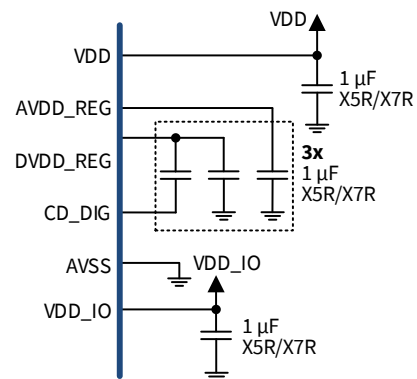


Figure 11.11: Decoupling/supply capacitor schematic with recommended specifications

internally driven by the VDD_IO supply.

For simplicity, VDD_IO and VDD can be tied to the same low voltage supply in the application.

11.6.2 Flying Capacitors

The MA2306DNS power stage uses flying capacitors to generate a $\frac{1}{2}$ PVDD supply voltage for multilevel operation. Each output switch node pin OUTxx has a corresponding flying capacitor, with a positive and a negative terminal, VCFxxP and VCFxxN pins. The fly-cap pins are high power pins and care must be taken to reduce inductance/resistance in the PCB layout as the full output current will flow through pins/caps. Figure 11.12 shows an example of how the capacitors should be connected. Keep the flying capacitors as close to the device as possible with as short and wide PCB traces as possible.

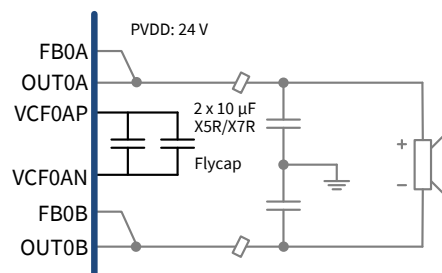


Figure 11.12: Flying capacitor schematic with recommended specifications

When choosing flying capacitors, it is necessary to keep capacitance derating vs. DC bias voltage in mind if multi-layer ceramic capacitors (MLCC) are used. The fly-caps are constantly charged to $\frac{1}{2}$ PVDD, which will derate the expected capacitance. In general, high quality 10 µF 25V X5R/X7R 0805 MLCCs are recommended (example: GRM21BR61E106KA73K). The minimum effective capacitance should be 6.0 µF at $\frac{1}{2}$ PVDD if operation at PVDD ≥ 24 V and 8 A of output current per channel is required.

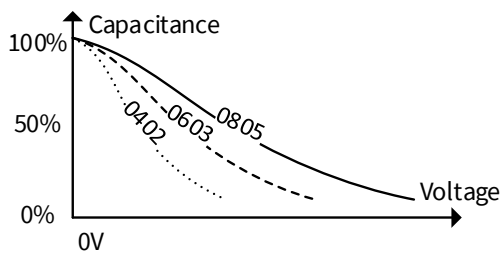


Figure 11.13: Typical derating for multi-layer ceramic capacitors (MLCC) with different package sizes

11.6.3 Power Stage Supply (PVDD)

PVDD supplies current to the output power stage to drive the load. A bulk decoupling capacitor is recommended on the PCB to keep the supply stable, e.g. aluminium electrolytic type capacitor. Capacitance value will depend on the application (lowest playback frequency, ripple voltage and maximum peak power requirements). In general, a 470 μ F aluminium electrolytic capacitor will be sufficient for most applications.

To decouple fast transients, it can be beneficial to place two low ESR capacitors with smaller capacitance value, e.g. 1 μ F and 10 μ F, close to the PVDD pins on each opposing side of the MA2306DNS. Figure 11.14 shows the recommended PVDD decoupling schematic.

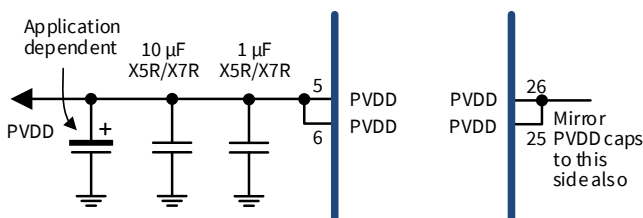


Figure 11.14: Typical decoupling for multi-layer ceramic capacitors (MLCC) with different package sizes

11.7 Clock System

MA2306DNS generates its own internal clock through a PLL in the presence of a serial audio bit clock (I2S_SCK) and a word clock (I2S_WC).

The frequency of the audio bit clock is auto-detected and clock frequencies up to 24.576 MHz are supported. The audio bit clock frequency will depend on sampling frequency, slot size (frame width) and the number of channels in the audio stream according to Equation 1.

$$f_{\text{SCK}} = f_s \cdot \text{slot_size} \cdot N_{\text{CH}} \leq 24.576\text{MHz} \quad (1)$$

11.8 Audio Interface

11.8.1 Digital Serial Audio Input

MA2306DNS has a single serial data audio input port that consists of the pins I2S_WC (word clock), I2S_SCK (bit clock) and I2S_DI (data in). The input port supports two-channel I2S and multi-channel TDM audio formats with sampling rates of 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz with data-words of 16, 24 or 32 bits in length. The format alignment is configured in the [data_alignment](#) register. MA2306DNS is always configured as an audio sink device (receiver). TDM format is capable of up to 16 audio channels on a single data line, making it ideal for multi-channel applications with multiple ICs.

By default, the internal audio receiver in MA2306DNS will look for starting edge on the word clock and receive packages based on the package slot size (also known as frame width, see [slot_size](#) register), irrelevant of the frame midpoint transition on the word clock. This means that I2S (2-channel) and TDM (multichannel) are processed similarly by the receiver, the difference being the amount of slot size packages received between two starting edges of the word clock. For example, a 2-channel 32 bit I2S audio stream will have a 64 bit audio frame cycle between word clock starting edges, whereas a 4-channel 32 bit TDM audio stream will have 128 bit between starting edges (refer to audio data configuration examples in Figures 11.16 and 11.17). In this way, MA2306DNS can automatically detect if the format is 2-channel or multichannel (I2S/TDM) as long as [slot_size](#), [data_size](#) (bit depth), [data_alignment](#), [sck_pol](#), [ws_fs_rising](#) and [lsb_first](#) registers are configured to match for both the external transmitter (source) and the MA2306DNS (sink).

To configure the input channel routing, refer to the [tdm_input_map](#) register.

11.8.2 Digital Serial Audio Output

MA2306DNS features a serial audio data output (pin 13: I2S_DO) with the same audio format properties as the serial audio input. To enable the audio output, the [tx_enable](#) register must be enabled. By default (refer to [ROM code](#)), the DSP output channels 1 and 2 (the signals received by the amplifier) are routed to I2S_DO, but this can be configured using the [tdm_output_map0-15](#) registers.

11.8.3 Input-to-Output Audio Propagation Delay

MA2306DNS offers a very low propagation delay from audio input to amplified output, making it ideal for delay sensitive applications such as echo-cancelling speaker phones and conference equipment. Refer to [specifications](#) for more info.

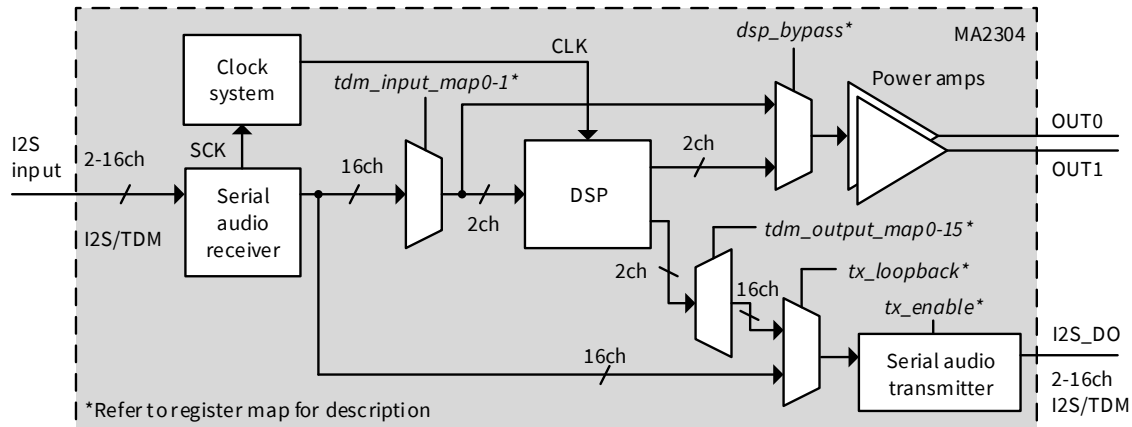


Figure 11.15: Audio routing

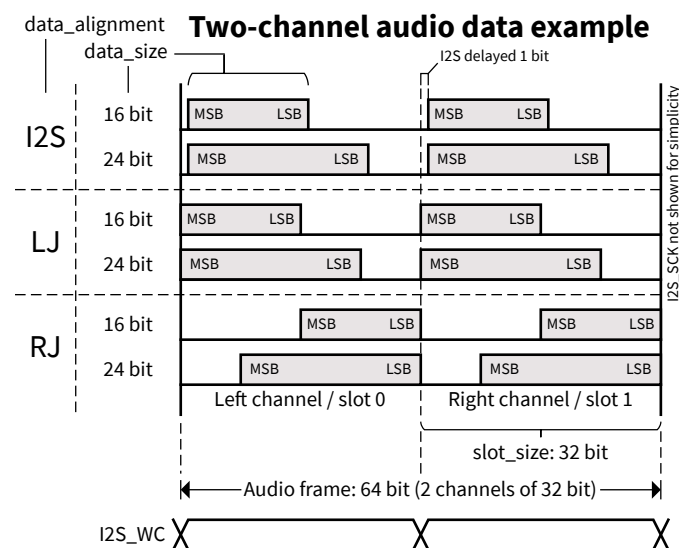


Figure 11.16: Audio data configuration/timing for two channels

11.9 Digital Signal Processor (DSP)

11.9.1 Graphical User Interface (GUI)

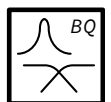
MA2306DNS integrates a configurable dual-core DSP for equalization and audio enhancement to compensate for limitations in real applications with speakers. The DSP is controlled with the MA2306DNS software GUI which features a set of pre-defined audio flows including building blocks such as equalizers, filters, volume control, limiters, dynamic range compressors, signal routing and more. DSP code can be exported as a set of register addresses and values to be written over I2C at boot-up from the host device. Figure 11.18 shows a snapshot of the visual interface of the GUI. The software documentation can be found in the product website.

11.9.2 Configurable Audio Blocks

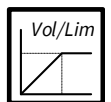
Selectable pre-defined audio flows in the GUI consist of configurable audio blocks. The audio flows are designed

and computed to preserve dynamic range throughout the flow. Some of the audio blocks are:

Biquad: A generic second order IIR filter for highpass, lowpass, peaking filters etc. Parameters like quality factor, corner frequency and gain can be adjusted.



Volume control / limiter: The volume control and limiter are combined into one block in the end of the audio flow to preserve dynamic range. The limiter can either be RMS or peak based and will reduce / increase gain with attack/release times at a specified threshold.



Multiband DRC: Two and three band dynamic range compressors. Can be used for level-dependent EQ to act as a 'loudness' function; Bass and treble are more accentuated at lower playback levels to compensate for human hearing.



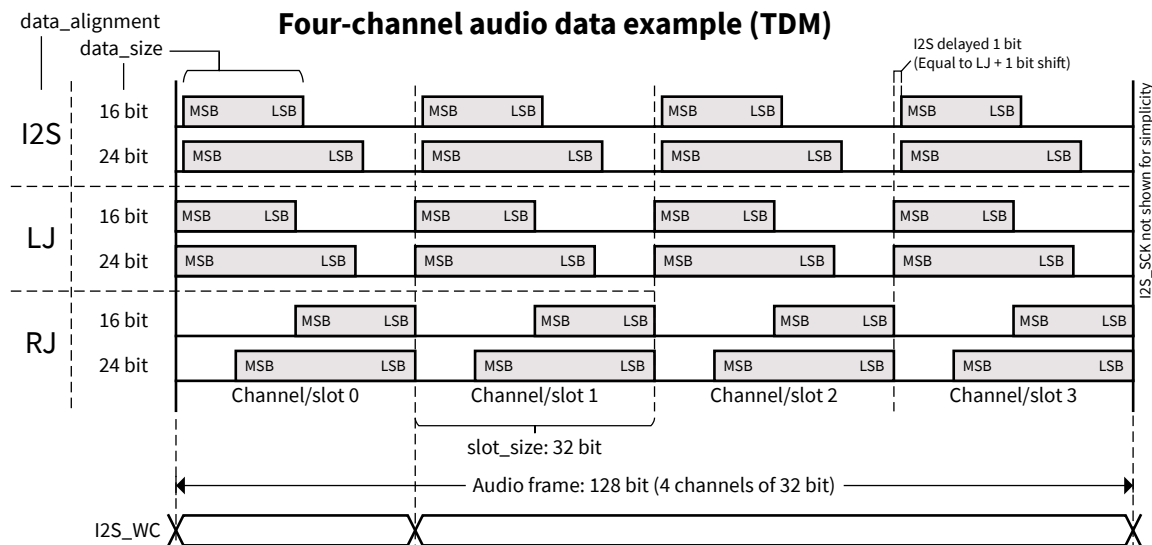


Figure 11.17: Audio data configuration/timing for four channels. Note that choosing 'I2S' in data_alignment for MA2306DNS does not restrict the data stream to only two channels. 'I2S' in data_alignment just refers to the data being aligned to the left and delayed by one bit.

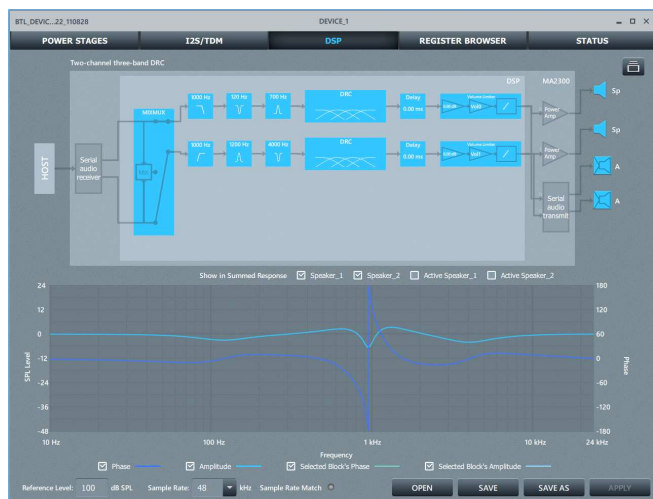
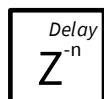


Figure 11.18: MA2306DNS GUI used for configuring the DSP

Dynamic EQ: A block that implements level dependent equalization to increase loudness perception specially at low playback levels.



Delay: Standard delay block with up to 2×10 ms in a 2-channel system (or 1×20 ms) at 48 kHz sampling frequency.



Refer to the manual of the GUI for in-depth information of all features.

11.9.3 DSP Core

The DSP core operates at a maximum frequency of 49.152 MHz. The program and data memory for each DSP core consist of 1024 instructions for each DSP flow, and is executed

sample-by-sample. As a result, the core clock is 49.152 MHz at 48 kHz sampling rate (fs) for 2048 instructions. At 96 kHz (2×fs) and 192 kHz (4×fs) sampling rates, the amount of instructions available will be reduced to 1024 and 512, respectively. At 48 kHz, 2048 instructions correspond to roughly 100 configurable biquads, leaving plenty of equalization power for 2-channel operation.

11.9.4 Writing to the DSP Memory

The DSP memory consists of 6 kB of program memory and 8 kB of data memory. The DSP memory must be programmed over I2C from the host for every reset as MA2306DNS contains volatile memory only. It is important that the entire DSP memory must be written in a successive manner from lowest to highest register address, e.g. using a standard block write.

It is recommended to use the following routine when writing to the DSP to avoid audible artifacts of the DSP memory changing during the writing process:

1. Mute the amplifier output using the NMUTE pin or the `mute_ch0/1` registers (remember to also set the `mute_source` register if muting with registers is desired).
2. Write the entire DSP code (which has been exported from the GUI) to the DSP memory using block writing.
3. Restart the DSP by setting the `dsp_enable` register bit to 0 and then to 1.
4. Unmute the amplifier output again.

MA2306DNS

MERUS™ Multilevel Switching Class-D Audio Amplifier

11.9.5 ROM Code / Static Memory

The MA2306DNS contains ROM code (static memory) with a preconfigured DSP program that includes volume control and peak limiters. The ROM code is applied to the DSP by default when MA2306DNS is reset.

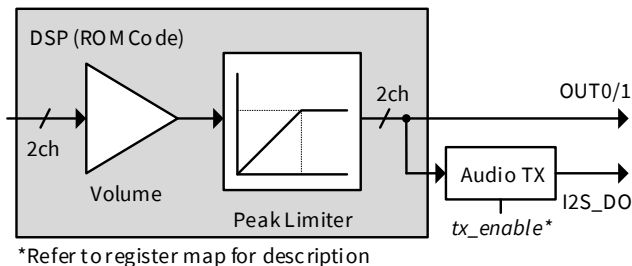


Figure 11.19: DSP ROM code

The ROM code can be disabled by disabling the DSP entirely in the [dsp_enable](#) register. Alternatively, the DSP can be bypassed with the [dsp_bypass](#) register. The output signal would be identical using either method, but the power consumption is slightly reduced by disabling the DSP instead of bypassing.

11.9.6 Volume Control

Volume can be controlled with the [volume_ch](#) register. The audio volume is not applied instantly but ramped to avoid audible click/pop artifacts. Volume ramping can be disabled by enabling the [vol_instant](#) register.

11.9.7 Peak Limiter (ROM Code)

The peak limiters in the ROM code can be configured with [attack_ch](#), [release_ch](#) and [threshold_ch](#) registers, which control the attack and release times as well as the threshold for limiting. The attack and release times are sample rate dependent in the way that a higher register value should be chosen for higher sample rates to achieve an equivalent attack/release time.

The peak limiter in the ROM code is overwritten when a DSP program, exported from the GUI containing peak/RMS, is written to the DSP memory. In this case, the ROM code peak limiter registers effectively become non-applicable.

11.10 Auxiliary ADC

MA2306DNS features an 8-bit auxiliary ADC. The ADC can sample from the power stage supply PVDD, the internal temperature sensor or a voltage on the ADC_IN pin from an external source. The sampled data is available in registers [pvdd_chip](#), [temp_chip](#) and [adc_pin](#). The ADC_IN pin voltage range is 0 V (min) to 1 V (max).

The ADC can be useful for general purpose monitoring, e.g. keeping temperature below a specified point by adjusting

[volume](#) if temperature readings become too high according to the application specification. The ADC is not designed for tasks with high precision.

11.11 I2C Serial Control Interface

MA2306DNS offers a serial control interface through the standard 2-wire I2C protocol using I2C_SDA (data) and I2C_SCL (clock) lines. An application host device may then access the register map to configure the MA2306DNS.

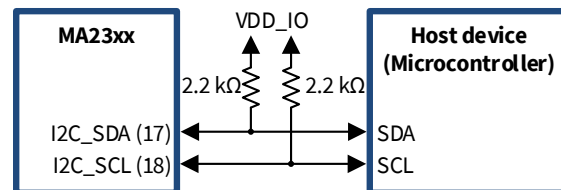


Figure 11.20: I2C serial control interface block diagram

MA2306DNS uses 16 bit register addresses for its internal register map (example: 0x0001). The SDA line is sampled on the rising edge of the SCL line and the I2C command is shifted/sampled with MSB first.

Communicating properly with the MA2306DNS to access a single register must contain the following I2C sequence:

Device address	Register address	Data
7 bits + R/W bit	16 bits	8 bits

Please see Section [11.11.2](#) and [11.11.3](#) for device addressing and write/read commands.

The SDA and SCL lines must be pulled high once per application to the voltage supplying VDD_IO through a resistor, e.g. 2.2 kΩ, to ensure correct I2C functionality. The minimum and maximum recommended pull-up resistor value is shown in [specifications](#).

Please refer to the original I2C bus specification and user manual provided by NXP Semiconductors for more detailed information on I2C communication.

11.11.1 Device Address

Device addresses for I2C communication can be set by pulling the I2C_AD0 (pin 36) and I2C_AD1 (pin 35) pins to VDD_IO (high) or ground (low). This gives four unique device addresses for applications with up to eight BTL channels. The pin configuration on I2C_AD0 and I2C_AD1 are only read once during start-up of the device.

If four device addresses are not sufficient, hardware resistor programming can be used for the I2C_AD0 and I2C_AD1 pins to enable up to 64 unique device addresses. The pins must be connected to ground through a resistor of a specific value as shown in [Figure 11.21](#). [Table 11](#) illustrates the combination of resistors to yield a specific address.

Table 10: Device addresses combinations

I2C address	I2C_AD1	I2C_AD0
0x20	Low	Low
0x21	Low	High
0x22	High	Low
0x23	High	High

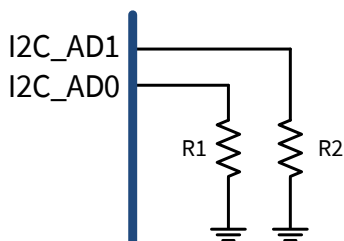


Figure 11.21: Resistor programming schematic

Table 11: Device addresses using resistor programming.
Addresses are shown in decimal format

R2 R1	150k	100k	68k	47k	33k	22k	15k	10k
150k	0	1	2	3	4	5	6	7
100k	8	9	10	11	12	13	14	15
68k	16	17	18	19	20	21	22	23
47k	24	25	26	27	28	29	30	31
33k	32	33	34	35	36	37	38	39
22k	40	41	42	43	44	45	46	47
15k	48	49	50	51	52	53	54	55
10k	56	57	58	59	60	61	62	63

11.11.2 I2C Write Operation

Each I2C transaction is initiated from an I2C transmitter by sending an I2C start condition followed by the 7-bit I2C device address and the read/write bit (bit 8, write=0).

If the transmitted I2C address matches the configured address of the device, the device will acknowledge the request by pulling the SDA line to ground (bit 9). The I2C transmitter samples the acknowledged bit from the device on the next rising edge of SCL.

To complete the write operation, the I2C transmitter must continue transmitting the address and at least one data byte. The device continues to acknowledge each byte received on the 9th SCL rising edge. Each additional data byte written to the device is written to the next address in the register bank.

The write transaction is terminated when the I2C transmitter sends a stop condition to the device (rising edge on SDA during SCL kept high).

Block writing large amounts of data is also supported.

Refer to Figure 11.22 for write sequence.

11.11.3 I2C Read Operation

To read data from the device register bank, the read transaction is started by the I2C transmitter, sending a write command to the I2C address (bit 8, write=1), followed by the device address to read from.

The device will acknowledge the two bytes and data can now be read from the device by sending a repeated start, followed by an I2C read command (bit 8, read=1).

The device will acknowledge the read request and start to drive the SDA bus with the bits from the requested register bank address.

If the user tries to read in a non-existing address, acknowledge will be sent anyway but read will be ignored internally (0x00 will be sent to the I2C read requester).

The read transaction continues until the I2C source does not acknowledge the 9th bit of the data read byte transaction and sends a stop condition (rising edge on SDA during SCL kept high).

Refer to Figure 11.22 for read sequence.

Read Operation without Write Start

To read data from the device register bank, the I2C source can send a read transaction without write command first, meaning an I2C read command consisting of a byte with the device I2C address and the R/W bit set. The device will acknowledge the read request and start to drive the SDA bus with the bits from the last requested register bank address+1.

11.12 EMI Mitigation

In addition to the inherently low EMI levels from the MERUS™ multilevel switching output, MA2306DNS features ways to mitigate EMI further, which can be useful for applications with multiple devices.

11.12.1 Configurable Switching Edge

Fast square wave switching transients usually increase the amount of unwanted high frequency EMI. The switching edge steepness (slew rate) can be controlled in the [gd_dVdt](#) register which can be used as a tool for tuning applications for EMI compliance. The compromise is efficiency, as slower transients will result in higher switching losses. Additional EMI suppression can be achieved by reducing the switching edge steepness (tested using the MA2306DNS EVK).

11.12.2 PWM Synchronization for EMI Reduction

In multi-channel systems with multiple MA2306DNS devices, it can be increasingly necessary to suppress EMI. The NCLIP pin (12) can be used as an input/output to synchronize PWM signals of multiple devices and allow them to be

MA2306DNS

MERUS™ Multilevel Switching Class-D Audio Amplifier

I2C write single byte:

S	Device addr [6:0]	W	A	Register addr [15:8]	A	Register addr [7:0]	A	Data [7:0]	A	S
---	-------------------	---	---	----------------------	---	---------------------	---	------------	---	---

I2C write multiple bytes:

S	Device addr [6:0]	W	A	Register addr [15:8]	A	Register addr [7:0]	A	Data [7:0]	A	S	Data [7:0]	A	...	S
---	-------------------	---	---	----------------------	---	---------------------	---	------------	---	---	------------	---	-----	---

I2C read single byte:

S	Device addr [6:0]	W	A	Register addr [15:8]	A	Register addr [7:0]	A	S
---	-------------------	---	---	----------------------	---	---------------------	---	---

S	Device addr [6:0]	R	A	Data [7:0]	A	S
---	-------------------	---	---	------------	---	---

I2C read multiple bytes:

S	Device addr [6:0]	W	A	Register addr [15:8]	A	Register addr [7:0]	A	S
---	-------------------	---	---	----------------------	---	---------------------	---	---

S	Device addr [6:0]	R	A	Data [7:0]	A	Data [7:0]	A	...	S
---	-------------------	---	---	------------	---	------------	---	-----	---

A	Acknowledge
W	Write
R	Read
S	Start/stop

Figure 11.22: I2C write and read sequences



Figure 11.23: Configurable PWM switching edges to reduce high frequency EMI content

driven out of phase which can have an influence on EMI performance. PWM sync is configured according to Figure 11.24 as follows:

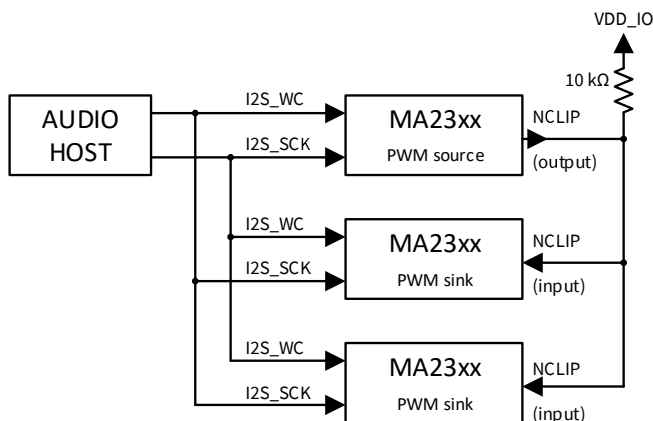


Figure 11.24: PWM synchronization for multiple MA2306DNS devices

1. Configure NCLIP pin to act as PWM input/output [gpio_sync_zclip](#)
2. Configure PWM source device by setting [sync_out_enable](#)
3. Configure PWM sink devices by setting [sync_in_enable](#)

4. Control PWM phase relationship in either source or sink devices by setting time lag in [reg_pwm_phase](#)

NCLIP must be pulled up to VDD_IO through a 10 kΩ resistor. The clock signals I2S_SCK and I2S_WC in the audio stream must be the same for all devices.

12 Application Information

12.1 EMC Ferrite Output Filter

The MA2306DNS allows for inductor-less operation while achieving EMI compliance. This is mainly due to the MERUS™ multilevel switching technology which reduces the magnitude of the switching waveform at all output levels. A simple and inexpensive ferrite-capacitor output filter can be used to suppress the emissions from the amplifier output. A resistor of 3.9 Ω connected in series with the capacitor can help to reduce residual noise when the capacitor value is 470 pF or higher. The filter schematic is shown in Figure 12.1 and recommended filter component values are shown in Table 12.

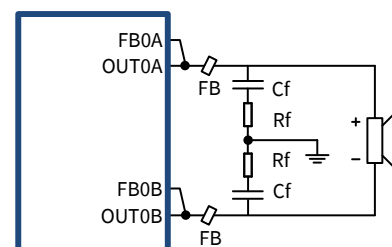


Figure 12.1: EMC ferrite output filter

Table 12: EMC ferrite filter recommendation

Ferrite	Capacitor
NFZ2MSD150SN10L	220 pF - 470 pF
NFZ2MSD301SZ10L	220 pF - 470 pF

PCB layout for the output filter should be tight and with the smallest possible current return path for optimal EMI performance. In an application, cables connected from speaker terminals to the PCB should be twisted if possible for the same reason.

12.1.1 Capacitor Value Impact on Power Consumption

The filter capacitor can have a significant impact on the MA2306DNS power consumption and must be of relatively low capacitance value, e.g. 220 pF-470 pF for minimal impact. For a 220 pF capacitor on each output channel in a BTL configuration results in approximately 10-20 mW additional power consumption at idle operation. Higher capacitance values will increase power consumption further, but also provide a lower corner frequency with improved suppression of EMI. The capacitor value should be balanced for the target application, however, no more than 1 nF should be used.

12.1.2 Ferrite Filter Selection

The most important factor in EMI suppression is the output filter ferrite bead. Ferrite bead performance may vary greatly in terms of effective frequency region and suppression magnitude. This means that one ferrite part cannot necessarily replace another directly, and must be tested at an EMC lab for verification of compliance with regulations. An important characteristic is saturation current of ferrite material, which must comply with the maximum application output current in order to be effective at high output levels. Ferrites in 0805/1206 SMD packages will usually provide sufficient specifications. The NFZ-series from Murata yields good results, e.g. NFZ2MSD301SZ10L and NFZ2MSD150SN10L.

12.1.3 Ferrite Filter Stability Under Light Loads

Operating the MA2306DNS under very light output loads above 500 Ω can result in the amplifier's feedback loop becoming unstable, which can be a real scenario if the load is planned to be disconnected from time to time. If the load is planned to be disconnected during normal operation, it is recommended to use an RC damping network (snubber) similar to the damping network using an LC filter (Refer to Section 12.1.4). Starting point RC values can be $R < 500 \Omega$ and $C = 22 \text{ nF}$ but they need to be tuned to the specific application. The RC network will help maintain loop stability when the load is removed.

12.1.4 LC filter options

MA2306DNS can also operate with a LC filter for even higher EMI suppression. An LC filter can provide additional suppression of EMI, but will usually be higher cost and footprint size on board than a ferrite filter.

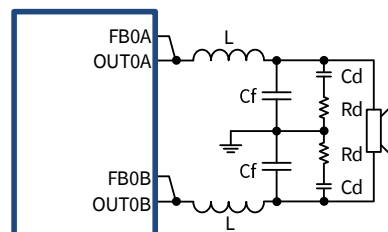


Table 13: LC filter schematic

The LC filter has to be carefully designed and tested to properly avoid instability with MA2306DNS. Stability issues can occur if the filter corner frequency is too low and non-sufficient EMI suppression may occur if the corner frequency is too high. The LC filter should consist of a filtering part (L and Cf) and a damping network (Cd and Rd) as shown in Figure 13. Typical recommended LC filter component values are shown in Table 14.

Table 14: Recommended LC filter component values

Design	L	Cf	Cd + Rd
#1	3.3 μH	33 nF	82 nF + 15 Ω
#2	4.7 μH	47 nF	470 nF + 10 Ω
#3	6.8 μH	33 nF	220 nF + 22 Ω
#4	10 μH	220 nF	1 μF + 10 Ω

Refer to MA2306DNS application notes for more information and EMI measurement results.

12.2 Thermal Design

The MA2306DNS is designed to be used in applications without external heatsink. A well-designed 4-layer PCB can act as a heatsink. The bottom thermal pad (EPAD) of the IC package should be thermally connected to the top layer copper with as many vias as possible to the other layers. It is recommended to keep routed traces in the middle layers to a minimum, avoiding any routing at all if possible. Let the bottom layer only be used for routing traces between layers. Deadspace in all layers should be filled with copper connected to ground to maintain unhindered thermal flow away from the IC. Refer to Figure 12.6 for PCB layout reference.

Heat is generated primarily in the on-resistance of the internal MOSFETs, as well as the bond wires from the silicon to the IC pins, and will be dependent on load current. The losses due to heat will be more severe with lower load impedances, as conduction losses in the IC will dominate with increasing current.

12.3 Start-up Procedure

The recommended procedure for proper start-up of the device:

1. Keep the device disabled and muted: ENABLE = 0, NMUTE = 0.

2. Ensure MSEL, AD0 and AD1 pins are configured correctly.
3. Enable VDD, VDD_IO and PVDD supplies and wait for them to become stable.
4. Ensure I2S bit clock and frame clock are present.
5. Enable device: ENABLE = 1.
6. Wait T_{ENABLE} until the device has started up in order to read the NERR pin status and start communicating with I2C.
7. Program/initialize the device via I2C (if needed)
8. Unmute device: NMUTE = 1. When NMUTE time has elapsed, the device is ready for audio playback.
9. The device is now in normal operation state (idle) and ready to play audio.

12.4 Procedure for handling discontinuous audio clock

In some applications the audio clocks may be stopped by the transmitter side from time to time, which will also halt the MA2306DNS audio playback. When the clocks return, MA2306DNS will continue operation once the PLL has locked again. MA2306DNS is designed to handle loss of clocks without any audio artifacts without muting. For optimal performance, it is recommended to follow this procedure:

1. The device is in normal operation and audio clocks are present.
2. Mute the device: NMUTE=0. Alternatively, put the device in **standby** mode.
3. Disable the audio clocks from the transmitting side. The device is now only operational through I2C. PLL error is reported to the error register internally.
4. When audio playback is required again, enable the audio clocks, wait for the PLL to lock and the device to be fully operational again (see timing for T_{ENABLE})
5. Unmute the device: NMUTE=1. Alternatively, put the device out of **standby** mode.
6. The device is now in normal operation again and ready to play audio.

12.5 Power-down Procedure

The recommended procedure for proper power-down described below:

1. The device is in normal operation state.
2. Mute device: NMUTE = 0.
3. Disable device: ENABLE = 0.

4. The device is now in power-down state.
5. (Optional: Bring down VDD, VDD_IO and PVDD supplies.)

12.6 Recommended Layout

The recommended application/PCB layout is shown in Figure 12.6:

- **Decoupling:** Decoupling capacitors for power supplies VDD, AVDD_REG, DVDD_REG, CD_DIG, PVDD and VDD_IO must be kept as close to the device as possible. The smallest value capacitors should be placed closest to the device to handle fast transients.
- **Fly-caps:** Flying capacitors for VFCxxx pins must be kept as close to the device as possible and care must be taken to keep the current loop tight and short to ensure multilevel switching stability.
- **PCB layers:** A PCB with four layers is recommended to achieve power output performance stated in the electrical characteristics. Via stitching/array between board layers is encouraged on the ground net (GND), especially below the bottom thermal pad of the device which uses the PCB as a heatsink to dissipate heat. In general, the unused copper (deadspace) in all layers should be connected to ground for optimal thermal and EMI performance. Avoid breaking up the ground planes with any routing traces in all layers as much as possible to ensure good thermal connection throughout all PCB layers.
- **Output filter:** The traces from the output to the filter should be kept as short as possible for optimal EMI performance.
- **RC filter on I2S:** Digital audio/control lines (I2S/I2C) can have an impact on EMI performance. It is suggested to implement a RC first order lowpass filter close to the source on these lines to slow the transients and hence avoiding high frequency EMI. Values for the resistor and capacitor in the lowpass filter will be application dependent, but a good starting point could be 33 Ω and 180 pF.
- **Output cables placement:** Keep output speaker terminals/cables on the opposite side of the PCB from PVDD for EMI reasons. Radiated emission from the output switching waveform can couple from the output cables to the PVDD traces/cables and influence conducted emission performance significantly.

12.7 Evaluation Board as Reference

The EVAL_AUD_MA2306DNS_DUO evaluation board can be used as reference when designing an application. The evaluation board layout has specifically been optimized to achieve best possible thermal performance without an external heatsink. Refer to Figures 12.2 through 12.5 and/or refer to design files on [infineon.com](https://www.infineon.com)

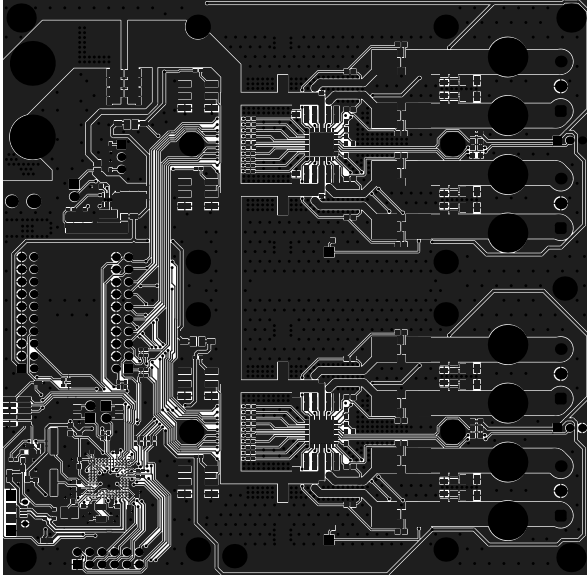


Figure 12.2: Top Layer

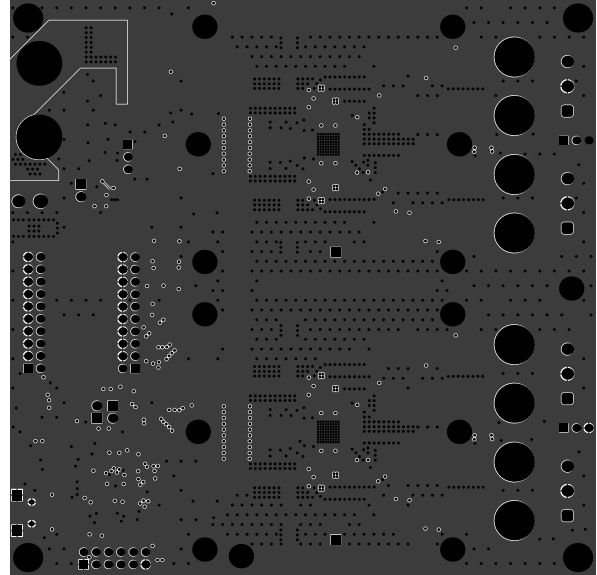


Figure 12.3: Mid Layer 1

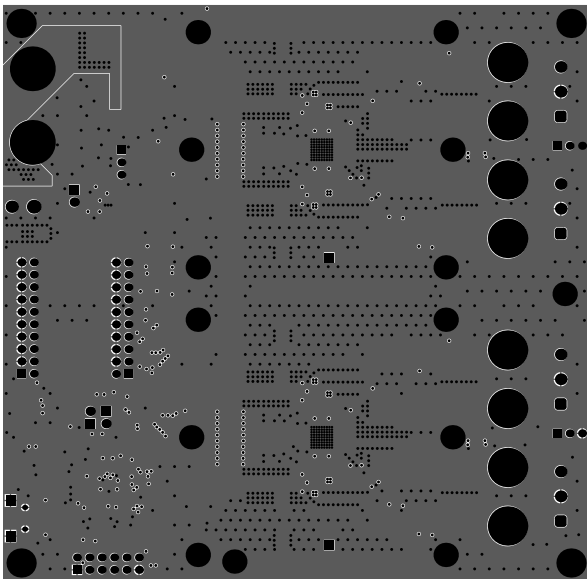


Figure 12.4: Mid Layer 2

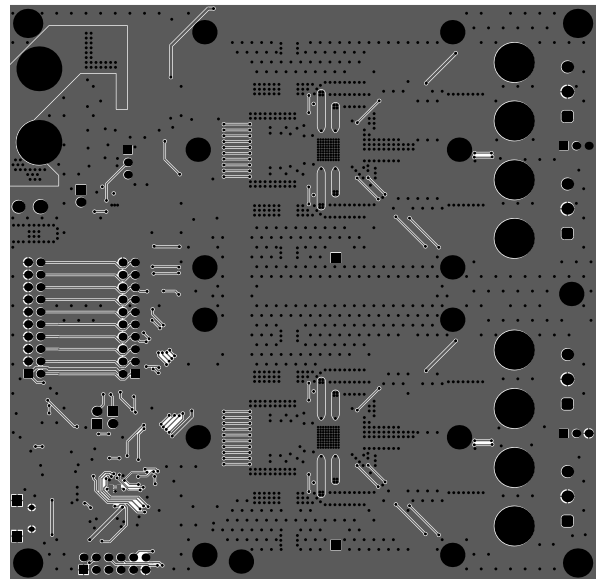
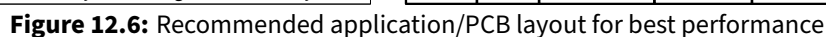


Figure 12.5: Bottom Layer



13 Application Examples

13.1 22V Max. PVDD Simple Amplifier Driving 6Ω

Refer to Figure 13.1 for schematic. Intended for a simple stereo implementation without DSP/I2C functionality driving two medium-range loudspeakers. The amplifier powers up with default settings. NMUTE and ENABLE are controlled with simple hardware high/low voltages, e.g. from basic BT module or switches. The output filter is using ferrite beads which requires the speaker cables to be relatively short and preferably twisted to reduce emissions.

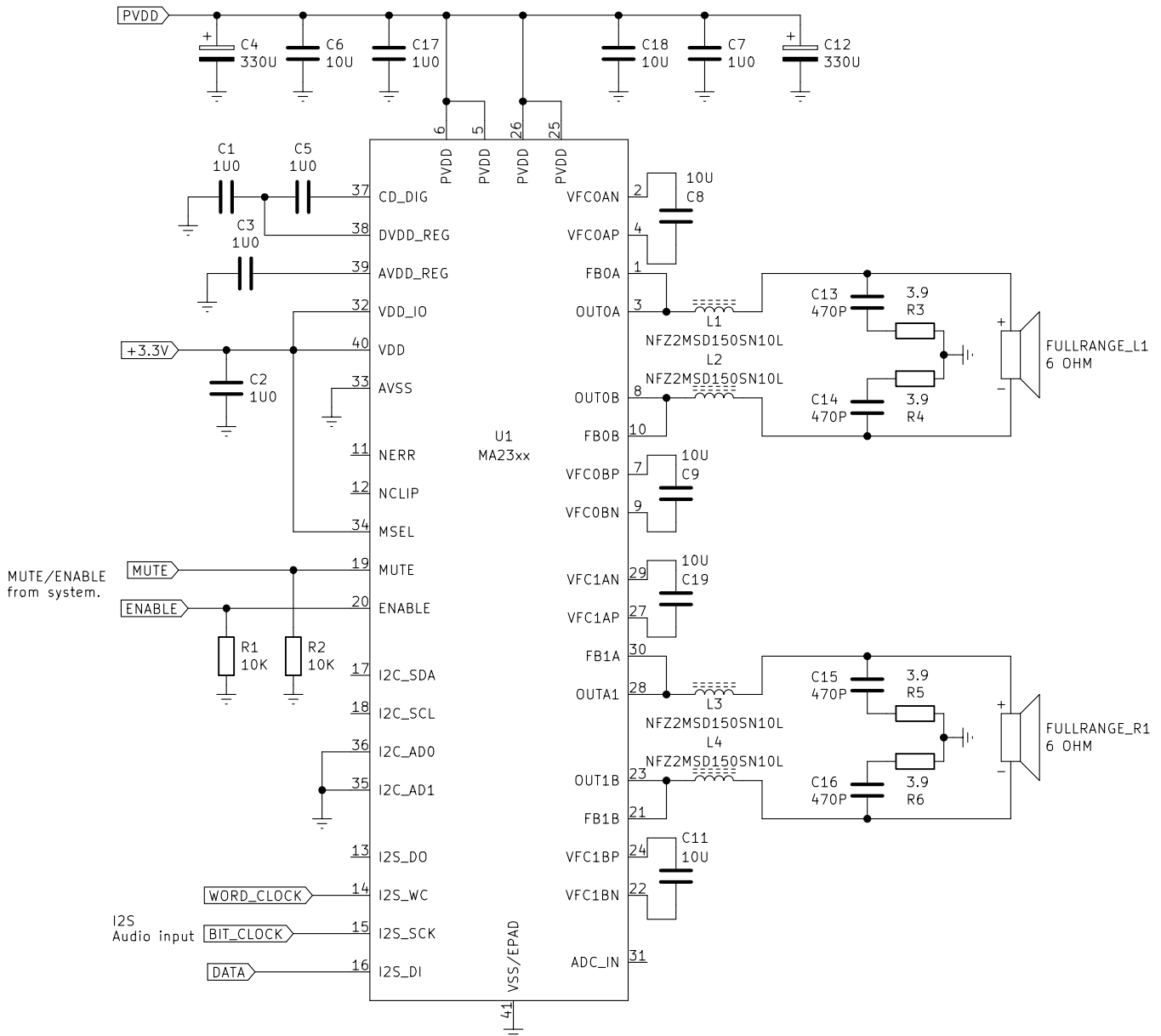


Figure 13.1: Application schematic for a 22 V simple amplifier driving 6Ω

Designator	Description	Manufacturer	Part number	Comment
C4,C12	Electrolytic cap, 330 μ F, 35 V.	Vishay / BC Components	MAL215099003E3	Medium ripple current, bulk capacity.
C8,C9, C10,C11,	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X5R, 25V, 0805	MURATA	GRM21BR61E106KA73K	Low ESR. De-rate capacity at working voltage.
C6,C18	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X5R, 50V, 0805	MURATA	GRM21BR61H106KE43L	Low ESR. De-rate capacity at working voltage.
C1,C2,C3,C5	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 10V, 0603	YAGEO	CC0603KRX5R6BB105	Close to device supply pins decoupling, low ESR.
C7, C17	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 50V, 0603	TDK	C1608X5R1H105K080AB	Close to device supply pins decoupling, low ESR.
C13,C14,C15, C16	Ceramic Cap, 470 pF, $\pm$ 10 percent, X7R, 50V, 0402	MURATA	GRM155R71H471KA01J	Output filter.
R1,R2	Resistor, 10 kohm, 62.5 mW, $\pm$ 5 percent, 0402	VISHAY	CRCW040210K0JNED	Pull-down.
R3,R4,R5,R6	Resistor, 3.9 ohm, 250 mW, $\pm$ 1 percent, 0603	VISHAY	RCS06033R90FKEA	Output filter.
L1,L2,L3,L4	Ferrite Bead, 200 ohm @ 100 MHz, 4.4A, 0806	MURATA	NFZ2MSD150SN10L	Output filter ferrite. Observe audio THD at saturation.
U1	Multilevel Class D amplifier, MA2306xNS, 2 x 63W	INFINEON	MA2306xNS	Amplifier device.

Figure 13.2: Bill of Materials for [13.1](#)

13.2 24V Max. PVDD Simple Amplifier Driving 4Ω

Refer to Figure 13.3 for schematic. Intended for a simple stereo implementation without DSP/I2C functionality driving two full-range loudspeakers. The amplifier powers up with default settings. NMUTE and ENABLE are controlled with simple hardware high/low voltages, e.g. from basic BT module or switches. The output filter is using ferrite beads which requires the speaker cables to be relatively short and preferably twisted to reduce emissions.

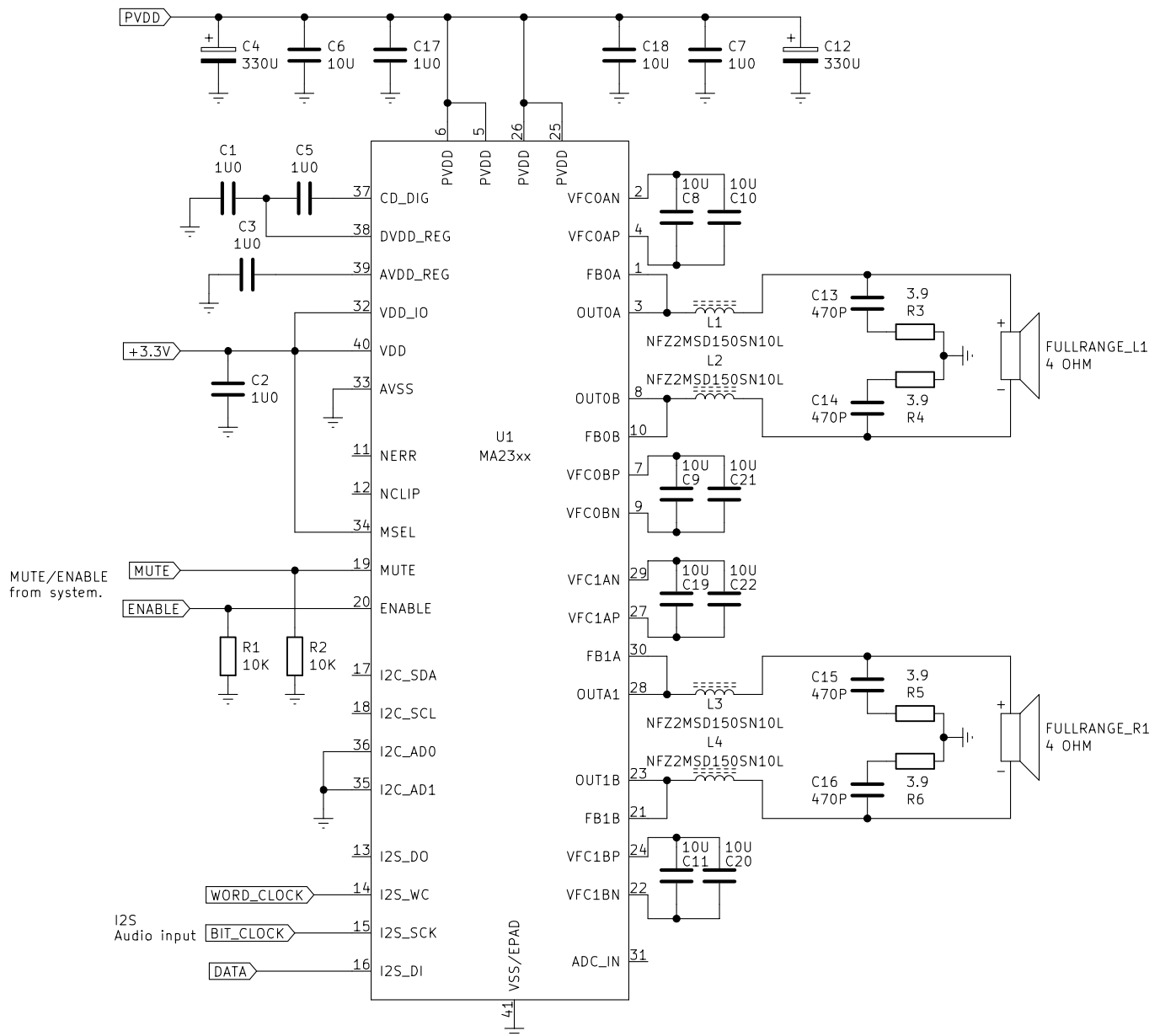


Figure 13.3: Application schematic for a 24 V simple amplifier driving 4Ω

Designator	Description	Manufacturer	Part number	Comment
C4,C12	Electrolytic cap, 330 μ F, 35 V.	Vishay / BC Components	MAL215099003E3	Medium ripple current, bulk capacity.
C8,C9, C10,C11,C19,C20,C21,C22	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X5R, 25V, 0805	MURATA	GRM21BR61E106KA73K	Low ESR. De-rate capacity at working voltage.
C6,C18	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X5R, 50V, 0805	MURATA	GRM21BR61H106KE43L	Low ESR. De-rate capacity at working voltage.
C1,C2,C3,C5	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 10V, 0603	YAGEO	CC0603KRX5R6BB105	Close to device supply pins decoupling, low ESR.
C7, C17	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 50V, 0603	TDK	C1608X5R1H105K080AB	Close to device supply pins decoupling, low ESR.
C13,C14,C15, C16	Ceramic Cap, 470 pF, $\pm$ 10 percent, X7R, 50V, 0402	MURATA	GRM155R71H471KA01J	Output filter.
R1,R2	Resistor, 10 kohm, 62.5 mW, $\pm$ 5 percent, 0402	VISHAY	CRCW040210K0JNED	Pull-down.
R3,R4,R5,R6	Resistor, 3.9 ohm, 250 mW, $\pm$ 1 percent, 0603	VISHAY	RCS06033R90FKEA	Output filter.
L1,L2,L3,L4	Ferrite Bead, 200 ohm @ 100 MHz, 4.4A, 0806	MURATA	NFZ2MSD150SN10L	Output filter ferrite. Observe audio THD at saturation.
U1	Multilevel Class D amplifier, MA2306xNS, 2 x 63W	INFINEON	MA2306xNS	Amplifier device.

Figure 13.4: Bill of Materials for 13.3

13.3 26V Max. PVDD High Current Amplifier Driving 2Ω with Host MCU

Refer to Figure 13.5 for schematic. High-power application with host MCU and LC output filter, for driving a single full-range loudspeaker or subwoofer. A DSP program for loudspeaker frequency response correction or sound enhancements can be written by the host MCU via the I2C communication line. Amplifier I2C address is hardwired by AD0 and AD1 pins to 0x20 (both pins connected to ground). If multiple devices are on the same I2C bus, the AD0/AD1 pins should be configured so that all devices have unique addresses. The NERR pin is used as an interrupt pin for the MCU signaling if the amplifier is in an error state. NMUTE and ENABLE pins are controlled by the MCU and pulled low through resistors, disabling and muting the amplifier by default. Fly-cap capacitors should be low ESR and adequately de-rated to maintain capacity.

Relevant register settings:

- Error registers reset at start-up [reg.errTrig_reset](#) to make sure error registers are nulled before reading.
- Error register [errVect_acc.errVector_ch0/1](#) is read whenever MCU senses that NERR pin becomes low.
- Continuously monitor device temperature with [temp_chip](#) and reduce volume in [volume_ch0/1](#) if temperature becomes too high due to the low impedance load.
- Put the device in standby mode for low power consumption when not playing audio. Standby mode is set by first muting the output (NMUTE pin pulled low by MCU) and then enabling the [standby](#) register. Vice versa for exiting standby mode.

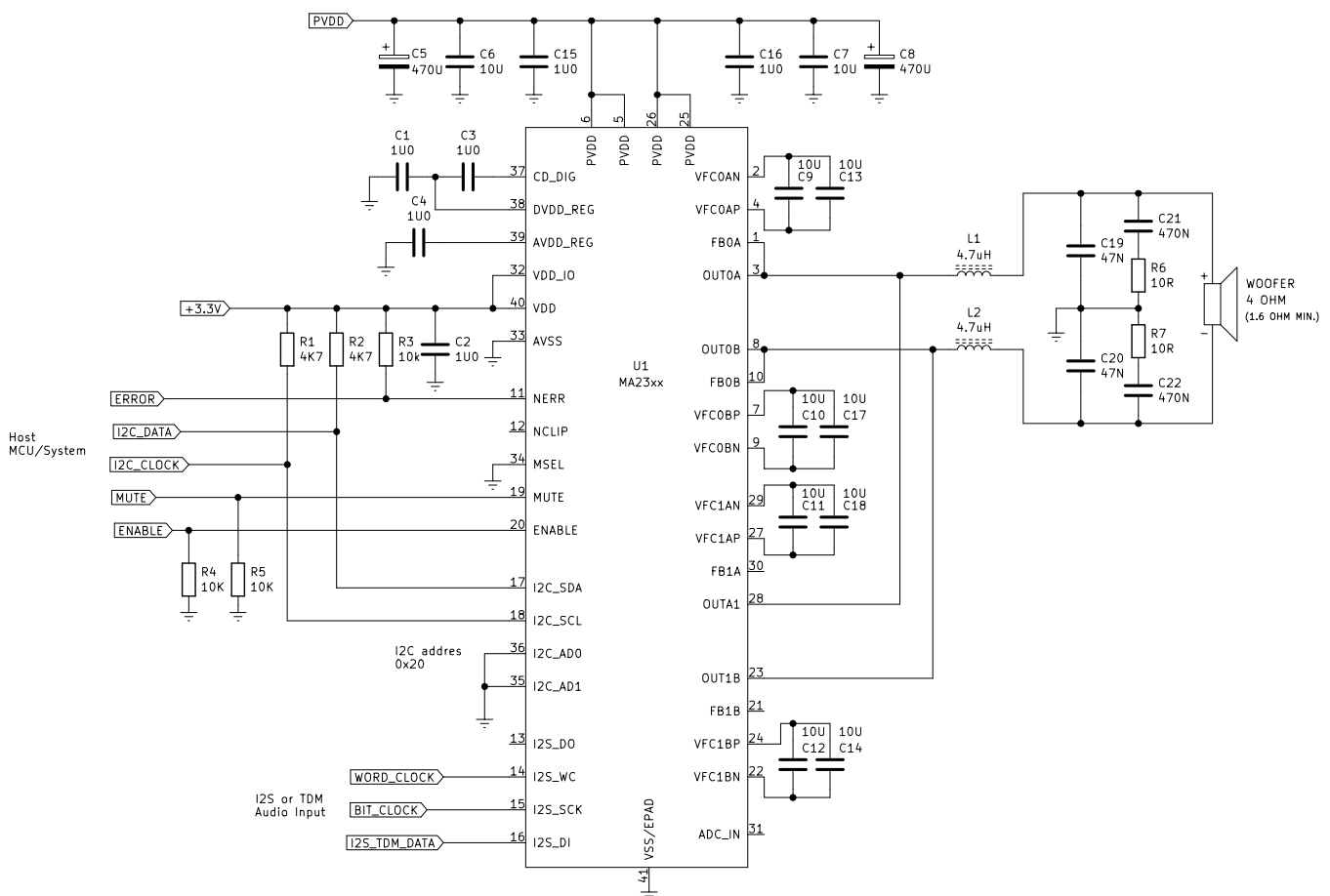


Figure 13.5: Application schematic for a 26V Max. PVDD high current amplifier

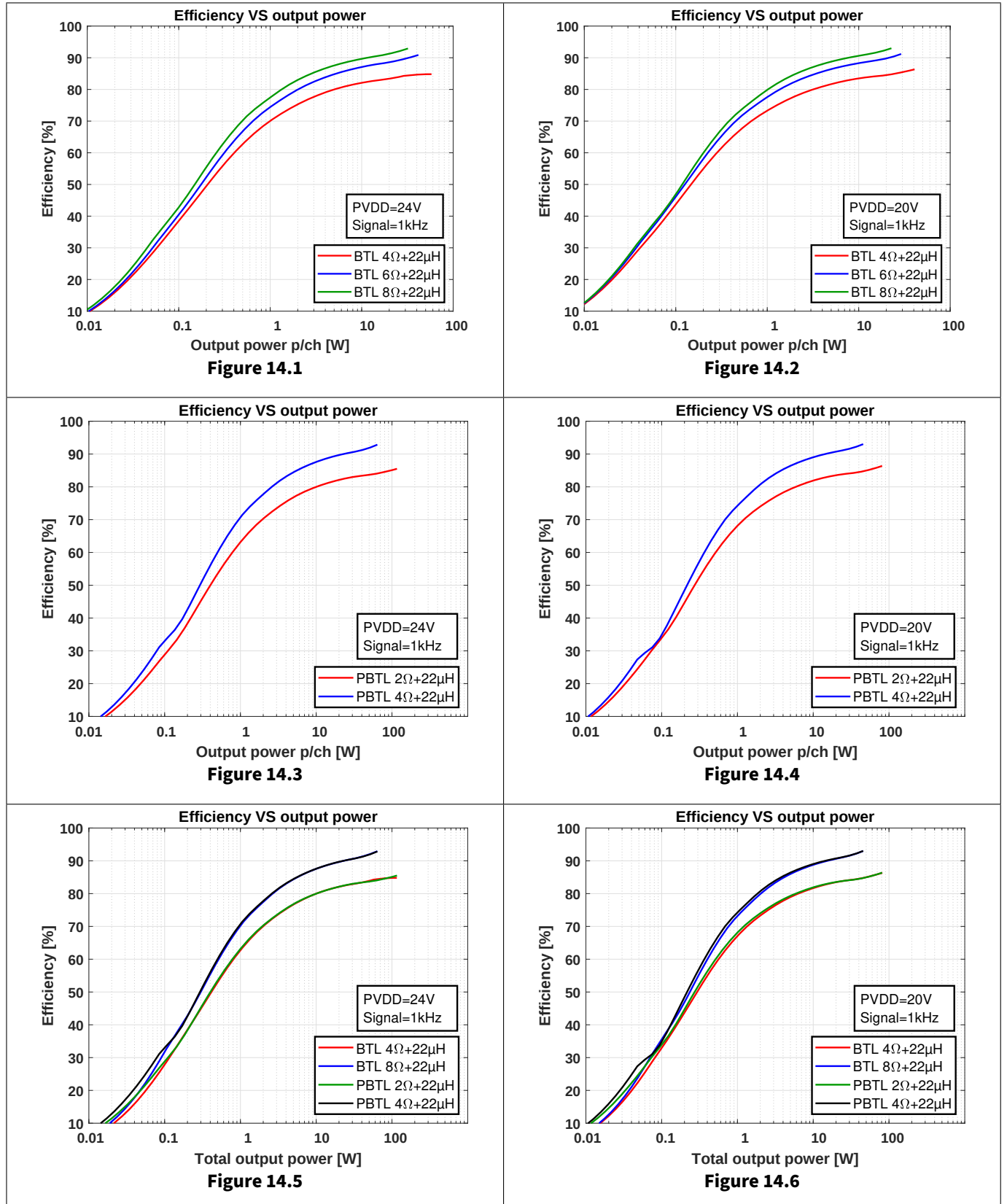
Designator	Description	Manufacturer	Part number	Comment
C5,C8	Electrolytic cap, 470 μ F, 35 V.	Vishay / BC Components	EEV-FK1V471Q	Medium ripple current, bulk capacity.
C9, C10, C11, C12, C13, C14, C17, C18	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X7R, 25V, 1206	MURATA	GRM31CR71E106KA12L	Low ESR. De-rate capacity at working voltage.
C6,C7	Ceramic Cap, 10 μ F, $\pm$ 10 percent, X5R, 50V, 0805	MURATA	GRM21BR61H106KE43L	Low ESR. De-rate capacity at working voltage.
C1,C2,C3,C4	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 10V, 0603	YAGEO	CC0603KRX5R6BB105	Close to device supply pins decoupling, low ESR.
C15, C16	Ceramic Cap, 1 μ F, $\pm$ 10 percent, X5R, 50V, 0603	TDK	C1608X5R1H105K080AB	Close to device supply pins decoupling, low ESR.
C19,C20	Ceramic Cap, 47 nF, $\pm$ 10 percent, X7R, 50V, 0603	KEMET	C0603C473K5RACTU	Output filter.
C21,C22	Ceramic Cap, 470 nF, $\pm$ 10 percent, X7R, 50V, 0805	KEMET	C0805X103K5RAC3316	Output filter.
R6,R7	Resistor, 10 ohm, 250 mW, $\pm$ 1 percent, 0805	BOURNS	CRS0805-FX-10R0ELF	Output filter.
L1,L2	Inductor, 4.7 μ , 6.3A, 8mm x 8mm	MURATA	1217AS-H-4R7N	Output filter Inductor. Observe audio THD at saturation.
R1, R2	Resistor, 4.7 kohm, 62.5 mW, $\pm$ 5 percent, 0402	VISHAY	CRCW04024K70JNED	I/O pull-up.
R3,R4,R5	Resistor, 10 kohm, 62.5 mW, $\pm$ 5 percent, 0402	VISHAY	CRCW040210K0JNED	Pull-down.
U1	Multilevel Class D amplifier, MA2306xNS, 2 x 63W	INFINEON	MA2306xNS	Amplifier device.

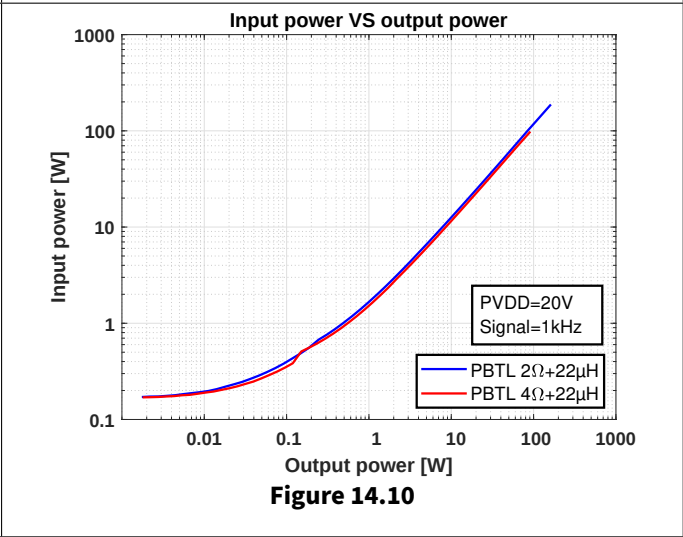
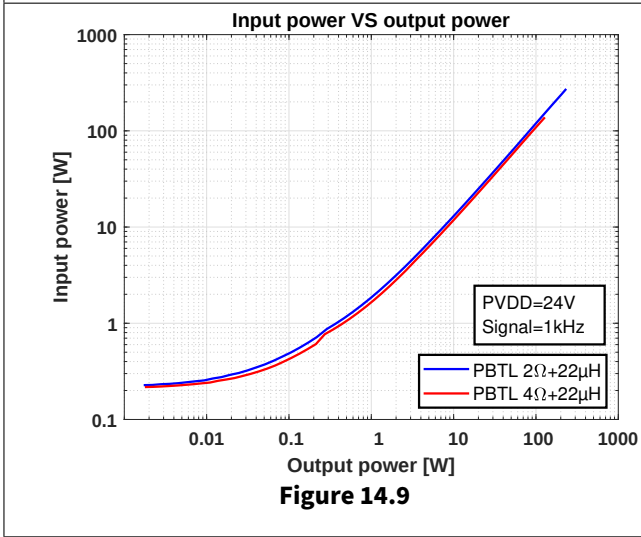
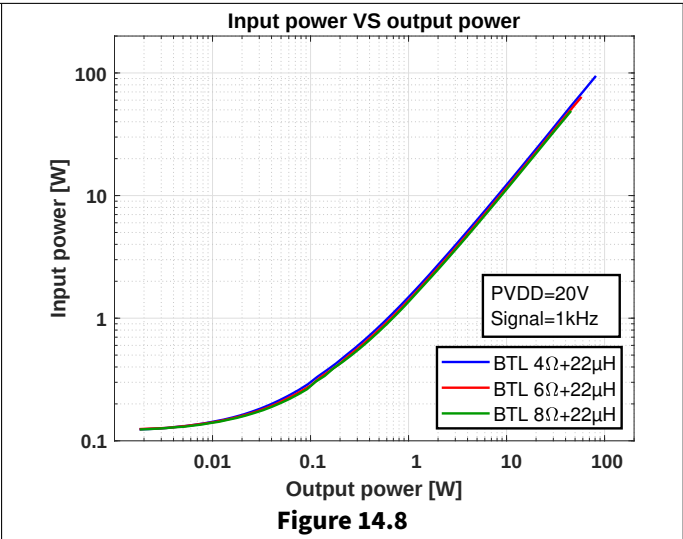
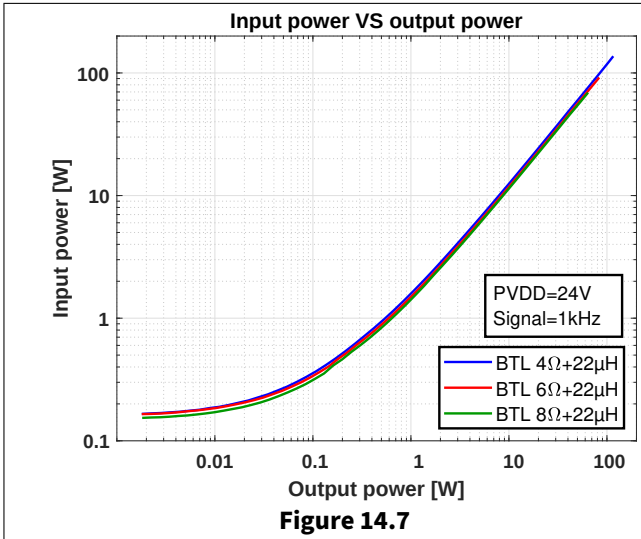
Figure 13.6: Bill of Materials for 13.5

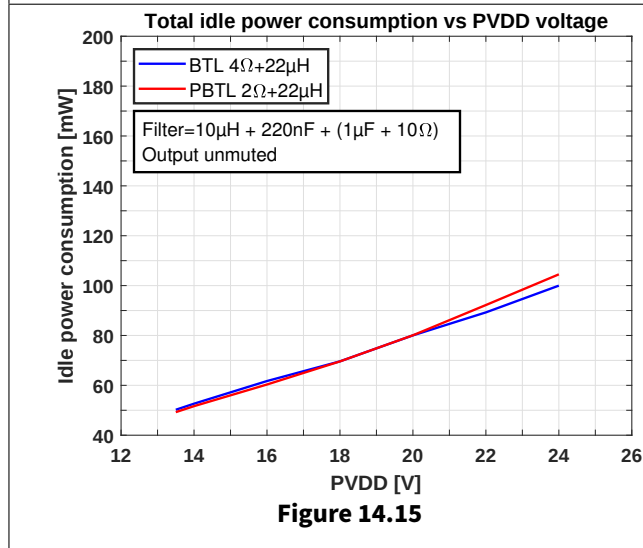
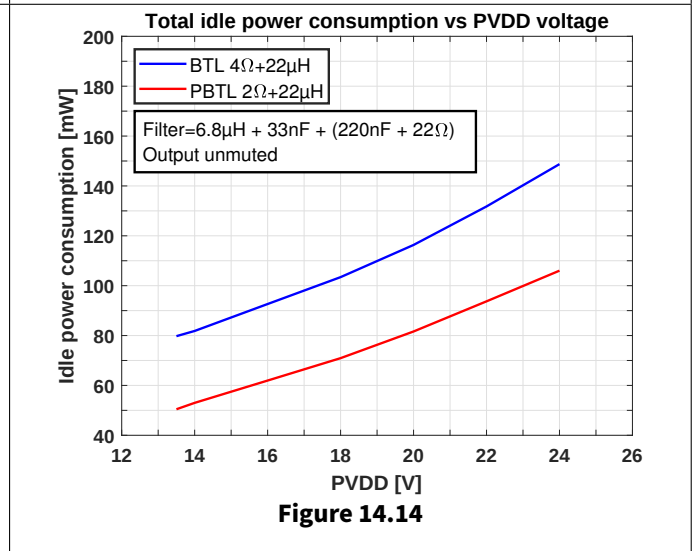
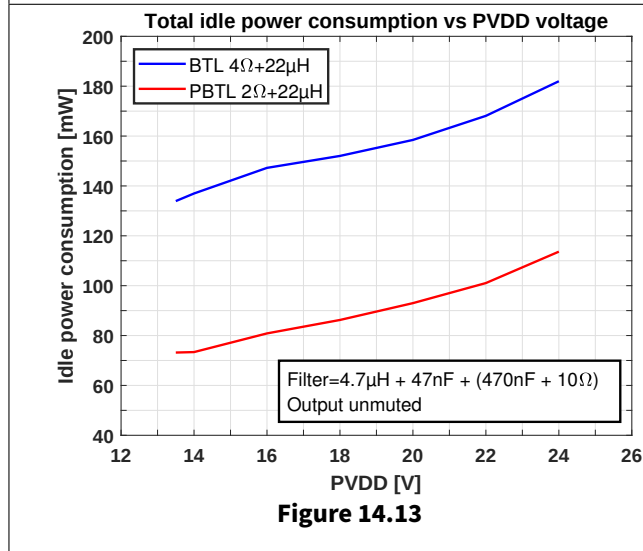
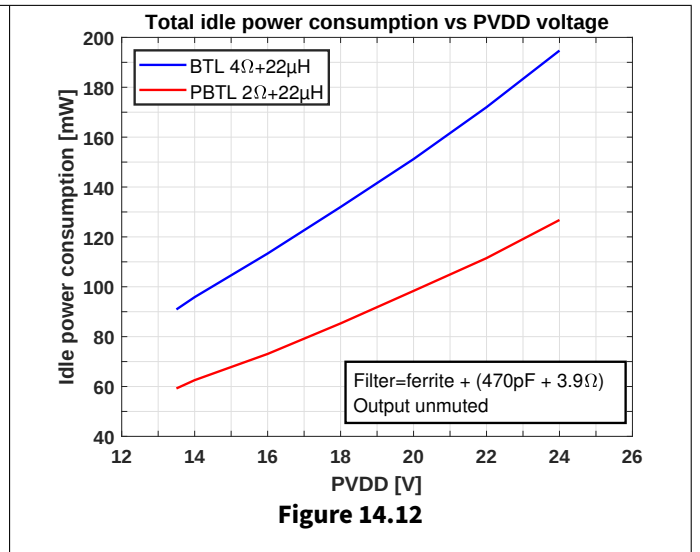
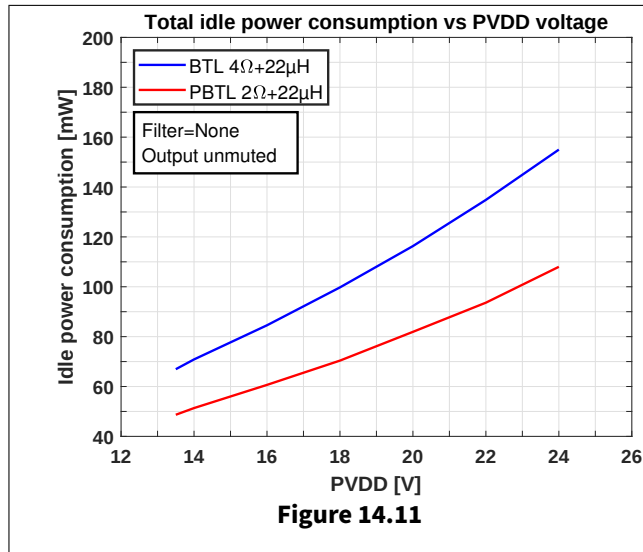
14 Typical Characteristics

Note that some characteristics are based on interpolated/averaged data.

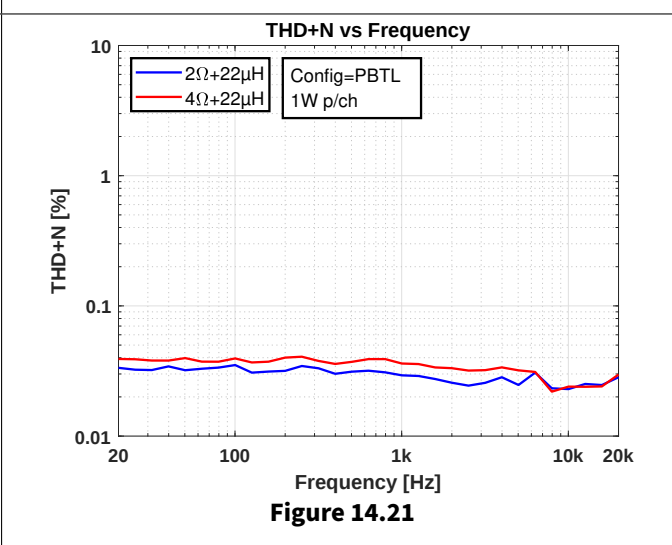
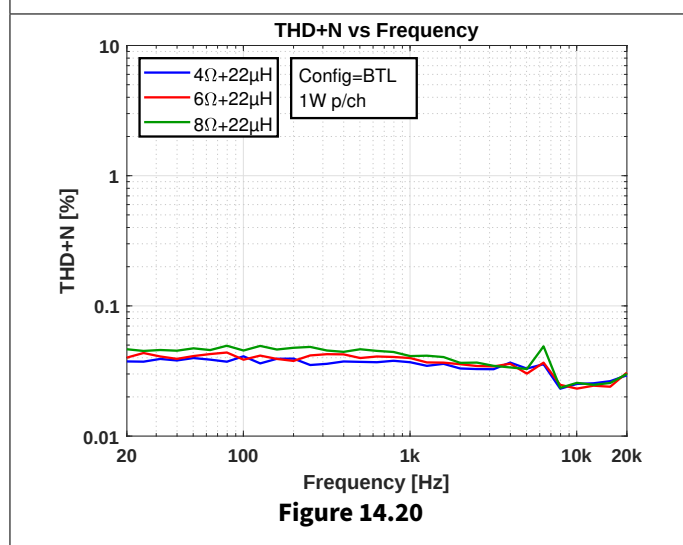
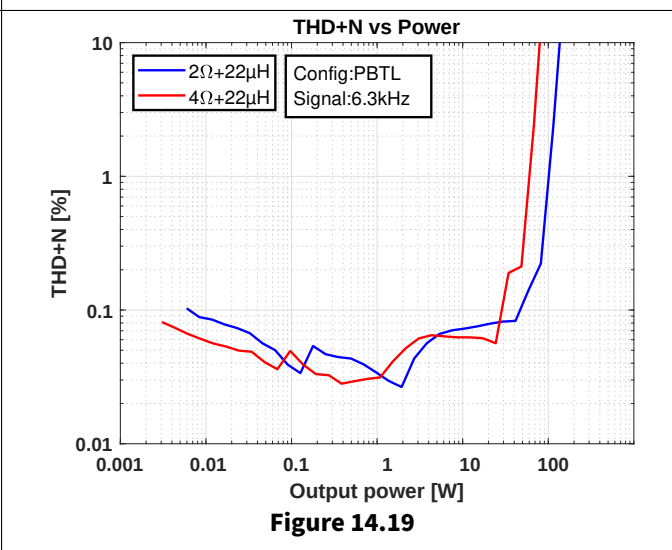
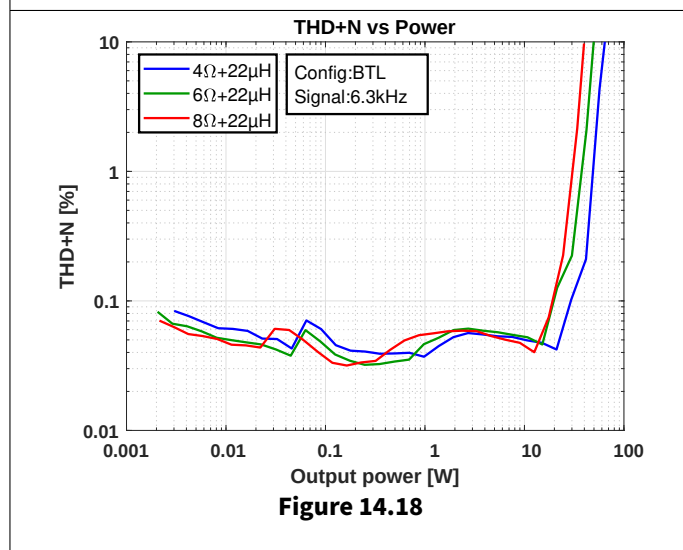
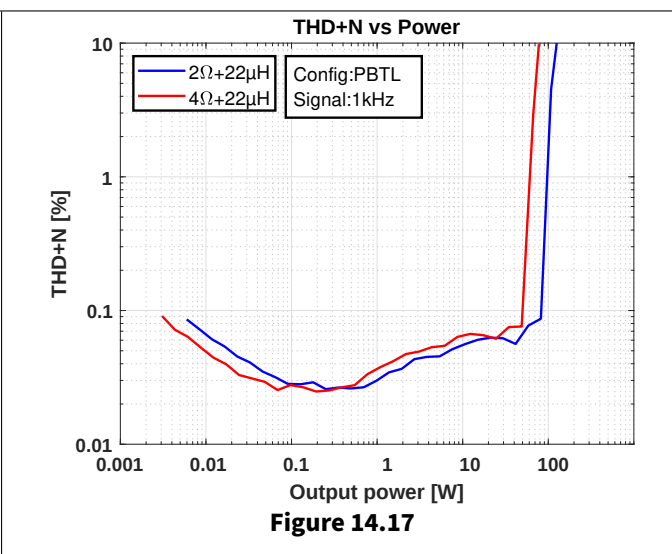
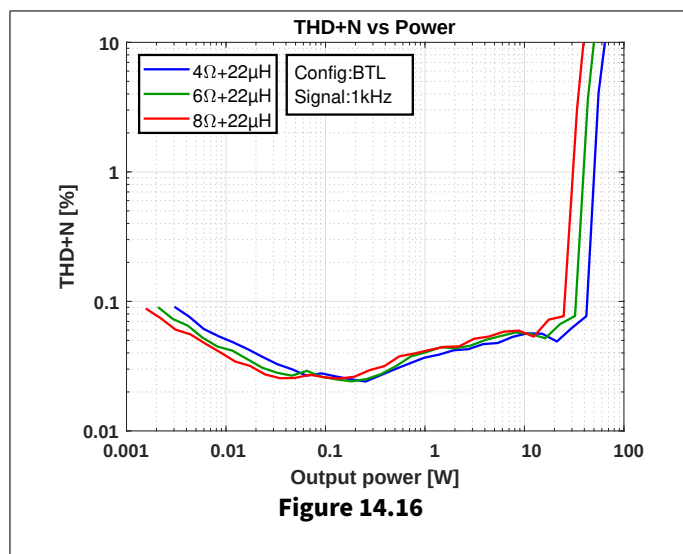
14.1 Efficiency and power consumption





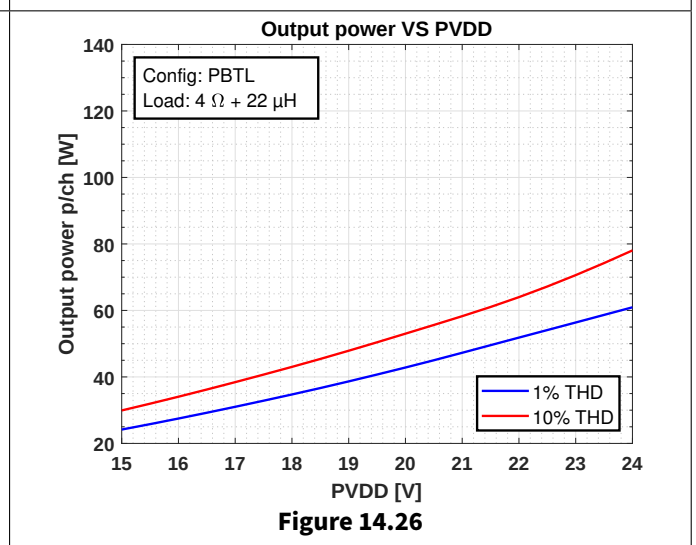
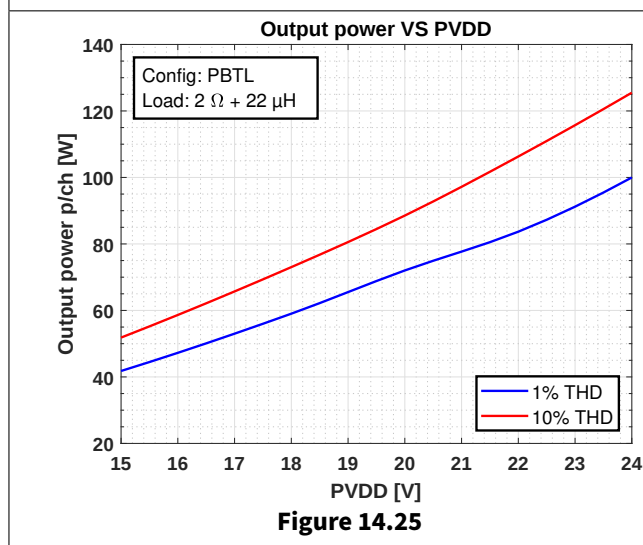
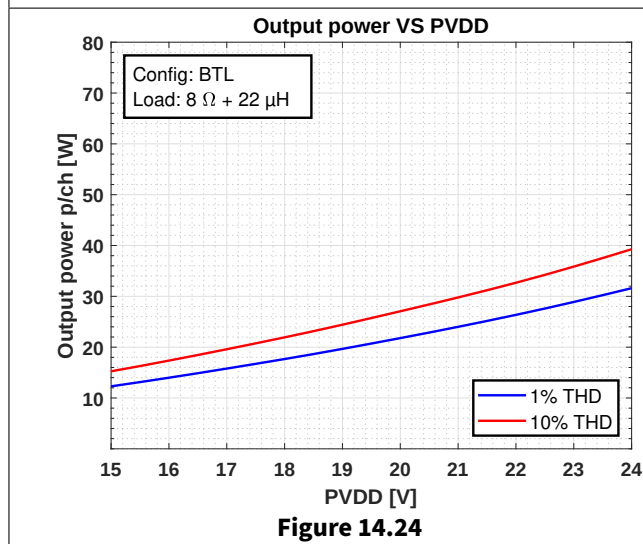
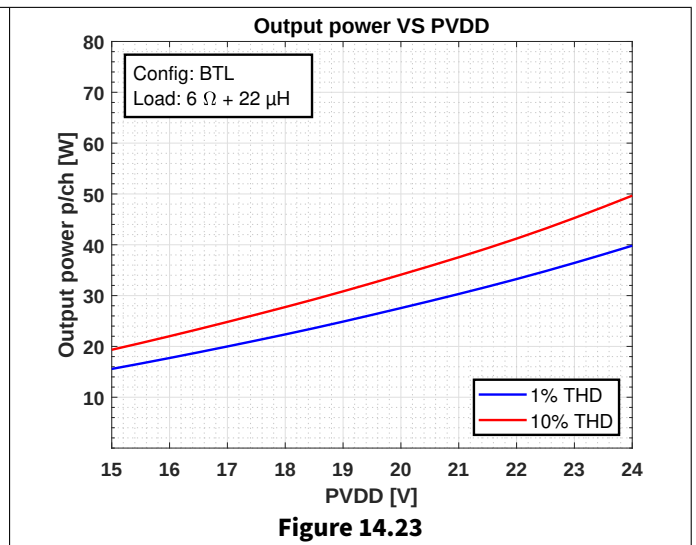
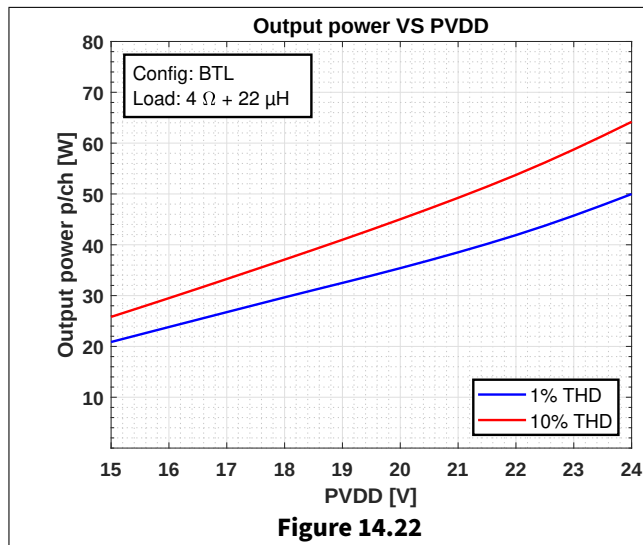


14.2 Audio performance



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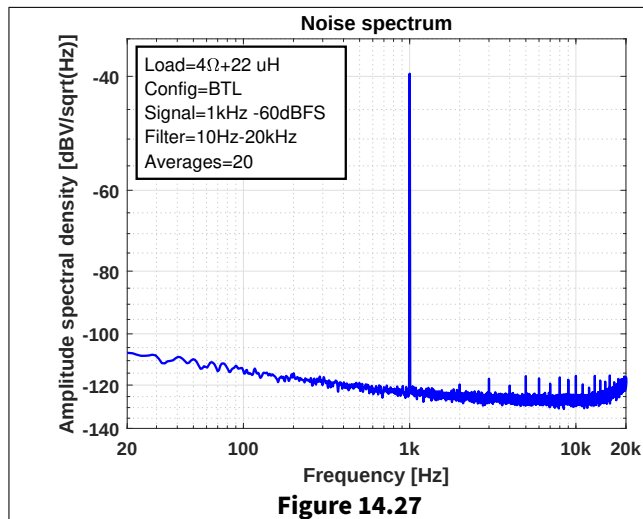


Figure 14.27

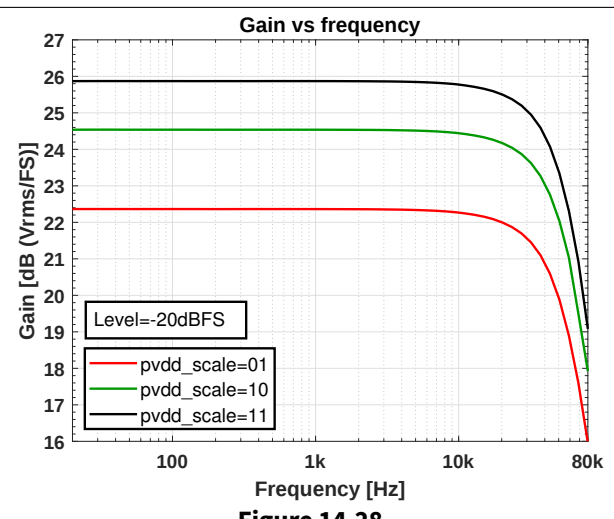


Figure 14.28

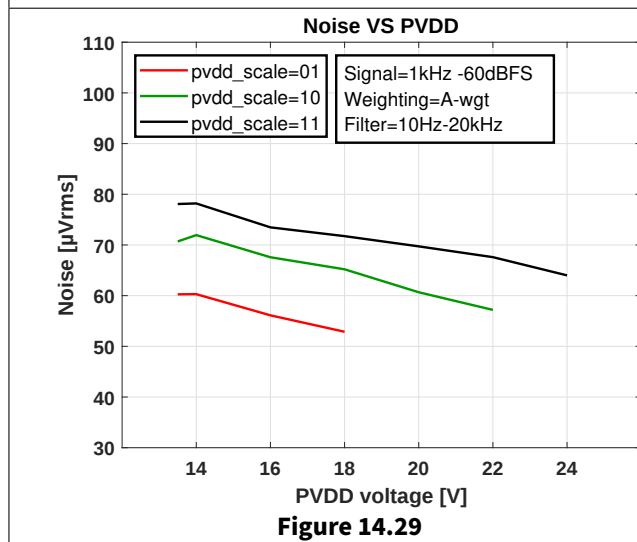


Figure 14.29

15 Register map

Legend:

Red: Bits in the register which correspond to the specific Name/Function.

pa					
Address	Reset	Name/Function	Bits	Value	Description
0x0000	0x30	mode_pbtl	3	00110000	Output channel configuration 0: BTL mode 1: PBTL mode
		pvdd_scale	5:4	00110000	Gain scaling. 01: Optimized for PVDD=16V 10: Optimized for PVDD=20.5V 11: Optimized for PVDD=24V
		msel_reg_ctrl	6	00110000	Override pin/hardware programmed settings with register settings 0: Hardware settings are chosen 1: Register settings are chosen
0x0001	0x03	gd_dVdt	1:0	00000011	Gate drive strength (dV/dt) 00: Lowest 01: Low 10: High 11: Highest
0x0002	0x00	mute_ch0	0	00000000	Mute channel 0 (mute_source must be set first) 0: Unmute 1: Mute
		mute_ch1	1	00000000	Mute channel 1 (mute_source must be set first) 0: Unmute 1: Mute
		disable_ch0	2	00000000	0: Channel 0 is enabled 1: Channel 0 is disabled
		disable_ch1	3	00000000	0: Channel 1 is enabled 1: Channel 1 is disabled
		standby	4	00000000	0: Disable standby 1: Enable standby
		mute_source	5	00000000	Select source for the internal mute signal 0: NMUTE pin 1: mute_ch0/1 register settings
		nmute_action	6	00000000	Select action when NMUTE pin is asserted; 0: mute amplifiers, 1: device standby
0x0003	0x20	volume_ch0	7:0	00100000	Channel 0 volume setting. Step size: -0.75 dB per register value increment. 0x00: +24 dB 0x01: +23.25 dB .. 0x1F: +0.75 dB 0x20: +0.00 dB (default) 0x21: -0.75 dB .. 0xFF: -167.25 dB
0x0004	0x20	volume_ch1	7:0	00100000	Channel 1 volume setting. See volume_ch0 for more information.
0x0005	0x00	dsp_enable	1	00000000	Enable digital audio processor (DSP) 0: DSP disabled 1: DSP enabled
		dsp_bypass	3	00000000	Audio routing bypasses DSP 0: Audio is routed through DSP 1: Audio is routed directly to amplifier

		vol_instant	0	00000000	Volume control ramp disable 0: Volume is ramped 1: Volume is applied instantly - no ramp
		gpio_sync_zclip	4	00000000	NCLIP pin function select 0: NCLIP is output pin indicating amp clipping 1: NCLIP pin is used for inter-IC PWM synchronization (use sync_in_enable and sync_out_enable registers to select if NCLIP is input/output)
0x0006	0x00	clip_pin	0	00000000	State of the clip signal driving the NCLIP pin (read-only) 0: No clipping 1: Clipping
		err_pin	1	00000000	State of the error signal driving the NERR pin 0: No error 1: Error
0x0007	0x00	adc_pin	7:0	00000000	ADC reading from ADC_IN pin spanning between 0 V (min) and 1 V (max)
0x0008	0x00	temp_chip	7:0	00000000	Read internal temperature sensor. Resolution is 1 °C per increment with 0x00=-50 °C
0x0009	0x00	pvdd_chip	7:0	00000000	Read internal PVDD sensor. Resolution is 125 mV per increment
0x000B	0x00	attack_ch1	4:0	00000000	Channel 1 attack time for peak limiter (ROM code). Sample rate dependent. At 48 kHz: 0x00: 0 ms/10 dB (default) 0x08: 1 ms/10 dB 0x09: 2 ms/10 dB 0x0A: 4 ms/10 dB 0x0B: 8 ms/10 dB 0x0C: 16 ms/10 dB 0x0D: 32 ms/10 dB 0x0E: 64 ms/10 dB 0x0F: 128 ms/10 dB
0x000A	0x00	attack_ch0	4:0	00000000	Channel 0 attack time for peak limiter (ROM code). See attack_ch0 for more information.
0x000C	0x12	release_ch0	4:0	00010010	Channel 0 release time for peak limiter (ROM code). Sample rate dependent. At 48 kHz: 0x0C: 16 ms/10 dB 0x0D: 32 ms/10 dB 0x0E: 64 ms/10 dB 0x0F: 128 ms/10 dB 0x10: 256 ms/10 dB 0x11: 512 ms/10 dB 0x12: 1024 ms/10 dB (default) 0x13: 2048 ms/10 dB
0x000D	0x12	release_ch1	4:0	00010010	Channel 1 release time for peak limiter (ROM code). See release_ch0 for more information.
0x000E	0x00	threshold_ch0	7:0	00000000	Channel 0 threshold for peak limiter (ROM code). Step size: -0.75 dB per register value increment. 0x00: +24 dB 0x01: +23.25 dB .. 0x1F: +0.75 dB 0x20: +0.00 dB (default) 0x21: -0.75 dB .. 0xFF: -167.25 dB

0x000F	0x00	threshold_ch1	7:0	00000000	Channel 1 threshold for peak limiter (ROM code). See threshold_ch0 for more information.
i2s_tdm					
Address	Reset	Name/Function	Bits	Value	Description
0x0010	0x10	data_alignment	1:0	00010000	I2S/TDM data alignment 00: I2S 01: Left Justified 10: Right Justified
		sck_pol	4	00010000	I2S/TDM clock polarity 0: Data changes on rising edge of SCK 1: Data changes on falling edge of SCK
		slot_size	6:5	00010000	I2S/TDM channel slot size (frame width) 00: 32 bit 01: 24 bit 10: 16 bit
		ws_fs_rising	7	00010000	I2S/TDM word/frame clock polarity 0: Word/frame starts at falling edge 1: Frame starts at rising edge
		data_size	3:2	00010000	Data size / bit depth 00: 24 bit 01: 20 bit 10: 18 bit 11: 16 bit
0x0011	0x00	lsb_first	0	00000000	I2S/TDM word order 0: MSB is transmitted first 1: LSB is transmitted first
0x0012	0x00	tdm_input_map0	4:0	00000000	Select channel (0-16) in received I2S/TDM stream to pass on to DSP/amp channel 0. 00000: Channel 0 00001: Channel 1 .. 01110: Channel 14 01111: Channel 15
0x0013	0x01	tdm_input_map1	4:0	00000001	Select channel (0-16) in received I2S/TDM stream to pass on to DSP/amp channel 1. See tdm_input_map0 register description for more information.
0x0016	0x1A	tdm_output_map0	2:0	00011010	Audio channel transmitted to I2S_DO pin in slot 0 of I2S/TDM stream. 000: Zero 001: High-Z 010: DSP output channel 0 011: DSP output channel 1
		tdm_output_map1	5:3	00011010	Audio channel transmitted to I2S_DO pin in slot 1 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0017	0x00	tdm_output_map2	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 2 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map3	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 3 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0018	0x00	tdm_output_map4	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 4 of I2S/TDM stream. Setup is similar to tdm_output_map0.

		tdm_output_map5	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 5 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0019	0x00	tdm_output_map6	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 6 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map7	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 7 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001A	0x00	tdm_output_map8	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 8 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map9	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 9 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001B	0x00	tdm_output_map10	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 10 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map11	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 11 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001C	0x00	tdm_output_map12	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 12 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map13	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 13 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001D	0x00	tdm_output_map14	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 14 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map15	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 15 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0026	0x0A	tx_loopback	0	00001010	Selects if transmitted audio data should be a copy of the received data. 0: I2S_DO is configured by tdm_output_map 1: I2S_DO is a copy of I2S_DI
		tx_enable	2	00001010	I2S/TDM transmitter enable 0: Disabled 1: Enabled
		rx_enable	1	00001010	I2S/TDM receiver enable (necessary to play audio) 0: Disabled 1: Enabled
		tx_strong_drive	3	00001010	Drive strength for I2S_DO pin 0: Normal 1: Strong
0x0027	0x04	sync_in_enable	0	00000100	Configure NCLIP pin as input for PWM synchronization 0: Disable 1: Enable
		sync_out_enable	1	00000100	Configure NCLIP pin as output (open-drain) for PWM synchronization. 0: Disable 1: Enable
		fast_sync	2	00000100	Select frequency of the PWM synchronization signal 0: Slow (fs/12288) 1: Fast (fs/12)

pmc					
Address	Reset	Name/Function	Bits	Value	Description
0x00BD	0x00	PM_ch0	2:0	00000000	Current selected Power Mode for channel 0
		PM_ch1	5:3	00000000	Current selected Power Mode for channel 1
0x00BE	0x00	Mdetector_ch0	7:0	00000000	Channel 0 modulation index M detector output. If register value is 0, modulation index is 0.0 (minimum). If register value is 255, modulation index is 1.0 (full modulation)
0x00BF	0x00	Mdetector_ch1	7:0	00000000	Channel 1 modulation index M detector output. If register value is 0, modulation index is 0.0 (minimum). If register value is 255, modulation index is 1.0 (full modulation)
prot_sys					
Address	Reset	Name/Function	Bits	Value	Description
0x0109	0x00	reg.errTrig_reset	1	00000000	Error register reset 0: Do not reset error trigger 1: Reset error trigger
0x011A	0x00	errVect_now.errVector_all__0	7:0	00000000	Instantaneous error vector 0. Bit 7: Low temperature warning Bit 6: I2S input error Bit 5: PLL not locked Bit 4: PVDD over-voltage Bit 3: Reserved Bit 2: PVDD under-voltage Bit 1: Over-temperature error Bit 0: Over-temperature warning
0x011C	0x00	errVect_acc.errVector_ch0	4:0	00000000	Accumulated channel 0 error vector. Bit 4: Reserved Bit 3: DC error Bit 2: Flying cap error Bit 1: Reserved Bit 0: Over-current protection
0x011D	0x00	errVect_acc.errVector_ch1	4:0	00000000	Accumulated channel 1 error vector. See description for errVect_acc.errVector_ch0
0x011E	0x00	errVect_acc.errVector_all__0	7:0	00000000	Accumulated error vector 0. Bit 7: Low temperature warning Bit 6: I2S input error Bit 5: PLL not locked Bit 4: PVDD over-voltage Bit 3: Reserved Bit 2: PVDD under-voltage Bit 1: Over-temperature error Bit 0: Over-temperature warning
pa_hw					
Address	Reset	Name/Function	Bits	Value	Description
0x0142	0x0D	otp.unmute_cnt	3:0	00001101	Unmute time delay from NMUTE=high to audio playback. 0011: 300 ms 1101: 30 ms (default)

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0x015F	0x00	reg.pwm_phase	6:0	00000000	Time/phase delay of PWM signal in 22.5 degree increments. Used with PWM sync to change relative PWM phase of synchronized devices. 0000000: 0 deg 0000001: +22.5 deg ... 0001111: +337.5 deg 0010000: +360 deg (equivalent to 0 deg)
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16 Package Information

Dimensions are in millimeter unless otherwise specified.

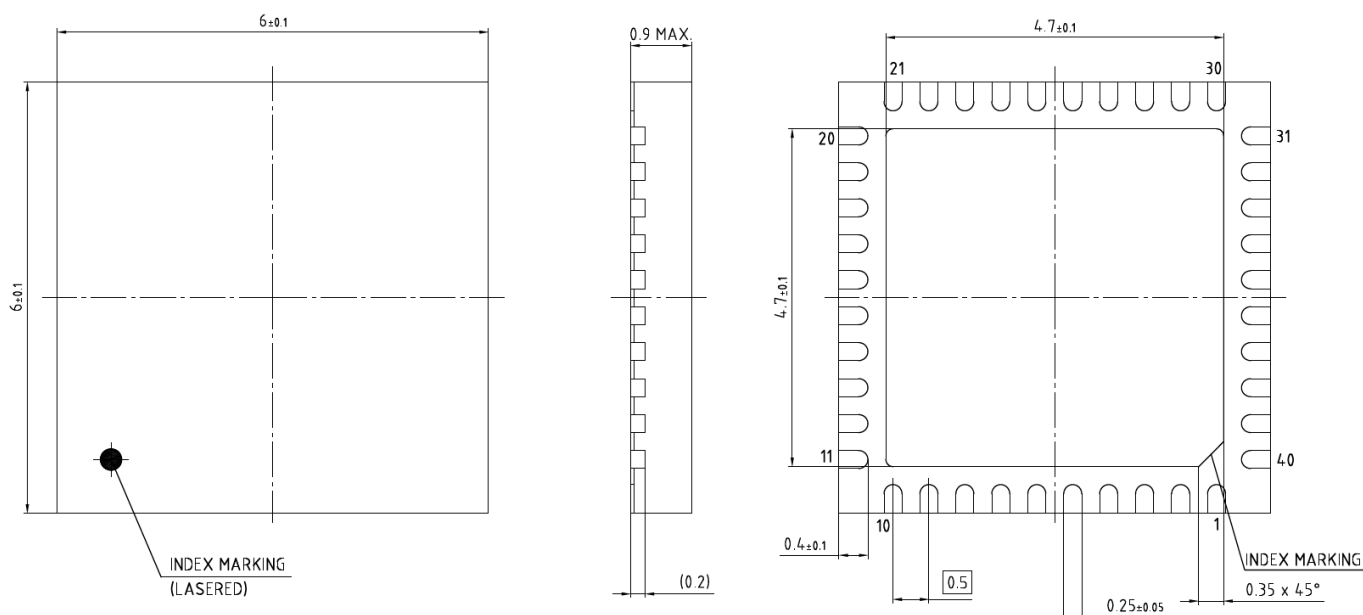


Figure 16.1: QFN pad-down 40-pin MA2306DNS package dimensions. Left: Top view. Middle: Side view. Right: Bottom view.

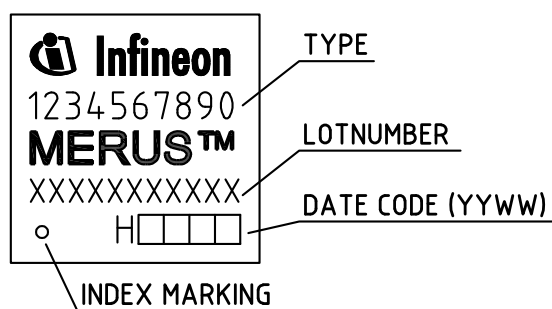


Figure 16.2: Package marking

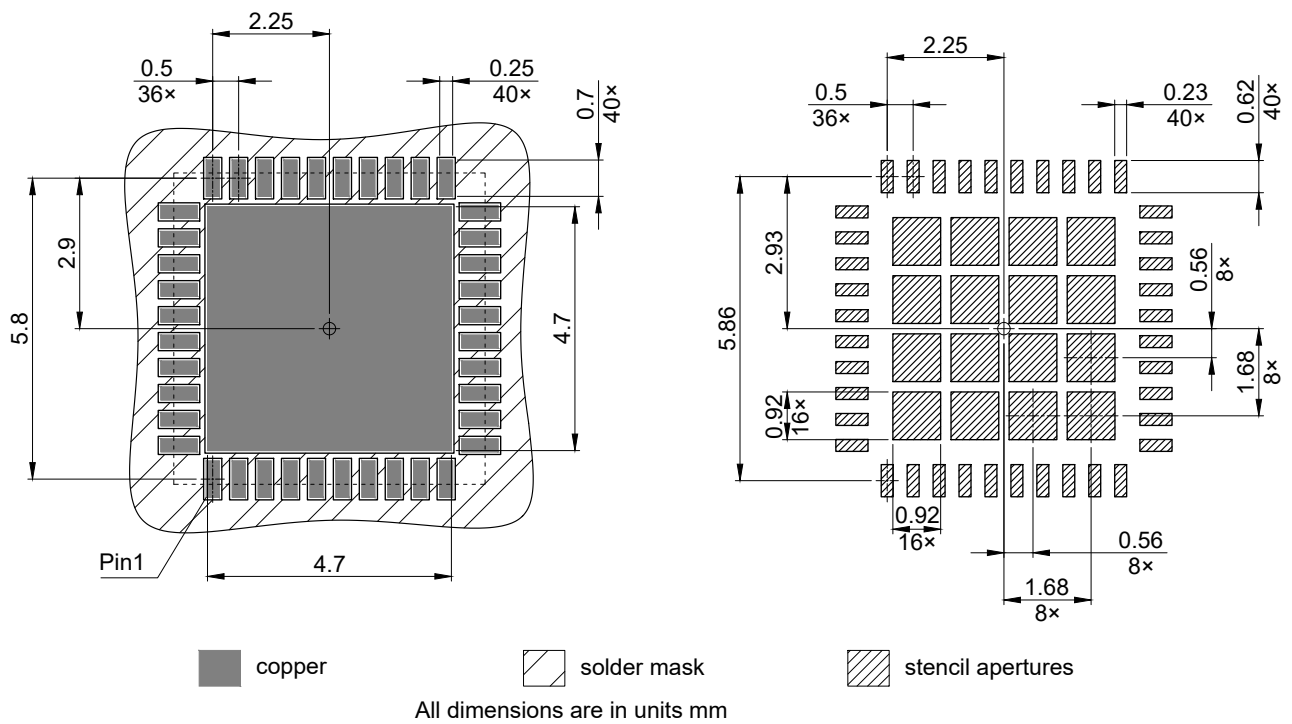


Figure 16.3: Recommended land pattern

17 Tape and Reel Information

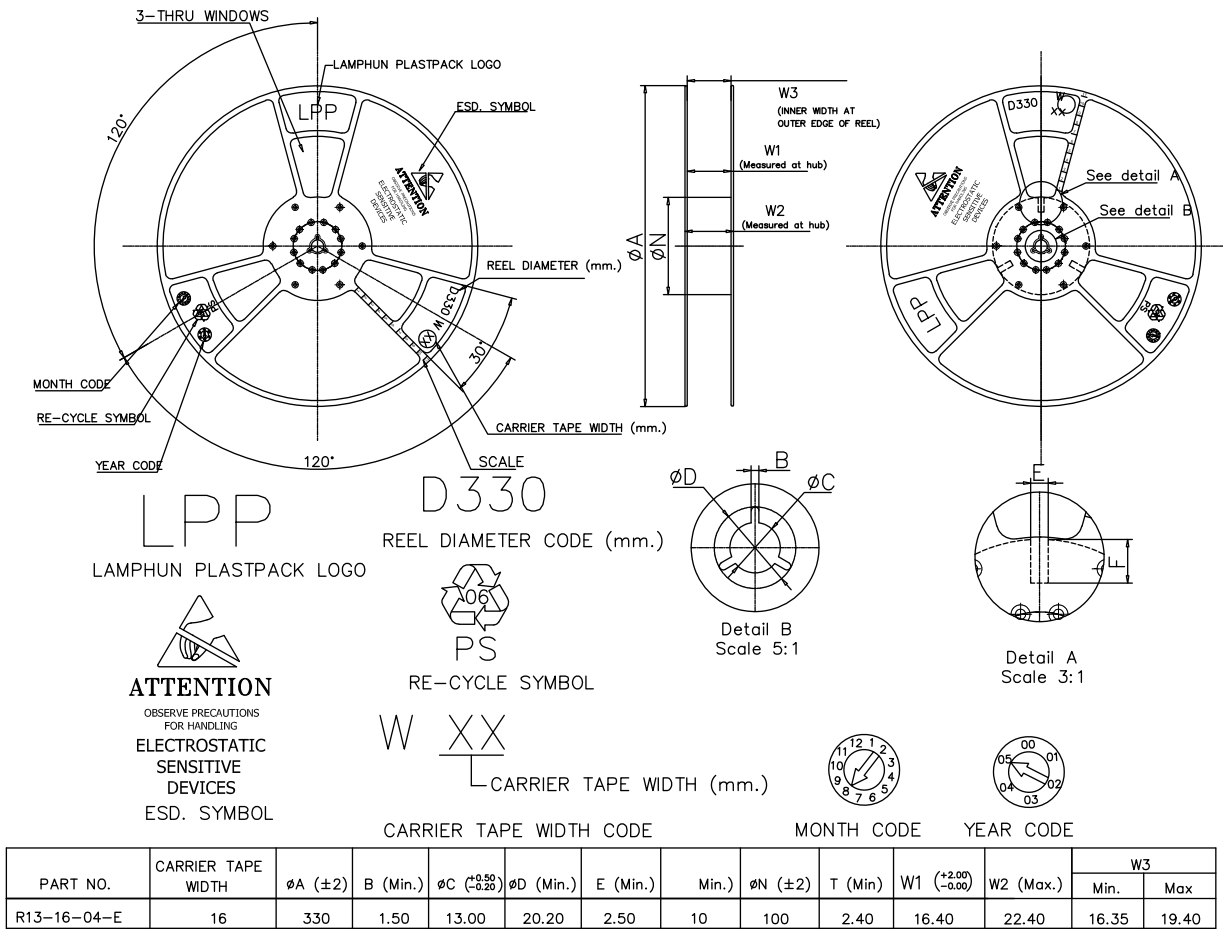
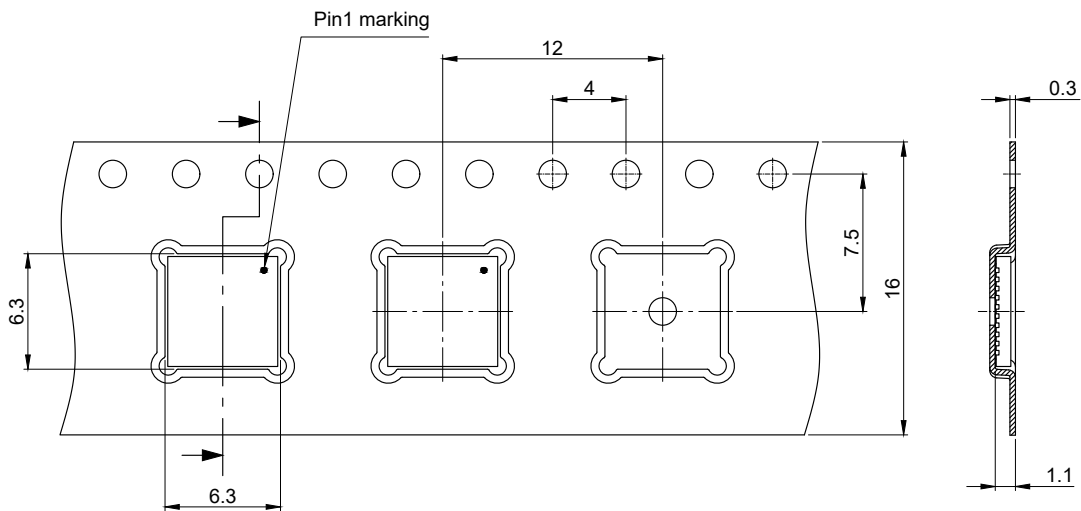


Figure 17.1: Tape reel information



All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 17.2: Carrier tape information

Revision History

MA2306DNS

Revision: 2024-01-17, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-01-17	Release of final version

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