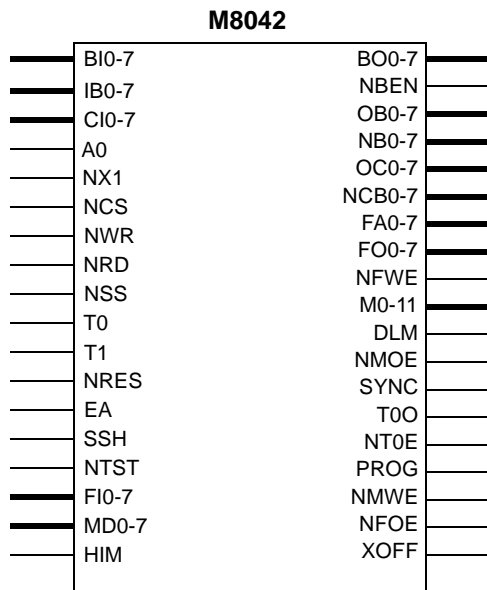


Features

- Functionally compatible with the industry standard 8042
- Uses AMI's ASIC Standard Library for technology independence
- Up to 256 bytes of data memory
- Up to 4K bytes of program memory
- Memory down-load mode
- 8-bit timer/counter
- DMA, interrupt or polled operation supported
- Power saving modes
- Equivalent gates (does not include RAM or ROM):
Standard Cell - 2,750; Gate Array - 3,500

LOGIC SYMBOL



Description

M8042 is an 8-bit slave microcontroller. This microcode-free design is software compatible with industry standard discrete devices. It can address data RAM of up to 256 bytes and program RAM or ROM of up to 4K bytes. If program memory is implemented with RAM a special down-load mode is available to program the RAM. An 8-bit timer/counter and 18 I/O pins are available.

Data is transferred between the M8042 and a master CPU through separate input and output data bus buffers. Communication can be controlled by two DMA handshaking lines or by interrupts.

The M8042 has two power saving modes; soft power down mode and hard power down mode. In soft power down mode the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the entire M8042 is stopped.

Signals are present that allow the end user to choose the appropriate memory block for each implementation. This allows memory size to be configured, and if necessary, the program memory block may be implemented as "down-loadable" RAM.

As no I/O cells are included in the design, all bidirectional lines (the Data Bus, the Port1 and Port2 buses) are split into input and output sections, and have associated control lines for enabling and disabling 3-state buffers where appropriate. There are individual enable lines for each of the Port1 and Port2 outputs. This allows implementation of the 'quasi-bidirectional' pins feature of the original device.

There is only one clock input (NX1), this is again due to the fact that there are no I/O cells in the design. The output of a suitable crystal oscillator I/O cell should be connected to this input. XOFF (which is high true) is used to disable the oscillator I/O cell in power saving mode.

This megacell requires the use of ROM and RAM which can be ordered from the AMI Memory group.

A per-use fee is associated with this megacell. Contact the factory for more information.