M62371GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62371GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D-A converters. It is operable with a low supply voltage between 2.7 ~ 3.6V, and is easy to use due to serial data input, and 3-pin(DI, CLK, LD)connection with microcomputer. The IC also contains Do pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer. (M62371GP is an advanced product of M62370GP on its buffer amp. drivability.)

FEATURES

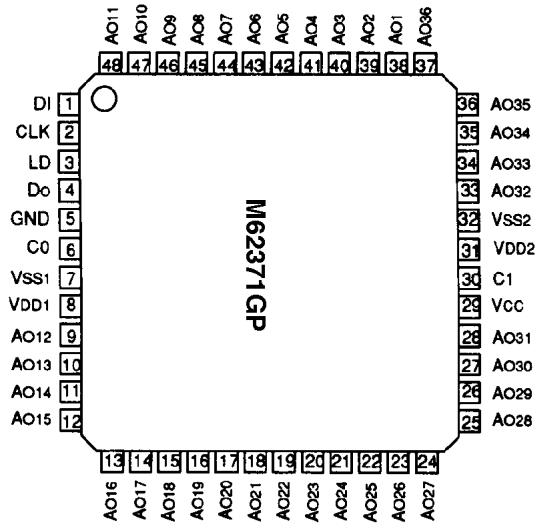
- Operable with a low voltage between 2.7 ~ 3.6V
- 16-bit serial data input(connected via 3 pins:DI, CLK , LD)
- 36 channels built-in of 8-bit D-A converter
- 6 channels of D-A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

APPLICATION

Digital-analog conversion in industrial or home-use electronic equipment

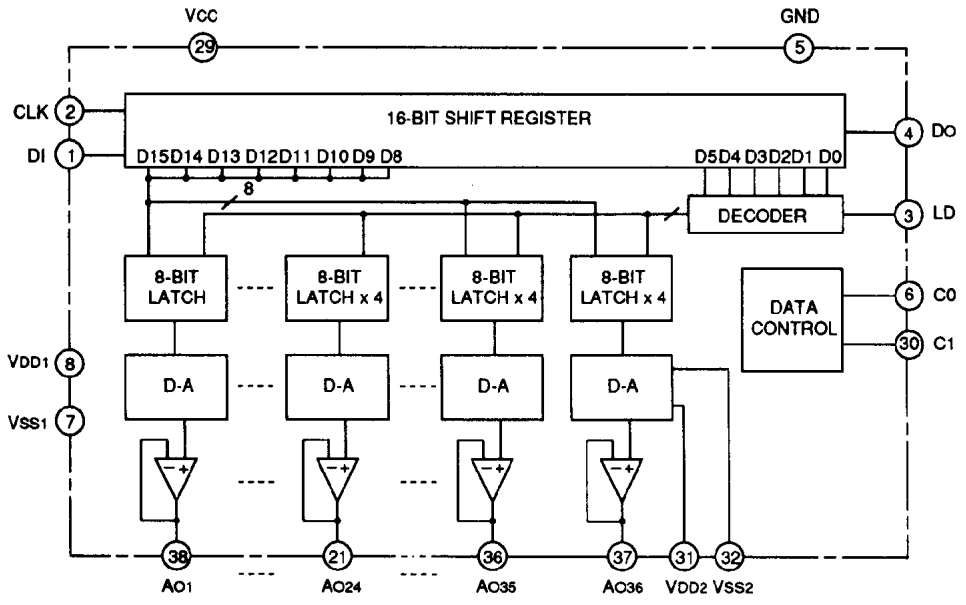
Automatic control in combination with EEPROM and microcomputer (Substiture for conventional semi-fixed resistor)

PIN CONFIGURATION (TOP VIEW)



Outline 48P6D-A

BLOCK DIAGRAM



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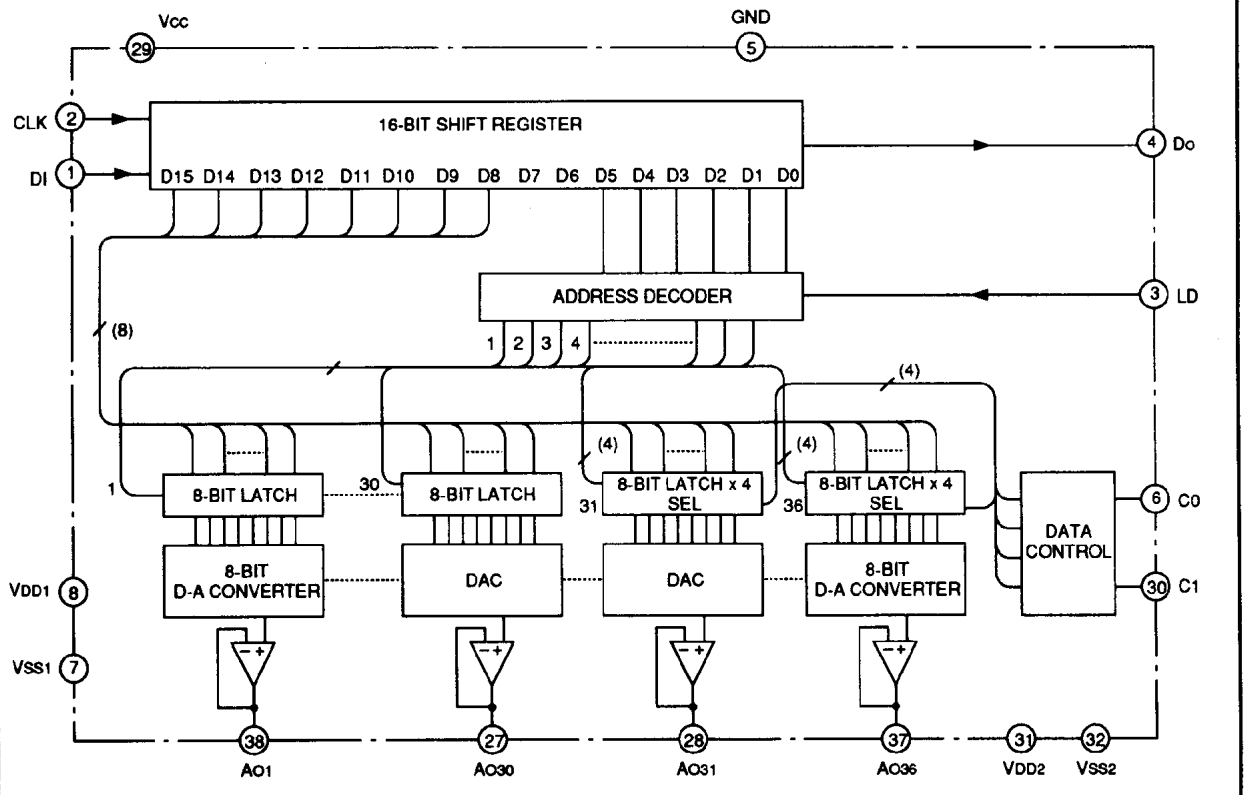
EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	DI	Serial data input terminal to input 16-bit long serial data
④	DO	Terminal to output MSB data of 16-bit shift register
②	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
③	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D-A converter output register
㊳	AO1	8-bit D-A converter output terminal
～	～	
㊶	AO11	
⑨	AO12	
～	～	
㉘	AO31	
㉝	AO32	
～	～	
㉗	AO36	
㉙	VCC	Power supply terminal
⑤	GND	GND terminal
⑥	C0	Data select signal input terminal 1 for channel No. 31 through 36
㉚	C1	Data select signal input terminal 2 for channel No. 31 through 36
⑧	VDD1	Upper reference voltage input terminal and power supply to operational amplifier for channel No. 1 through 24
⑦	VSS1	Lower reference voltage input terminal for channel No. 1 through 24
㉛	VDD2	Upper reference voltage input terminal and power supply to operational amplifier for channel No. 25 through 36
㉜	VSS2	Lower reference voltage input terminal for channel No. 25 through 36

BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



MITSUBISHI ELECTRIC

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DIGITAL DATA FORMAT

FIRST LSB ← → LAST MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
← DAC DATA →								← DAC SELECT DATA →							

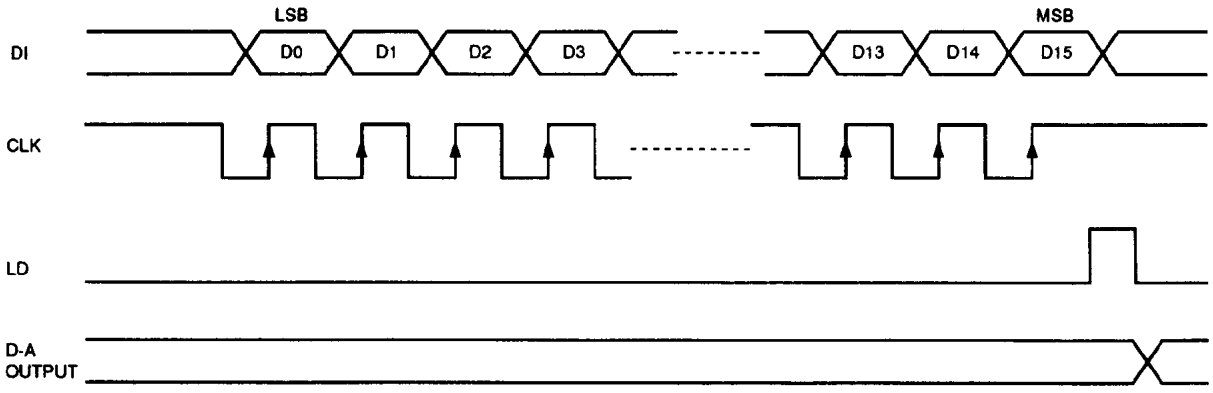
D8	D9	D10	D11	D12	D13	D14	D15	D-A output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

D5	D4	D3	D2	D1	D0	DAC selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	A_{O1} selection
0	0	0	0	1	0	A_{O2} selection
≀	≀	≀	≀	≀	≀	≀
0	1	1	1	1	0	A_{O30} selection
0	1	1	1	1	1	A_{O31}(0)selection
1	0	0	0	0	0	A_{O32}(0)selection
≀	≀	≀	≀	≀	≀	≀
1	0	0	1	0	0	A_{O36}(0)selection
1	0	0	1	0	1	A_{O31}(1)selection
≀	≀	≀	≀	≀	≀	≀
1	0	1	0	1	0	A_{O36}(1)selection
1	0	1	0	1	1	A_{O31}(2)selection
≀	≀	≀	≀	≀	≀	≀
1	1	0	0	0	0	A_{O36}(2)selection
1	1	0	0	0	1	A_{O31}(3)selection
≀	≀	≀	≀	≀	≀	≀
1	1	0	1	1	0	A_{O36}(3)selection
1	1	0	1	1	1	Don't care
≀	≀	≀	≀	≀	≀	≀
1	1	1	1	1	1	Don't care

C0	C1	A_{O31} through A_{O36} data selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

* $V_{refU} = V_{DD1}, V_{DD2}$
$V_{refL} = V_{SS1}, V_{SS2}$

TIMING CHART (MODEL)



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ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3~7.0	V
V_O	Output voltage		−0.3~Vcc+0.3	V
P_d	Power dissipation		400	mW
K_θ	Thermal derating	Ta≦25°C	4	mW/°C
T_{opr}	Operating temperature		−20~+85	°C
T_{stg}	Storage temperature		−40~+125	°C

ELECTRICAL CHARACTERISTICS

Digital part (V_{CC}=+3V+-10%, V_{CC}=V_{DD}, Ta=−20 ~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2.7	3.0	5.5	V
I_{CC}	Circuit carrent	CLK=1MHz operation, V_{CC}=3V, I_{AO}=0μA		1.0		mA
I_{ILK}	Input leak current		−10		10	μA
V_{IL}	Input low voltage				0.6	V
V_{IH}	Input high voltage		2.4			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=−400μA	V_{CC}−0.4			V

Note.Standard value is at Ta=25℃.

Analog part (V_{CC}=+3V+-10%, V_{CC}=V_{DD}, Ta=−20 ~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Current dissipation			8.0	12.0	mA
V_{DD}	D-A converter upper reference voltage range		2.7	3.0	5.5	V
V_{SS}	D-A converter lower reference voltage range		GND		V_{DD}−2	V
V_{AO}	Buffer amplifier output voltage range	I_{AO}=±0.5mA	0.1		V_{DD}−0.1	V
		I_{AO}=±1.0mA	0.2		V_{DD}-0.2	
I_{AO}	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-1.5		1.5	mA
SDL	Differential nonlinearity error	V_{CC}=2.700V	−1.0		1.0	LSB
S_L	Nonlinearity error	V_{DD}=2.700V	−1.5		1.5	LSB
S_{ZERO}	Zero code error	V_{SS}=0.050V	−2		2	LSB
S_{FULL}	Full scale error	No load (I_{AO}=±0)	−2		2	LSB
C_O	Output capacitative load				0.1	μF
R_O	Buffer amplifier output impedance			50		Ω

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AC CHARACTERISTICS (V_{CC}=V_{DD}, Ta=−20 ~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L" pulse width		200			ns
t_{CKH}	Clock "H" pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data setup time		30			ns
t_{CHD}	Data hold time		60			ns
t_{CHL}	LDsetup time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse duration		100			ns
t_{DO}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	D-A converter output settling time	$C_L \leqq 100pF$, V_{AO}:0.3V⇄2.7V The time until the output becomes the final value of ±2 LSB			100	µs

TIMING CHART