Mitsubishi CMOS Gate Arrays

INTRODUCTION

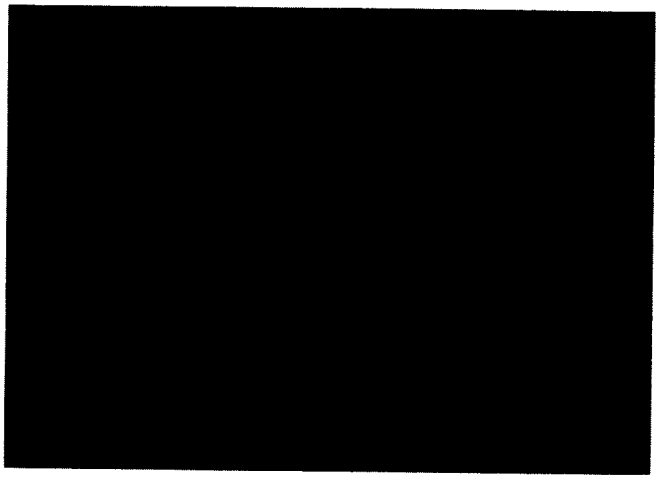
Mitsubishi offers three families of CMOS gate arrays: 1.0 µm, 1.3 µm, and 2.0 µm, with usable gates ranging from 200 to 35,000. The 1.0 and 1.3 µm devices are designed with low power, double-layer metal, single-poly, twin-well, silicon-gate CMOS processes.

All of the families feature Mitsubishi's patented gate isolation structure*. Gate isolation provides gate arrays with faster performance and higher gate density than conventional oxide isolation. Gate isolation results in an average of 15 percent faster performance and 20 percent higher gate density than conventional oxide isolation technology.

Mitsubishi's gate arrays are available in through-hole and surface-mount packages including Adaptable Pin Grid Arrays (APGA) and Very-Fine-Pitch Quad Flat Packages (VQFP).

All gate arrays are 100 percent burned-in, and electrically (AC and DC) and functionally tested. Design kits for Mitsubishi gate arrays include the following CAE hardware and software: Dazix™, FutureNet®, Hewlett-Packard®, Intergraph®, IKOS®, Mentor Graphics®, OrCAD™, Synopsys®, Valid Logic™, Viewlogic™, Verilog®.

* U.S. Patent No. 4,562,453.



Typical Mitsubishi Gate Array Packages

1.0 µm Gate Arrays

M6005X, M6006X CMOS Gate Array Features

Feature	Parameter
Available Gates	6,000 to 70,000
Usable Gates (50% utilization)	3,000 to 35,000
Array Sizes	8
Architecture	Channel-less
Cell Architecture	Gate Isolation
Routing and Power Distribution	2 Layer Metal
Gate Length	1.0 µm Drawn
Gate Delay (2 input NAND, 2x drive, FO = 2, 2 mm metal)	450 psec
Gate Delay (2 input NAND, 4x drive, FO = 2, 2 mm metal)	370 psec
Toggle Rate	320 MHz
I/O Interface	TTL or CMOS Compatible
Power Consumption (2 NAND, FO = 2, 1x drive)	5 µW/gate/MHz
Output Buffer Drive (single)	1, 2, 4, 8, 12 mA
Output Slew Selection	0.5 to 1.0 volt/nsec
Library	500 Cells
Speed/Power Cell Option	1x, 2x, 3x, 4x Drive

M6005X Series — Mitsubishi's 1.0 µm gate arrays are designed with a channel-less architecture and allow efficient use of silicon. The 1.0 µm arrays have a propagation delay of 370 picoseconds for a 2-input NAND (FO = 2, 2 mm wire), a latch toggle rate of 320 MHz, and clock rates approaching 100 MHz. A typical input buffer delay is 1.0 ns and a typical output buffer delay is 2.0 ns.

In order to achieve low power dissipation and reduce operating temperature, the 1.0 µm gate arrays are designed with a minimized gate size resulting in a power dissipation of 5 µW/MHz/gate.

M6006X Series — The Mitsubishi M6006X family of gate arrays uses the same architecture and features as the M6005X family. A higher pin count to gate ratio has been achieved making this family useful for array sizes from 3000 to 10,000 gates.

Features for 1.0 μm

Mitsubishi's 1.0 μm gate arrays include a speed/power option that allows design optimization to meet combined high speed, low power, and small die size requirements. The commonly used library cells are offered in a variety of sizes: 1, 2, 3, or 4 parallel transistors.

The optimization process is illustrated for the circuit path in Figure 1A. The optimum size of the second inverter is determined by the drive of the previous stage, as well as by the load. Since an increase in drive adds delay to the previous stage, this increase is added to the second stage delay in Figure 1B and 1C. The lowest attainable delay varies with buffer option, depending on load. The large selection of Mitsubishi cell size options allows designers to achieve both needed speed and small die size.

In most gate arrays, 90 percent of the logic does not require fast performance. This means that small cells with low power are most efficient. Driving large loads at high speed, however, requires large cells with high power. The M6005X and M6006X series features a speed/power option that allows the cell size to be set at x1, x2, x3 or x4 transistors, depending on the need for low power versus high speed. This feature allows the 1.0 micron gate arrays to take advantage of smaller cell size over the large area of the circuit where it is most appropriate and, at the same time, provide high speed where it is needed.

Figure 1A. Circuit Path

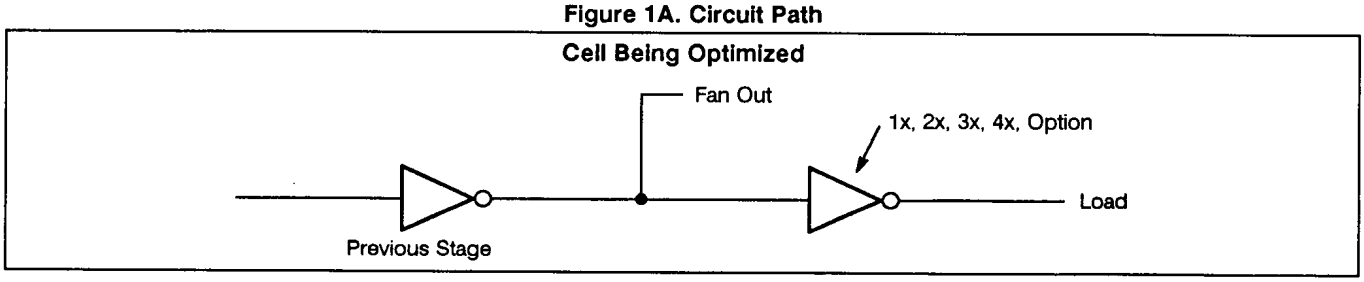


Figure 1B. Delay Characteristic Options

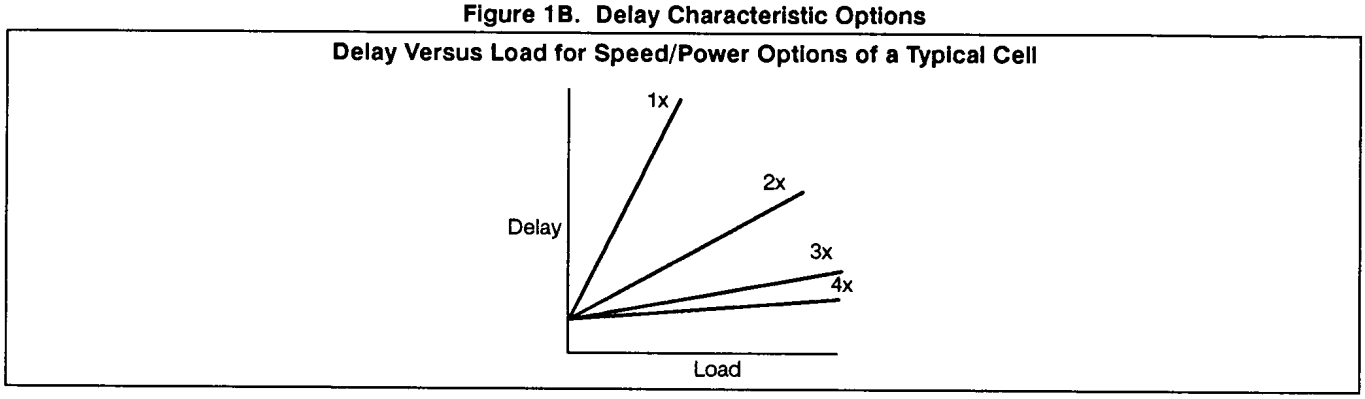
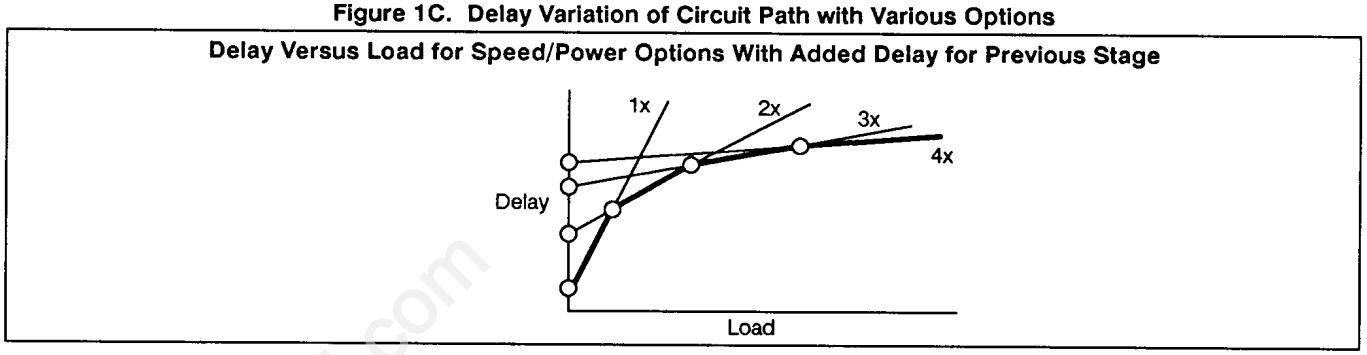


Figure 1C. Delay Variation of Circuit Path with Various Options



In addition to standard interface specifications, the M6005X series includes: optional pull-up or pull-down resistors for holding high or low states; a variable output drive, allowing buffer cells to be set for 1, 2, 4, 8 or 12 mA; and a selectable slew rate, ranging between 0.5 and 1.0 V/ns.

Figure 2 shows the improved gate utilization for 1.0 μm gate arrays. In a three-input NAND gate, only four pitches are required using gate isolation, as opposed to eight that are required by conventional oxide isolation. The ability to use individual basic cells (pairs of n and p transistors) instead of two-input NAND gates increases gate utilization. This three-input NAND example illustrates a 50 percent improvement in density with gate isolation.

Table 1A. Mitsubishi M6005X Series Gate Arrays

Part Number			M60050	M60051	M60052	M60053	M60054	M60055	M60056	M60057
Number of Usable Gates			5,000	6,000	8,000	10,000	12,000	15,000	25,000	35,000
Maximum I/O Ports			112	120	128	150	166	176	216	234
Package Type	**Lead Spacing**	**Pins**								
Plastic Flat Package (QFP)	0.80 mm	80	•	•	•	•				
	0.65	100	•	•	•	•	•	•		
	0.80	120	•	•	•	•	•	•		
	0.80	128		•	•	•	•	•		
	0.65	136			•	•	•	•	•	
	0.65	160				•	•	•	•	•
	0.50	208						•	•	•
Plastic Leaded Chip Carrier (PLCC)	50 mil	68	•	•	•	•	•	•		
	50	84	•	•	•	•	•	•		
Ceramic Pin-Grid-Array (PGA)	100 mil	281								•
Adaptable Pin-Grid-Array (APGA)	100 mil	***	***	***	***	***	***	***	***	***

Table 1B. Mitsubishi M6006X Series Gate Arrays

Part Number			M60062	M60063	M60064	M60065	M60066	M60067
Number of Usable Gates			3,000	4,000	5,000	6,000	8,000	10,000
Maximum I/O Ports			128	150	150	150	150	176
Package Type	**Lead Spacing**	**Pins**						
Plastic Flat Package (QFP)	0.80 mm	120	•	•				
	0.65	136	•	•	•			
	0.65	160		•	•	•	•	•
	0.50	208						•

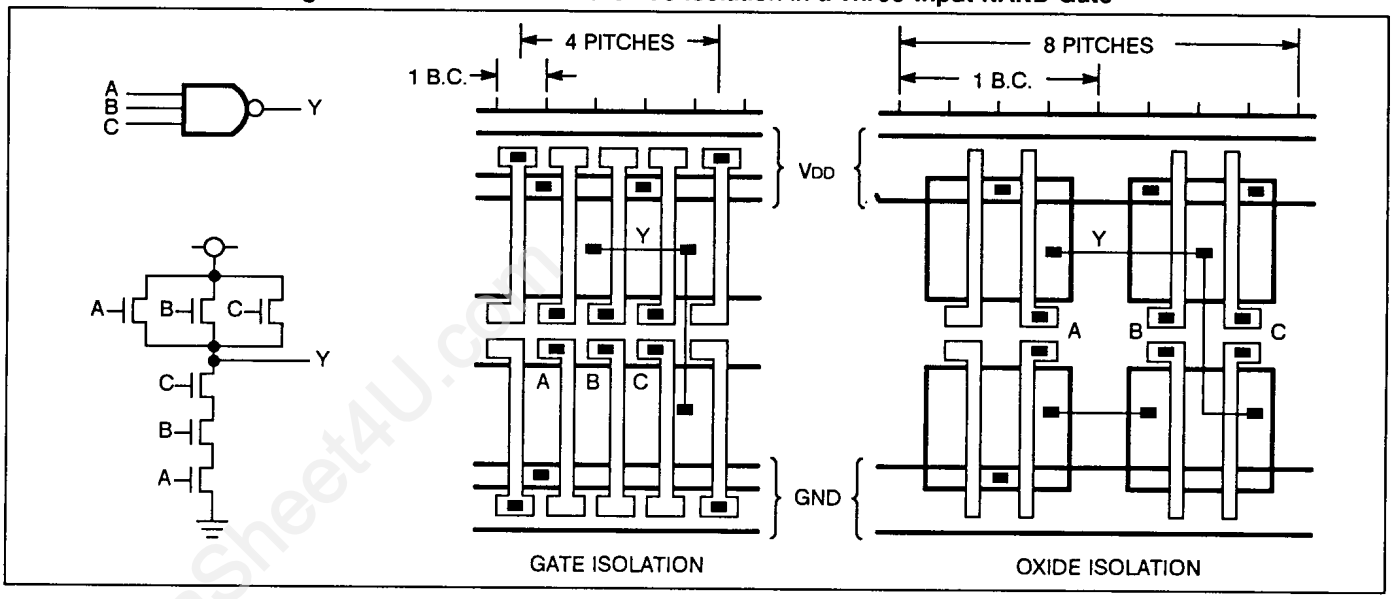
*****Adaptable Pin-Grid-Arrays (APGA)**

Gate arrays to be supplied in an APGA package are available in the configurations shown in the table below. After selecting a gate array master:

1. Determine the availability of a QFP with the required number of pins from the package matrix.
2. Find the APGA adapter available for the selected QFP.
3. Configurations not shown may be developed by Mitsubishi.

		ADAPTABLE PIN-GRID-ARRAY					
	Pins	**84**	**100**	**124**	**144**	**160**	**208**
Quad Flat Package	80	•					
	100	•	•				
	128			•			
	160				•	•	
	208						•

Figure 2. Gate Isolation and Oxide Isolation in a Three-Input NAND Gate



1.3 μm Gate Arrays

M6004X, M6003X, and M6002X CMOS Gate Array Features

Feature	Parameter
Usable Gates	224 to 20,000
Array Sizes:	
M6002X	6
M6003X	6
M6004X	5
Architecture	
M6002X	Channeled
M6003X, M6004X	Variable Track Masterslice
Cell Architecture	Gate Isolation
Routing and Power Distribution	2 Layer Metal
Gate Length	1.3 μm Drawn
Gate Delay (2 input NAND, FO = 2, 2 mm metal)	900 psec
Toggle Rate	175 MHz
I/O Interface	CMOS or TTL Compatible
Power Consumption	10 μW/gate/MHz
Output Drive M6002X, M6003X	14 mA
Output Drive M6004X	4, 8, 12 mA (selectable)*
Library	Over 300 Cells

*M6004X has narrow bonding pad pitch to achieve 25% higher I/O pin count than M6002X/M6003X

M6002X Series – The family includes six sizes, ranging from 224 usable gates with 22 I/Os to 2400 usable gates with 72 I/Os.

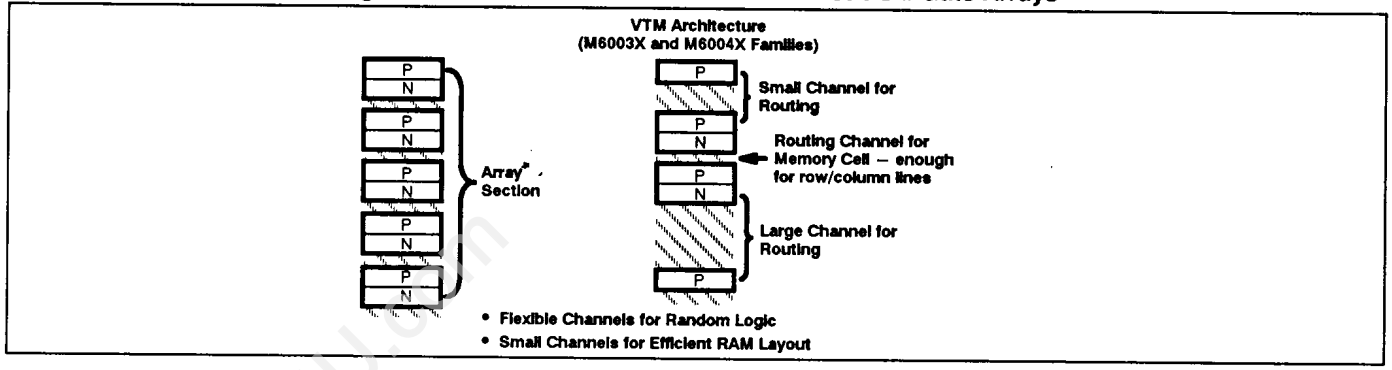
Conventional channeled architecture is used to route interconnect lines over thick oxide, producing low capacitance in the M6002X series gate arrays.

M6003X Series – With the same performance characteristics as the M6002X family, the M6003X 1.3 μm series offers large gate counts, ranging from 3200 usable gates with 88 I/Os to 20,000 usable gates with 256 I/Os. Series M6003X is also designed with VTM architecture.

M6004X Series – Mitsubishi's M6004X arrays are designed with variable track masterslice (VTM) architecture, providing variable-sized routing channel widths for efficient use of gates.

Figure 3 shows an example of variable width channels. Variable widths, achieved by the place and route software of VTM, increase an array's gate utilization by matching gate width requirements. For large gate arrays, up to 50 percent of the silicon may be required for the interconnect of random logic, resulting in a 50 percent utilization rate. RAM and ROM implementation, conversely, uses close to 100 percent of the array transistors, requiring very little interconnect space.

Figure 3. Variable Track Architecture of Mitsubishi Gate Arrays



Mitsubishi M6002X and M6003X Series 1.3 μm CMOS Gate Arrays

Part Number (1)(2)			M60020	M60021	M60022	M60023	M60024	M60025	M60030	M60031	M60032	M60034	M60035	M60037
Number of Usable Gates			224	507	800	1,104	1,773	2,400	3,200	4,100	6,300	8,400	11,000	20,000
Maximum I/O Ports			22	32	42	48	62	72	88	110	132	180	196	256
Package Type	**Lead Spacing**	**Pins**												
Plastic DIP	100 mil	16(3)	•											
		20(3)	•	•	•									
		28(4)	•	•	•	•								
Plastic Shrink DIP	70 mil	42		•	•	•	•	•	•			•		
		52			•	•	•	•	•					
		64					•	•	•	•	•	•		
Small Outline Package (SOP)	50 mil	24	•	•	•									
		36		•	•									
Plastic Flat Package (QFP)	1.00 mm	44			•	•	•	•						
	1.00	64				•	•	•	•	•				
	0.80	80					•	•	•	•	•	•		
	0.65	100							•	•	•	•	•	
	0.80	128								•	•	•	•	•
	0.65	160										•	•	•
	0.50	208											•	•
Adaptable Pin-Grid-Array (APGA)	100 mil	***	***	***	***	***	***	***	***	***	***	***	***	***
Plastic Leaded Chip Carrier (PLCC)	50 mil	44		•	•	•	•	•						
		52				•	•	•	•					
		68					•	•	•	•	•	•		
		84						•	•	•	•	•	•	
Ceramic Pin-Grid-Array (PGA)	100 mil	177												
		209											•	•
		281												•

Notes:

(1) M6002X Series is conventional (channel) architecture.

(2) M6003X Series is Variable Track Masterslice (VTM) architecture.

(3) 300 mil body only available.

(4) 600 mil body only available.

***Adaptable Pin-Grid-Arrays (APGA)

Gate arrays to be supplied in an APGA package are available in the configurations shown in the table below. After selecting a gate array master:

1. Determine the availability of a QFP with the required number of pins from the package matrix.
2. Find the APGA adapter available for the selected QFP.
3. Configurations not shown may be developed by Mitsubishi.

		ADAPTABLE PIN-GRID-ARRAY					
	Pins	**84**	**100**	**124**	**144**	**160**	**208**
Quad Flat Package	80	•					
	100	•	•				
	128			•			
	160				•	•	
	208						•

Mitsubishi M6004X Series 1.3 μm CMOS Gate Arrays

Part Number			M60043	M60044	M60045	M60047	M60049
Number of Usable Gates			2,400	3,200	4,100	6.300	8,400
Maximum I/O Ports			112	132	144	180	184
Package Type	**Lead Spacing**	**Pins**					
Plastic Flat Package (QFP)	0.65 mm	100	•				
	0.80	128	•	•	•		
	0.65	160		•	•	•	•
	0.50	208				•	•
Adaptable Pin-Grid-Array (APGA)	100 mil	***	***	***	***	***	***

*** Refer to APGA Availability Chart p.5

2.0 μm Gate Arrays

M6001X Series – This family of conventional architecture arrays includes nine gate sizes ranging from 500 usable gates with 64 I/Os to 8,000 usable gates with 190 I/Os.

Mitsubishi M6001X Series 2.0 μm CMOS Gate Arrays

Part Number			M60011	M60012	M60013	M60014	M60015	M60016	M60017	M60018	M60019
Number of Usable Gates			500	810	1,100	1,680	2,666	3,608	4,814	6,233	8,096
Maximum I/O Ports			64	82	96	116	132	148	176	178	190
Package Type	**Lead Spacing**	**Pins**									
Plastic DIP	100 mil	16(1)	•								
		18(1)	•								
		20(1)	•								
		24(2)	•	•	•	•	•	•	•		
		28(3)	•	•	•	•	•	•	•		
		40(3)	•	•	•	•	•	•	•		
		42(3)	•	•	•	•	•	•	•		
Plastic Shrink DIP	70 mil	42	•	•	•	•	•	•	•		
		52	•	•	•	•	•	•	•		
		64	•	•	•	•	•	•	•	•	•
Ceramic Pin-Grid-Array (PGA)	100 mil	124						•	•	•	•
		209						•	•		•
Plastic Flat Package (QFP)	1.00 mm	44	•	•	•	•					
	1.00	64	•	•	•	•	•	•			
	0.80	80	•	•	•	•	•	•	•	•	•
	0.65	100		•	•	•	•	•	•	•	•
	0.80	128					•	•	•	•	•
	0.65	160								•	•
Adaptable Pin-Grid-Array (APGA)	100 mil		***	***	***	***	***	***	***	***	***
Plastic Leaded Chip Carrier (PLCC)	50 mil	44	•	•	•						
		52	•	•	•	•	•				
		68		•	•	•	•	•	•		
		84		•	•	•	•	•	•	•	•

Notes:

(1) 300 mil body only available.

(2) 600 and 300 mil body available.

(3) 600 mil body only available.

***Adaptable Pin-Grid-Arrays (APGA)

Gate arrays to be supplied in an APGA package are available in the configurations shown in the table below. After selecting a gate array master:

1. Determine the availability of a QFP with the required number of pins from the package matrix.
2. Find the APGA adapter available for the selected QFP.
3. Configurations not shown may be developed by Mitsubishi.

		ADAPTABLE PIN-GRID-ARRAY				
	Pins	**84**	**100**	**124**	**144**	**160**
Quad Flat Package	80	•				
	100	•	•			
	128			•		
	160				•	•

SPECIFICATION TABLES

Tables 5 through 9 present the electrical specifications, typical DC and AC characteristics, and recommended operating conditions for Mitsubishi's 1.0, 1.3, and 2.0 μm gate arrays.

The worst case delays are calculated using the multiplication factors shown in Table 10. Typical performance characteristics for some commonly used library cells are shown in Table 11.

Absolute Maximum Ratings for Mitsubishi CMOS Gate Arrays

Symbol	Parameter	Limits		Unit
		Min	Max	
V_{DD}	Supply Voltage	V_{SS} - 0.3	6.5	V
V_I	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
I_O	Output Current(1)		10	mA
I_O	Output Current(2, 3, 5)		16	mA
I_O (T)	Total Output Current (per power supply pin)		80	mA
T_{opr}	Operating Temperature	-20	75	°C
T_{stg}	Storage Temperature	-55	150	°C
	Electrostatic Discharge(4)	-2000	2000	V
P_{DOUT}	Output Buffer Power Dissipation Limit*		360(6)	MHz • pF*
			550(7)	
			890(8)	

Notes:
(1) M6001X Series.
(2) M6002X and M6003X Series.
(3) M6005X and M6006X Series.
(4) Electrostatic discharge is measured from a 100 pF capacitor through a 1500 Ω resistor.
(5) M6004X Series
(6) Single Buffers rated at 12 mA.
(7) Single Buffers rated at 8 mA.
(8) Single Buffers rated at 4 mA.

*Calculated by multiplying output buffer by average output switching frequency.

Recommended Operating Conditions for Mitsubishi Gate Arrays

Symbol	Parameter		Limits		Unit
			Min	Max	
VDD	Supply Voltage		4.5	5.5	V
Topr	Operating Temperature		-20	75	°C
VI	Input Voltage		0	VDD	V
Vo	Output Voltage		0	VDD	V
Io	Output Current per Output(1)			6	mA
Io	Output Current per Output(2)			14	mA
Io	Output Current per Output(3)			12	mA
CL	Output Load Capacitance			50	pF
Io (T)	Total Output Sink Current (per Vss pin)			80	mA
Io (T)	Total Output Source Current (per VDD pin)			40	mA
tr, tf	Input Rise Time, Fall Time	Normal Input		500	nS
		Schmitt Input		5	sec

Notes:
(1) M6001X Series.
(2) M6002X and M6003X Series.
(3) For buffers rated at 12 mA.

Typical DC Characteristic of Mitsubishi Gate Arrays

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
V_{IL}	Input Voltage (TTL Interface)	V_{DD} = 4.5 V	0	0.8	V
V_{IH}		V_{DD} = 5.5 V	2.2	5.5	
V_{IL}	Input Voltage (CMOS Interface)	V_{DD} = 4.5 V	0	1.35	V
V_{IH}		V_{DD} = 5.5 V	3.85	5.5	
VT−	Input Voltage Schmitt Trigger (TTL Interface)	V_{DD} = 5 V	0.7	1.65	V
VT+			1.3	2.1	
VH			0.3	1.2	
VT−	Input Voltage Schmitt Trigger (CMOS Interface)	V_{DD} = 5 V	0.85	2.5	V
VT+			2.3	3.7	
VH			0.5	1.6	
V_{OL}	Output Voltage	V_{DD} = 5 V, I_O = 0 mA		0.05	V
V_{OH}			4.95		
I_{OL}	Output Current (1)	V_{OL} = 0.4 V, V_{DD} = 4.5 V	6		mA
I_{OH}		V_{OH} = 4.1 V, V_{DD} = 4.5 V	-2		
I_{OL}	Output Current (2)	V_{OL} = 0.4 V, V_{DD} = 4.5 V	14		mA
I_{OH}		V_{OH} = 4.1 V, V_{DD} = 4.5 V	-5		
I_{OL}	Output Current (5) (Selectable)	V_{OL} = 0.4 V, V_{DD} = 4.5 V	4(8)		mA
			8(7)		
			12(6)		
I_{OH}		V_{OH} = 4.1 V, V_{DD} = 4.5 V	-3		
I_{OL}	Output Current (3) (Selectable)	V_{OL} = 0.4 V, V_{DD} = 4.5 V	2(9)		mA
			4(8)		
			8(7)		
			12(6)		
I_{OH}		V_{OH} = 4.1 V, V_{DD} = 4.5 V	-6(10)		
			-2(11)		
I_I	Input Leakage Current	V_I = V_{DD}, V_{SS}	−1	+1	µA
I_{OZ}	Output Leakage Current	V_O = V_{DD}, V_{SS}	−1	+1	µA
RU	Pull-up Resistor (1)	V_{DD} = 5 V, V_I = 0 V	50	500	kΩ
RD	Pull-down Resistor (1)	V_{DD} = 5 V, V_I = 5 V	50	500	kΩ
RU	Pull-up Resistor (2, 5)	V_{DD} = 5 V, V_I = 0 V	23	230	kΩ
RD	Pull-down Resistor (2, 5)	V_{DD} = 5 V, V_I = 5 V	16	160	kΩ
RU	Pull-up Resistor (3)	V_{DD} = 5 V, V_I = 0 V	10	120	kΩ
RD	Pull-down Resistor (3)	V_{DD} = 5 V, V_I = 5 V	10	120	kΩ

Notes:

(1) M6001X Series.
(2) M6002X and M6003X Series.
(3) M6005X and M6006X Series.
(4) Electrostatic discharge is measured from a 100 pF capacitor through a 1500 Ω resistor.
(5) M6004X Series
(6) Buffers rated at 12 mA.
(7) Buffers rated at 8 mA.
(8) Buffers rated at 4 mA.
(9) Buffers rated at 2 mA.
(10) Buffers rated at 6 mA.
(11) Buffers rated at 2 mA.

Typical AC Characteristics of Mitsubishi Gate Arrays*

Parameter	Test Conditions	1.0 µm (M6005X, M6006X)	1.3 µm (M6002X, M6003X)	1.3 µm (M6004X)	2.0 µm (M6001X)	Unit
2-Input NAND Gate Delay	FO = 2, 2 mm Metal	0.45	0.9	0.9	1.4	nsec
Input Buffer Delay	FO = 2, 2 mm Metal	0.6	1.2	1.2	1.4	nsec
Output Buffer Delay	Load: 20 pF	1.9(1)	3.5	2.9	5.5	nsec
	Load: 50 pF	2.3(1)	4.8	4.3	7.7	
	Load: 100 pF	3.9(1)	7	6.5	11.9	
Power Dissipation/Output Buffer	Load: 20 pF	0.6	0.6	0.6	0.6	mW/MHz
	Load: 50 pF	1.3	1.3	1.3	1.3	
	Load: 100 pF	2.5	2.5	2.5	2.5	
Toggle Rate		320	175	175	100	MHz
Power Dissipation per Gate	FO = 2, 2 mm Metal	5	10	10	15	µW/MHz
Input Pin Capacitance	f = 1 MHz	8	8	8	8	pF
Output Pin Capacitance		8	8	8	8	
Bidirectional Pin Capacitance		8	8	8	8	

*V_{DD} = 5 V, T_{opr} = 25°C

Note:

(1) Output buffers for the M6005X and M6006X families have variable drive and slew rates. Choices of Sink Current are 1, 2, 4, 8, and 12 mA and of Source Current are 2 or 6 mA. The selectable slew rate is available on the 8, 12 mA drives. Delays shown are for the 12 mA buffer.

Simultaneous Switching Outputs

To avoid noise caused by simultaneous switching outputs (SSO), Mitsubishi recommends limiting drive to a total of 48 mA for each power/ground pin pair. For the M6005X family this would be:

Buffer	Number of SSOs Allowed Between Power/GND Pin Pairs
12 mA	4
8 mA	8
4 mA	16
2 mA	32
1 mA	48

The total current between power/ground pin pairs is limited to 48 mA. The buffers should be surrounded as close as possible by the power/ground pins on either side of the simultaneously switching group of buffers.

Worst Case Timing for Mitsubishi Gate Arrays

The following factors are used to calculate worst case delays using the typical delay values:

Condition	K (min.)	K (max.)
Temperature -20 to + 75°C	0.82	1.20
Voltage 4.5 to 5.5 volts	0.90	1.10
Process Variation:		
M6005X, M6006X	0.60	1.50
M6002X, M6003X, M6004X	0.60	1.40
M6001X	0.70	1.30
Family	**K (min.)**	**K (max.)**
M6001X	0.57	1.69
M6002X, M6003X, M6004X	0.48	1.82
M6005X, M6006X	0.48	1.98

Performance Characteristics of Mitsubishi Gate Array Library Cells

Cell	Function		M6001X 2.0 μm			M6002X, M6003X 1.3 μm			M6004X 1.3 μm			M6005X, M6006X 1.0 μm		
	Loads		1	2	5	1	2	5	1	2	5	1	2	5
	Metal		1.0	1.5	2.0	1.0	1.5	2.0	1.0	1.5	2.0	0.5	1.0	1.5
VO1S	Inverter	R	0.78	1.18	2.22	0.48	0.68	1.20	0.48	0.68	1.20	0.26	0.38	0.62
		F	0.90	1.13	1.71	0.52	0.65	0.97	0.52	0.65	0.97	0.44	0.54	0.73
N02S	2 NAND	R	0.76	1.18	2.22	0.48	0.68	1.20	0.48	0.68	1.20	0.30	0.42	0.66
		F	1.20	1.50	2.28	0.71	0.89	1.34	0.71	0.89	1.34	0.47	0.61	0.71
R02S	2 NOR	R	1.37	2.12	4.07	0.87	1.25	2.22	0.87	1.25	2.22	0.39	0.60	1.04
		F	0.90	1.13	1.71	0.52	0.65	0.97	0.52	0.65	0.97	0.47	0.57	0.76
N03S	3 NAND	R	0.92	1.32	2.36	0.59	0.79	1.31	0.59	0.79	1.31	0.29	0.41	0.65
		F	1.60	1.94	2.85	1.02	1.25	1.83	.02	1.25	1.83	0.70	0.91	1.35
R03S	3 NOR	R	2.10	3.20	6.00	1.49	2.03	3.43	1.49	2.03	3.43	0.56	0.89	1.50
		F	0.45	1.18	1.76	0.59	0.72	1.04	0.59	0.72	1.040	.46	0.56	0.73
XORS	Exclusive OR	R	1.96	2.62	4.34	1.24	1.57	2.41	1.24	1.57	2.410	.73	0.94	1.33
		F	2.23	2.51	3.26	1.27	1.40	1.76	1.27	1.40	1.76	0.65	0.82	1.12
FDDS	D Latch	R	3.48	3.89	4.96	1.80	2.00	2.52	1.80	2.00	2.52	1.54	1.58	1.67
		F	3.33	3.61	4.32	1.75	1.88	2.20	11.75	1.88	2.20	.75	1.79	1.88
BI1N[5] T54N[6] T22N[7]	TTL Input buffer	R	0.88	1.19	2.00	0.73	0.88	1.27	0.73	0.88	1.27	0.92	0.95	1.00
		F	3.07	4.46	8.38	1.72	1.85	2.21	1.72	1.85	2.21	0.91	0.95	1.01
BC1N[5] C54N[6] C22N[7]	CMOS Input Buffer	R	1.23	1.81	3.30	0.78	0.93	1.32	0.78	0.93	1.32	1.11	1.15	1.22
		F	1.05	1.43	2.40	0.89	1.04	1.43	0.89	1.04	1.43	0.74	0.77	0.84
Load (pF)			20	50	100	20	50	100	20[4]	50[4]	100[4]	20[4]	50[4]	100[4]
BO1N[5] O55N[6, 7]	Output Buffer	R	5.40	8.10	12.6	3.70	5.20	7.70	2.80	4.30	6.80	2.07	2.85	4.15
		F	5.60	7.70	11.2	4.12	5.32	7.32	3.10	4.30	6.30	1.75	2.71	4.31
BZ1N[5] Z77N[6] Z55N[7]	3-State Buffer	R	6.60	9.30	13.8	5.45	6.95	9.45	4.55	6.05	8.55	3.39	4.17	5.47
		F	7.40	9.50	13.0	5.01	6.21	8.21	3.45	4.69	6.69	3.20	4.16	5.76

Notes:

(1) All delays are for typical conditions (V_{DD} = 5 V, T_A = 25°C, and typical process conditions).

(2) Cell delays are rising output on first line and falling output on second line.

(3) Metal interconnect length is in mm.

(4) Performance for 12 mA buffer.

(5) M6001X, M6002X, M6003X.

(6) M6004X.

(7) M6005X, M6006X.

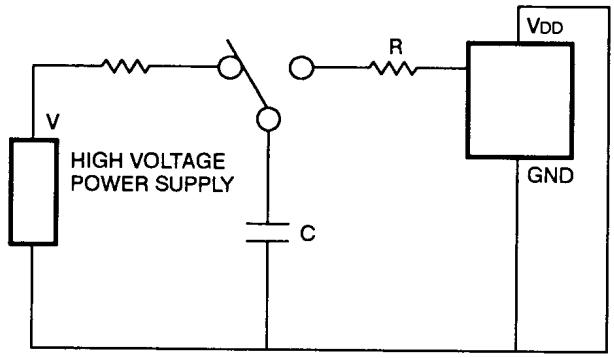
QUALITY AND RELIABILITY

All Mitsubishi gate arrays, except prototypes, undergo static burn-in at 125 degrees Centigrade and 7.0 volts. Burn-in duration varies between 12 and 40 hours, according to the product line maturity, in order to achieve a minimum failure rate for the array. All products, including prototypes, are 100 percent functionally and AC and DC tested.

Mitsubishi uses proprietary I/O protection techniques to enhance electrostatic discharge (ESD) and latch-up immunity. This results in the gate arrays being able to withstand discharges of over +2000 volts from a 100 pF capacitor when tested with 1500 ohms of series resistance, or ± 300 volts from a 200 pF capacitor with zero resistance. Current surges of 200 mA on any pin can be tolerated without latch-up. Test circuit and conditions for ESD and latch-up are shown in Figures 4 and 5.

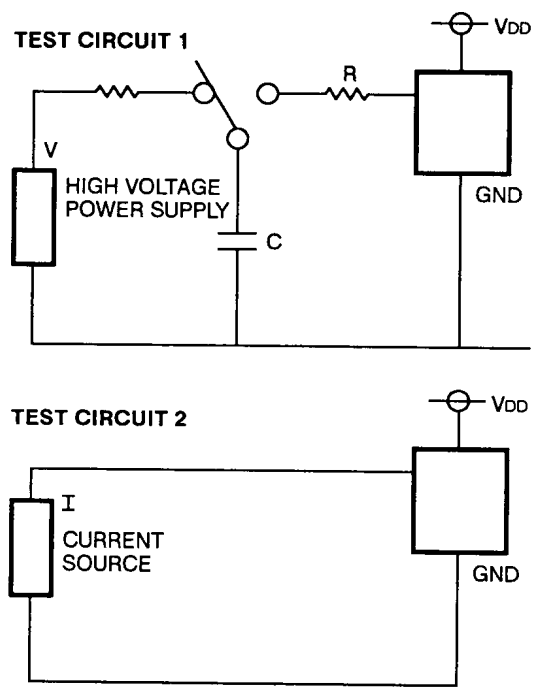
Each Mitsubishi part is internally qualified by being subjected to an accelerated life test, monitoring infant mortality and long-term failures.

Figure 4. Test Circuit and Conditions for ESD in Mitsubishi Gate Arrays



R	C	V
0 ohm	200 pF	± 300 volts
1500 ohm	100 pF	± 2000 volts

Figure 5. Test Circuits and Conditions for Latch-Up in Mitsubishi Gate Arrays



R	C	V
0 ohm	200 pF	± 300 V
1500 ohm	100 pF	± 2000 V

I = + 200mA

Internal Qualification Tests for Mitsubishi Gate Arrays

Test Items	Test Conditions	Failure Identification
Dynamic Life Test	T_A = 125°C, Vcc = 7.0 V, t = 1000 H	DC and functional stability of electrical margin
High Temperature Bias	T_A = 125°C, Vcc = 7.0 V, t = 1000 H, I/O; open	
Dynamic Life Test	T_A = -40°C, Vcc = 7.0 V, t = 1000 H	
Humidity	85°C, 85%, Vcc = 5.5 V output; open, t = 1000 H	
	130°C, 85%, Vcc = 5.5 V output; open, t = 500 H	
	140°C, 85%, storage, t = 240 H	
	Soldering Heat* 260°C, 10 sec x 4 = 40 sec + 85°C, 85% Bias, t = 1000 H	
High Temperature Storage	150°C, t = 1000 H	
Temperature Cycling	-65°C/150°C, 30 min/cycle, 200 cycle	
Soldering Heat	260°C, 10 sec x 4 = 40 sec*	DC and functional stability of electrical margin
Thermal Shock	-55°C/125°C, 10 min/cycle, 15 cycle	
Temperature Cycling	-65°C/150°C, 30 min/cycle, 100 cycle	Visual
Solderability	230°C, 10 sec	Visual
Mechanical Shock	1500 G, 0.5 msec, X1, Y1, Z1	DC and functional
Vibration	20 G, 20-2 KHz, X, Y, Z	Visual

*Leads are immersed up to the base of the outline, 4 directions.

PACKAGING AND THERMAL CHARACTERISTICS

Mitsubishi develops and manufactures its own ASIC packages. Table 13 summarizes the types of surface-mount and through-hole packages offered for Mitsubishi's gate arrays.

Summary of Packages Available for Mitsubishi Gate Arrays

		Number of Pins																									
		16	18	20	24	28	36	40	42	44	52	64	68	80	84	100	120	124	128	136	144	160	177	208	209	256	281	304
Through-Hole Devices	Plastic Standard DIP	•	•	•	•	•		•	•																			
	Plastic Shrink DIP								•		•	•																
	Ceramic Pin-Grid-Array (PGA)																	•					•		•		•	
	Adaptable Plastic Pin-Grid-Array (APGA)														•	•		•			•	•		•				
Surface Mount Devices	Plastic Small Outline Package (SOP)				•		•																					
	Plastic Quad Flat Package (QFP)									•		•		•		•	•		•	•		•		*		*		*
	Plastic Leaded Chip-Carrier (PLCC)									•	•		•		•													

*Available second half of 1990

Package Thermal Resistance — Table 14 shows the thermal resistances for Mitsubishi's gate array packages when mounted on standard printed circuit boards. Chip temperature (Tj) can be determined from the total power consumption (Pt), the thermal resistance (θja) of the package used, and the ambient temperature (TA), by using the formula:

$$T_j = T_A + \theta_{ja}\ (°C/W) \times P_t\ (w)$$

The chip temperature (Tj) must not exceed 100 °C. In order to keep the chip temperature below this limit, the power consumption or ambient temperature should be decreased.

Thermal Resistances of Mitsubishi Gate Arrays with Standard Board Mounting

Package Type	Number of Pins	Thermal Resistance (θja)		
		Natural Air Flow	With 1 m/s Air Flow	With 2 m/s Air Flow
Plastic DIP	16	129	75	70
	18	129	75	(70)
	20	72	(50)	(46)
	24 (300 mil)	86	63	55
	24 (600 mil)	(94)	(65)	(62)
	28	44	36	(32)
	40	63	49	(45)
	42	63	48	(44)
Plastic Shrink DIP	42	63	50	(46)
	52	59	47	(43)
	64	56	45	(42)
Plastic SOP	24	(96)	(76)	(70)
	36	(87)	(69)	(64)
Plastic QFP/APGA*	44	92	74	(68)
	64	87	72	(67)
	80	72	64	(59)
	100	72	(64)	(59)
	128	57	44	40
	160	57	(44)	(40)
	208	47	37	33
PLCC	44	70	50	44
	52	70	50	44
	68	68	55	50
	84	62	48	(44)

*For APGA thermal resistance, use data for the QFP package.

( ): Calculated Value

Standard board: Material composition — Glass epoxy single-surface board
Dimensions — 70 mm x 70 mm, thickness 1.6 mm
Copper foil thickness — 18 μm

GATE ARRAY DESIGN

Mitsubishi Design Kits — Working with major design hardware and software suppliers, Mitsubishi has developed design kits for schematic entry, design rule check and circuit simulation. Software is also available for converting completed designs to a standard format so they can be submitted to Mitsubishi for circuit layout. Mitsubishi's gate array design kits contain the following, as appropriate to the design:

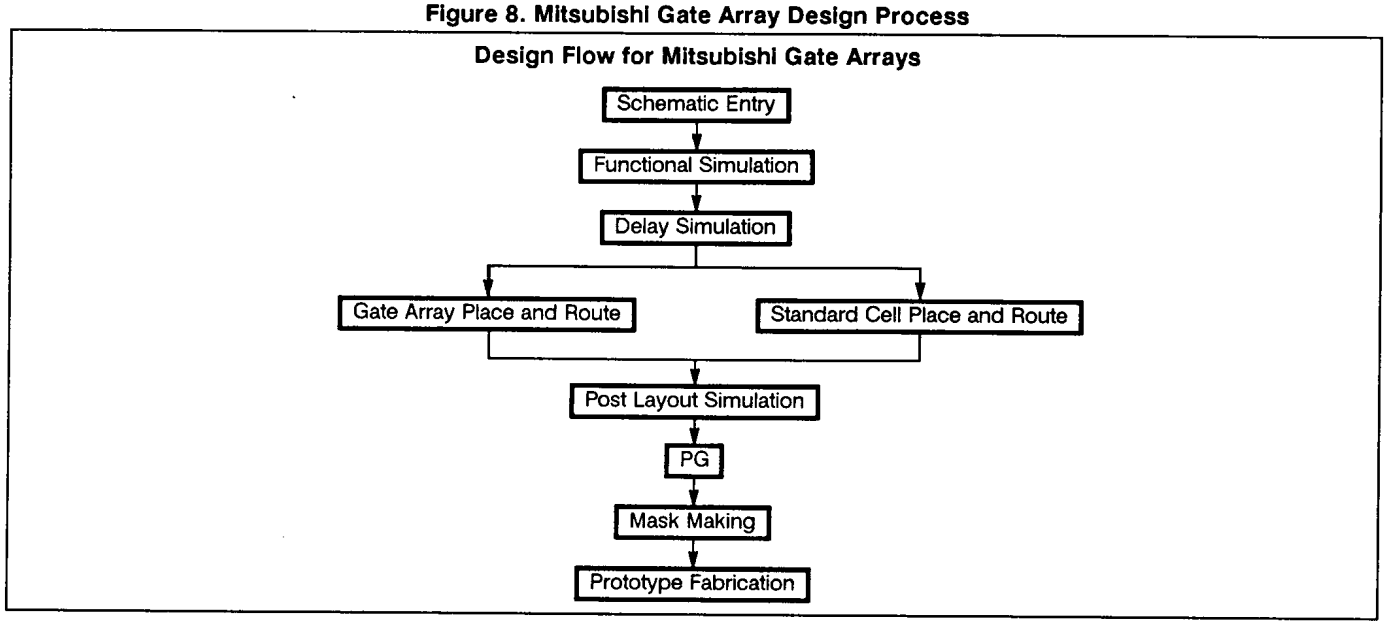
- Symbol Library — Graphic symbols for the Mitsubishi ASIC library used in producing schematics on a workstation or personal computer (PC).
- Simulation Library — Simulation models and time delay data for the ASIC library cells.
- Design Rule Check — Program for checking a workstation or PC schematic for design errors such as fan-out violations, floating nodes, shorted outputs, and illegal or duplicate names.
- Net List Converter — Program for converting a workstation or PC net list to the format used by Mitsubishi to produce circuit layout.
- Test Vector Conversion — Program for converting the simulation vectors to the format used by Mitsubishi production tester programs.
- Compare — Program for comparing simulation output with the expected output values on a workstation or PC, and listing the bits that do not match.
- Back Annotation — Software for converting wire length data from the circuit layout to delay information for the simulator in order to assure accurate simulation based on the final circuit layout.

Hardware and Software CAE Support – The CAE hardware and software supported by Mitsubishi for design of its gate arrays is summarized in Table 15. Figure 8 shows the overall design process for Mitsubishi gate arrays, while Table 16 summarizes Mitsubishi's customer design interface.

Mitsubishi Workstation and Simulator Support for Gate Array Design

Workstation	Schematic Entry	DRC	Functional Simulation	Delay Simulation
Mentor®	X	X	X	X
Dazix™	X	X	X*	X
Valid™	X	X	X	X
Viewlogic™	X	X	X	X
HP 9000®	X		X*	X
Integraph®	X	X	X	X
OrCAD®	X			
FutureNet®	X			
* Support of M6005X not available				
Simulator			**Functional Simulation**	**Delay Simulation**
IKOS®			X	X
Verilog®			X	X
Logic Synthesis	**Design Entry**	**Technology Mapping**	**Design Optimization**	
Synopsys®	X	X	X	

Figure 8. Mitsubishi Gate Array Design Process



Mitsubishi Customer Design Interface

	Schematic & Test Vectors	Schematic Entry	Functional Simulation	Net List & Test Vectors	Timing Simulation	Verification	Routing	Post Layout Simulation	Test Program Generation
Turnkey	C	M/C	M/C	M/C	M/C	M	M	M	M
Net List	C	C	M/C	M/C	M/C	M	M	M	M
Functional Simulation	C	C	C	C	M/C	M	M	M	M
Timing Simulation	C	C	C	C	C	M/C	M	M/C	M

C = Customer Functions on Customers EWS
M = Mitsubishi
M/C = Joint Effort

Mitsubishi Design Network – Mitsubishi operates design centers in Sunnyvale, California; Boston, Massachusetts; and Raleigh, North Carolina and Ottawa, Canada. The centers provide design assistance and access to Mitsubishi supported CAE hardware and software.

The four design centers are linked by satellite to Mitsubishi Electric Corporation's automated gate array production facilities in Kita-Itami and Kumamoto, Japan.

CELL LIBRARIES

Mitsubishi has a gate array cell library of over 500 cells, including macro cells with fixed cell configuration and more complex macro functions. A sample of macro functions is presented in Table 17. Macro functions are designed using macro cells, and layout is done as part of the gate array schematic. A sample of commonly used Mitsubishi macro cells is shown in Table 18.

RAM is implemented with a compiler and can be configured for the required memory size. Word lengths are from 1 to 8 bits. Sizes are in 16 word increments from 16 to 1024 words. Larger sizes are implemented with multiple cells. Dual port RAM is available in the same size cells. The gate count for single RAM cells is less than two gates per bit. Access times vary with cell size, from 8 to 15 nsec.

ROM cells are also compiled to the required size. Sizes are 32 to 2048 words in increments of 32, with word lengths from 1 to 8 bits. Gate counts are about 0.8 gate per bit. Access times for ROM cells are similar to RAM cells at 8 to 15 nsec.

A Sample of the Macro Functions in Mitsubishi's Gate Array Cell Library

Cell Name	LSTTL Equiv	Description	Basic Cells (1)
T04200SA	LS42	BCD: Decimal Decoder	66
T04800SA	LS48	BCD: 7 Segment Decoder/Driver	146
T07500WA	LS75	4-Bit Through Latch	64
T08300WB	LS83	4-Bit Full Adder	137
T08301WA	LS83	4-Bit Full Adder	137
T08500WB	LS85	4-Bit Magnitude Comparator	194
T09000WA	LS90	Decade Counter	157
T09100SA	LS91	8-Bit Shift Register	171
T09101SA	LS91	8-Bit Shift Register	190
T09200WA	LS92	Divide-by-12 Counter	132
T09300SA	LS93	4-Bit Binary Counter	103
T09500WA	LS95	4-Bit Parallel Register	135
T09600WA	LS96	5-Bit Shift Register	157
T13700SA	LS137	3:8 Decoder/Demux with Latch	95
T13800SA	LS138	3:8 Decoder/Demux	60
T13800WA	LS138	3:8 Decoder/Demux	130
T13900SA	LS139	2:4 Decoder/Demux	54
T13901SA	LS139	2:4 Decoder/Demux	26
T14700WB	LS147	10-Dec: 4-BCD Priority Encoder	115
T14800WB	LS148	8:3 Priority Encoder	163
T15100WA	LS151	8:1 Data Selector/Mux	77
T15300WA	LS153	4:1 Data Selector/Mux	82
T15301SB	LS153	4:1 Data Selector/Mux	35
T15500SA	LS155	2-Bit Binary: 4-Dec Demux with Strobe	56
T15700SA	LS157	2:1 Data Selector/Mux	40
T15700WA	LS157	2:1 Data Selector/Mux	49
T15800WA	LS158	2:1 Data Selector/Mux	53
T16000WA	LS160	Synchronous Presettable Decade Counter with Reset	225
T16100WB	LS161	Synchronous Presettable 4-Bit Counter with Reset	212
T16200WA	LS162	Fully Synchronous Presettable Decade Counter	194
T16300WA	LS163	Synchronous 4-Bit Binary Counter	199
T16400SA	LS164	8-Bit Serial-In/Parallel-Out Shift Retgister	211
T16500WA	LS165	8-Bit Parallel-In/Serial-Out Shift Register	268
T16600WA	LS166	8-Bit Shift Register	247
T17300WA	LS173	4-Bit D-Type Register with 3-State Output	172
T17400SA	LS174	Hex D Flip-Flop with Reset	151
T17500SA	LS175	Quad D Flip-Flop with Reset	100

Cell Name	LSTTL Equiv	Description	Basic Cells (1)
T18100SB	LS181	ALU/Function Generator	341
T18200SB	LS182	Look-Ahead Carry Generator	95
T19000WA	LS190	Synchronous Presettable Up-Down Decade Counter	288
T19100WA	LS191	Synchronous Presettable Up-Down 4-Bit Counter	278
T19200WA	LS192	Synchronous Presettable Up-Down Decade Counter	230
T19300WA	LS193	Synchronous Presettable Up-Down 4-Bit Counter	229
T19400WB	LS194	4-bit Bidirectional Universal Shift Register	208
T19500WA	LS195	Parallel Access Shift Register with Reset	176
T19600WA	LS196	Presettable Decade Counter/Latch	222
T19700SA	LS197	Presettable 4-Bit Binary Counter/Latch	192
T24800WA	LS248	BCD: 7-Segment Decoder/Driver	157
T25100WA	LS251	8:1 Data Selector/Mux with 3-State Output	100
T25700WA	LS257	2:1 Data Selector/Mux with 3-State Output	84
T25800WA	LS258	Quad 2:1 Data Selector/Mux with 3-State Output	71
T27300WA	LS273	Octal Positive Edge-Triggered D Flip-Flop with Reset	202
T28000WB	LS280	9-Bit Odd/Even Parity Generator/Checker	159
T28001WA	LS280	9-Bit Even Parity Generator/Checker	72
T28002WA	LS280	9-Bit Odd Parity Generator/Checker	72
T29500WA	LS295	4-Bit Shift Register with 3-State Output	162
T29800WA	LS298	Quad 2-Input Mux with Storage	122
T35200WA	LS352	Dual 4:1 Data Selector/Mux with Strobe	74
T35300WA	LS353	Dual 4:1 Data Selector/Mux with 3-State Output	94
T36700WA	LS367	Hex Bus Driver with 3-State Output	72
T36800WA	LS368	Hex Bus Driver with 3-State Output (Inverter)	84
T37300WA	LS373	Octal Positive Edge D Flip-Flop with 3-State Output	193
T37400WA	LS374	Octal Positive Edge D Flip-Flop with 3-State Output	287
T37700WA	LS377	Octal Positive Edge D Flip-Flop with Enable	244
T39000WA	LS390	Dual Decade Counter	135
T39300SA	LS393	Dual 4-Bit Binary Counter	214
T39500WA	LS395	4-Bit Cascadable Shift Register	179
T49000WA	LS490	Dual 4-Bit Decade Counter	165
T59500WA	LS595	8-Bit Shift Register/Latch with 3-State Output	451
T66800WA	LS668	Synchronous Presettable Up-Down Counter	285
T66900WB	LS669	Synchronous 4-Bit Up-Down Counter	261
T67001WB	LS670	4 x 4 Register Files with 3-State Output	505
T68401WA	LS684	8-Bit Magnitude Comparator	224
T68801WA	LS688	8-Bit Magnitude Comparator with Enable	130

Note:

(1) A basic cell is the pair of correspoinding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.

A Sample of the Macro Cells in Mitsubishi's Gate Array Cell Library

Cell Name	Drive	Description	Basic Cells (1)	Availability 2.0 µm	1.3 µm	1.0 µm
INVERTERS						
V01S		Inverter	2	X	X	X
V01W	X2	Inverter	3	X	X	X
V01T	X3	Inverter	4			X
V01Q	X4	Inverter	5	X	X	X
DRIVERS						
K0ZW	X2	Driver, 3-State, High Enable	9	X	X	X
K0ZQ	X4	Driver, 3-State, High Enable	11			X
K1NS		Driver, Clock Line	3	X	X	X
K1NW	X2	Driver, Clock Line	4	X	X	X
K1NQ	X4	Driver, Clock Line	6	X	X	X
K1ZW	X2	Driver, 3-State, L Enable	9	X	X	X
K1ZQ	X4	Driver, 3-State, Low Enable	11			X
K2GW	X2	Driver, Clock Line, Gated	5	X	X	P
KH1S		Driver, 3-State, Active High	7	X	X	P
KH4S		Driver, 3-State, Active High, 4 Bit	19	X	X	P
KH1W	X2	Driver, 3-State, H Enable	9			X
KH4W	X2	Driver, 3-State, H Enable, 4 Bit	25			X
KH8W	X2	Driver, 3-State, H Enable, 8 Bit	53			X
KL1S		Driver, 3-State, Active Low	7	X	X	P
KL4S		Driver, 3-State, Active Low, 4 Bit	19	X	X	P
KL1W	X2	Driver, 3-State, L Enable	9			X
KL4W	X2	Driver, 3-State, L Enable, 4 Bit	25			X
KL8W	X2	Driver, 3-State, L Enable, 8 Bit	53			X
AND GATES						
AN2S		AND Gate, 2 Input	4	X	X	X
AN2W	X2	AND Gate, 2 Input	5	X	X	X
AN3S		AND Gate, 3 Input	5	X	X	X
AN3W	X2	AND Gate, 3 Input	6	X	X	X
AN4S		AND Gate, 4 Input	6	X	X	X
AN4W	X2	AND Gate, 4 Input	7	X	X	X
NAND GATES						
NO2S		NAND Gate, 2 Input	3	X	X	X
NO22	X2	NAND Gate, 2 Input	5			X
NO23	X3	NAND Gate, 2 Input	7			X
NO24	X4	NAND Gate, 2 Input	9			X
NO2W	X2	NAND Gate, 2 Input	6	X	X	X
NO3S		NAND Gate, 3 Input	4	X	X	X
NO32	X2	NAND Gate, 3 Input	7			X
NO33	X3	NAND Gate, 3 Input	10			X
NO34	X4	NAND Gate, 3 Input	13			X
NO3W	X2	NAND Gate, 3 Input	7	X	X	X
NO4S		NAND Gate, 4 Input	5	X	X	X
NO42	X2	NAND Gate, 4 Input	9			X
NO43	X3	NAND Gate, 4 Input	13			X
NO44	X4	NAND Gate, 4 Input	18			X
NO4W	X2	NAND Gate, 4 Input	8	X	X	X
NO5S		NAND Gate, 5 Input	6	X	X	X
NO52	X2	NAND Gate, 5 Input	13			X
NO6W	X2	NAND Gate, 6 Input	12	X	X	X
NO8W	X2	NAND Gate, 8 Input	14	X	X	X
NO9W	X2	NAND, 9 Input	16	X	X	
N12W	X2	NAND, 12 Input	19	X	X	
N16W	X2	NAND, 16 Input	25	X	X	
OR GATES						
OR2S		OR Gate, 2 Input	4	X	X	X
OR2W	X2	OR Gate, 2 Input	5	X	X	X
OR3S		OR Gate, 3 Input	5	X	X	X
OR3W	X2	OR Gate, 3 Input	6	X	X	X
OR4S		OR Gate, 4 Input	6	X	X	X
OR4W	X2	OR Gate, 4 Input	7	X	X	X
NOR GATES						
RO2S		NOR Gate, 2 Input	3	X	X	X
RO22	X2	NOR Gate, 2 Input	5			X
RO23	X3	NOR Gate, 2 Input	7			X
RO24	X4	NOR Gate, 2 Input	9			X
RO2W	X2	NOR Gate, 2 Input	6	X	X	X
RO3S		NOR Gate, 3 Input	4	X	X	X
RO32	X2	NOR Gate, 3 Input	7			X
RO33	X3	NOR Gate, 3 Input	10			X
RO34	X4	NOR Gate, 3 Input	13			X
RO3W	X2	NOR Gate, 3 Input	7	X	X	X
RO4S		NOR Gate, 4 Input	5	X	X	X
RO42	X2	NOR Gate, 4 Input	9			X
RO43	X3	NOR Gate, 4 Input	13			X
RO44	X4	NOR Gate, 4 Input	18			X
RO4W	X2	NOR Gate, 4 Input	8	X	X	X
RO6W	X2	NOR Gate, 6 Input	12	X	X	X
RO8W	X2	NOR Gate, 8 Input	14	X	X	
RO9W	X2	NOR Gate, 9 Input	16	X	X	
R12W	X2	NOR Gate, 12 Input	19	X	X	
R16W	X2	NOR Gate, 16 Input	25	X	X	

Cell Name	Drive	Description	Basic Cells (1)	Availability 2.0 µm	1.3 µm	1.0 µm
EXCLUSIVE OR/NOR						
XORS		Exclusive OR	6	X	X	X
XORW	X2	Exclusive OR	8	X	X	X
XNOS		Exclusive NOR	6	X	X	X
XNOW	X2	Exclusive NOR	8	X	X	X
XOR2	X2	Exclusive OR	11			X
XNO2	X2	Exclusive NOR	11			X
COMBINATIONAL GATES						
A01S		2 Input OR Into 2 Input AND Into 2 Input NOR	5	X	X	X
A012	X2	2 Input OR Into 2 Input AND Into 2 Input NOR	10			X
A23S		2 Input AND Into 2 Input NOR	4	X	X	X
A232	X2	2 Input AND Into 2 Input NOR	7			X
A24S		2 Input AND Into 3 Input NOR	5	X	X	X
A242	X2	2 Input AND Into 3 Input NOR	9			X
A34S		3 Input AND Into 2 Input NOR	5	X	X	X
A342	X2	3 Input AND Into 2 Input NOR	9			X
O01S		2 Input AND Into 2 Input OR Into 2 Input NAND	5	X	X	X
O012	X2	2 Input AND Into 2 Input OR Into 2 Input NAND	10			X
O23S		2 Input OR Into 2 Input NAND	4	X	X	X
O232	X2	2 Input OR Into 2 Input NAND	7			X
O24S		2 Input OR Into 3 Input NAND	5	X	X	X
O242	X2	2 Input OR Into 3 Input NAND	9			X
O34S		3 Input OR Into 2 Input NAND	5	X	X	X
O342	X2	3 Input OR Into 2 Input NAND	9			X
MULTIPLEXERS						
LM1W	X2	2 Wide 2 Input AND Into 2 Input OR	7	X	X	X
LM2W	X2	2 AND 3 Input AND Into 2 Input OR	8	X	X	X
T24S		2 Wide 2 Input AND Into 2 Input NOR	5	X	X	X
T242	X2	2 Wide 2 Input AND Into 2 Input NOR	9			X
T26S		3 Wide 2 Input AND Into 3 Input NOR	7	X	X	X
T262	X2	3 Wide 2 Input AND Into 3 Input NOR	13			X
T28W	X2	4 Wide 2 Input AND Into 4 Input NOR	13	X	X	X
T2GW	X2	8 Wide 2 Input AND Into 8 Input NOR	25	X	X	
T36W	X2	2 Wide 3 Input AND Into 2 Input NOR	10	X	X	X
T39W	X2	3 Wide 3 Input AND Into 3 Input NOR	14	X	X	P
T3CW	X2	4 Wide 3 Input AND Into 4 Input NOR	17	X	X	
T48W	X2	2 Wide 4 Input AND Into 2 Input NOR	12	X	X	X
T4CW	X2	3 Wide 4 Input AND Into 3 Input NOR	18	X	X	
T4GW	X2	4 Wide 4 Input AND Into 4 Input NOR	22	X	X	
U24S		2 Wide 2 Input OR Into 2 Input NAND	5	X	X	X
U242	X2	2 Wide 2 Input OR Into 2 Input NAND	9			X
U26S		3 Wide 2 Input OR Into 3 Input NAND	7	X	X	X
U262	X2	3 Wide 2 Input OR Into 3 Input NAND	13			X
U28W	X2	4 Wide 2 Input OR Into 4 Input NAND	13	X	X	X
U2CW	X2	6 Wide 2 Input OR Into 6 Input NAND	21	X	X	
U2GW	X2	8 Wide 2 Input OR Into 8 Input NAND	25	X	X	
U36W	X2	2 Wide 3 Input OR Into 2 Input NAND	10	X	X	X
U39W	X2	3 Wide 3 Input OR Into 3 Input NAND	14	X	X	P
U3CW	X2	4 Wide 3 Input OR Into 4 Input NAND	17	X	X	
U48W	X2	2 Wide 4 Input OR Into 2 Input NAND	12	X	X	X
ADDERS						
AD2S		Adder, Full, 2 Bit	35	X	X	X
SFAW	X2	Adder, Full, 1 Bit	19	X	X	X
SHAW	X2	Adder, Half, 1 Bit	10	X	X	X
SHAS		Adder, Half, 1 Bit	9	X	X	P
SFAS		Adder, Full, 1 Bit	18	X	X	P
SA2S		Adder, Full, 2 Bit	49	X	X	P
SA3S		Adder, Full, 2 Bit	41	X	X	P
SELECTORS						
D12S		Selector, Dual 1 to 2	9	X	X	X
D122	X2	Selector, Dual 1 to 2	16			X
D21S		Selector, Dual 2 to 1	9	X	X	X
D21W	X2	Selector, Dual 2 to 1	11			X
S12S		Selector, 1 to 2	5	X	X	X
S122	X2	Selector, 1 to 2	8			X
S21S		Selector, 2 to 1	5	X	X	X
S212	X2	Selector, 2 to 1	11			X
S21B		Selector, 2 to 1	6	X	X	X
S21W	X2	Selector, 2 to 1	6	X	X	X
S24S		Selector, 2 to 1, 4 Bit	35	X	X	X
S24W	X2	Selector, 2 to 1, 4 Bit	52	X	X	X
S34W	X2	Selector, 3 to 1, 4 Bit	40	X	X	X
S41S		Selector, 4 to 1	12	X	X	X
S44W	X2	Selector, 4 to 1, 4 Bit	52	X	X	X
DECODERS						
D2GW		Decoder, 2 to 4 With Output Enable	24	X	X	X
D2GS		Decoder, 2 to 4 With Output Enable	24	X	X	X
D3GS		Decoder, 3 to 8	51	X	X	P

Table 18. A Sample of the Macro Cells in Mitsubishi's Gate Array Cell Library (continued)

Cell Name	Drive	Description	Basic Cells (1)	Availability 2.0 µm	1.3 µm	1.0 µm
DECODERS(continued)						
D4GS		Decoder, 4 to 16	97	X	X	P
LATCHES						
FDAS		D Latch, NAND Type	12	X	X	X
FDAW	X2	D Latch, NAND Type	13	X	X	X
FLAS		RS Latch, NAND Type	8	X	X	X
FLA2	X2	RS Latch, NAND Type	13			X
FLOS		RS Latch, NOR Type	8	X	X	X
FLO2	X2	RS Latch, NOR Type	15			X
HLAS		Half Latch, NAND Type	11	X	X	X
HLAW	X2	Half Latch, NAND Type	12	X	X	X
HLBS		Half Latch	10	X	X	X
HLBW	X2	Half Latch	11	X	X	X
HLOS		Half Latch, NOR Type	12	X	X	X
HLOW	X2	Half Latch, NOR Type	13	X	X	X
LF1S		D Latch, Hazard Free	12	X	X	X
LF1W	X2	D Latch, Hazard Free	14	X	X	X
LF4S		D Latch, 4 Bit	52	X	X	X
LF4W	X2	D Latch, 4 Bit	57	X	X	X
LFAS		D Latch, 4 Bit	39	X	X	X
LFAW	X2	D Latch, 4 Bit	45	X	X	X
LFBS		D Latch, 4 Bit	42	X	X	X
LFBW	X2	D Latch, 4 Bit	47	X	X	X
FLIP-FLOPS						
FD1S		D Flip-Flop, + Negative Edge Trigger	19	X	X	X
FD1W	X2	D Flip-Flop, + Negative Edge Trigger	21	X	X	X
FD2S		D Flip-Flop With Set, + Negative Edge Trigger	21	X	X	X
FD2W	X2	D Flip-Flop With Set, + Negative Edge Trigger	23	X	X	X
FD3S		D Flip-Flop With Reset, + Negative Edge Trigger	21	X	X	X
FD3W	X2	D Flip-Flop With Reset, + Negative Edge Trigger	23	X	X	X
FD4S		D Flip-Flop With Set and Reset, + Negative Edge Trigger	23	X	X	X
FD4W	X2	D Flip-Flop With Set and Reset, + Negative Edge Trigger	25	X	X	X
FD7S		D Flip-Flop With Reset, + Edge Trigger	23	X	X	X
FD7W	X2	D Flip-Flop With Reset, + Edge Trigger	24	X	X	X
FD8W	X2	D Flip-Flop With Set and Reset, + Edge Trigger	26	X	X	X
FDBS		D Flip-Flop	15	X	X	X
FDBW	X2	D Flip-Flop	17	X	X	X
FDCS		D Flip-Flop With Set	19	X	X	X
FDCW	X2	D Flip-Flop With Set	21	X	X	X
FDDS		D Flip-Flop With Reset	19	X	X	X
FDDW	X2	D Flip-Flop With Reset	21	X	X	X
FDES		D Flip-Flop With Set and Reset	21	X	X	X
FDEW	X2	D Flip-Flop With Set and Reset	23	X	X	X
FDFS		D Flip-Flop and Latch	22	X	X	X
FDFW	X2	D Flip-Flop and Latch	24	X	X	X
FDQS		D Flip-Flop, 4 Bit, With Reset	85	X	X	X
FDQW	X2	D Flip-Flop, 4 Bit, With Reset	89	X	X	X
FDRS		D Flip-Flop, 4 Bit	60	X	X	X
FDRW	X2	D Flip-Flop, 4 Bit	67	X	X	X
FDSS		D Flip-Flop, 4 Bit, With Reset	75	X	X	X
FDSW	X2	D Flip-Flop, 4 Bit, With Reset	79	X	X	X
FJBS		JK Flip-Flop	22	X	X	X
FJBW	X2	JK Flip-Flop	23	X	X	X
FJES		JK Flip-Flop With Set and Reset, + Edge Trigger	29	X	X	X
FJEW	X2	JK Flip-Flop With Set and Reset, + Edge Trigger	30	X	X	X
FJ3W	X2	JK Flip-Flop With Reset, Master-Slave	28	X	X	P
FJ4W	X2	JK Flip-Flop With Set and Reset, Master-Slave	30	X	X	P
FJAS		JK Flip-Flop With Set and Reset, Positive Edge Triggered	32	X	X	P
FJ7W	X2	JK Flip-Flop, With Reset, Positive Edge Triggered	29	X	X	P
COUNTERS						
CA1S		Counter, 1 Bit With Reset + Edge Trigger	23	X	X	X
CA1W	X2	Counter, 1 Bit With Reset + Edge Trigger	24	X	X	X
CA2S		Counter, 1 Bit	20	X	X	X
CA2W	X2	Counter, 1 Bit	22	X	X	X
FC1S		Counter, 4 Bit + Binery Asynchronous Up	66	X	X	X
FC1W	X2	Counter, 4 Bit + Binery Asynchronous Up	70	X	X	X
FT7S		Counter, 1 Bit With Direct Reset	27	X	X	X
FT7W	X2	Counter, 1 Bit With Direct Reset	28	X	X	X

Cell Name	Drive	Description	Basic Cells (1)	Availability 2.0 µm	1.3 µm	1.0 µm
PULSE GENERATORS						
PGN1		Edge Sensitive Pulse Generator	23	X	X	P
PGN2		Edge Sensitive Pulse Generator	34	X	X	P
PGN3		Edge Sensitive Pulse Generator	45	X	X	P
PGN4		Edge Sensitive Pulse Generator	56	X	X	P
PGN5		Edge Sensitive Pulse Generator	67	X	X	P
PGN6		Edge Sensitive Pulse Generator	78	X	X	P
PGR1		Edge Sensitive Pulse Generator	23	X	X	P
PGR2		Edge Sensitive Pulse Generator	34	X	X	P
PGR3		Edge Sensitive Pulse Generator	45	X	X	P
PGR4		Edge Sensitive Pulse Generator	56	X	X	P
PGR5		Edge Sensitive Pulse Generator	67	X	X	P
PGR6		Edge Sensitive Pulse Generator	78	X	X	P
SHIFT REGISTERS						
FR1S		Shift Registers, 4 Bit, Serial-In Parallel-Out	41	X	X	X
FR2S		Shift Register, 4 Bit, Serial-In Parallel-Out, With Synchronous Load	97	X	X	P
FR3S		Shift Register, 4 Bit, Serial-In Parallel-Out, With Synchronous Load	82	X	X	P
I/O BUFFERS						
C22N		Buffer, Input, CMOS	0			X
C52N		Buffer, Input/Output, CMOS Input	0			X
C54N		Buffer, Input/Output, CMOS Input	0			X
C75N		Buffer, Input/Output, CMOS Input	19			X
C77N		Buffer, Input/Output, CMOS Input	19			X
C88N		Buffer, Input, CMOS, With Pull-Up	0			X
CBEN		Buffer, Input, CMOS, With Pull-Down	0			X
O52N		Buffer, Output	0			X
O54N		Buffer, Output	0			X
O75N		Buffer, Output	0			X
O77N		Buffer, Output	0			X
T22N		Buffer, Input, TTL	0			X
T52N		Buffer, Input/Output, TTL Input	0			X
T54N		Buffer, Input/Output, TTL Input	0			X
T75N		Buffer, Input/Output, TTL Input	19			X
T77N		Buffer, Input/Output, TTL Input	19			X
T88N		Buffer, Input, TTL With Pull-Up	0			X
TBEN		Buffer, Input, TTL With Pull-Down	0			X
Z24N		Buffer, Output, L Level Out Open Drain	0			X
Z25N		Buffer, Output, L Level Out Open Drain	0			X
Z26N		Buffer, Output, L Level Out Open Drain	0			X
Z27N		Buffer, Output, L Level Out Open Drain	0			X
Z34N		Buffer, Output, H Level Out Open Drain	0			X
Z46N		Buffer, Output, H Level Out Open Drain	0			X
Z52N		Buffer, Output, 3-State	0			X
Z54N		Buffer, Output, 3-State	0			X
Z75N		Buffer, Output, 3-State	19			X
Z77N		Buffer, Output, 3-State	19			X
BOSN		Buffer, Oscillator	4	X	X	
BI1N		Buffer, Input, TTL	0	X	X	
BK1N		Buffer, Input, Clock Line, TTL	5	X	X	
BC1N		Buffer, Input, CMOS	0	X	X	
BS1N		Buffer, Input, TTL, Schmitt Trigger	14	X	X	
BCSN		Buffer, Input, CMOS, Schmitt Trigger	12	X	X	
BPUN		Buffer, Input, TTL With Resistor Pull-Up	0	X	X	
BPDN		Buffer, Input, TTL With Resistor Pull-Down	0	X	X	
BO1N		Buffer, Output	0	X	X	
BZ1N		Buffer, Output, 3-State	12	X	X	
BPON		Buffer, Output, Source-Only	0	X	X	
BNON		Buffer, Output, Sink-Only	0	X	X	
BR1N		Buffer, Input/Output, 3-State, TTL Input	12	X	X	
BQ1N		Buffer, Input/Output, 3-State, CMOS Input	12	X	X	
BSDT		Buffer, Input, TTL Schmitt In, Pull-Down	14	X	X	
BSUT		Buffer, Input, TTL Schmitt In, Pull-Up	14	X	X	
BUCN		Buffer, Input, CMOS Input, Pull-Up	0	X	X	
BDCN		Buffer, Input, CMOS Input, Pull-Down	0	X	X	
BSUC		Buffer, Input, CMOS Schmitt In, Pull-Up	12	X	X	
BSDC		Buffer, Input, CMOS Schmitt In, Pull-Down	12	X	X	
BSRN		Buffer, Input/Output, 3-State, TTL Schmitt In	26	X	X	
BSQN		Buffer, Input/Output, 3-State, CMOS Schmitt In	24	X	X	
VDD AND GND						
ZHHH		VDD	1	X	X	X
ZLLL		GND	1	X	X	X

Note:

(1) A basic cell is the pair of corresponding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.

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