M5M5V32R16J,TP-10,-12,-15

1997.01.22

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

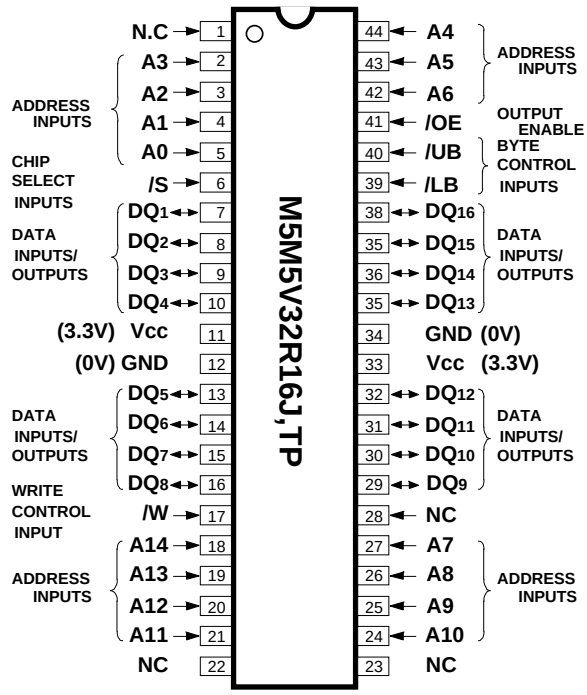
524288-BIT (32768-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V32R16 is a family of 32768-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible.

They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controled either togethe or separately by /LB and /UB.

PIN CONFIGURATION (TOP VIEW)



Outline 44P0K(J)
44P3W-H(TP)

FEATURES

- Fast access time M5M5V32R16J,TP-10 ---10ns(max)
  M5M5V32R16J,TP-12 --- 12ns(max)
  M5M5V32R16J,TP-15 --- 15ns(max)
- Low power dissipation Active --------- 297mW(typ)
  Stand by ------- 0.33mW(typ)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by /S
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs
- Separate control of lower and upper bytes by /LB and /UB

APPLICATION

High-speed memory system

PACKAGE

M5M5V32R16J : 44pin 400mil SOJ
M5M5V32R16VP: 44pin 400mil TSOP(II)

FUNCTION

The operation mode of the M5M5V32R16 is determined by a combination of the device control inputs /S, /W, /OE, /LB, and /UB. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with low level /LB and/or low level /UB and low level /S. The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the traling edge of /W, /LB, /UB or /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting W at a high level and /OE at a low level while /LB and/or /UB and /S are in an active state. (/LB and/or /UB=L, /S=L)

When setting /LB at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting /UB at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

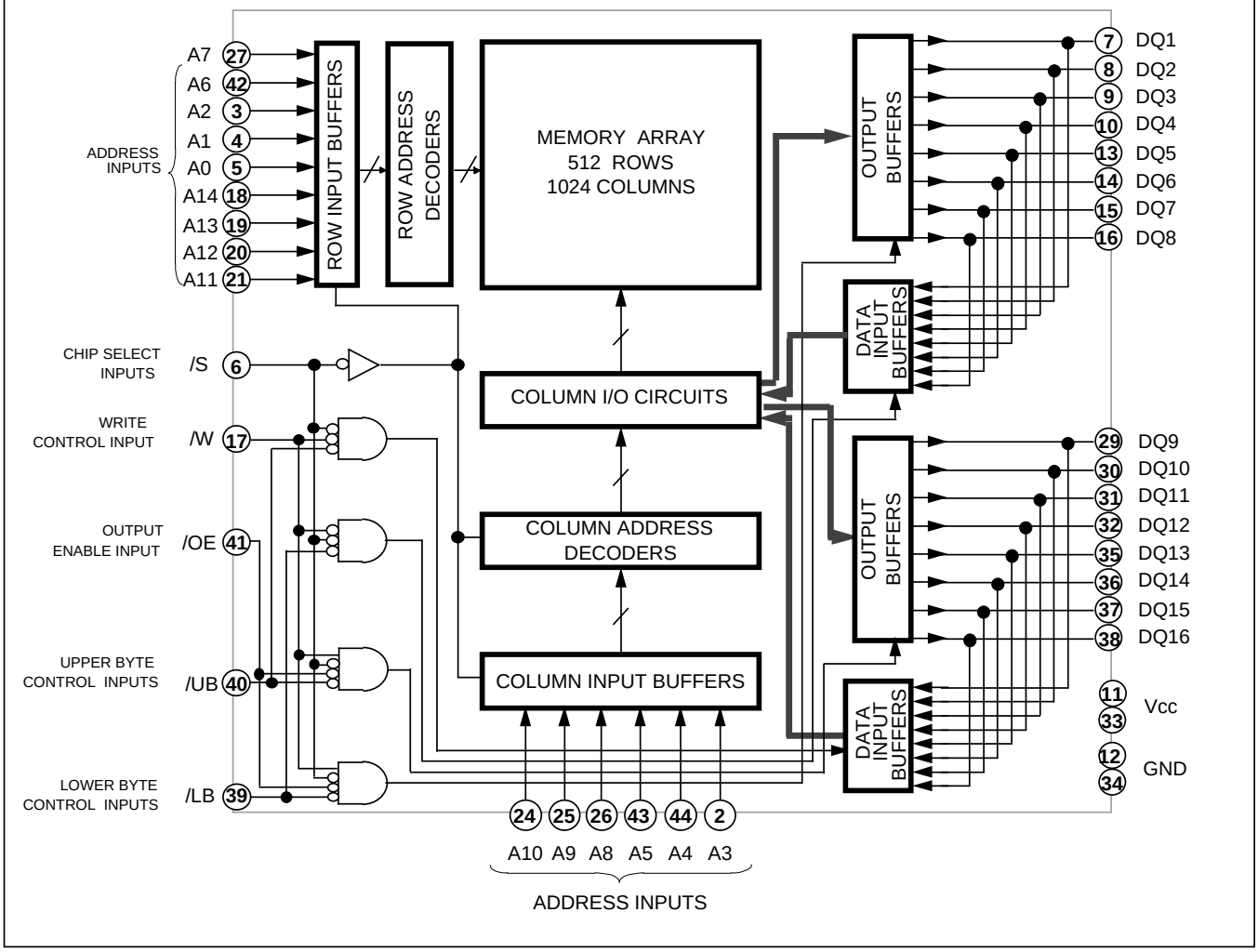
When setting /LB and /UB at a high level or /S at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /LB, /UB and /S.

Signal-/S controls the power-down feature. When /S goes high, power dissapation is reduced extremely. The access time from /S is equivalent to the address access time.

FUNCTION TABLE

/S	/W	/OE	/LB	/UB	Mode	DQ1 - 8	DQ9 - 16	Icc
L	H	L	L	L	Read cycle All Bytes	D OUT	D OUT	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D OUT	Active
L	H	L	L	H	Read cycle Lower Bytes	D OUT	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D IN	D IN	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D IN	Active
L	L	X	L	H	Write cycle Lower Bytes	D IN	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-2.0* ~ 4.6	V
V_I	Input voltage		-2.0* ~ Vcc+0.5	V
V_O	Output voltage		-2.0* ~ Vcc	V
Pd	Power dissipation	Ta=25℃	1000	mW
Topr	Operating temperature		0 ~ 70	℃
Tstg(bias)	Storage temperature(bias)		-10 ~ 85	℃
Tstg	Storage temperature		-65 ~ 150	℃

* Pulse width ≦ 20ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Condition		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage			-0.3*		0.8	V
V_{OH}	High-level output voltage	IOH = - 4mA		2.4			V
V_{OL}	Low-level output voltage	IOL= 8mA				0.4	V
I_I	Input current	V_I = 0 ~ Vcc				2	µA
|IOZ|	Output current in off-state	VI (/S)= VIH VO= 0 ~ Vcc				10	µA
I_{CC1}	Active supply current (TTL level)	VI (/S)= VIL other inputs VIH or VIL Output-open(duty 100%)	AC(10ns cycle)			150	mA
			AC(12ns cycle)			130	
			AC(15ns cycle)			110	
			DC		90	100	
I_{CC2}	Stand-by supply current (TTL level)	VI (/S)= VIH	AC(10ns cycle)			60	mA
			AC(12ns cycle)			55	
			AC(15ns cycle)			50	
			DC			40	
I_{CC3}	Stand-by current (MOS level)	VI (/S)= Vcc≧ 0.2V other inputs VI ≦ 0.2V or VI ≧ Vcc - 0.2V			0.1	1	mA

* Pulse width ≦ 20ns, in case of AC : - 3.0V

CAPACITANCE (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test Condition	Limit Min	Limit Typ	Limit Max	Unit
C_I	Input capacitance	V_I =GND,V_i =25mVrms,f=1MHz			6	pF
C_O	Output capacitance	V_O =GND,V_o =25mVrms,f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=3.3V,Ta=25℃
3: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

(1) MEASUREMENT CONDITION

Input pulse levels ---------- V_{IH} =3.0V, V_{IL} =0.0V
Input rise and fall time ---------- 3ns
Input timing reference levels ---------- V_{IH} =1.5V, V_{IL} =1.5V
Output timing reference levels ---------- V_{OH} =1.5V, V_{OL} =1.5V
Output loads ---------- Fig1,Fig2

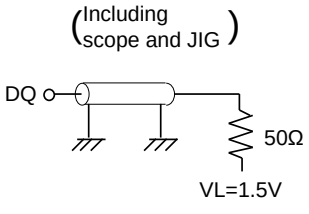


Fig.1 Output load

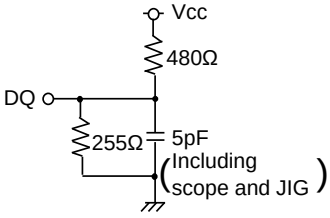


Fig.2 Output load for ten , tdis

READ CYCLE

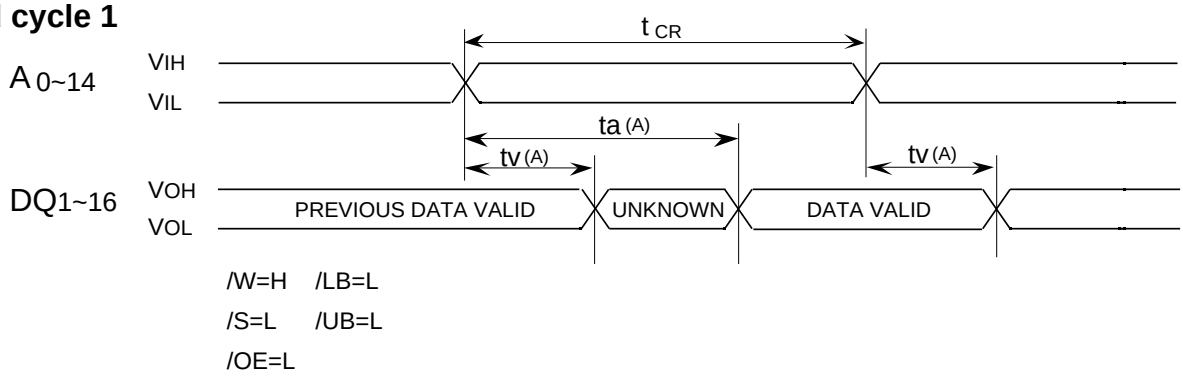
Symbol	Parameter	Limits						Unit
		M5M5V32R16 -10		M5M5V32R16 -12		M5M5V32R16 -15		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	10		12		15		ns
ta (A)	Address access time		10		12		15	ns
ta (S)	Chip select access time		10		12		15	ns
ta (OE)	Output enable access time		5		6		7	ns
ta (B)	/LB,/UB access time		5		6		7	ns
tdis (S)	Output disable time after /S high	0	5	0	6	0	7	ns
tdis (OE)	Output disable time after /OE high	0	5	0	6	0	7	ns
tdis (B)	Output disable time after /LB,/UB high	0	5	0	6	0	7	ns
ten (S)	Output enable time after /S low	4		4		4		ns
ten (OE)	Output enable time after /OE low	3		3		3		ns
ten (B)	Output enable time after /LB,/UB low	3		3		3		ns
tv (A)	Data valid time after address change		4		4		4	ns
tPU	Power-up time after chip selection	0		0		0		ns
tPD	Power down time after chip selection		10		12		15	ns

Write cycle

Symbol	Parameter	Limits						Unit
		M5M5V32R16 -10		M5M5V32R16 -12		M5M5V32R16 -15		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	10		12		15		ns
tw(W)	Write pulse width	9		10		12		ns
tsu(B)	/LB,/UB setup time	9		10		12		ns
tsu(A)1	Address setup time(/W)	0		0		0		ns
tsu(A)2	Address setup time(/S)	0		0		0		ns
tsu(S)	Chip select setup time	9		10		12		ns
tsu(D)	Data setup time	5		6		7		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	0		0		0		ns
tdis(W)	Output disable time after /W low	0	5	0	6	0	7	ns
tdis (OE)	Output disable time after /OE high	0	5	0	6	0	7	ns
ten (W)	Output enable time after /W high	0		0		0		ns
ten (OE)	Output enable time after /OE low	0		0		0		ns
ten (B)	Output enable time after /LB,/UB low	0		0		0		ns
tsu(A-WH)	Address to /W High	9		10		12		ns
tsu(A-SH)	Address to /S High	9		10		12		ns
tsu (A-BH)	Address to /LB,/UB High	9		10		12		ns

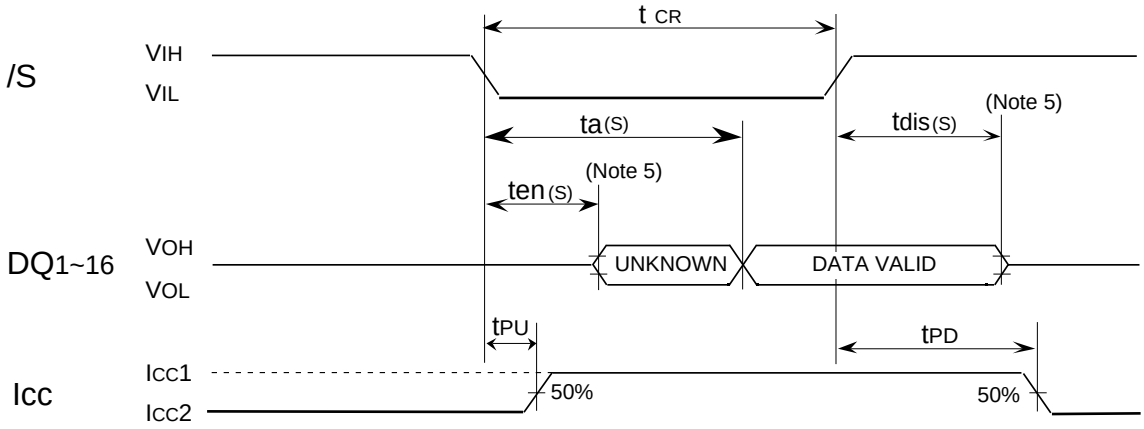
(4)TIMING DIAGRAMS

Read cycle 1



/W=H /LB=L
/S=L /UB=L
/OE=L

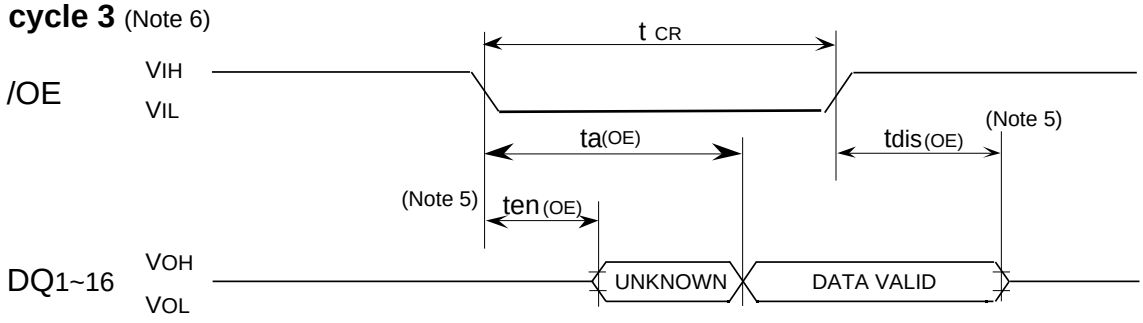
Read cycle 2 (Note 4)



/W=H /UB=L
/OE=L /LB=L

Note 4. Addresses valid prior to or coincident with /S transition low.
5. Transition is measured ±500mv from steady state voltage with specified loading in Figure 2.

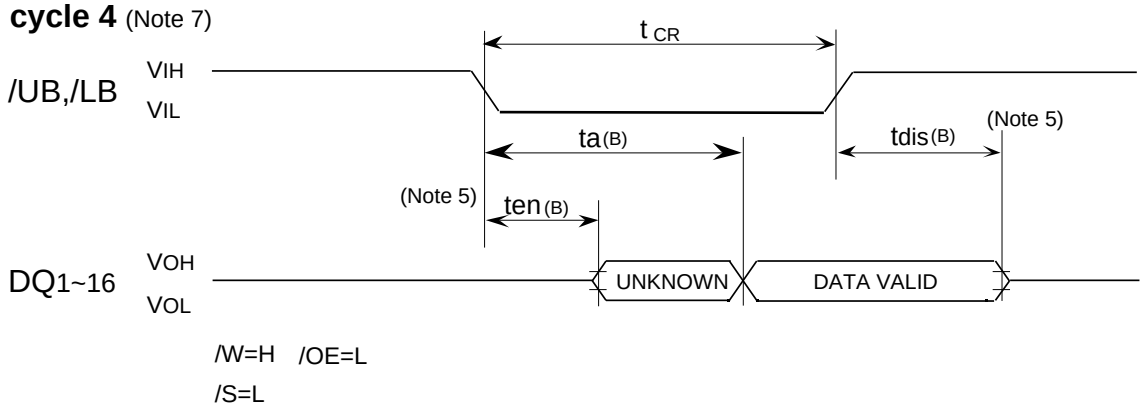
Read cycle 3 (Note 6)



/W=H /UB=L
/S=L /LB=L

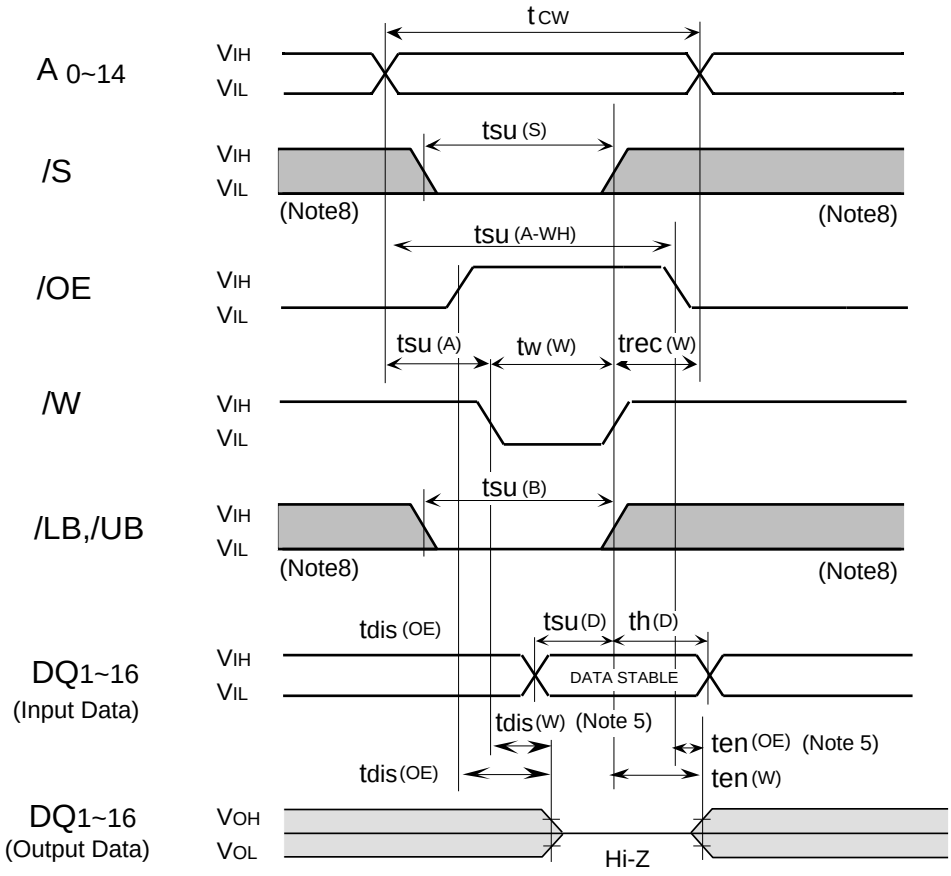
Note 6. Addresses and /S valid prior to /OE transition low by (ta(A)-ta(OE)), (ta(S)-ta(OE))

Read cycle 4 (Note 7)



Note 7. Addresses , /S and /OE valid prior to /LB,/UB transition low by (ta(A)-ta(B)), (ta(S)-ta(B)), (ta(OE)-ta(B)).

Write cycle (/W control mode)

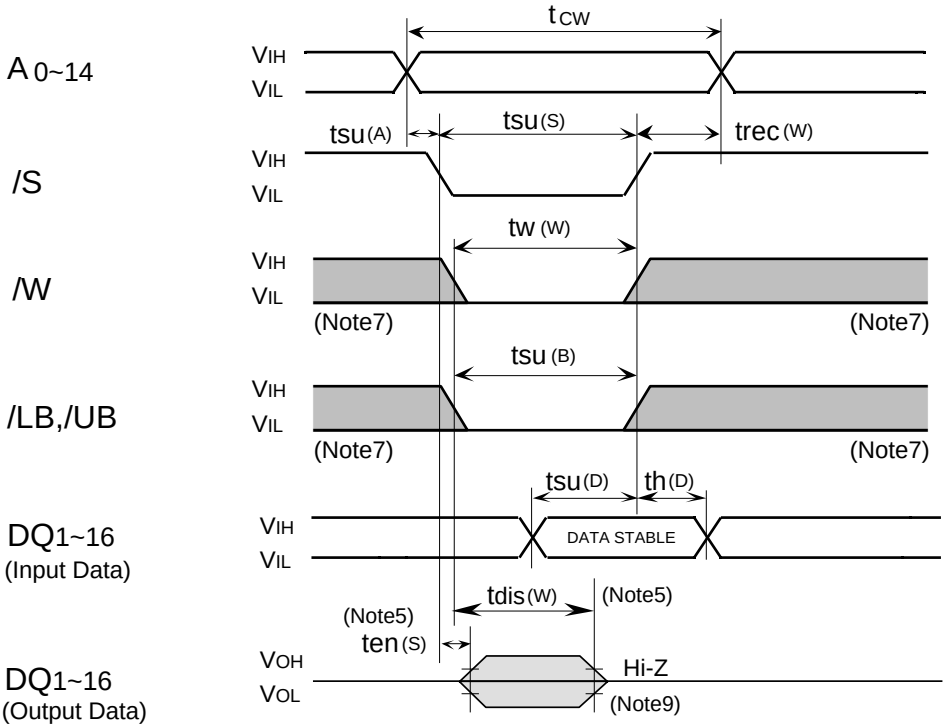


Note 8: Hatching indicates the state is don't care.

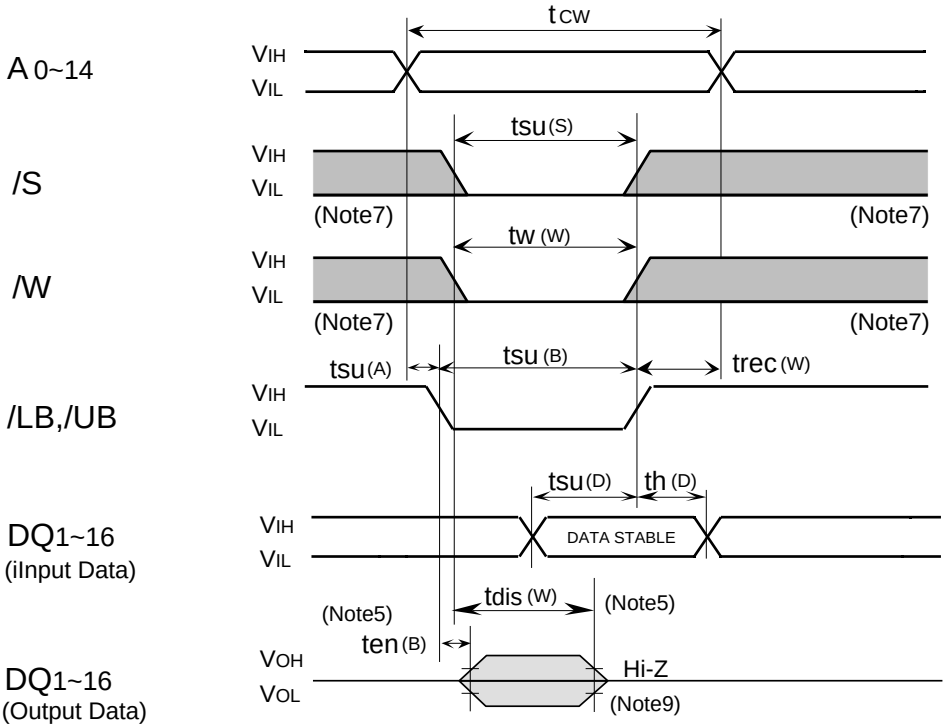
9: When the falling edge of /W is simultaneous or prior to the falling edge of /S, the output is maintained in the high impedance.

10: ten,tdis are periodically sampled and are not 100% tested.

Write cycle(/S control)



Write cycle(/LB,/UB control)



'96.11.20	P3	Vref --> 5.0V	k.kubo
'97.01.22	P3	Output loads=50Ω	k.kubo
'97.02.04	P3	Vref --> Vcc	k.kubo