M5M5V208FP,VP,RV,KV,KR -70L-W , -85L -W, -10L-W , -12L-W , -70LL-W, -85LL-W, -10LL-W, -12LL-W

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V208 is 2,097,152-bit CMOS static RAM organized as 262,144-words by 8-bit which is fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor(TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5V208 is designed for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5V208VP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).Two types of devices are available.
VP,KV(normal lead bend type package),RV,KR(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5V208FP,VP,RV,KV,KR-70L	70ns	27mA (Vcc=3.6V)	60µA (Vcc=3.6V)
M5M5V208FP,VP,RV,KV,KR-85L	85ns		
M5M5V208FP,VP,RV,KV,KR-10L	100ns		
M5M5V208FP,VP,RV,KV,KR-12L	120ns		
M5M5V208FP,VP,RV,KV,KR-70LL	70ns		10µ A (Vcc=3.6V)
M5M5V208FP,VP,RV,KV,KR-85LL	85ns		
M5M5V208FP,VP,RV,KV,KR-10LL	100ns		
M5M5V208FP,VP,RV,KV,KR-12LL	120ns		

- Single 2.7 ~ 3.6V power supply
- W-version: operating temperature of -20 to +70°C
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by S1 & S2
- Data retention supply voltage=2.0V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current · · · · · · · · · · 0.3µA(typ.)

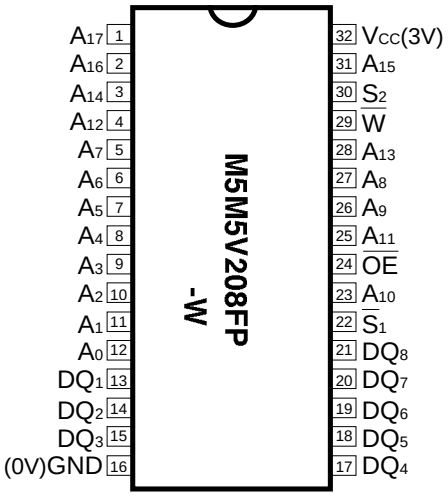
PACKAGE

M5M5V208FP : 32 pin 525 mil SOP
M5M5V208VP,RV : 32pin 8 X 20 mm2 TSOP
M5M5V208KV,KR : 32pin 8 X 13.4 mm2 TSOP

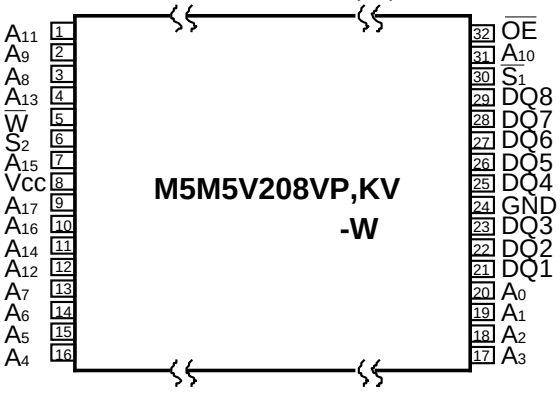
APPLICATION

Small capacity memory units
Battery operating system
Handheld communiation tools

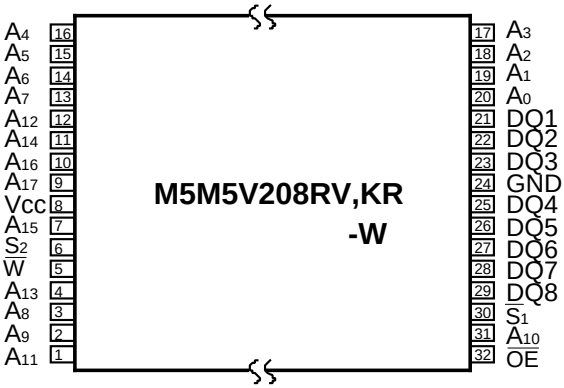
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV), 32P3K-C(KR)

M5M5V208FP,VP,RV,KV,KR -70L-W , -85L -W, -10L-W , -12L-W , -70LL-W, -85LL-W, -10LL-W, -12LL-W

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5V208 is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

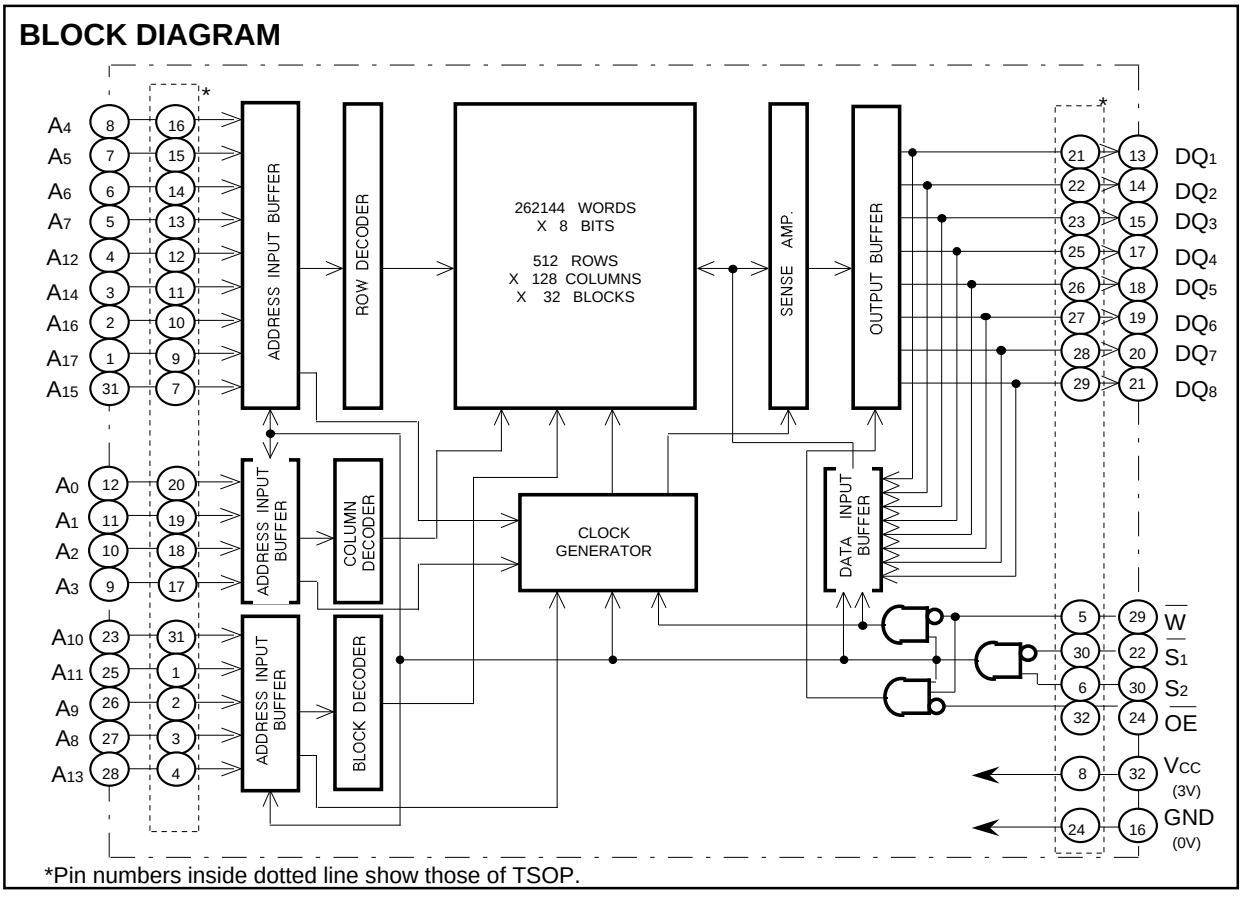
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state (S_1 = L ,S_2 = H).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ or S_2. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Standby
H	X	X	X	Non selection	High-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



*Pin numbers inside dotted line show those of TSOP.

M5M5V208FP,VP,RV,KV,KR -70L-W , -85L -W, -10L-W , -12L-W , -70LL-W, -85LL-W, -10LL-W, -12LL-W

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	– 0.5*~4.6	V
V_I	Input voltage		– 0.5* ~ Vcc + 0.5 (Max 4.6)	V
V_O	Output voltage		0 ~ Vcc	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		– 20 ~ 70	°C
Tstr	Storage temperature		– 65 ~150	°C

* –3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Ta=– 20~70°C, Vcc= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage				–0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}= –0.5mA			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= –0.05mA			Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA					0.4	V
I_I	Input current	V_I=0 ~ Vcc					±1	µA
I_O	Output current in off-state	$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 ~ Vcc					±1	µA
Icc1	Active supply current (CMOS-level Input)	$\overline{S_1}$ ≤ 0.2V, S_2≥ Vcc-0.2V, other inputs ≤ 0.2V or ≥ Vcc-0.2V,output-open		f= 10MHz		20	25	mA
				f= 5MHz		10	13	
Icc2	Active supply current (TTL-level Input)	$\overline{S_1}$=V_{IL},S_2=V_{IH}, other inputs=V_{IH} or V_{IL} output-open		f= 10MHz		22	27	mA
				f= 5MHz		12	15	
Icc3	Stand-by current	1) S_2 ≤ 0.2V or 2) $\overline{S_1}$ ≥ Vcc-0.2V, S_2 ≥ Vcc-0.2V other inputs=0 ~ Vcc	-L	-20 ~ +70°C			60	µA
			-LL	-20 ~ +70°C			10	
				-20 ~ +40°C			1	
				+25°C		0.3	0.6	
Icc4	Stand-by current	$\overline{S_1}$=V_{IH} or S_2=V_{IL},other inputs=0 ~ Vcc					0.33	mA

* –3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE

(Ta=– 20 ~ 70°C, Vcc= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			7	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is for Vcc = 3V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS

(Ta =– 20 ~ 70°C, Vcc= 2.7 ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Vcc ..... 2.7 ~ 3.6V
Input pulse level ..... V_{IH}=2.2V,V_{IL}=0.4V
Input rise and fall time 5ns
Reference level ..... V_{OH}=V_{OL}=1.5V
Output loads ..... Fig.1,CL=30pF
CL=5pF (for ten,tdis)
Transition is measured ±500mV from steady state voltage. (for ten,tdis)

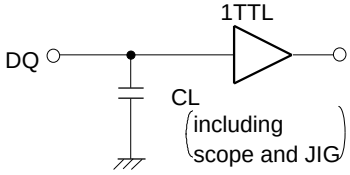


Fig.1 Output load

(2) READ CYCLE

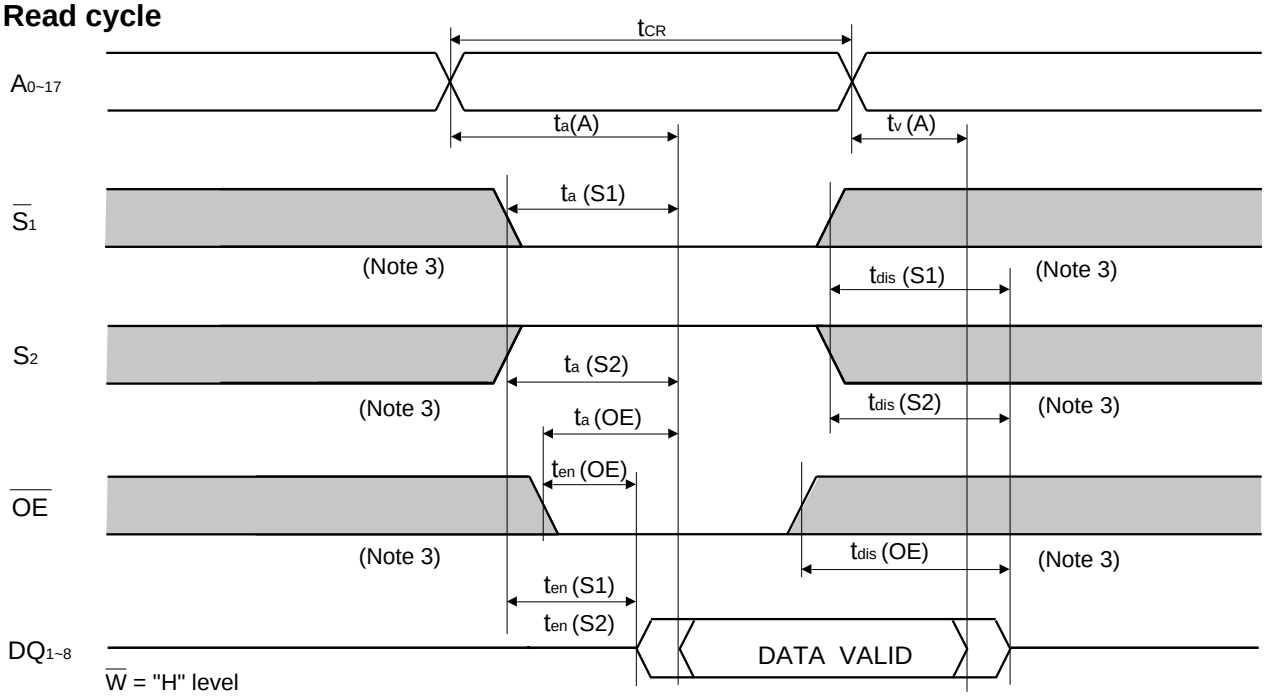
Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		ns
t_a(A)	Address access time		70		85		100		120	ns
t_a(S_1)	Chip select 1 access time		70		85		100		120	ns
t_a(S_2)	Chip select 2 access time		70		85		100		120	ns
t_a(OE)	Output enable access time		35		45		50		60	ns
t_{dis}(S_1)	Output disable time after $\overline{S_1}$ high		25		30		35		40	ns
t_{dis}(S_2)	Output disable time after S_2 low		25		30		35		40	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		25		30		35		40	ns
t_{en}(S_1)	Output enable time after $\overline{S_1}$ low	10		10		10		10		ns
t_{en}(S_2)	Output enable time after S_2 high	10		10		10		10		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
t_v(A)	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

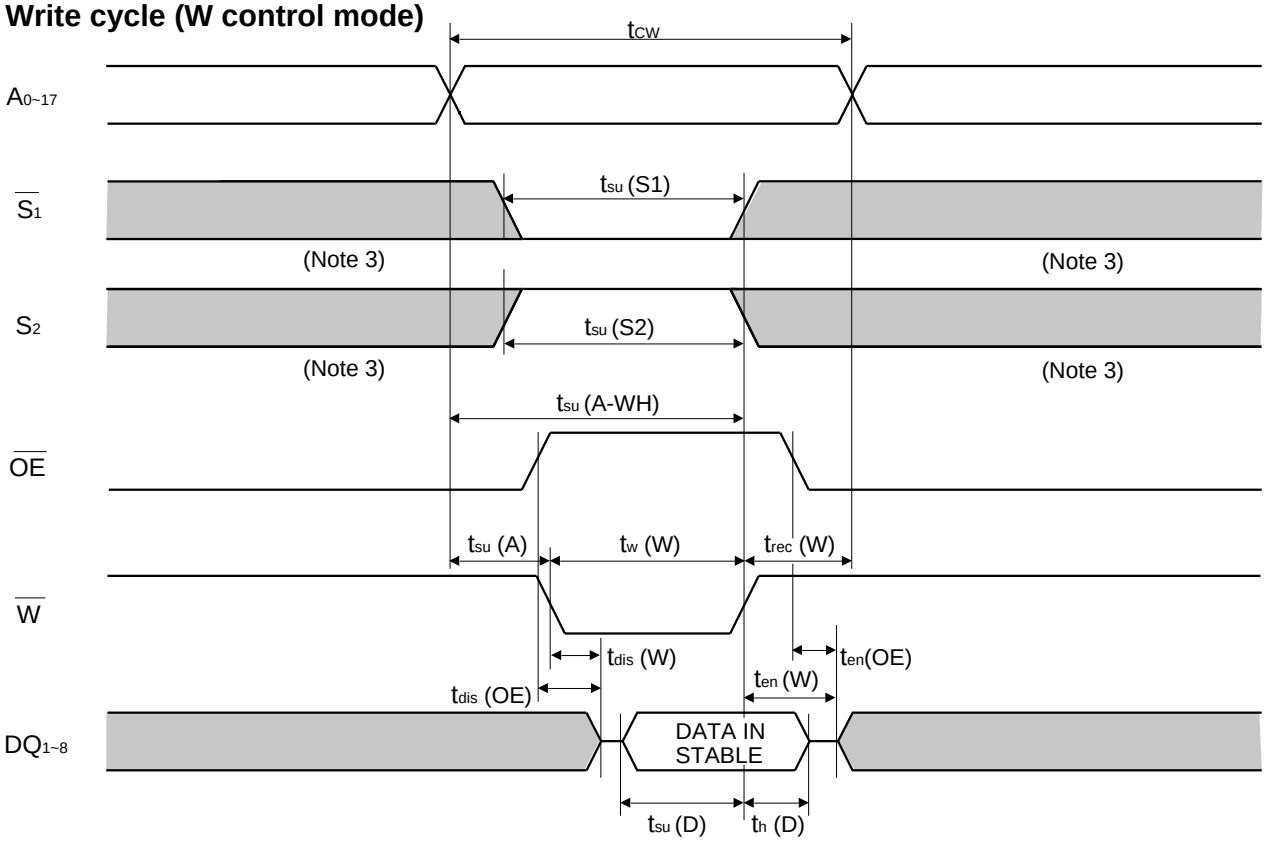
Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		ns
t_w(W)	Write pulse width	55		60		75		85		ns
t_{su}(A)	Address setup time	0		0		0		0		ns
t_{su}(A-WH)	Address setup time with respect to $\overline{W}$	65		70		85		100		ns
t_{su}(S_1)	Chip select 1 setup time	65		70		85		100		ns
t_{su}(S_2)	Chip select 2 setup time	65		70		85		100		ns
t_{su}(D)	Data setup time	30		35		40		45		ns
t_h(D)	Data hold time	0		0		0		0		ns
t_{rec}(W)	Write recovery time	0		0		0		0		ns
t_{dis}(W)	Output disable time from $\overline{W}$ low		25		30		35		40	ns
t_{dis}(OE)	Output disable time from $\overline{OE}$ high		25		30		35		40	ns
t_{en}(W)	Output enable time from $\overline{W}$ high	5		5		5		5		ns
t_{en}(OE)	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

(4) TIMING DIAGRAMS

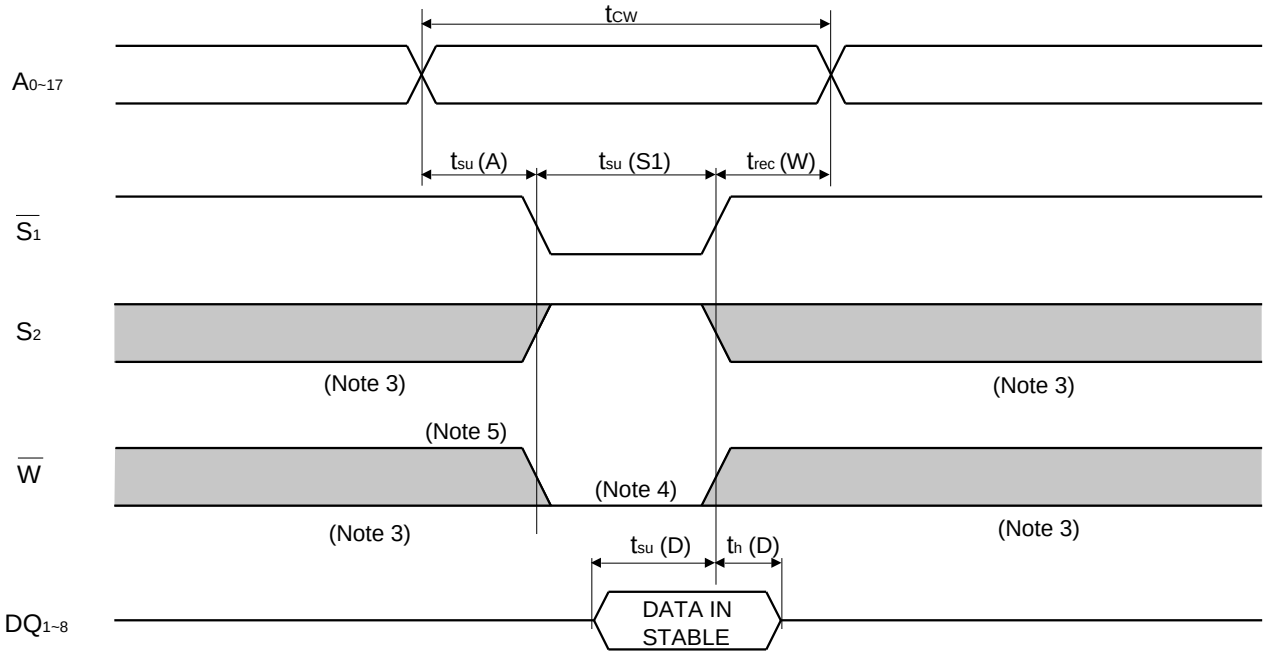
Read cycle



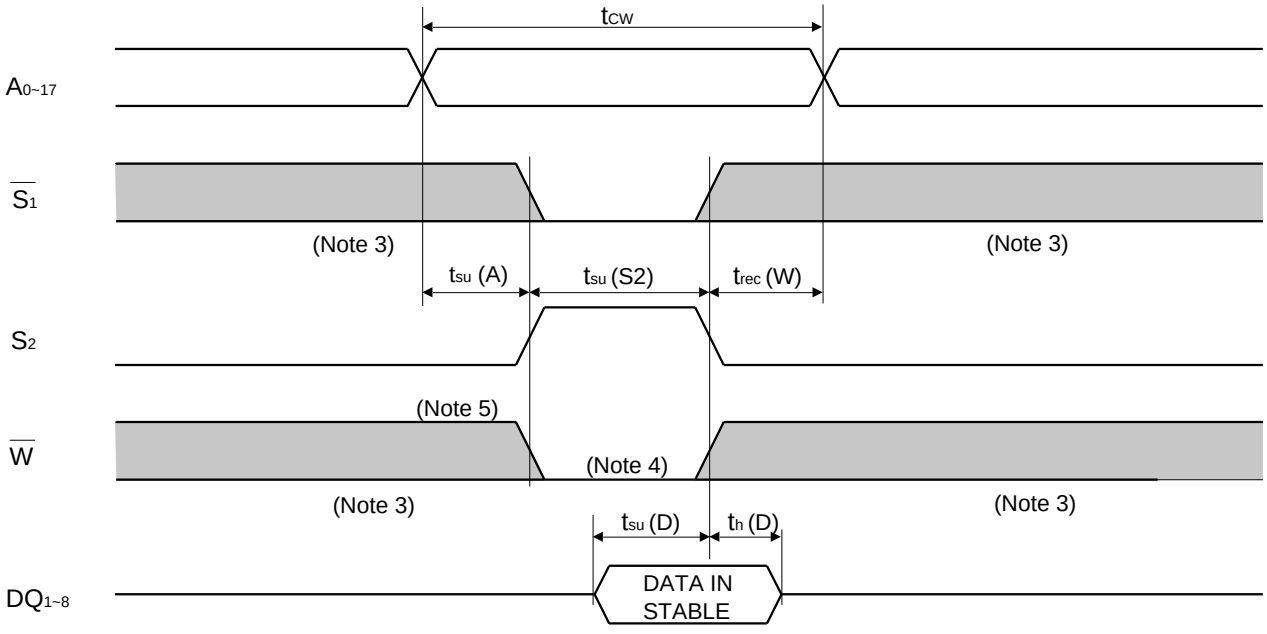
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S2 high overlaps S1 and W low.
5: When the falling edge of W is simultaneously or prior to the falling edge of S1 or rising edge of S2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

(Ta = – 20 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S1})}$	Chip select input $\overline{S_1}$			2.0			V
$V_{I\ (S2)}$	Chip select input S_2					0.2	V
$I_{CC\ (PD)}$	Power down supply current	Vcc = 3.0V $S_2 \le 0.2V$ or $\overline{S_1} \ge Vcc - 0.2V, S_2 \ge Vcc - 0.2V$	-L			50	µA
			-LL		0.3	8 (Note 7)	

Note7: ICC (PD) = 0.5µA (Max.) in case of Ta = +25°C

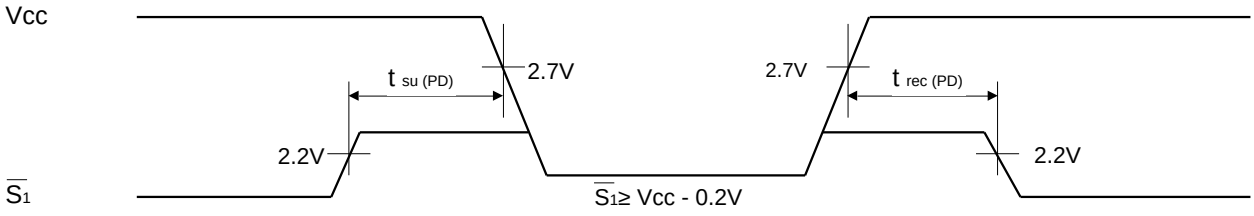
(2) TIMING REQUIREMENTS

(Ta = – 20 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode