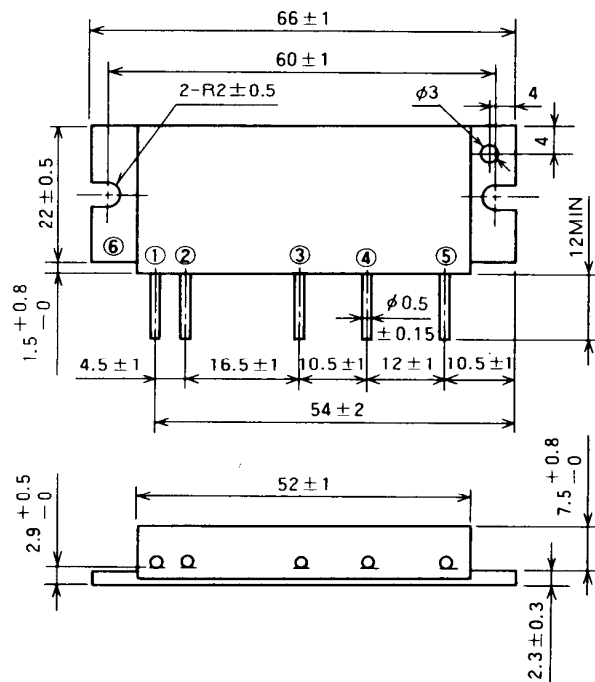


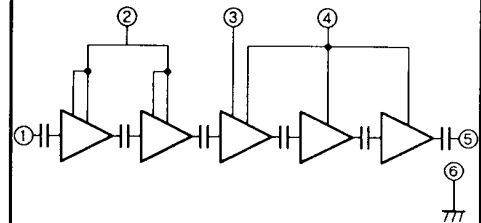
OUTLINE DRAWING

Dimensions in mm



H3

BLOCK DIAGRAM



PIN :

- ① P_{in} : RF INPUT
- ② V_{CC1} : 1st. DC SUPPLY
- ③ V_{BB} : BASE BIAS SUPPLY
- ④ V_{CC2} : 2nd. DC SUPPLY
- ⑤ P_o : RF OUTPUT
- ⑥ GND : FIN

ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage		13	V
V_{CC2}			17	V
V_{BB}	Base bias		9	V
I_{CC}	Total current	$Z_G = Z_L = 50\ \Omega$	5	A
$P_{in(max)}$	Input power	$Z_G = Z_L = 50\ \Omega$, $V_{CC1} \leq 12.5\text{V}$	10	mW
$P_{o(max)}$	Output power	$Z_G = Z_L = 50\ \Omega$	20	W
$T_{c(OP)}$	Operation case temperature		- 30 to 110	$^\circ\text{C}$
T_{stg}	Storage temperature		- 40 to 110	$^\circ\text{C}$

Note. Above parameters are guaranteed independently.

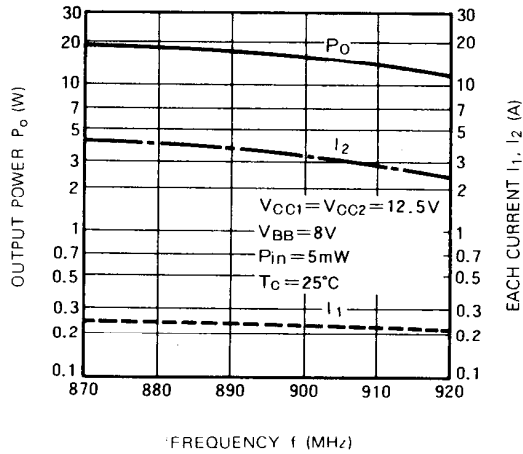
ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	$V_{CC1} = V_{CC2} = 12.5$, $V_{BB} = 8\text{V}$ $P_{in} = 5\text{mW}$ $Z_G = Z_L = 50\ \Omega$	889	915	MHz
P_o	Output power		12		W
η_T	Total efficiency		30		%
2fo	2nd. harmonic			- 30	dBc
ρ_{in}	Input VSWR			2.8	-
-	Load VSWR tolerance	$V_{CC1}=12.5\text{V}$, $V_{CC2}=15.2\text{V}$, $V_{BB}=8\text{V}$ $P_o = 12\text{W}$ (P_{in} : controlled), $Z_G = 50\ \Omega$ Load VSWR=20:1 (All phase), 5sec.	No degradation or destroy		-

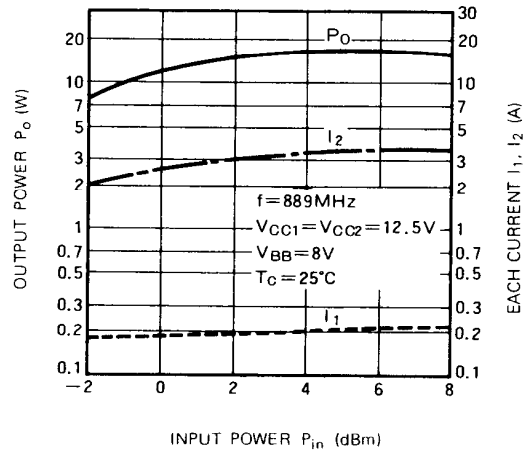
Note. Above parameters, ratings, limits and conditions are subject to change.

TYPICAL PERFORMANCE DATA

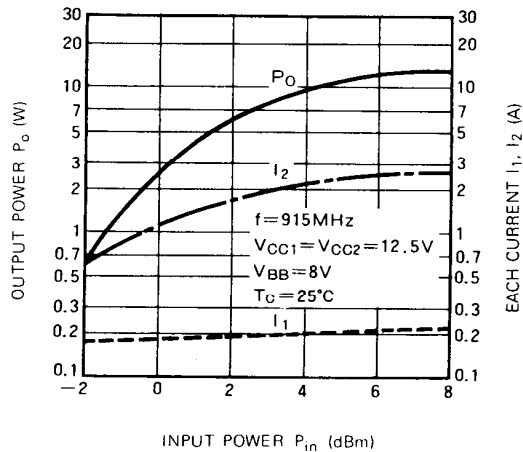
OUTPUT POWER, EACH CURRENT
VS. FREQUENCY



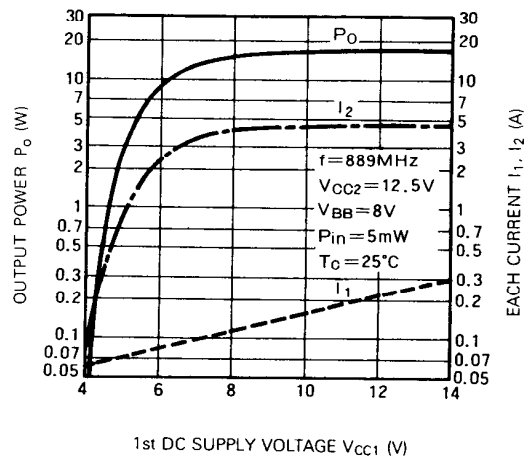
OUTPUT POWER, EACH CURRENT
VS. INPUT POWER



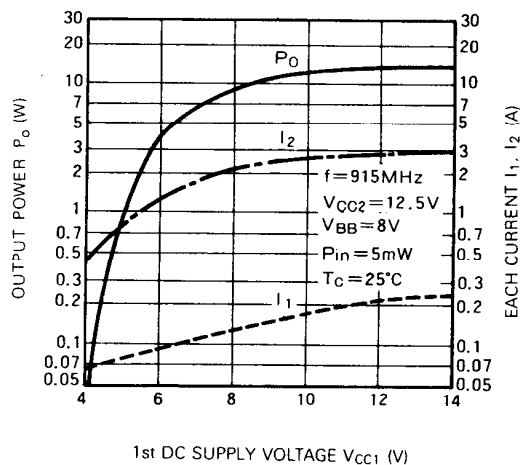
OUTPUT POWER, EACH CURRENT
VS. INPUT POWER



OUTPUT POWER, EACH CURRENT
VS. 1st DC SUPPLY VOLTAGE



OUTPUT POWER, EACH CURRENT
VS. 1st DC SUPPLY VOLTAGE



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to the following consideration when designing a heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistances between junction of incorporated transistors and case are shown in the followings.

a) First stage transistor

$$R_{th(j-c)1} = 20^{\circ}\text{C/W (Typ.)}$$

b) Second stage transistor

$$R_{th(j-c)2} = 17.5^{\circ}\text{C/W (Typ.)}$$

c) Third stage transistor

$$R_{th(j-c)3} = 15^{\circ}\text{C/W (Typ.)}$$

d) Fourth stage transistor

$$R_{th(j-c)4} = 7.5^{\circ}\text{C/W (Typ.)}$$

e) Final stage transistor

$$R_{th(j-c)5} = 3.75^{\circ}\text{C/W (Typ.)}$$

(2) V_{CC} , I_T , RF input & output power conditions at standard operation for each stage transistors are estimated as follows.

$P_O = 12\text{W}$, $V_{CC1} = V_{CC2} = V_{CC3} = 12.5\text{V}$, $P_{in} = 5\text{mW}$, $\eta_T = 30\%$ (minimum ratings),

$I_1 = 0.23\text{A}$ (Total current from 1st stage to 2nd stage)

$I_2 = 2.97\text{A}$ (Total current from 3rd stage to 5th stage)

The conditions at standard operation for each stage transistors are shown in Table 1.

- Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC1} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C \text{ (Note 1)} \\ &= (12.5 \times 0.06 - 0.02 + 0.005) \times 20 + T_C \\ &= 14.6 + T_C \text{ (}^{\circ}\text{C)} \end{aligned}$$

Note 1: Case temperature of device

- Junction temperature of the second stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC1} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C \\ &= (12.5 \times 0.17 - 0.4 + 0.03) \times 17.5 + T_C \\ &= 30.7 + T_C \text{ (}^{\circ}\text{C)} \end{aligned}$$

- Junction temperature of the third stage transistor

$$\begin{aligned} T_{j3} &= (V_{CC2} \times I_{T3} - P_{O3} + P_{O2}) \times R_{th(j-c)3} + T_C \\ &= (12.5 \times 0.28 - 1.3 + 0.4) \times 15 + T_C \\ &= 39.0 + T_C \text{ (}^{\circ}\text{C)} \end{aligned}$$

- Junction temperature of the fourth stage transistor

$$\begin{aligned} T_{j4} &= (V_{CC2} \times I_{T4} - P_{O4} + P_{O3}) \times R_{th(j-c)4} + T_C \\ &= (12.5 \times 0.77 - 4.8 + 1.3) \times 7.5 + T_C \\ &= 45.9 + T_C \text{ (}^{\circ}\text{C)} \end{aligned}$$

- Junction temperature of the final stage transistor

$$\begin{aligned} T_{j5} &= (V_{CC3} \times I_{T5} - P_{O5} + P_{O4}) \times R_{th(j-c)5} + T_C \\ &= (12.5 \times 1.92 - 12 + 4.8) \times 3.75 + T_C \\ &= 63.0 + T_C \text{ (}^{\circ}\text{C)} \end{aligned}$$

2. Heating sink design

In thermal design of heat sink, keep the case temperature below 90°C at output power $P_O = 12\text{W}$ and ambient temperature = 60°C .

Table 1: The conditions at standard operation

Stage	V_{CC} (V)	I_T (mA)	P_{in} (mW)	P_O (mW)
1st	12.5	60	5	30
2nd	12.5	170	30	400
3rd	12.5	280	400	1300
4th	12.5	770	1300	4800
5th	12.5	1920	4800	12000

The thermal resistance $R_{th(c-a)}$ (Note 2) of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_C - T_a}{(P_O/\eta_T) - P_P + P_{in}} = \frac{90 - 60}{(12/0.3 - 12 + 0.001)} \\ &= 1.00 \text{ (}^{\circ}\text{C/W)} \end{aligned}$$

Note 2: Including the contact thermal resistance between device and heat sink

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistor become;

$$\begin{aligned} T_{j1} &= 105^{\circ}\text{C}, T_{j2} = 121^{\circ}\text{C}, T_{j3} = 129^{\circ}\text{C}, T_{j4} = 136^{\circ}\text{C}, \\ T_{j5} &= 153^{\circ}\text{C at } T_a = 60^{\circ}\text{C}, T_C = 90^{\circ}\text{C}. \end{aligned}$$

Since the annual average of ambient temperature is 30°C , junction temperatures of each transistor become;

$$\begin{aligned} T_{j1} &= 75^{\circ}\text{C}, T_{j2} = 91^{\circ}\text{C}, T_{j3} = 99^{\circ}\text{C}, T_{j4} = 106^{\circ}\text{C}, \\ T_{j5} &= 123^{\circ}\text{C}. \end{aligned}$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 153°C , application under fully derated condition is ensured.