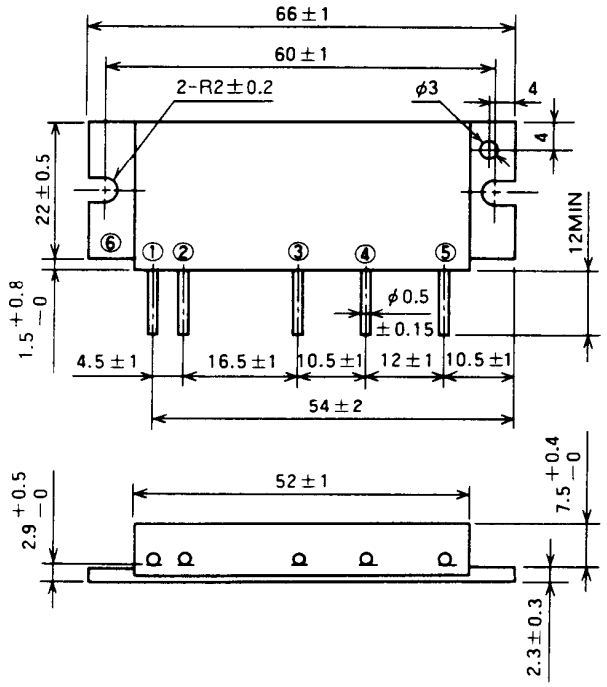
M57714

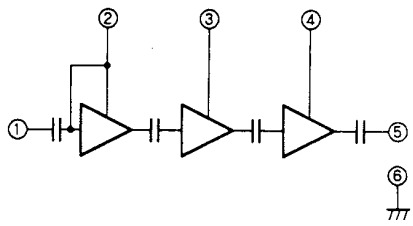
450-470MHz, 12.5V, 7W, FM MOBILE RADIO

OUTLINE DRAWING Dimensions in mm



H3

BLOCK DIAGRAM



PIN :
①Pin : RF INPUT
②Vcc1 : 1st. DC SUPPLY
③Vcc2 : 2nd. DC SUPPLY
④Vcc3 : 3rd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		17	V
Icc	Total current		4	A
Pin(max)	Input power	ZG = ZL = 50 Ω	0.2	W
Po(max)	Output power	ZG = ZL = 50 Ω	12	W
Tc(OP)	Operation case temperature		− 30 to 110	℃
Tstg	Storage temperature		− 40 to 110	℃

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise noted)

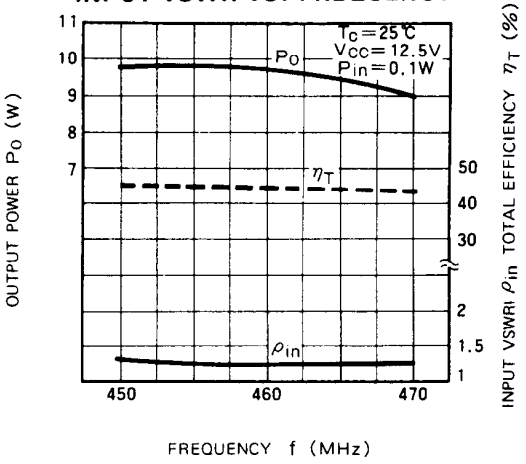
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	Pin = 0.1W Vcc = 12.5V ZG = ZL = 50 Ω	450	470	MHz
Po	Output power		7		W
ηT	Total efficiency		38		%
2fo	2nd. harmonic			− 30	dBc
ρin	Input VSWR			2	−
−	Load VSWR tolerance	Vcc = 15.2V, Po = 7W (Pin : controlled) Load VSWR=20:1 (All phase), 2sec. ZG = 50 Ω	No degradation or destroy		−

Note. Above parameters, ratings, limits and conditions are subject to change.

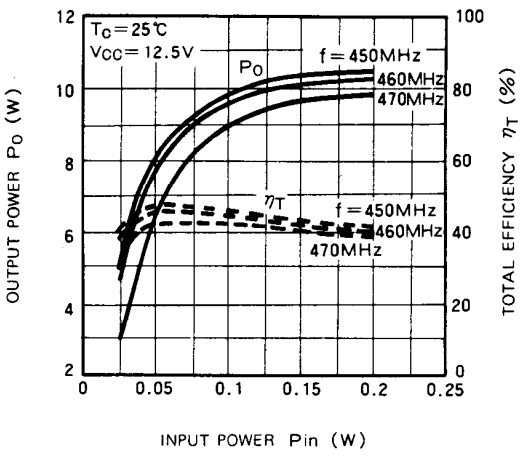
MITSUBISHI ELECTRIC

TYPICAL PERFORMANCE DATA

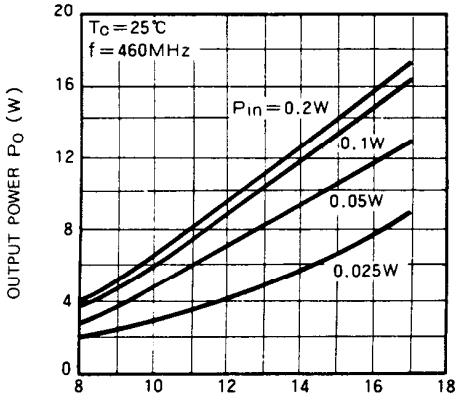
OUTPUT POWER, TOTAL EFFICIENCY INPUT VSWR VS. FREQUENCY



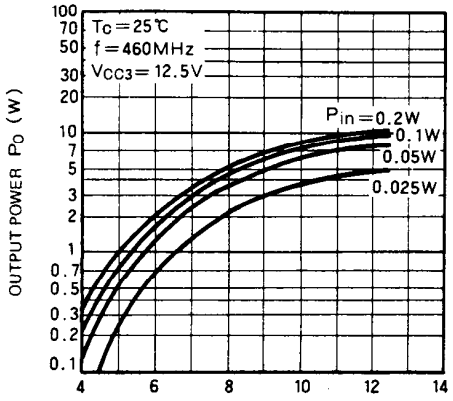
OUTPUT POWER, TOTAL EFFICIENCY VS. INPUT POWER



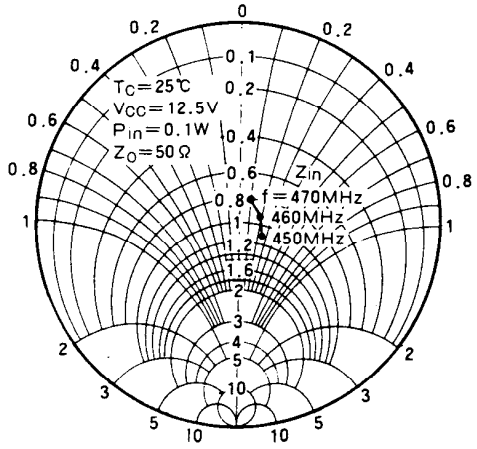
OUTPUT POWER VS. DC SUPPLY VOLTAGE



OUTPUT POWER VS. 1st AND 2nd VOLTAGE



INPUT IMPEDANCE VS. FREQUENCY



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to following consideration when designing heat shink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$R_{th(j-c)1}$ = 20°C/W (Type)

b) Second stage transistor

$R_{th(j-c)2}$ = 10°C/W (Type)

c) Final stage transistor

$R_{th(j-c)3}$ = 5°C/W (Typ.)

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

P_O = 7W, V_{CC} = 12.5V, P_{in} = 0.1W, η_T = 38% (minimum rating), P_{O1} (Note 1) = 0.8W, P_{O2} (2) = 3.2W, I_T = 1.47A (I_{T1} (3) = 0.12A, I_{T2} (4) = 0.42A, I_{T3} (5) = 0.93A)

Note 1: Output power of the first stage transistor

Note 2: Output power of the second stage transistor

Note 3: Circuit current of the first stage transistor

Note 4: Circuit current of the second stage transistor

Note 5: Circuit current of the final stage transistor

Junction temperature of the first stage transistor

$T_{j1} = (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (6)

$= (12.5 \times 0.12 - 0.8 + 0.1) \times 20 + T_C$

$= 16 + T_C$ (°C)

Note 6: Package temperature of device

Junction temperature of the second stage transistor

$T_{j2} = (V_{CC} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C$

$= (12.5 \times 0.42 - 3.2 + 0.8) \times 10 + T_C$

$= 29 + T_C$ (°C)

Junction temperature of the final stage transistor

$T_{j3} = (V_{CC} \times I_{T3} - P_O + P_{O2}) R_{th(j-c)3} + T_C$

$= (12.5 \times 0.93 - 7 + 3.2) \times 5 + T_C$

$= 39 + T_C$ (°C)

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally T_a = 60°C) and at the output power of 7W below 90°C.

The thermal resistance $R_{th(c-a)}$ (7) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(7/0.38) - 7 + 0.1}$$

$= 2.6$ (°C/W)

Note 7: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

T_{j1} = 106°C, T_{j2} = 119°C, T_{j3} = 129°C at T_a = 60°C, T_C = 90°C.

In the annual average of ambient temperature is 30°C,

T_{j1} = 76°C, T_{j2} = 89°C, T_{j3} = 99°C.

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C, application under fully derated condition is ensured.