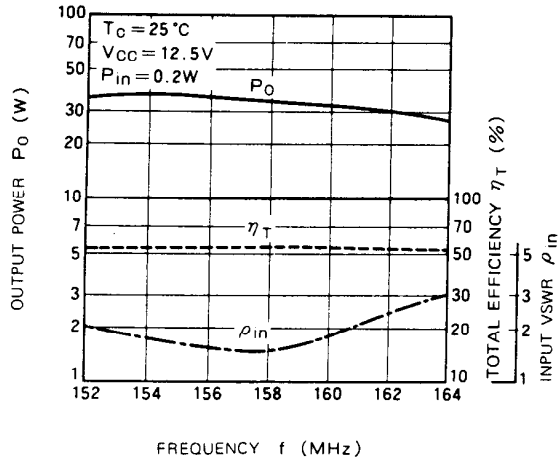
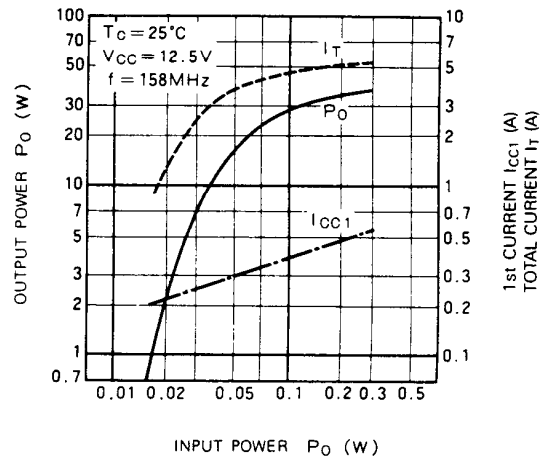


TYPICAL PERFORMANCE DATA

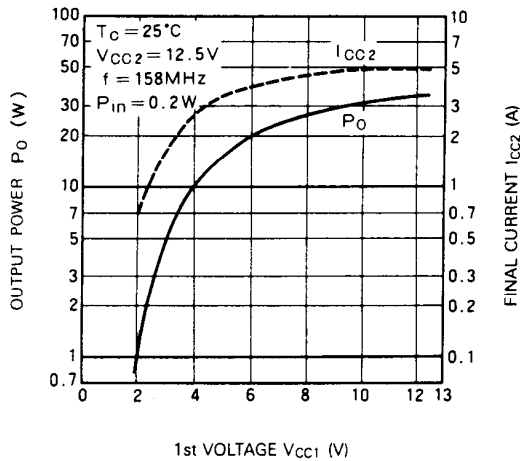
OUTPUT POWER, TOTAL EFFICIENCY,
INPUT VSWR VS. FREQUENCY



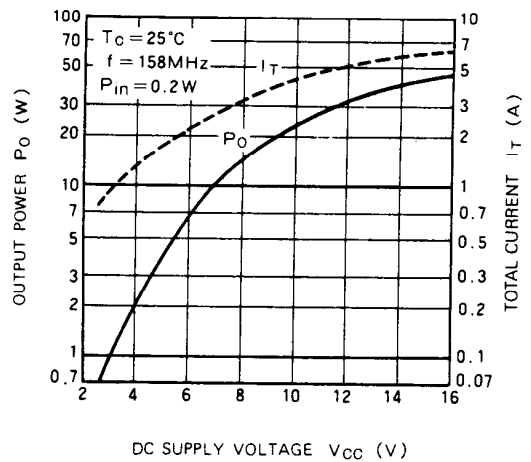
OUTPUT POWER, TOTAL CURRENT,
1st CURRENT VS. INPUT POWER



OUTPUT POWER, FINAL
CURRENT VS. 1st VOLTAGE



OUTPUT POWER, TOTAL CURRENT
VS. DC SUPPLY VOLTAGE



DESIGN CONSIDERATION OF HEAT RADIATION.

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 8^{\circ}\text{C/W (Typ.)}$$

b) Final stage transistor

$$R_{th(j-c)2} = 2^{\circ}\text{C/W (Typ.)};$$

(2) Junction temperature of incorporated transistors at standard operation.

• Conditions for standard operation.

$P_o = 28\text{W}$, $V_{CC} = 12.5\text{V}$, $P_{in} = 0.2\text{W}$, $\eta_T = 45\%$ (minimum rating), P_{o1} (Note 1) = 5W , $I_T = 5.0\text{A}$ (I_{T1} (2) = 0.9A , I_{T2} (3) = 4.1A)

Note 1: Output power of the first stage transistor

Note 2: Circuit current of the first stage transistor

Note 3: Circuit current of the final stage transistor

• Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC} \times I_{T1} - P_{o1} + P_{in}) \times R_{th(j-c)1} + T_c^{(4)} \\ &= (12.5 \times 0.9 - 5 + 0.2) \times 8 + T_c \\ &= 52 + T_c (^{\circ}\text{C}) \end{aligned}$$

Note 4: Package temperature of device

• Junction temperature of the final stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC} \times I_{T2} - P_o + P_{o1}) \times R_{th(j-c)2} + T_c \\ &= (12.5 \times 4.1 - 28 + 5) \times 2 + T_c \\ &= 57 + T_c (^{\circ}\text{C}) \end{aligned}$$

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally $T_a = 60^{\circ}\text{C}$) and at the output power of 8W below 90°C .

The thermal resistance $R_{th(c-a)}$ (5) of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_c - T_a}{(P_o/\eta_T) - P_o + P_{in}} = \frac{90 - 60}{(28/0.45) - 28 + 0.2} \\ &= 0.87 (^{\circ}\text{C/W}) \end{aligned}$$

Note 5: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 142^{\circ}\text{C}, T_{j2} = 147^{\circ}\text{C} \text{ at } T_a = 60^{\circ}\text{C}, T_c = 90^{\circ}\text{C}.$$

In the annual average of ambient temperature is 30°C ,

$$T_{j1} = 112^{\circ}\text{C}, T_{j2} = 117^{\circ}\text{C}$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensure.