M54940P/FP

8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTER

DESCRIPTION

The M54940P, a monolithic integrated circuit fabricated with using an IIL technology, is designed for driving an 8-digit, 7-segment fluorescent display.

FEATURES

- Separated power supplies; 5V (Logic circuit), and 35V (Output circuit)
- Integral scanning oscillator circuit for display

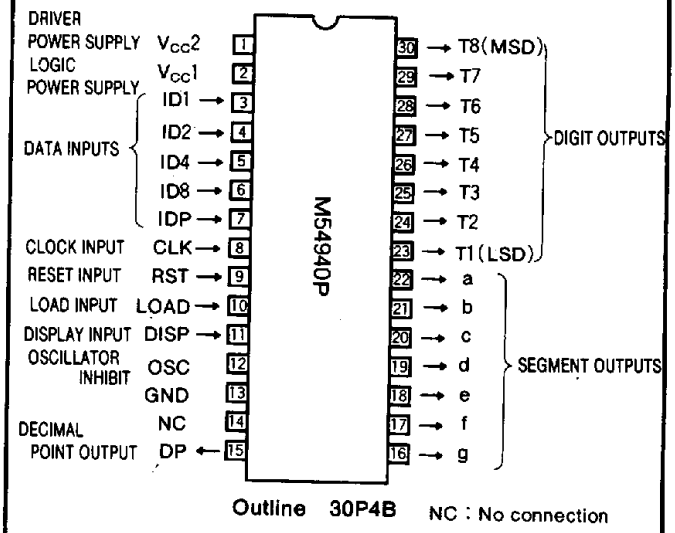
APPLICATION

Micro computer display. Digital equipment for consumer and Industrial use.

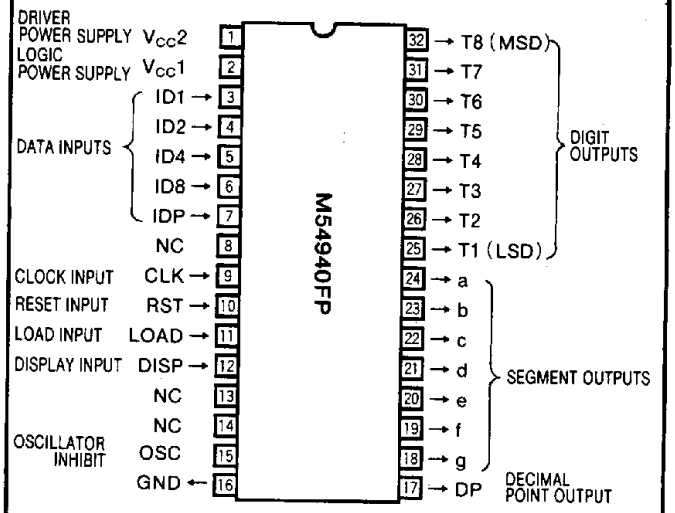
FUNCTION

The M54940P, having a 5-bit×8-digit memory, is a decoder driver for dynamic displaying of a vacuum fluorescent tubes. The data for one digit section is organized into a 4-bit BCD and an 1-bit decimal point. The data memory consists of a shift register and a latch, and is capable of displaying the previous data while the data is being transported.

PIN CONFIGURATION (TOP VIEW)

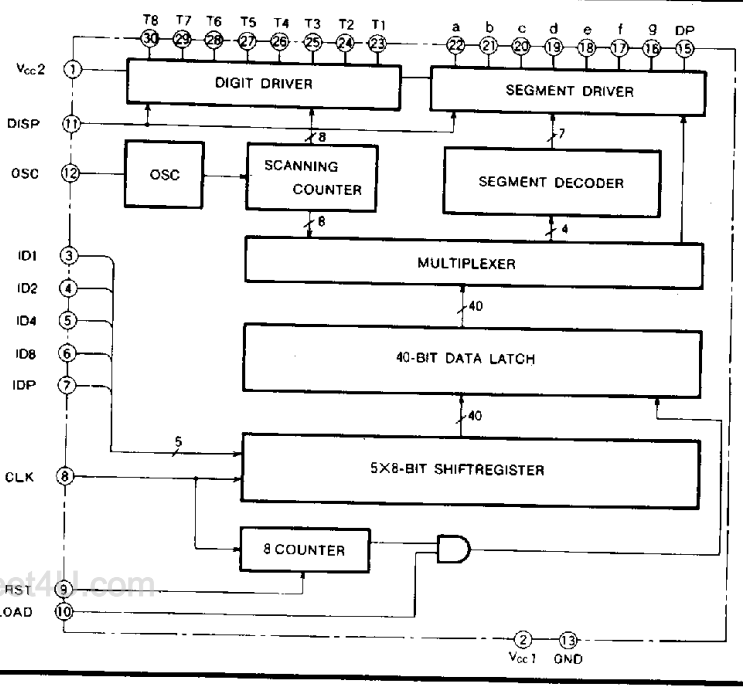


Outline 30P4B NC : No connection



Outline 32P2W-A NC : No connection

BLOCK DIAGRAM



INPUT PIN FUNCTION

1) OSC : External capacitor connecting terminal for the oscillator circuit.

2) ID 1, ID 2, ID 4, ID 8 : BCD Data Input; refer to the numerical Designations-resultant displays for the relation of the input data to the display.

3) IDP : decimal point data Input

4) CLK : Data transport clock Input: the data can be input at a positive-going edge of the CLK

5) RST : Reset Input : the CLK input counter is reset at "H".

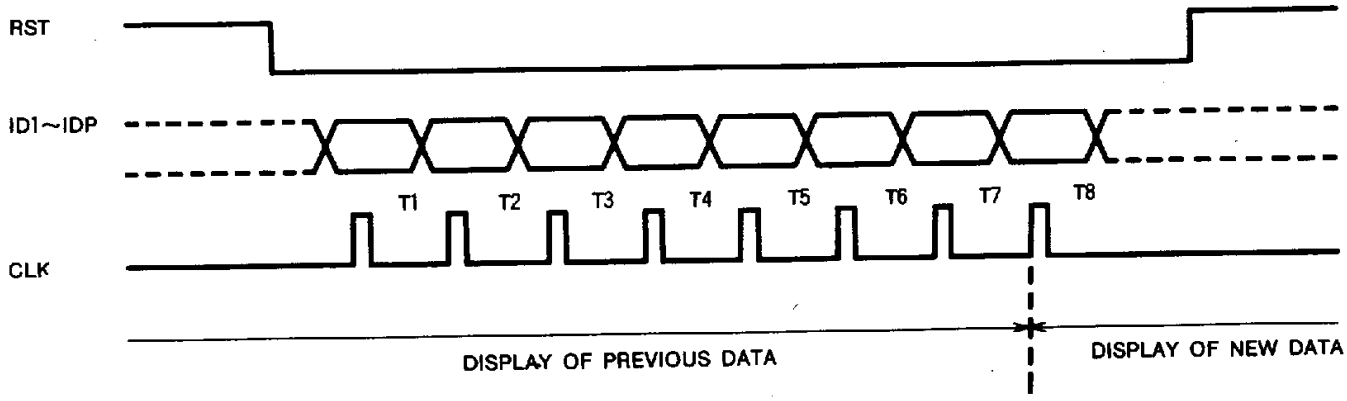
6) LOAD : Signal Input to load the data latch with the data of the shift register. The Input LOAD will not be accepted until the 8th CLK Input has been received.

7) DISP : When it is set to "H" it displays. When it is set to "L", the display is inhibitted. During the display inhibition period, both the segment and digit outputs will be at "L".

TIMING CHART

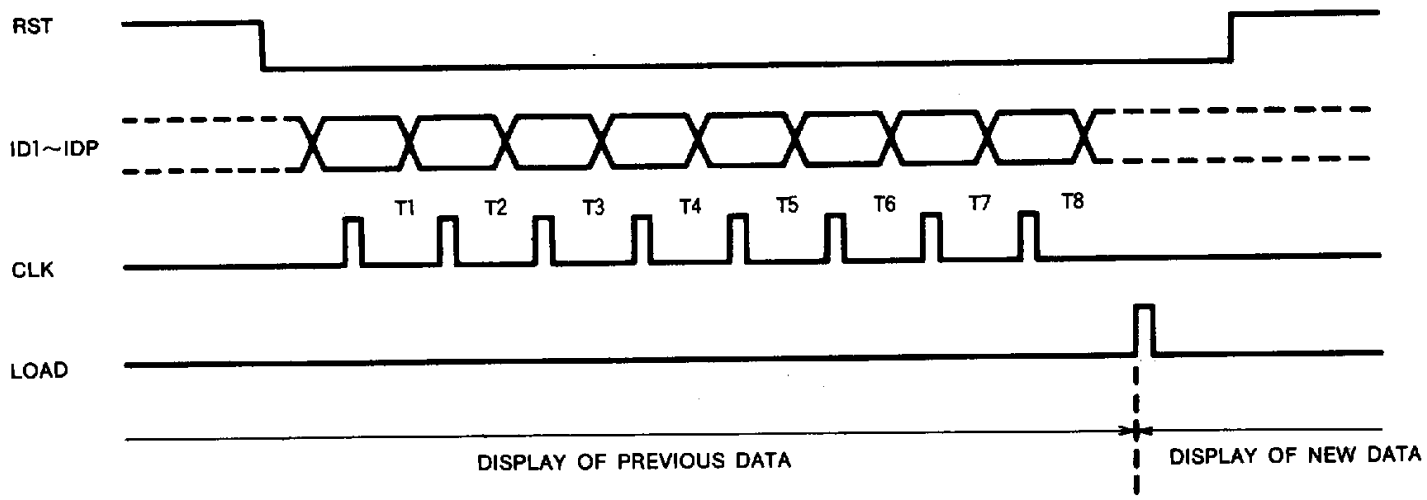
DATA PROGRAMMING

(1) USING CLK AND RST inputs with LOAD=" H ".



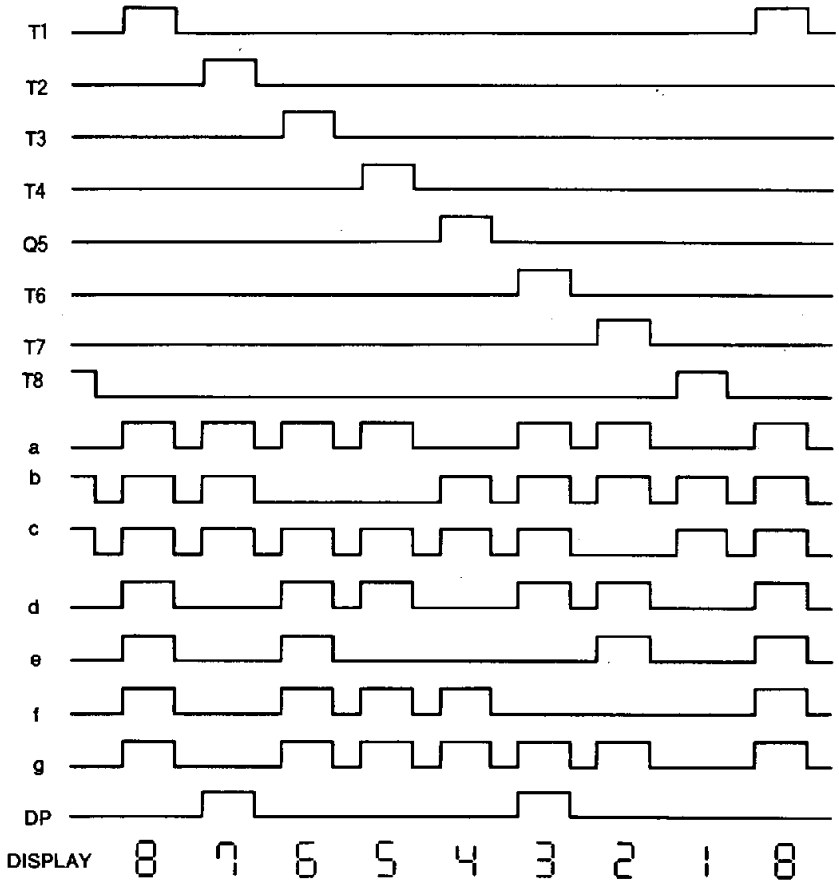
When LOAD is kept at " H ", LOAD is automatically done at the 8th CLK input when RST=" L ".
However, while RST=" L ", if there is a 9th CLK input, the 9th data will be loaded and displayed.

(2) Using CLK, RST and LOAD inputs.



After the 8th clock input, the LOAD is valid only in the period while RST=" L ".
Furthermore, if there is 9th CLK input before the LOAD input, the LOAD input is ignored.

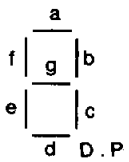
OUTPUT TIMING CHART



NUMERICAL DESIGNATIONS-RESUITANT DISPLAYS

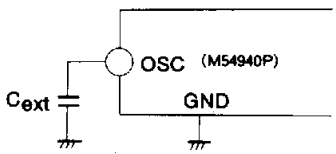
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
BCD DATA	ID1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	ID2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	ID4	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	ID8	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Display		0	1	2	3	4	5	6	7	8	9	-	E	P	L	⌐	Blank

*The decimal point, independent of BCD data, is output when the decimal bit of the corresponding digit is at " H ". Furthermore, when the decimal point bit is set at " H " at plural digits, plural decimal points are displayed.



OSCILLATOR CIRCUIT

1) External connection



2) Oscillation period

$t_{osc} \fallingdotseq 20\ C_{ext} \times 10^{-3} [\mu s]$ (Typ.)

(Unit of C_{ext}: [pF])

DISPLAYS IMMEDIATELY "AFTER POWER ON."

The display which appears immediately after "power-on" is indefinable. During the period bofore the regular data is transported the display can be erased if DISP input is set at " L ".

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Logic supply voltage		−0.3~+9	V
V_{CC2}	Driver supply voltage		−0.3~+38	V
V_I	Input voltage		−0.3~V_{CC1}	V
V_O	Output voltage		0~V_{CC2}	V
T_{stg}	Storage temperature		−55~+150	℃
T_{opr}	Operating temperature		−20~+75	℃
P_d	Power dissipation		600	mW

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC1}	Logic supply voltage	4	5	7	V
V_{CC2}	Driver supply voltage	10	30	35	V

ELECTRICAL CHARACTERISTICS (T_a=−20~+75℃, V_{CC1}=5V, V_{CC2}=35V, unless otherwise noted)

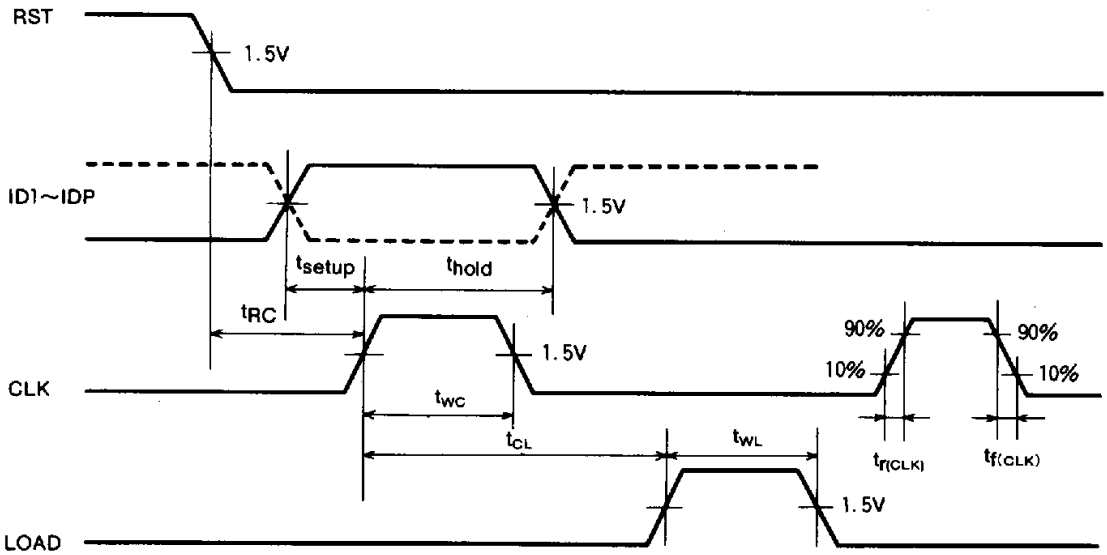
Symbol	Parameter		Test Conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	"H" Input voltage		V_{CC}1 =4~7V	2.7		V_{CC1}	V
V_{IL}	"L" Input voltage		V_{CC}= 1 =4~7V	0		0.7	V
I_{IH}	"H" Input current		V_{IH}=5V		0	20	μA
I_{IL}	"L" Input current		V_{IL}=0V		−0.25	−0.4	mA
V_{OH}	"H" Output voltage	Digit output	I_{OH}=−10mA	33	33.8		V
		Segment output	I_{OH}=−2mA	33	34		
V_{OL}	"L" Output voltage		I_{OL}=0mA		0	2	V
I_{CC1}	Logic circuit current		Input : open All segment outputs; ON		12	22	mA
I_{CC2}	Driver circuit current		Output : Open All segment outputs : ON		8	14	mA
t_{OSC}	Oscillation Period		C_{ext}=1000pF	10	20	40	μs

*Typical values are measured at 25℃

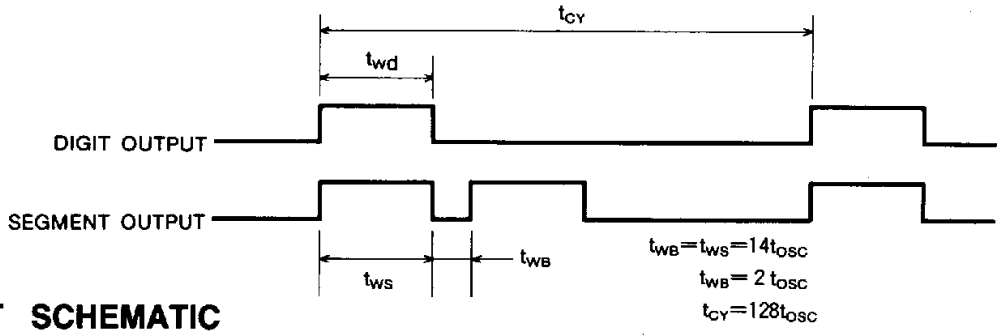
TIMING CHARACTERISTICS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
f_{CLK}	Clock Frequency				100	kHz
f_{OSC}	Oscillation frequency		10		100	kHz
t_{WC}	Clock pulse width		2			μs
t_{WL}	Load Pulse width		2			μs
t_{setup}	Data setup time (DATA→CLK)		4			μs
t_{hold}	Data Hold time(CLK→DATA)		2			μs
t_{RC}	Reset-clock time(RST→CLK)		4			μs
t_{CL}	Clock-load, time(CLK→LOAD)		4			μs
$t_{r(CLK)}$	Clock pulse rise time				10	μs
$t_{f(CLK)}$	Clock pulse fall time				10	μs

INPUT TIMING CHART



OUTPUT TIMING CHART



I/O CIRCUIT SCHEMATIC