**TWIN PLL VIF/SIF** 

#### **DESCRIPTION**

M52319SP integrated circuit processes intermediate-frequency (IF) signals. It is intended for audio-vidual color televisions and video cassette recorders.

This IC uses the twin phase-locked loop (PLL) detection method. It processes signals with low power dissipation because the supply voltage is 5V (Icc is 63 mA with 5V power supply).

Video signals and sound signals are processed separately. This IC is optimal for high-quality IF signal processing systems.

#### **FEATURES**

#### Twin PLL detection system

Video IF signals and sound IF signals (including picture signal carriers) are input separately through a quasi-parallel type surface acoustic wave filter. Sound IF signals are detected completely synchronously by PLL. The PLL's voltage-controlled oscillator (VCO) is also used to detect video IF signals completely sysnchronously. Sound IF signals are not let through Nyquist slope, reducing buzzes.

The video detection output is perfectly synchronous, ensuring excellent performance in DG, DP, 920 kHz beat frequency, and cross-color characteristics.

Dynamic AGC (automatic gain control) circuit

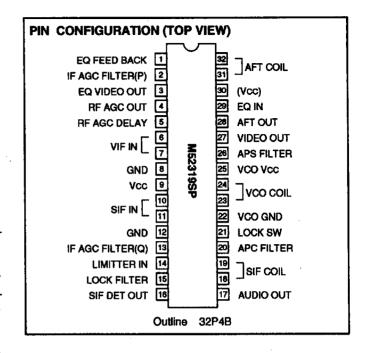
While conventional processors have used two pins for the IF AGC filter, this IC uses only one pin, improving voltage sag and operation speed.

AGC is applied to both video IF and sound IF.

• Equalizer-amplifier and video mute circuit

This IC has a built-in video equalizer, and is optimal for VCRs and color TVs with image output terminals.

When EQ feedback (pin ①) is set to LOW, video cutput can be muted.

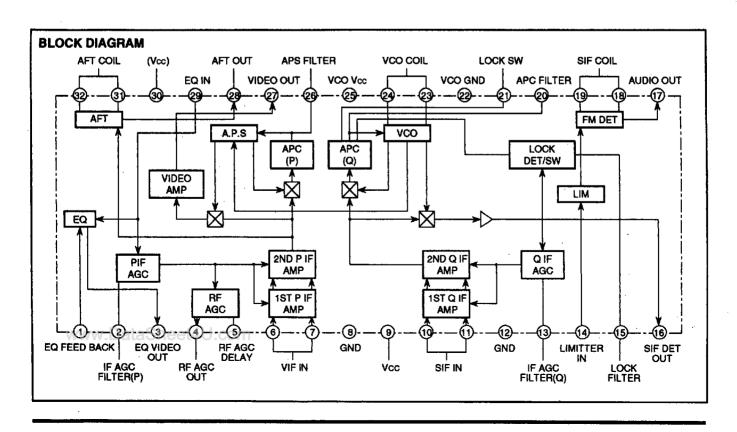


#### FM demodulation circuit

A quadrature detection circuit is provided for sound IF signal frequency modulation detection. This circuit is exclusively used with a coil, simplifying external circuits and improving linearity.

#### **APPLICATION**

TV picture receivers and VCR tuners



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### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6.0	- V
Pd	Power dissipation	290	mW
Topr	Operating temperature	-20~75	С
Tstg	Storage temperature	-40~125	Ç
Vopr	Recommended operating voltage range	4.5~5.5	. ۷
Surge	Electrostatic discharge	±200	V

## ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc = 5V unless otherwise noted)

Q		Test	input			External supply (V)					Switch setting						Limits			4.144	
Symbol	Parameter	point	VIF	QIF	SIF	V2	V5	V13	V15	1	2	3	4	5	6	7	Min.	Тур.	Max.	ax. Unit	Remark
lcc	Circuit current	Α	_	· —	_	_	_	_		2	1	1	1	1	1	1	45	63	81	.mA	
V27	Video detection output DC voltage1	TP9			}	1	1	1	1	1	1	3	3	1	1	1	2.0	2.5	3.0	٧	
Vз	Video detection output DC voltage2	TP1	_	-	-	-	-		ı	1	1	3	3	1	1	1	2.72	3.4	4.08	٧	
Vodet1	Video detection output 1	TP9	SG1	SG1	-		-		ı	1	1	1	1	1	1	1	0.76	0.95	1.14	Vp-p	
Vodet2	Video detection output 2	TP1	SG1	SG1	_	_	_	_	-	1	1	1	1	1	1	1	1.52	1.9	2.28	Vp₊p	
P/N	Video sound noise	TP10	SG2	SG2		_		_	-	1	1	1	1	1	1	2	45	51	_	dB	
BW	Video frequency characteristic	TP9	SG3	SG3	_	_		_		1	1	1	1	1	1	1	5.5	7.0	-	MHz	
Vin (min)	Input sensitivity	TP9	SG4	SG4	-	-	-	1	1	1	1	1	1	1	1	1	1	44	52	dB μ	÷
Vin (max)	Maximum allowable input	TP9	SG5	SG5	-	_	_	_	_	.1	1	1	1	1	1	1	103	109	_	dB μ	
GR	AGC control range			_	-	1	ı	ł	1	ł	1	_	_	1	1	1	58	65	_	dB	
V <sub>2</sub> H	VIF AGC maximum voltage	TP11	_	-	_	.1	1	_	ı	1	1	1	1	1	1	1	3.8	4.8	-	٧	
V2 (90dΒ μ)	VIF AGC voltage	TP11	SG2	SG2	_	<u> </u>		_	-	1	1	1	1	1	1	1	2.04	2.8	3.56	٧	
V2L	VIF AGC minimum voltage	TP11	SG7	SG7	_		-	-	_	ť	1	1	1	1	1	1	1.75	2.4	3.05	· V	
V26	AFT output voltage	TP8	_	_	_	_	1	_	_	1	1	3	3	1	1	1	1.29	2.7	4.18	٧	
μ	AFT detection sensitivity	TP8	SG10	SG10	_ 1	_	_	_	_	1	1	1	1	1	1	1	43.5	63	81.5	mV/kHz	
μBlack/ White	AFT detection sensitivity ratio (black/white)	TP8	SG22	SG22	_	-	1		-	1	1	1	1.	1	1	1	-	0.9	1.8	-	
V28H	AFT maximum voltage	TP8	SG10	SG10		-	_	-	_	1	1	1	1	1	1	1	4.37	4.75	. —	V	,
V28L	AFT minimum voltage	TP8	SG10	SG10		-	-	-	1	1	1	1	1	1	1	1	_	0.1	0.5	٧	
V4H	RF AGC maximum voltage	TP2	SG2	SG2	_ [	_	.2	-	_	1	1	1	1	1	1.	1	_	5.0	Vcc	V	
V4L	RF AGC minimum voltage	TP2	SG2	SG2	_	_	3		_	1	1	1	1	1	1	1	_	0.2	0.5	V	
V15	Lock detection threshold voltage	TP6	ı	_	_	3	1	3	Vari- able	1	1	2	2	2	2	1	2.36	2.65	2.94	٧	
DG	DG	TP9	SG16	SG16	_	_			_	1	1	1	1	1	-1	. 1	_	4	8	%	
DP	DP	TP9	SG16	SG16				_		1	1	1	1	1	1	1	_	2	5	deg	
V16	QIF detection output DC voltage	ТРЗ		-	_	_	_	_	_	1	1	3	3	1	1	1	2.08	2.6	3.12	٧	
Vodet3	QIF detection output	TP3	SG1	SG1	_	·, — ]	_	1	_	1	1	1	1.	1	1	1	0.78	1.05	1.31	VP-P	
QBW	OIF detection output frequency characteristic	ТР3	SG3	SG3	_	_	_	_	-	1	1	1	1	1	1	1	5.5	7.0	_	MHz	
VQmin	QIF detection output input sensitivity	ТР3	SG4	SG4	-	_	-	-	_	1.	1	1	1	1	1	1	_	45	53	dB μ	

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## **ELECTRICAL CHARACTERISTICS(cont.)**

Symbol	B	Test		Input		Exte	rnal s	upply	(V)		Sv	vitch	itch setting				Limits			Unit	Remark
Symbol	Parameter	point	VIF	QIF	SIF	V2	V5	V13	V15	1	2	3	4	5	6	7	Min.	Тур.	Max.	Oint	Roman
VQmex	QIF detection output maximum allowabel input	трз	SG5	SG5	-	-		_	_	1	1	1	1	1	1	1	103	109	-	dB μ	
CL-U1	Capture range (U-1)	TP9	SG11	SG11	-	-			-	1	1	1	1	1	1	1	0.8	1.3	-	MHz	
CL-L1	Capture range (L-1)	TP9	SG11	SG11	1	_	-	1	-	1	1	1	1	1	1	1	1.0	2.2	-	MHz	
CL-T1	Capture range (T-1)	TP9	-	_	. 1	-	-	+	-	1	ı	-	-	-	1	-	2.8	3.5	-	MHz	
CL-U2	Capture range (U-2)	TP9	SG11	SG11	. 1	1	-	ı	ı	1	1	1	1	2	1	1	0.72	1.2	1.92	MHz	
CL-L2	Capture range (L-2)	TP9	SG11	SG11	1	1	ı	-	-	1	1	1	1	2	1	1	1.54	2.2	2.86	MHz	
V26	Pin (5) minimum voltage	TP6		_	1	5	-	5	Vari- abie	1	1	2	2	2	2	1	-	0.3	0.6	٧	
VEQBW	EQ output frequency characteristic	TP1	SG3	SG3	1	_	1	-	_	1	1	1	1	1	1	1	-3 3	0 6	+3	dB	3MHz 4.43MHz
IM	Intermodulation	TP9	SG15	SG15	1	Vari- able	1	-	_	1	1	2	1	1	1	1	38	50	_	dB	
Vsync	EQ output sync chip level	TP1	SG2	SG2	-	-	-	_	_	1	1	1	1	1	1	1	1.09	1.28	1.47	٧	
fvт	VCO frequency temperature drift	TP7	-	-	_	_	_	_	_	1	1	3	3	1	1	1	-0.1	0.3	0.4	МНz	
∆fsw	VCO frequency SW ON drift	TP7	-	-	-	-	_		-	1	1	3	3	1	1	1	-0.04	0.04	0.14	MHz	
Rin(P)	PIF input resistance		90dB µ	-	_	_	_	_	_	_	-	] –	_	_	_	_	_	1.35		kΩ	Test circuit2
CIN(P)	PIF input capacitance	-	90dB µ			_	_			_	_	_	_	<u> </u>	_	_	<u> </u>	4.0	_	PF	Test circuit2
Rin(Q)	QIF input resistance		<u> </u>	90dB µ	_	<u> </u>	_	<u> </u>	_	_	<u> </u>	<u> </u>	_	<u> </u>	_	<u> </u>		1.35	<u> </u>	kΩ	Test circuit2
CIN(Q)	QIF input capacitance	_	_	90d8 µ		<u> </u>		<u> </u>	_	_	_	_	上	_	_	_	<u> </u>	4.0		PF	Test circuit2
V17	AF output DC voltage	TP4	<u> </u>		_		_	<u>  -                                   </u>		1	1	3	3	1	1	1	0.75	1.5	2.25	٧	
Voaf (max)	Maximum AF output	TP4	-	_	SG17	-	_	_	_	1	1	3	3	1	1	1	206	275	344	mVrms	
THD AF	AF output distortion	TP4	_		SG21	_	_	_	_	1	1	3	3	1	1	1	_	0.5	1.5	%	
Vin (LIN)	Input limiting sensitivity	TP4	-	_	SG18	_		_	_	1	. 1	3	3	1	1	1		44	50	dB μ	
AMR	AMR	TP4	_	_	SG19	_	_		_	1	1	3	3	1	1	1	48	58	-	dB	
S/N	AF S/N	TP4	<u> </u>	_	SG20				-	1	1	3	3	1	1	1	48	72		dB	

# ELECTRICAL CHARACTERISTIC TEST METHODS P/N

- 1. Let pin ② noise through low-pass filter (-3 dB at 5 MHz) and measure output voltage at TP10 in root-mean-square.
- 2. P/N = 20 log {Vodet1(VP-P)×0.7÷noise(Vr.m.s)} Vodet1: Video detection output 1

#### BW

- Set SG3, and measure TP9 1-MHz element. The measured value is referred to as V1.
- Decrease frequency f2 gradually. When (f1-f2) element at TP9 is 3 dB less than V1, read the frequency.
- 3. BW = 38.9 f2 (MHz)

#### Vin(min)

 Lower the SG4 level gradually, and read the level when pin @ detection output is 3 dB less than Vodet1.

#### Vin(max)

 Raise the SG5 level gradually, and read the level when pin @ detection output is 3 dB less than Vodet1.

#### GR

AGC control range is defined as follows:
 GR = Maximum allowable input - input sensitivity (dB)

μ

- 1. Monitor frequency difference between when TP8 DC voltage is  $1.5 \, \text{V}$  and when it is  $3.5 \, \text{V}$ . The frequency is referred to as  $\triangle f$ .
- 2. AFT detection sensitivity  $\,\mu\,$  is defined as follows:

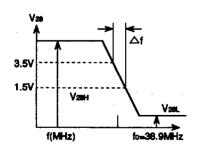
3. 
$$\mu = \frac{2000 (\text{mV})}{\triangle f.(\text{kHz})}$$
 [mV/kHz]

#### V28H

1.VzeH is the maximum DC voltage as in the diagram below.

#### **V28**L

1.V28L is the maximum DC voltage as in the diagram below.



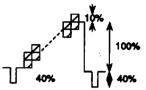
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#### V15

- 1. Set voltage V1s to 1 V, and monitor TP6.
- 2. Increase voltage V15 until TP6 voltage becomes 0.3V, and read the boltage (V15TH).

#### DG and DP

- 1. The SG16 modulation waveform has 10 stages as shown in the illustration. Video modulation is 87.5%.
- Measure DG and DP with a vector scope at TP9.



#### QBW

- Set SG3 and measure TP3 1MHz element. The element is referred to as V1.
- 2. Decrease f2 gradually until TP3 (f1 f2) element becomes 3 dB less than V1, and read the frequency.
- 3. QBW = 38.9 f2 (MHz)

#### **VQmin**

1. Lower the SG4 level gradually, and read the level when pin light detection output is 3 dB less than Vodet3.

#### **VQmax**

1. Raise the SG5 level gradually, and read the level when pin lib detection output is 3 dB less than Vodet3.

#### CL-U1 and CL-U2

- Input SG11 to QIF IN, and increase the frequency until VCO becomes unlocked.
- Decrease the SG11 frequency gradually, and read it when VCO becomes locked. This frequency is referred to as f L(MHz).
- 3. Capture range (U) is the defference between 38.9 MHz and f L (MHz).

#### CL-L1 and CL-L2

- Input SG11 to QIF IN, and decrease frequency until VCO becomes unlocked.
- Decrease the SG11 frequency gradually, and read it when VCO becomes locked. The frequency is referred to as f L(MHz).
- 3. Capture range (L) is the difference between 38.9MHz and fL (MHz).

#### CL-T1

1.(CL-T1) = (CL-U1) - (CL-L1)

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#### **V26**

1. Read the TP6 minimum voltage at voltage V 15.

#### VEGBW

- 1. Set SG3, and measure the TP1 1MHz element. The measurement is referred to as V1, and is 0 dB in this stage.
- 2. Read V1 when the TP1(f1 f2) element is 3 MHz and 4.43 MHz, and calculate the difference from when the TP1 element is 1MHz.

#### 13.4

 Monitor TP9 with an oscilloscope. Adjust voltage V2 for the detection output waveform minimum level to be 1.5 V.

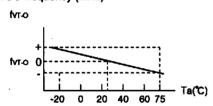


Monitor TP9 with a spectrum analyzer. The intermodulation is the ratio of the 1,070kHz element level to the 4.43MHz element level.

#### fvt

- 1. Read the VCO frequency at ambient temperature 25 ℃. The frequency is referred to as fvr-o.
- 2. Raise ambient temperature from -20 ℃ to +75℃, and measure the VCO frequency, and calculate difference between the frequency and fvr-o.

#### VCO frequency (MHz)



#### △fSW

- 1. Set SW1 to ON, and measure VCO frequency at TP7 in 3 seconds. This frequency is referred to as f 1(MHz).
- 2. Set SW1 to ON, and measure VCO frequency at TP7 in 1 second. This frequency is referred to as f<sub>2</sub> (MHz).
- 3.  $\triangle fsw = f_1 f_2 (MHz)$

### Vin(LIM)

- 1. Set SG18 to 80 dB  $\mu$  and input it to SIF IN.
- 2. Decrease SG18 output gradually until TP4 detection output becomes 3 dB less than VoaF(MAX).
- 3. Read the SG18 level. This level is the input limiting sensitivity.

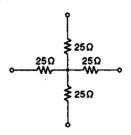
#### AMR

- 1. Measure TP4 output voltage. The voltage is referred to as V AM.

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#### S/N

- Measure TP4 output voltage. This measurement is referred to as Vn.
- 2. AF S/N is defined as follows:



 $S/N = 20 \log {VOAF(MAX)(mVrms)/VN(mVrms)} (dB)$ 

#### μ Black/White

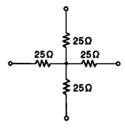
- Change SG22 input frequency according to △fw(kHz), and read the TP8 output voltage. This voltage is referred to as △Vw(mV).
- 2. AFT detection sensitivity  $\mu$  (white) is defined as follows:

 $\mu$  (White) =  $\triangle$ Vw(mV)  $/\triangle$ fw(kHz)(mV/kHz)

3. AFT detection sensitivity ratio (black/white) is defined as follows:  $\mu$  (Black/White) =  $\mu/\mu$  (White)

#### Notes

- All AM (amplitude modulation) wave amplitude levels refer to the peak level of the modulation.
- When PIF IN and QIF IN are applied at the same time, the phase difference between them should be 0 degree.
- 3. Mixer should be as shown below:



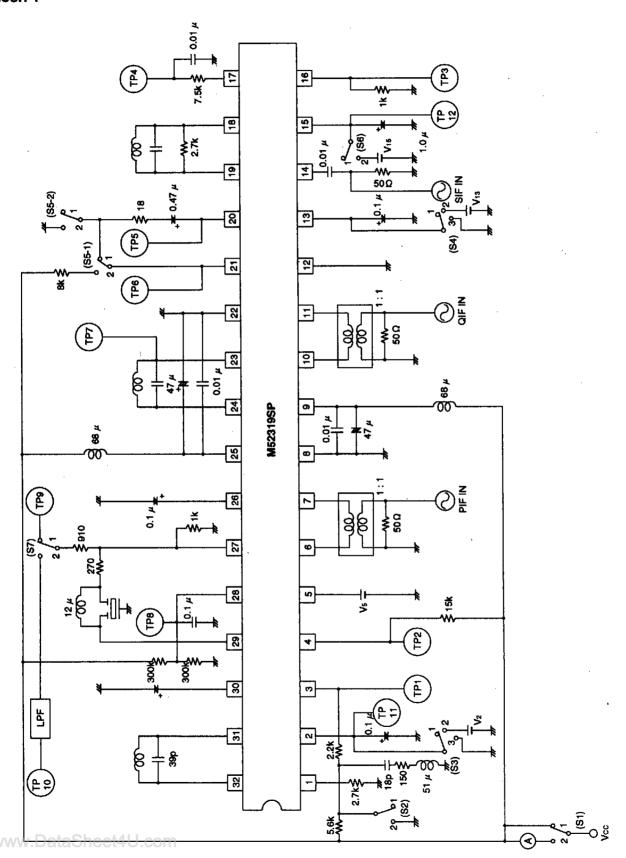
- As for the VCO coil, QIF AGC voltage should be 0 V. Adjust freerunning frequency to 38.9 MHz under no-input condition.
- VCO frequencies (parameters No. 37,38) are measured with Mitsubishi Electric standard jigs.

TWIN PLL VIF/SIF

## , INPUT SIGNALS

Input signal (Values at terminal with 50 Ω)   1   fo=38.9MHz   VI=90dB μ   77.78%AM (Video modulation 87.5%, fm=20kHz)   2   fo=38.9MHz   VI=90dB μ   f1=38.9MHz   VI=90dB μ   f2=38.9MHz   VI=70dB μ   4   fo=38.9MHz   VI=Variable   fm=20kHz   77.78%AM   fo=38.9MHz   VI=Variable   fm=20kHz   77.78%AM   f1=38.9MHz   VI=Variable   fm=20kHz   VI=Va	
1 (Video modulation 87.5%, fm=20kHz) 2 fo=38.9MHz Vi=90dB μ 3 f1=38.9MHz Vi=90dB μ f2=38.9MHz Vi=70dB μ 4 f0=38.9MHz Vi=Variable fm=20kHz 77.78%AM	
(Video modulation 87.5%, fm=20kHz)  2	
3 f1=38.9MHz Vi=90dB μ f2=38.9MHz Vi=70dB μ 4 f0=38.9MHz Vi=Variable fm=20kHz 77.78%AM	
3 f2=38.9MHz Vi=70dB μ 4 f0=38.9MHz Vi=Variable fm=20kHz 77.78%AM	
12=38.9MHz Vi=70dB μ 4 fo=38.9MHz Vi=Variable fm=20kHz 77.78%AM	
5 fo=38.9MHz Vi=Variable fm=20kHz 16%AM	
6 fo=38.9MHz Vi=80dB μ	
7 fo=38.9MHz Vi=110dB μ	
8 fo=33.4MHz Vi=100dB μ	
9 fo=33.4MHz Vi=80dB μ	
10 fo=38.9MHz±5MHz Vi=90dB μ	
11 fo=38.9MHz±5MHz VI=90dB μ fm=20kHz 77.78%A	M
f1=38.9MHz Vi=90dB μ	
12 12=38.4MHz Vi=60dB μ	
f1=38 9MHz Vi=90dR //	
13   f2=35.9MHz   Vi=60dB μ	
f1=38.9MHz Vi=90dB μ	
14 f <sub>2</sub> =33.9MHz Vi=60dB μ	
f1=38.9MHz VI=90dB μ	
15 f <sub>2</sub> =34.47MHz Vi=70dB μ	
f₃=33.4MHz Vi=70dB μ	
fo=38.9MHz, standard 10-step modulation, m = 87.5%, vic	lec
modulation, sync chip level 90 dB $\mu$	`
17 fo=5.5MHz±30kHz dev Vi=90dB μ fm=400Hz	$\neg$
18 fo=5.5MHz±30kHz dev Vi=Variable fm=400Hz	$\neg$
19 fo=5.5MHz Vi=100dB μ 30%AM fm=400kHz	
19 fo=5.5MHz Vi=100dB μ 30%AM fm=400kHz 20 fo=5.5MHz Vi=90dB μ	
20 fo=5.5MHz Vi=90dB μ	
20 fo=5.5MHz Vi=90dB μ	

## **TEST CIRCUIT 1**

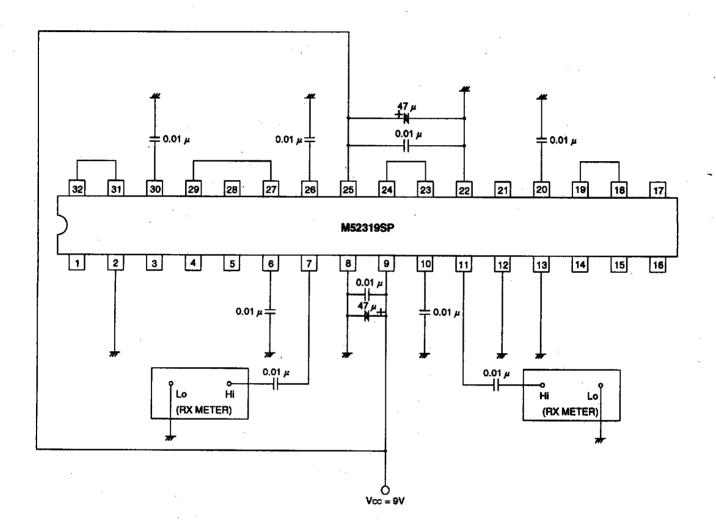


Units Resistance :  $\Omega$ 

. Capacitance : F

Reactance: H

## **TEST CIRCUIT 2**



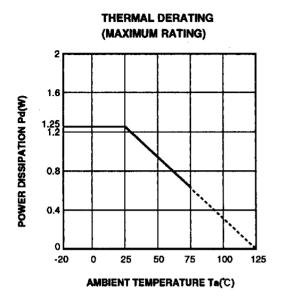
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Units Resistance :  $\Omega$ 

Capacitance: F

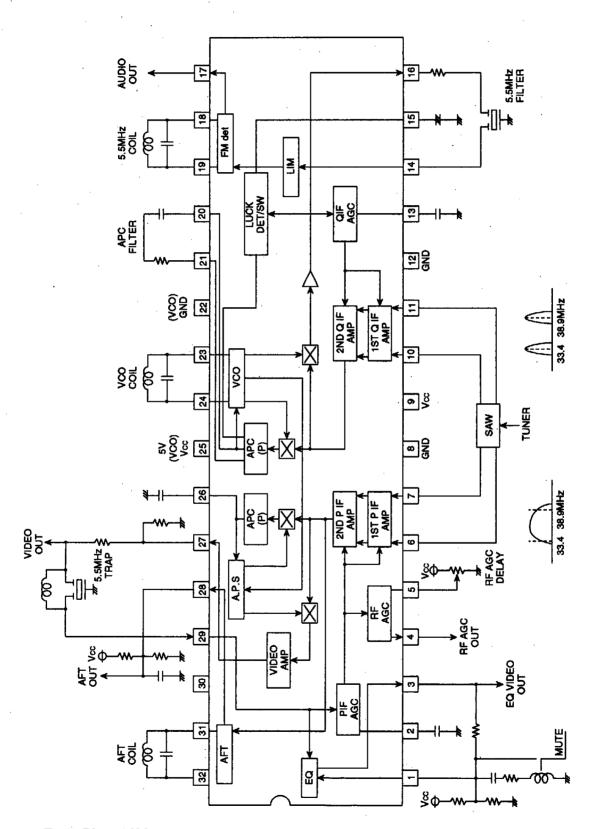
TWIN PLL VIF/SIF

## **TYPICAL CHARACTERISTICS**



Units Resistance: Ω Capacitance: F

## **APPLICATION EXAMPLE**



TWIN PLL VIF/SIF

## **DESCRIPTION OF PIN**

Pin No.	Symbol	Description
①	EQ FEED BACK	Pin ③ video output can be provided with particular frequency characteristics by applying feedback to pin ①.
3	EQ VIDEO OUT	Pin ① may be used for fixed gain amplifier by changing the external constant. Pin ③ EQ output can be muted by setting pin ① to LOW.
2	IF AGC FILTER(P)	Serves as IF AGC FILTER pin on the (P) side. Performs peak AGC.
•	RF AGC OUT	Outputs signals in the open collector form. Requires pull-up resistance.
\$	RF AGC DELAY	Delay point can be changed by varying internal bias with external variable resistance.
<b>⑥</b>	VIF IN	Serves as IF input pin on the (P) side.  Be sure to apply balance input.
8	GND	Used for grounding.
9	Vcc	Used for power supply.
(1) (1)	SIF IN	Serves as input pin on the (Q) side.  Be sure to apply balance input.
12	GNC	Used for grounding.
(3)	IF AGC FILTER(Q)	Output pin similar to pin ②. Serves as IF AGC FILTER pin on the (Q) side.
<b>(4)</b>	LIMITTER IN	Intercarrier input pln
(15)	LOCK FILTER	Forms a low pass filter with pin (5) external capacitor and internal resistance.
16	SIF DET OUT	Serves as detection output pin on the (Q) side. Driven by connecting resistance $1k\Omega$ externally.
17	AUDIO OUT	Used for output after sound FM detection.
18 19	SIF COIL	Serves as sound FM detection coil pin. When $2.7k\Omega$ damping resistance i connected during 5.5MHz/30 kHz, the output voltage is approx. 275mVrms.
<b>Ø</b>	APC FILTER	Outputs voltage related to phase difference between input signal and VCO output Connected to pin ② and lag-lead filter.
<b>Ø</b>	LOCK SW	Outputs judgment whether P LL is locked to IF signal.
<b>Ø</b>	VCO GND	Serves as GND pin for VCO.
<b>Ø</b>	VCO COIL	Used to connect VCO coil. Capture range varies depending or connected coil capacitance.
<b>Ø</b>	VCO Vcc	Used for VCO power supply.
8	APS FILTER	Outputs voltage related to phase difference between VCO output locked on the (Q) side and IF input signal on the (P) side.
Ø	VIDEO OUT	Detection output pin on the (P) side. Driven by externally connecting resistance $1k\Omega$ .
· Ø	AFT OUT	Outputs AFT waveform by connecting external resistance. Detection sensitivity can be adjusted by changing the resistance.
<b>@</b>	EQ IN	Serves as EQ AMP input pin. Also inputs IF AGC on the (P) side.
	(\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Connected to power supply internally.
<b>30</b>	(Vcc)	our course to porter deppty manually.