MITSUBISHI CMOS LOGIC

M4053BP
M4053BFP

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M4053BP is a semiconductor integrated circuit consisting of three multiplexer/demultiplexers which use 1-bit digital inputs to perform selection of two analog switches.

FEATURES

- Low ON resistance: 50Ω typ. (V_{DD}=15V)
- High OFF resistance: 10^9Ω or greater (typ)
- Small differences in ON resistance between each switch in the package: 10Ω typ. (V_{DD} = 7.5V, V_{SS} = −7.5V)
- Linearized transfer characteristics: 0.07% distortion (typ)
- Signals with amplitude greater than the logic level amplitude of the control inputs may be switched.
- Provided with an inhibit input

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

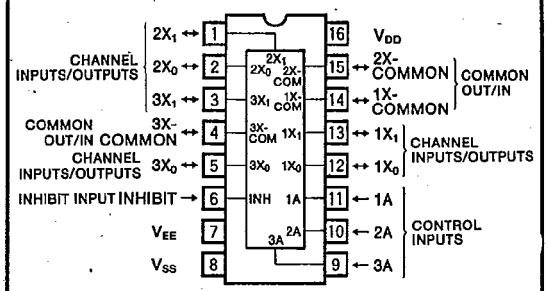
FUNCTIONAL DESCRIPTION

When a 1-bit binary input signal is applied to the control inputs (A), the channel numbers corresponding to the binary value input (X_0, X_1) are set to low impedance with respect to the corresponding (X-COMMON). All other channels remain at high impedance.

In this operation, if the (INHIBIT) input is held high, all channels (X_0, X_1) will be put in the high-impedance state, regardless of the state of the other inputs.

It is possible to switch an analog signal of amplitude V_{DD}-V_{EE} if this is greater than the logic level span V_{DD}-V_{SS} for inputs (A).

PIN COFIGRATION (TOP VIEW)



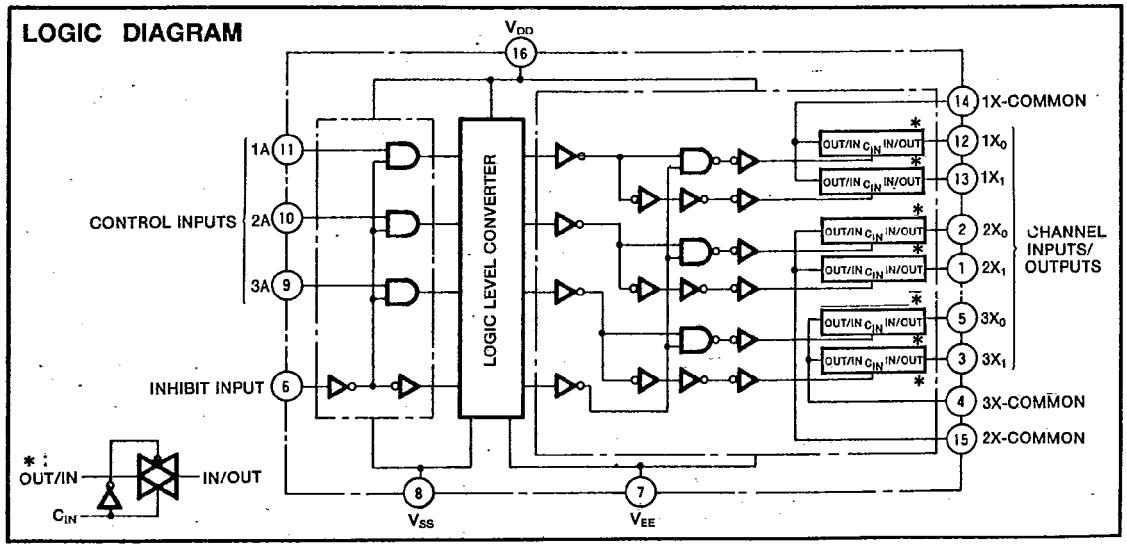
Outline 16P4
16P2N

FUNCTION TABLE (Note 1)

Inhibit Input	Control Inputs	Channel INPUT/OUTPUT to COMMON switch selection	
INHIBIT	A	X_0	X_1
L	L	ON	OFF
L	H	OFF	ON
H	X	FF	OFF

Note 1 : X : Irrelevant
ON : Low impedance between X_n and X-COMMON (n=0,1)
OFF : High impedance between X_n and X-COMMON (n=0,1)

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage		−0.5∼20	V
V_{DD}-V_{EE}			−0.5∼20	V
V_I	Input voltage	Control and inhibit inputs	V_{SS}−0.5∼V_{DD}+0.5	V
		Channel and common inputs	V_{EE}−0.5∼V_{DD}+0.5	
V_{IO}	Input-to-output voltage		±0.5	V
I_I	Input current	Control and inhibit inputs	±10	mA
I_O	Output current	Switch-off	±10	mA
V_O	Output voltage	Channel and common outputs	V_{EE}−0.5∼V_{DD}+0.5	V
Topr	Operating temperature range		−40∼+85	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATNG CONDITING CONDITIONS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{DD}-V_{SS}	Supply voltage		3		18	V
V_{DD}-V_{EE}			3		18	V
V_I	Input voltage	Control and inhibit inputs	V_{SS}		V_{DD}	V
		Channel and common inputs	V_{EE}		V_{DD}	
V_O	Output voltage		V_{EE}		V_{DD}	V

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

Symbol	Parameter	Test conditions	V_{EE}(V)	V_{DD}(V)	Limits −40℃ Min	−40℃ Max	25℃ Min	25℃ Typ	25℃ Max	85℃ Min	85℃ Max	Unit
V_{IH}	"H" input voltage (A, B, C, INHIBIT)	Input-to-output current=10μA	0	5	3.5		3.5			3.5		V
			0	10	7.0		7.0			7.0		
			0	15	11.0		11.0			11.0		
V_{IL}	"L" input current (A, B, C, INHIBIT)	Input-to-output current=10μA	0	5		1.5			1.5		1.5	V
			0	10		3.0			3.0		3.0	
			0	15		4.0			4.0		4.0	
R_{ON}	ON resistance	V_I=5V	0	5		500			600		800	Ω
		V_I=2.5V	0	5		850			950		1300	
		V_I=0.25V	0	5		500			600		800	
		V_I=10V	0	10		210			250		300	
		V_I=5V	0	10		210			250		300	
		V_I=0.25V	0	10		210			250		300	
		V_I=15V	0	15		140			160		200	
		V_I=7.5V	0	15		140			160		200	
		V_I=0.25V	0	15		140			160		200	
		V_I=5V	−5	5		210			250		300	
		V_I=±0.25V	−5	5		210			250		300	
		V_I=−5V	−5	5		210			250		300	
		V_I=7.5V	−7.5	7.5		140			160		200	
		V_I=±0.25V	−7.5	7.5		140			160		200	
	Test circuit 1	V_I=−7.5V	−7.5	7.5		140			160		200	
ΔR_{ON}	ON resistance variations between switches of the same pckage		−2.5	2.5				30				Ω
			−5	5				15				
			−7.5	7.5				10				
I_{OFF}	Input-to-output off-state leakage current (X_0∼X_1-X-COMMON)	$V_{I/O}$=10V, $V_{O/I}$=0V	0	10					125			nA
		$V_{I/O}$=0V, $V_{O/I}$=10V	0	10					−125			
		$V_{I/O}$=18V, $V_{O/I}$=0V	0	18		250			250		1000	
		$V_{I/O}$=0V, $V_{O/I}$=18V	0	18		−250			−250		−1000	
I_{DD}	Quiescent supply current	V_I=V_{DD}, V_{SS}	0	5		20			20		150	μA
			0	10		40			40		300	
			0	15		80			80		600	
I_{IH}	"H" input corrent (A, INH)	V_{IH}=18V	0	18		0.3			0.3		1.0	μA
I_{IL}	"L" input current (A, INH)	V_{IL}=0V	0	18		−0.3			−0.3		−1.0	μA

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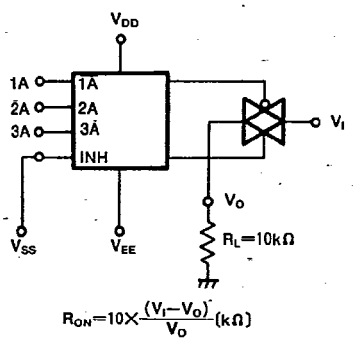
SWITCHING CHARACTERISTCS (T_a=25℃, V_{SS}=0V)

Symbol	Parameter	Tset conditions	V_{EE}(V)	V_{DD}(V)	Limits Min	Limits Typ	Limits Max	Unit
$f_{max(I/O)}$	Maximum transfer frequency	R_L=10kΩ, C_L=15pF Test circuit 2	−5	5		25		MHz
t_{PLH}	"L-H" and "H-L" output propagation time (A-X_0, X_1, X-COMMON)	R_L=10kΩ, C_L=50pF Test circuit 3	0	5			1000	ns
			0	10			500	
			0	15			400	
			−5	5			700	
			−7.5	7.5			500	
t_{PHL}			0	5			1000	ns
			0	10			500	
			0	15			400	
			−5	5			700	
			−7.5	7.5			500	
t_{PLH}	"L-H" and "H-L" output propation time (INHIBIT-X_0, X_1, X-COMMON)	R_L=10kΩ, C_L=50pF Tset circuit 4	0	5			1400	ns
			0	10			700	
			0	15			500	
			−5	5			900	
			−7.5	7.5			500	
t_{PHL}			0	5			1400	ns
			0	10			700	
			0	15			500	
			−5	5			900	
			−7.5	7.5			500	
t_{PLH}	"L-H" and "H-L" output propagation time (X_0, X_1/X-COMMON-X-COMMON/X_0, X_1)	R_L=10kΩ, C_L=50pF Test circuit 5	0	5			45	ns
			0	10			30	
			0	15			20	
t_{PHL}			0	5			45	ns
			0	10			30	
			0	15			20	
—	Sine-wave distortion	R_L=10kΩ, f_i=1kHz Test circuit 2	−5	5		0.1		%
—	Feedthrough (switch off)	R_L=1kΩ Test circuit 6	−5	5		500		kHz
—	Crosstalk (A, INHIBIT-X_0, X_1, X-COMMON)	R_i=1kΩ, R_L=10kΩ, C_L=15pF Test circuit 7	0	5		200		mV
			0	10		300		
			0	15		400		
C_I	Input capacitance	Control and inhibit inputs					7.5	pF
		Channel and common inputs				10		

TEST CIRCUITS (V_{SS}=0V, capacitance C_L includes stray wirig capacitance and probe input capacitance)

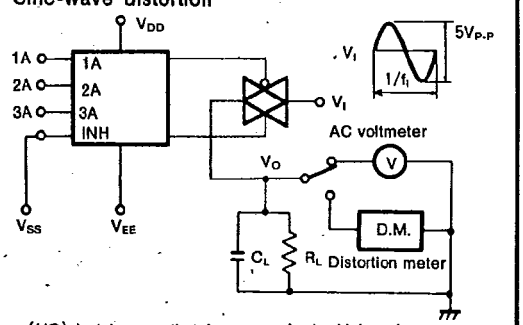
1 ON resistance (R_{ON})



$$R_{ON}=10\times\frac{(V_I-V_O)}{V_O}(k\Omega)$$

Refer to the function table for conditions of control input A.

2 Maximum transfer frequency (fmax(I/O))
Sine-wave distortion



fmax (I/O) is taken as that frequency f_i at which, using a sine-wave input of 2.5V_{P-P}, 20 $\log_{10}(V_O/V_I)$ = −3dB. Refer to the function table for conditions of control input A.

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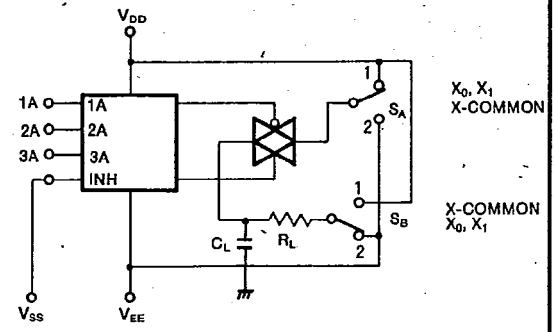
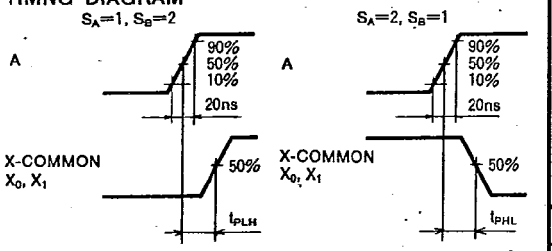
3 "L-H" and "H-L" output propagation time
(A-X_0, X_1, X-COMMON)

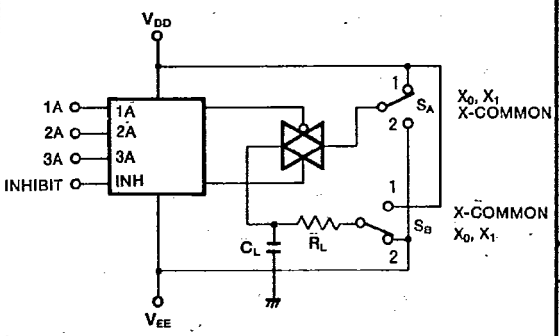


TIMNG DIAGRAM

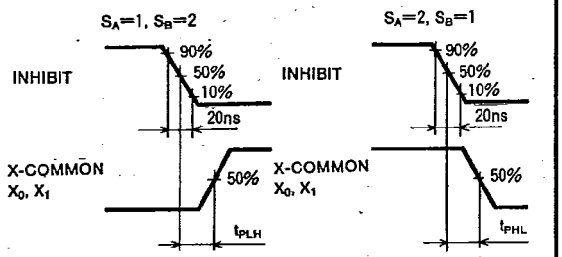


Refer to the function table for conditions of control input A.

4 "L-H" and "H-L" output propagation time
(INHIBIT-X_0, X_1, X-COMMON)

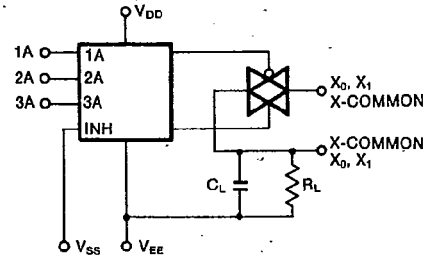


TIMNG DIAGRAM

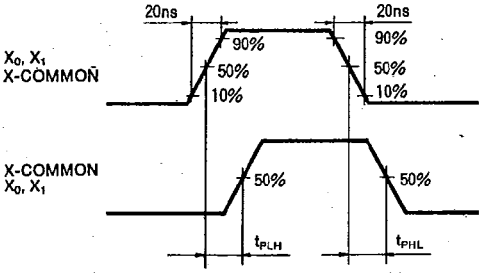


Refer to the function table for conditions of control input A.

5 "L-H" and "H-L" output propagation time
(X_0, X_1/X-COMMON-X-COMMON/X_0, X_1)

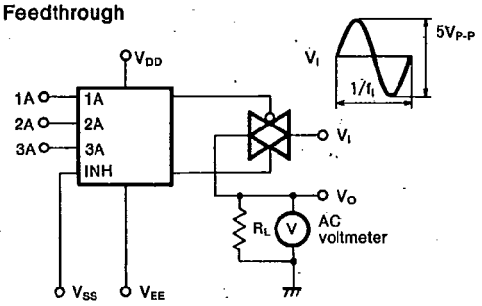


TIMNG DIAGRAM



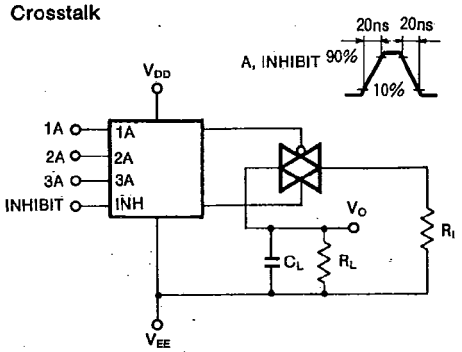
Refer to the function table for conditions of control input A.

6 Feedthrough



The feedthrough is taken as that frequency f_I at which, using a sine-wave input of $2.5V_{P-P}$, $20\log_{10}(V_O/V_I) = -50$dB. Refer to the function table for conditions of control input A.

7 Crosstalk



Refer to the function table for conditions of control input A.

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