M3800x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3800x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3800x group is designed for office automation equipment, household appliances and include four timers, serial I/O function.

The various microcomputers in the M3800x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3800x group, see the section on group expansion.

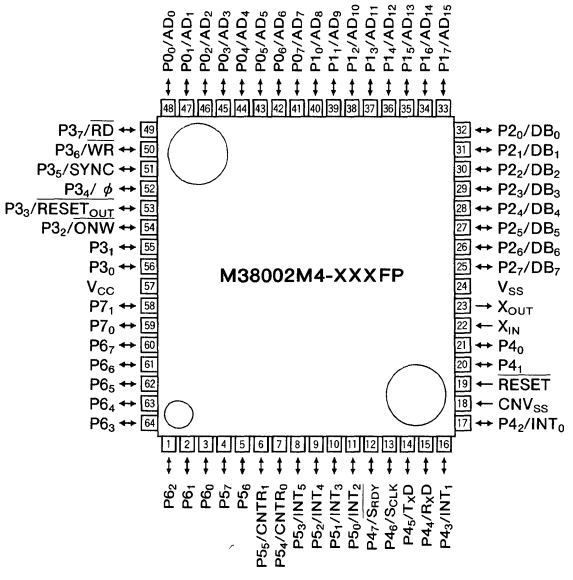
FEATURES

- Basic machine-language instructions 71
- Instruction execution time 0.5μs
  (shortest instruction at 8MHz oscillation frequency)
- Memory size
  ROM ..... 4K to 32K bytes
  RAM ..... 192 to 1024 bytes
- Programmable input/output ports 58
- Interrupts ..... 15 sources, 15 vectors
- Timers ..... 8 bit×4
- Serial I/O ..... 8-bit×1(UART or Clock-synchronized)
- Clock generation circuit ..... Internal feedback amplifier
  (connect to external ceramic resonator or quartz crystal)
- Supply voltage ..... 3.0 to 5.5V
- Low power dissipation 32mW
- Memory expansion possible
- Operating temperature range ..... −20 to 85°C

APPLICATIONS

Office automation, factory automation, household appliances, and other consumer applications, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N
64-pin plastic-molded QFP

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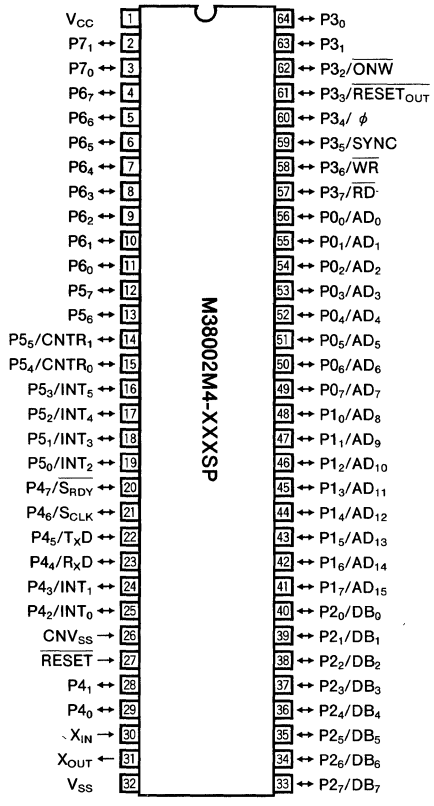
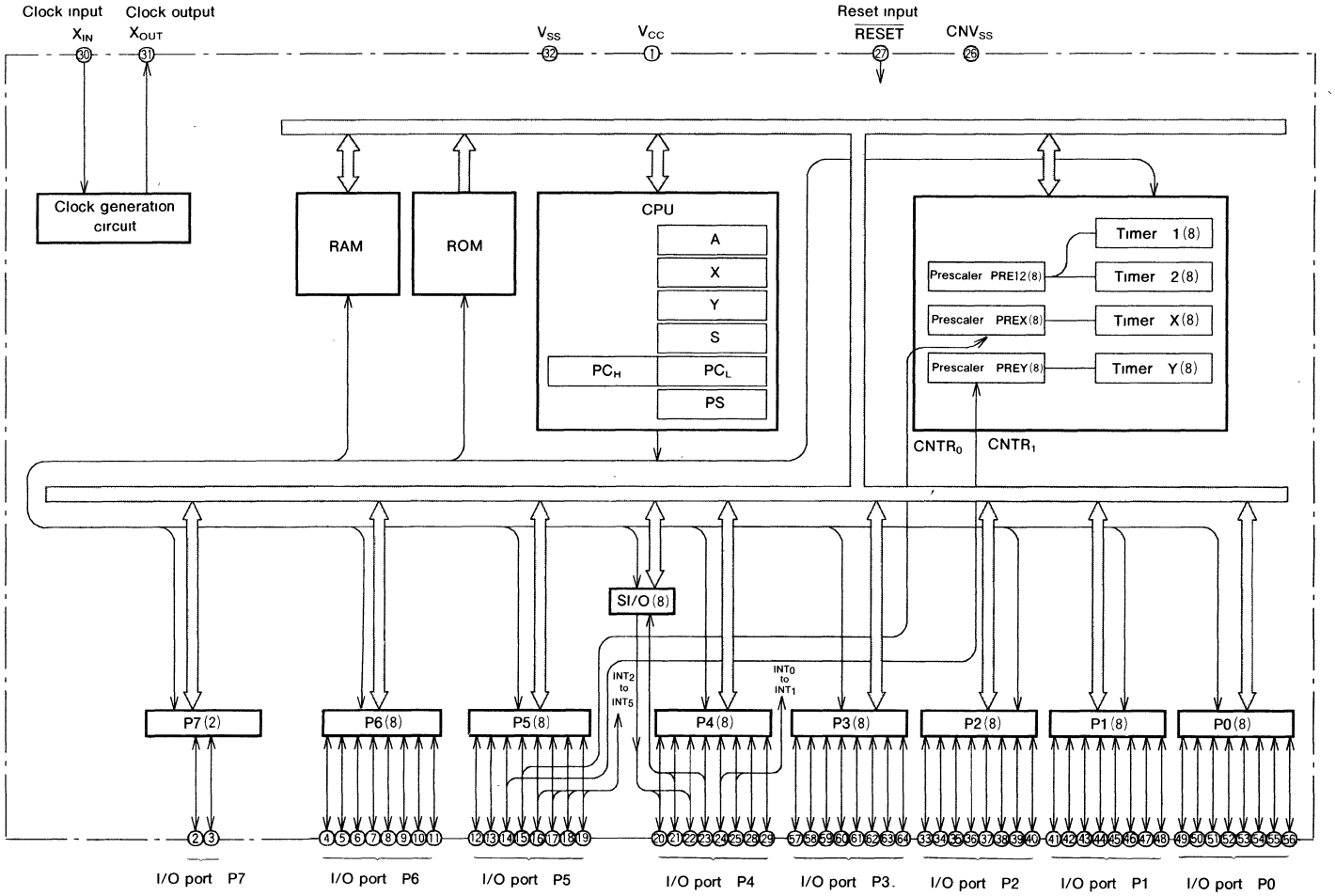
PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B
64-pin shrink plastic-molded DIP

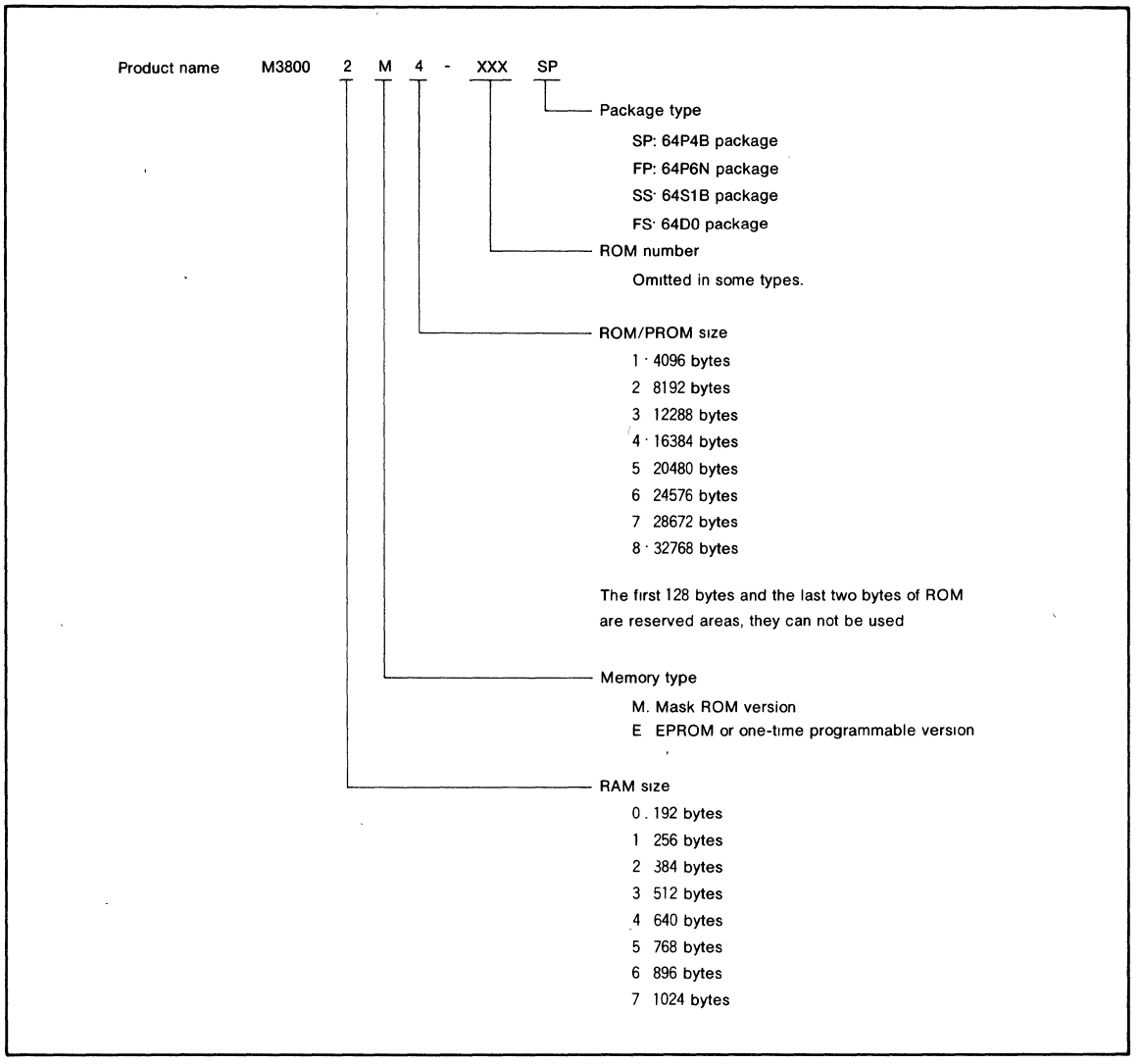
FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}	Power supply	Power supply inputs 3.0 to 5.5V to V_{CC}, and 0V to V_{SS}	
V_{SS}			
CNV_{SS}	CNV_{SS}	This pin controls the operation mode of the chip. Normally connected to V_{SS}. If this pin is connected to V_{CC}, the internal ROM is inhibited and external memory is accessed.	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions.	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$—$P0_7$	I/O port P0	An 8-bit CMOS I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. At reset this port is set to input mode. In modes other than single-chip, these pins are used as address, data, and control bus I/O pins.	
$P1_0$—$P1_7$	I/O port P1		
$P2_0$—$P2_7$	I/O port P2		
$P3_0$—$P3_7$	I/O port P3		
$P4_0$, $P4_1$	I/O port P4	An 8-bit CMOS I/O port with the same function as port P0	
$P4_2/INT_0$, $P4_3/INT_1$			External interrupt input pins
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/S_{CLK}$, $P4_7/\overline{S_{RDY}}$			Serial I/O I/O pins
$P5_0/INT_2$—$P5_3/INT_5$	I/O port P5	An 8-bit CMOS I/O port with the same function as port P0	External interrupt input pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			Timer X and Timer Y I/O pins
$P5_6$, $P5_7$			
$P6_0$—$P6_7$	I/O port P6	An 8-bit CMOS I/O port with the same function as port P0	
$P7_0$, $P7_1$	I/O port P7	An 2-bit CMOS I/O port with the same function as port P0	

PART NUMBERING



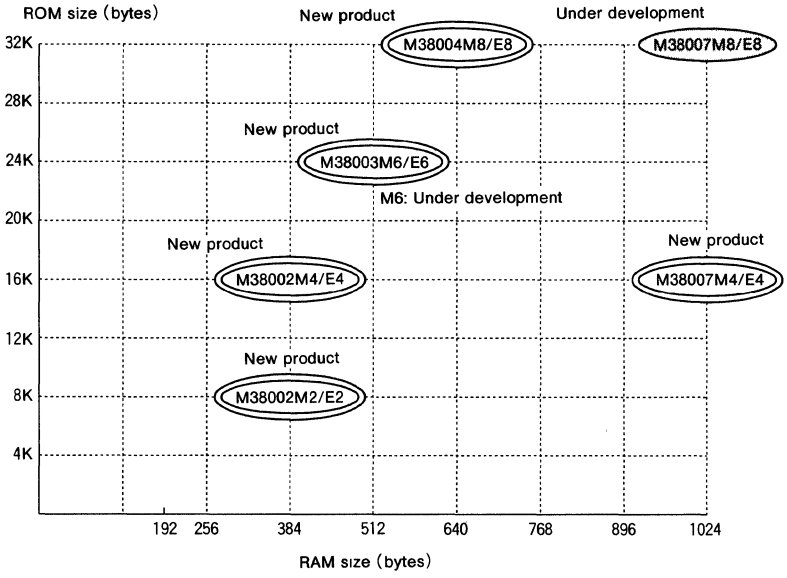
GROUP EXPANSION

Mitsubishi plans to expand the M3800x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions
ROM/PROM capacity ..... 8K to 32K bytes
RAM capacity ..... 384 to 1024 bytes

(2) Packages
64P4B ..... Shrink plastic molded DIP
64P6N ..... Plastic molded QFP
64S1B ..... Shrink ceramic DIP
64D0 ..... Ceramic LCC

Memory expansion plan



The development schedule and other details of products under development may be revised without notice
Currently supported products are listed below

As of March 1992

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38002M4-XXXSP	16K	384	64P4B	Mask ROM version
M38002E4-XXXSP				One-time programmable version
M38002E4SP				One-time programmable version (blank)
M38002M4-XXXFP			64P6N	Mask ROM version
M38002E4-XXXFP				One-time programmable version
M38002E4FP				One-time programmable version (blank)
M38002E4SS			64S1B	EPROM version
M38002E4FS			64D0	EPROM version
M38002M2-XXXSP	8K	384	64P4B	Mask ROM version
M38002E2-XXXSP				One-time programmable version
M38002E2SP				One-time programmable version (blank)
M38002M2-XXXFP			64P6N	Mask ROM version
M38002E2-XXXFP				One-time programmable version
M38002E2FP				One-time programmable version (blank)
M38002E2SS			64S1B	EPROM version
M38002E2FS			64D0	EPROM version
M38004M8-XXXSP	32K	640	64P4B	Mask ROM version
M38004E8-XXXSP				One-time programmable version
M38004E8SP				One-time programmable version (blank)
M38004M8-XXXFP			64P6N	Mask ROM version
M38004E8-XXXFP				One-time programmable version
M38004E8FP				One-time programmable version (blank)
M38004E8SS			64S1B	EPROM version
M38004E8FS			64D0	EPROM version
M38007M4-XXXSP	8K	1024	64P4B	Mask ROM version
M38007E4-XXXSP				One-time programmable version
M38007E4SP				One-time programmable version (blank)
M38007M4-XXXFP			64P6N	Mask ROM version
M38007E4-XXXFP				One-time programmable version
M38007E4FP				One-time programmable version (blank)
M38007E4SS			64S1B	EPROM version
M38007E4FS			64D0	EPROM version
M38003E6-XXXSP	24K	512	64P4B	One-time programmable version
M38003E6SP				One-time programmable version (blank)
M38003E6-XXXFP			64P6N	One-time programmable version
M38003E6FP				One-time programmable version (blank)
M38003E6SS			64S1B	EPROM version
M38003E6FS			64D0	EPROM version

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

Microcomputers of the M3800x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

The FST and SLW instructions are not available for use.

The STP, WIT, MUL, and DIV instructions can be used.

CPU Mode Register

The CPU mode register (address $003B_{16}$) contains processor mode bits that specify the operating mode of the chip. The CPU mode register also contains the stack page select bit.

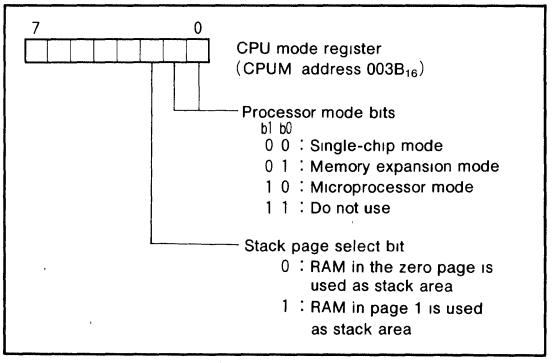


Fig. 1 Structure of CPU mode register

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MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

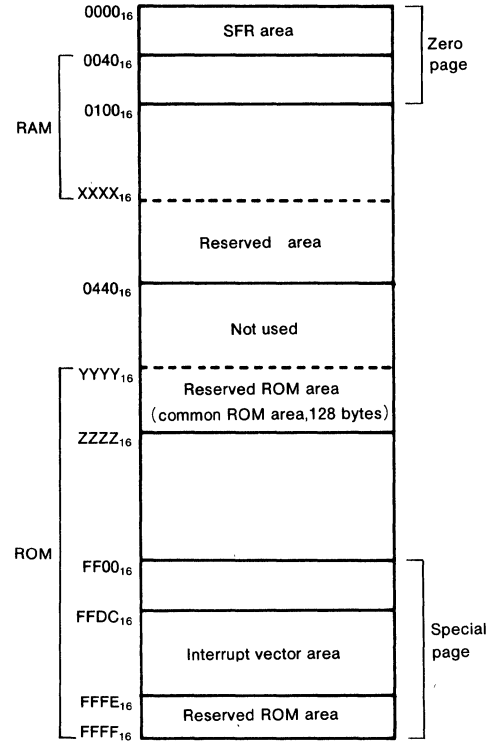


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Port P7 (P7)
$000F_{16}$	Port P7 direction register (P7D)
0010_{16}	
0011_{16}	
0012_{16}	
0013_{16}	
0014_{16}	
0015_{16}	
0016_{16}	
0017_{16}	
0018_{16}	Transmit/receive buffer (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	
$001E_{16}$	
$001F_{16}$	

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	
0029_{16}	
$002A_{16}$	
$002B_{16}$	
$002C_{16}$	
$002D_{16}$	
$002E_{16}$	
$002F_{16}$	
0030_{16}	
0031_{16}	
0032_{16}	
0033_{16}	
0034_{16}	
0035_{16}	
0036_{16}	
0037_{16}	
0038_{16}	
0039_{16}	
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

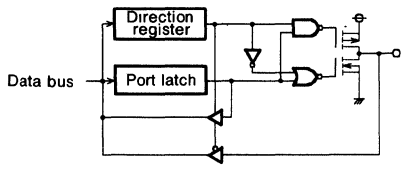
The M3800x group microprocessors have 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P7). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

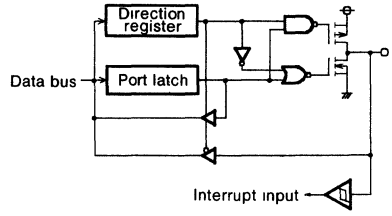
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref No.
$P0_0$—$P0_7$	Port P0	Input/output, individual bits	CMOS 3-state output CMOS level input	Address lower-byte output	CPU mode register	(1)
$P1_0$—$P1_7$	Port P1	Input/output, individual bits	CMOS 3-state output CMOS level input	Address upper-byte output	CPU mode register	
$P2_0$—$P2_7$	Port P2	Input/output, individual bits	CMOS 3-state output CMOS level input	Data bus I/O	CPU mode register	
$P3_0$—$P3_7$	Port P3	Input/output, individual bits	CMOS 3-state output CMOS level input	Control signal I/O	CPU mode register	
$P4_0$, $P4_1$	Port P4	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P4_2/INT_0$, $P4_3/INT_1$				External interrupt input	Interrupt edge selection register	(2)
$P4_4/R_XD$,				Serial I/O function I/O	Serial I/O control register UART control register	(3)
$P4_5/T_XD$,						(4)
$P4_6/S_{CLK}$,						(5)
$P4_7/\overline{S_{RDY}}$						(6)
$P5_0/INT_2$, $P5_1/INT_3$, $P5_2/INT_4$, $P5_3/INT_5$	Port P5	Input/output, individual bits	CMOS 3-state output CMOS level input	External interrupt input	Interrupt edge selection register	(7)
$P5_4/CNTR_0$, $P5_5/CNTR_1$				Timer XY function I/O		(8)
$P5_6$, $P5_7$						(9)
$P6_0$—$P6_7$	Port P6	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P7_0$, $P7_1$	Port P7	Input/output, individual bits	CMOS 3-state output CMOS level input			

Note : For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, see the applicable sections

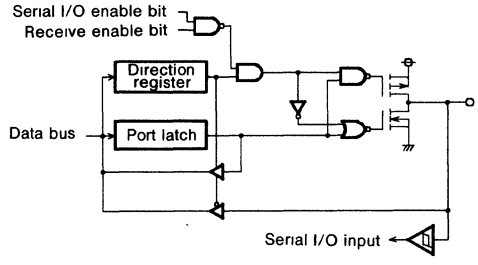
(1) Port P0, P1, P2, P3, $P4_0$ or $P4_1$



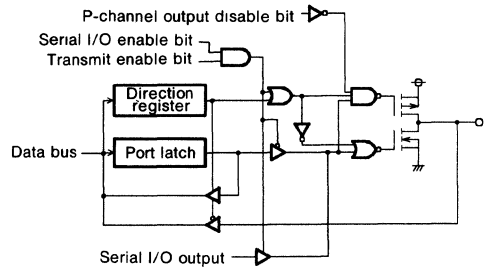
(2) Port $P4_2$ or $P4_3$



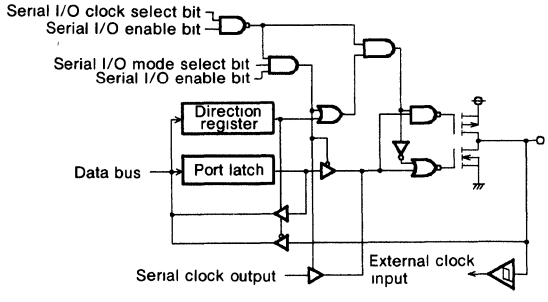
(3) Port $P4_4$



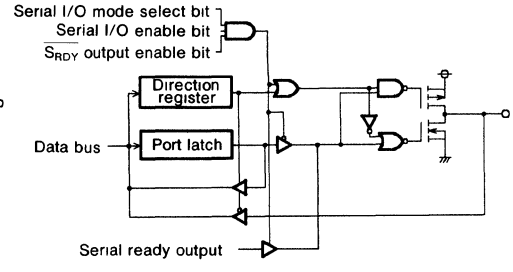
(4) Port $P4_5$



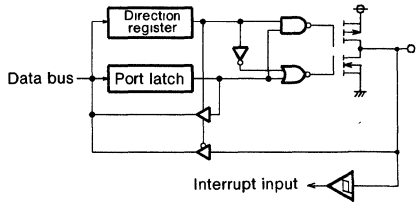
(5) Port $P4_6$



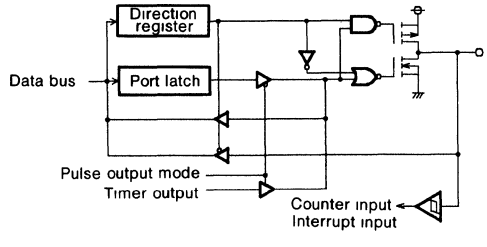
(6) Port $P4_7$



(7) Port $P5_0$ to $P5_3$



(8) Port $P5_4$ or $P5_5$



(9) Port $P5_6$, $P5_7$, P6 or P7

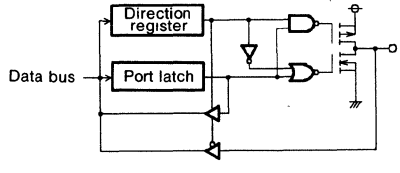


Fig. 4 Port block diagram (single-chip mode)

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INTERRUPTS

A total of 15 sources can generate interrupts: 8 external, 6 internal, and 1 software.

● **Interrupt Control**

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag-except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software

Interrupt request bits can be cleared by software, but cannot be set by software.

The I flag disables all interrupts except for the BRK instruction interrupt.

● **Interrupt Operation**

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

● **Notes on Use**

When the active edge of an external interrupt (INT_0 to INT_5, $CNTR_0$, or $CNTR_1$) is changed, the corresponding interrupt request bit may also be set. To insure proper operation when selecting the active edge, disable interrupts before setting the interrupt edge selection.

Table 1 Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O reception	4	$FFF7_{16}$	$FFF6_{16}$	At end of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O transmission	5	$FFF5_{16}$	$FFF4_{16}$	At end of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X overflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y overflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 overflow	STP release timer overflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 overflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
INT_2	12	$FFE7_{16}$	$FFE6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
INT_5	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_5 input	External interrupt (active edge selectable)
BRK instruction	16	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1 : Vector addresses contain interrupt jump destination addresses
2 : Reset function in the same way as an interrupt with the highest priority

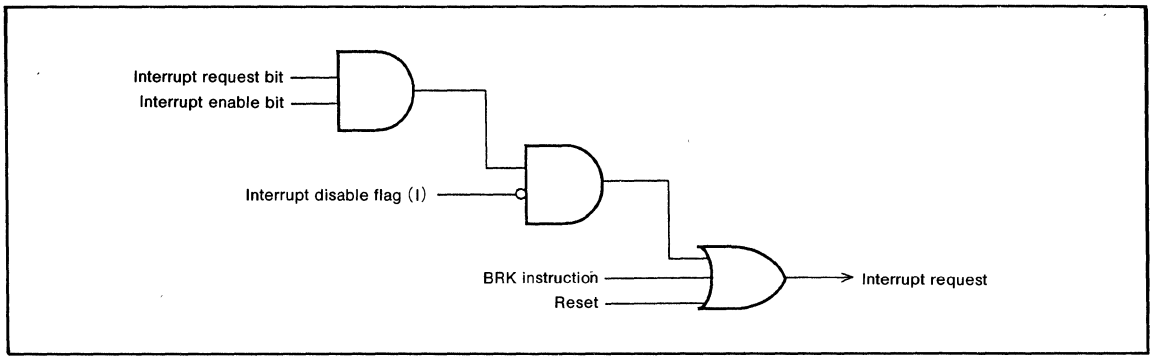


Fig. 5 Interrupt control

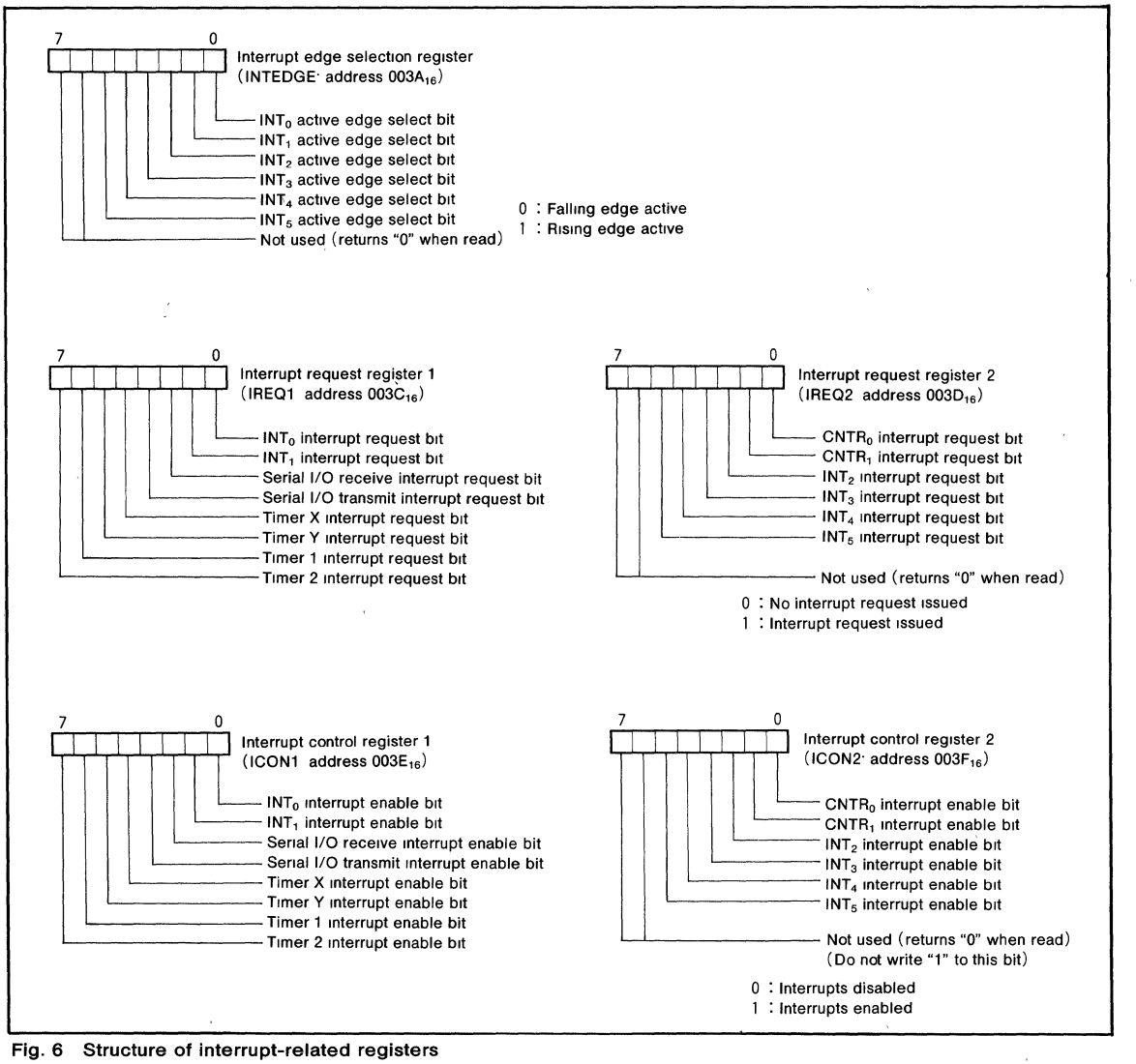


Fig. 6 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3800x group have 4 timers: timer X, timer Y, timer 1, and timer 2.

The timers count down. Once a timer reaches 00_{16}, the next count pulse reloads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1.

The divide ratio of each timer or prescaler is given by $1/(n+1)$, where n is the value in the corresponding timer or prescaler latch.

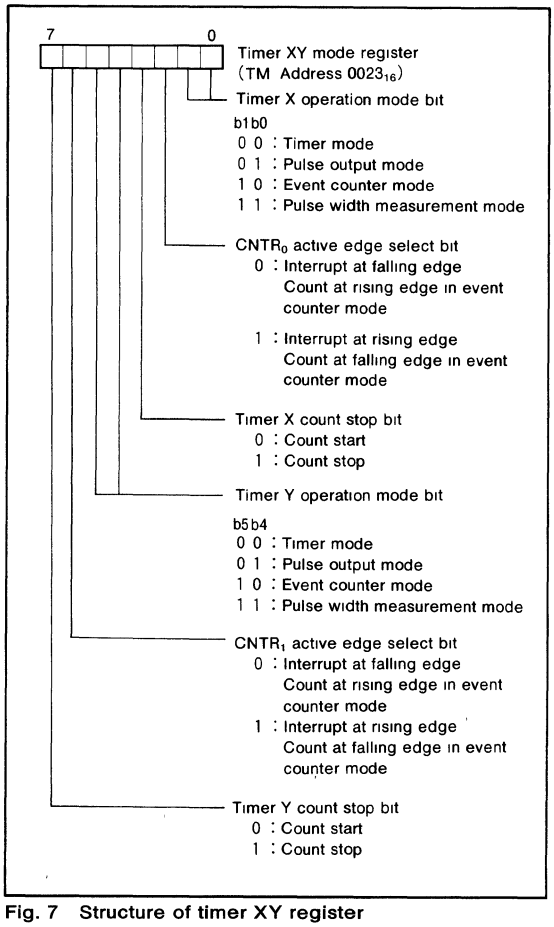


Fig. 7 Structure of timer XY register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer overflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each be set to operate in one of four operating modes by setting the timer XY mode register.

1. Timer Mode
   In timer mode, the timer counts a signal that is the oscillation frequency divided by 16.
2. Pulse Output Mode
   Timer X (or timer Y) counts a signal which is the oscillation frequency divided by 16. Whenever the contents of the timer reach "0", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", output begins at "H". If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.
3. Event Counter Mode
   Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.
4. Pulse Width Measurement Mode
   If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", the timer counts at the oscillation frequency divided by 16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "1", the count continues during the time that the $CNTR_0$ (or $CNTR_1$) pin is at "L"

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer overflows, the corresponding interrupt request bit is set.

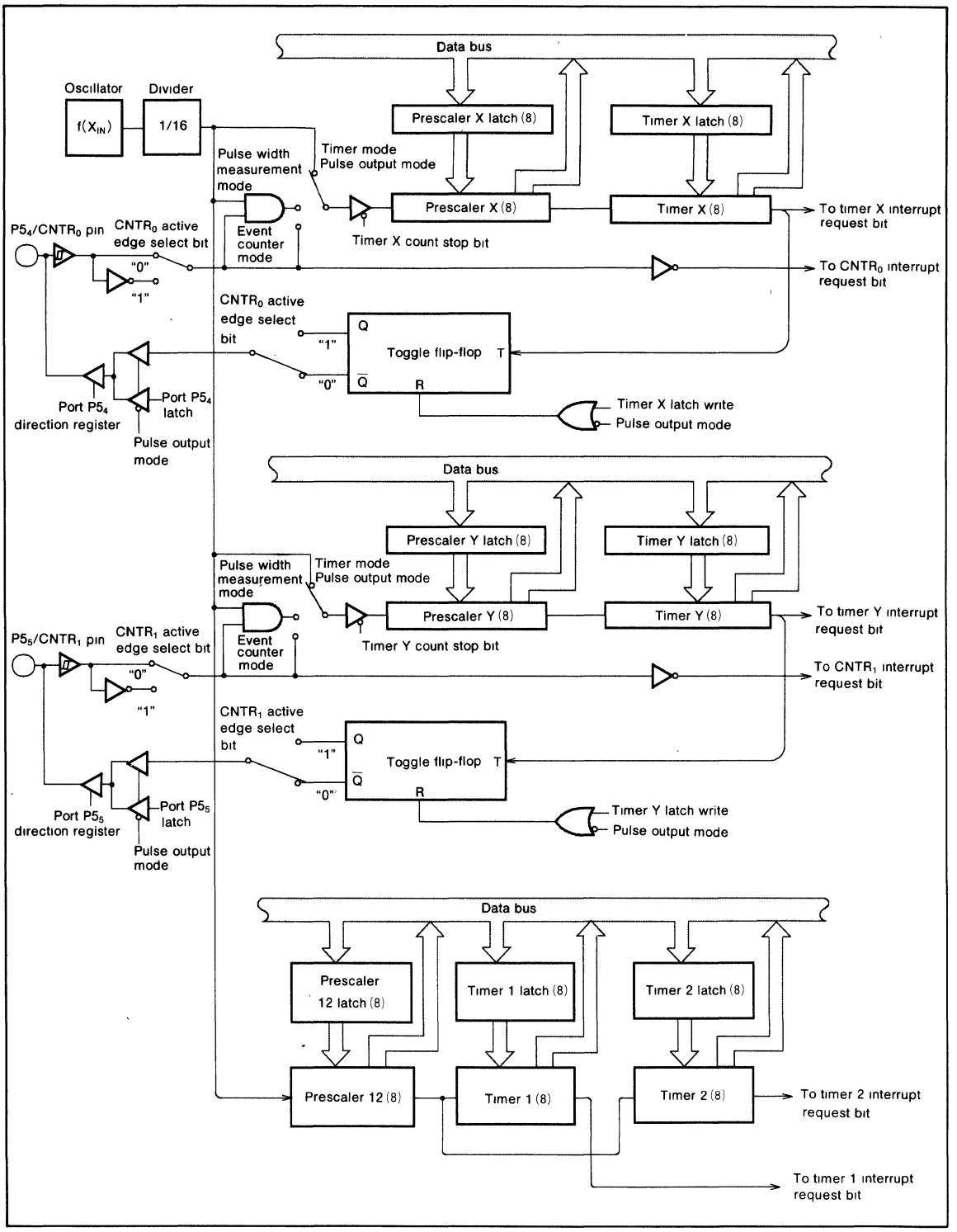


Fig. 8 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O mode can be selected by setting the mode select bit of the serial I/O control register to "1"

For clock-synchronized serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

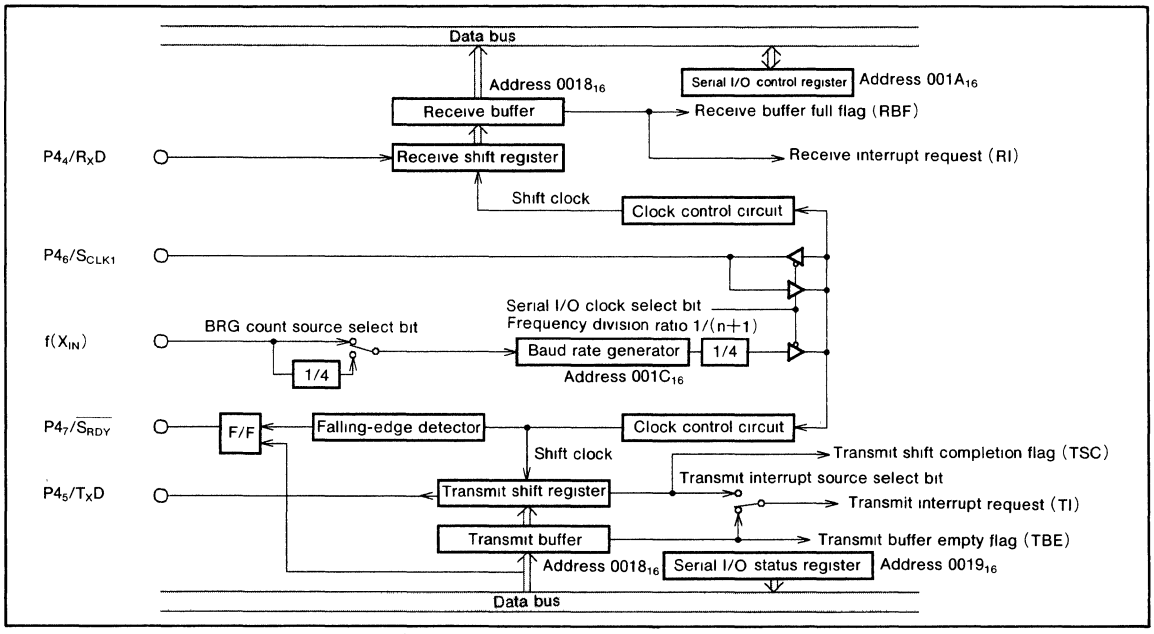
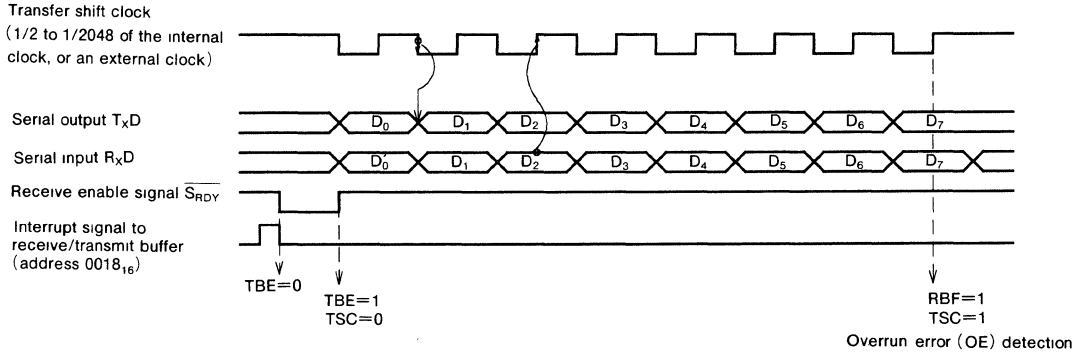


Fig. 9 Block diagram of clock-synchronized serial I/O



Note 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source select bit (TIC) of the serial I/O control register

2 : If data is written to the transfer buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin

3 : The receive interrupt (RI) is set when the receive buffer full (RBF) flag becomes "1"

Fig. 10 Operation of clock-synchronized serial I/O function

(2) Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode select bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

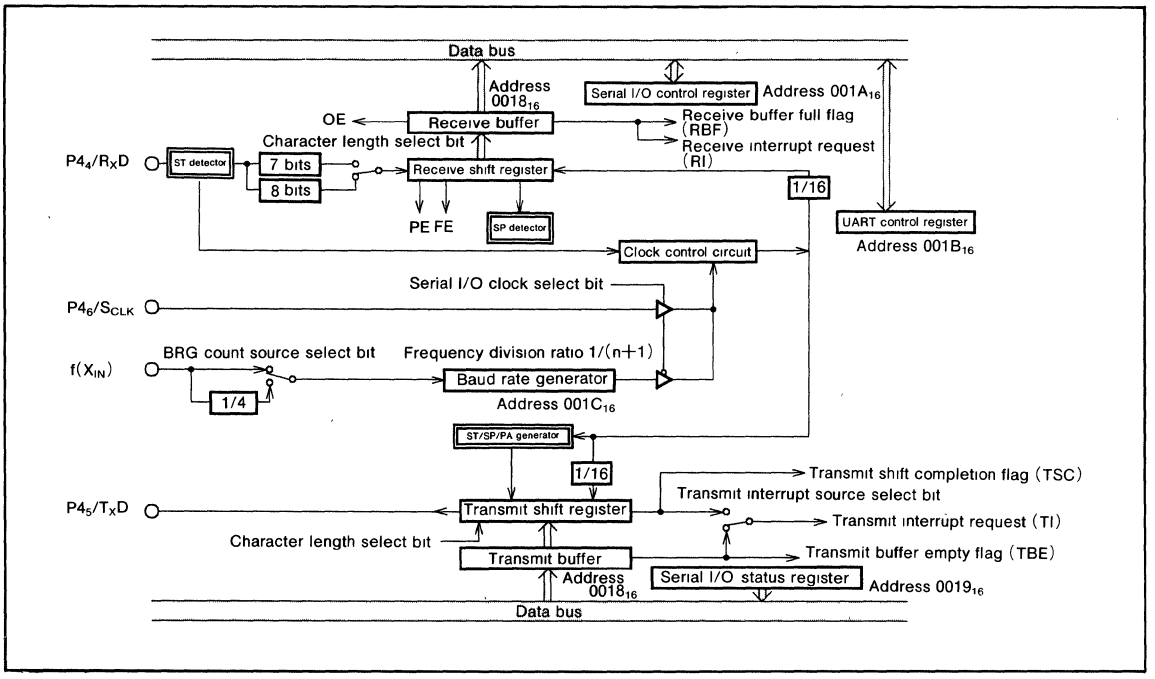
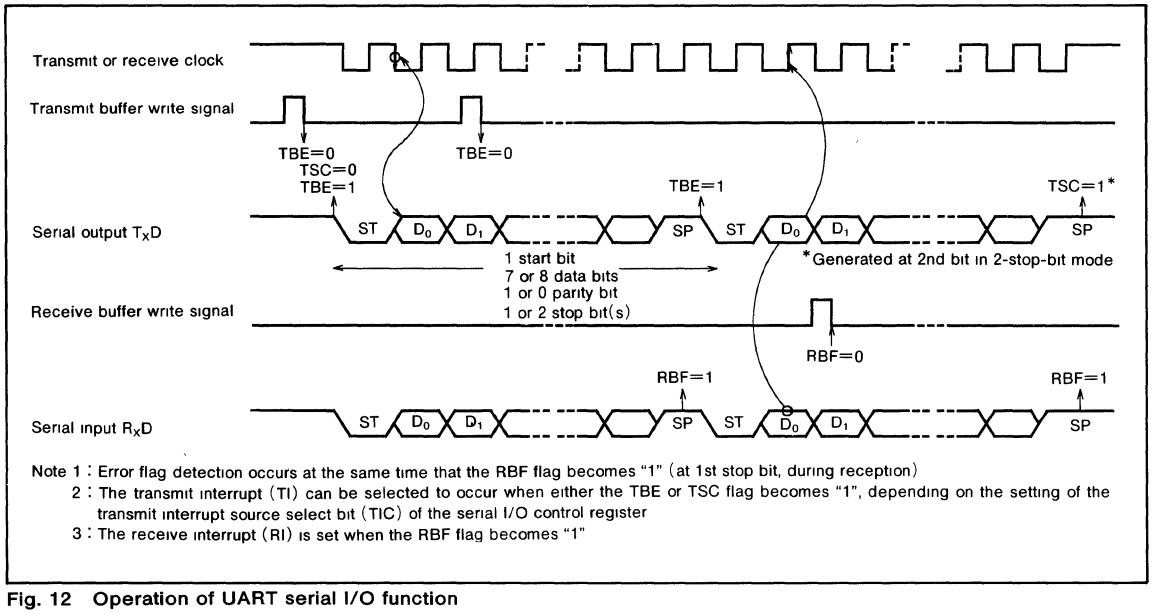


Fig. 11 Block diagram of UART serial I/O



Note 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception)
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source select bit (TIC) of the serial I/O control register
3 : The receive interrupt (RI) is set when the RBF flag becomes "1"

Fig. 12 Operation of UART serial I/O function

[Serial I/O Control Register (SIOCON) $001A_{16}$]

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON) $001B_{16}$]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P4_5/T_XD$ pin.

[Serial I/O Status Register (SIO1STS) 0019_{16}]

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit six, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmitter shift completion flag (bit 2) and the transmitter buffer empty flag (bit 0) become "1".

[Transmit Buffer/Receive Buffer (TB/RB) 0018_{16}]

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0"

[Baud Rate Generator (BRG) $001C_{16}$]

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the Baud Rate Generator.

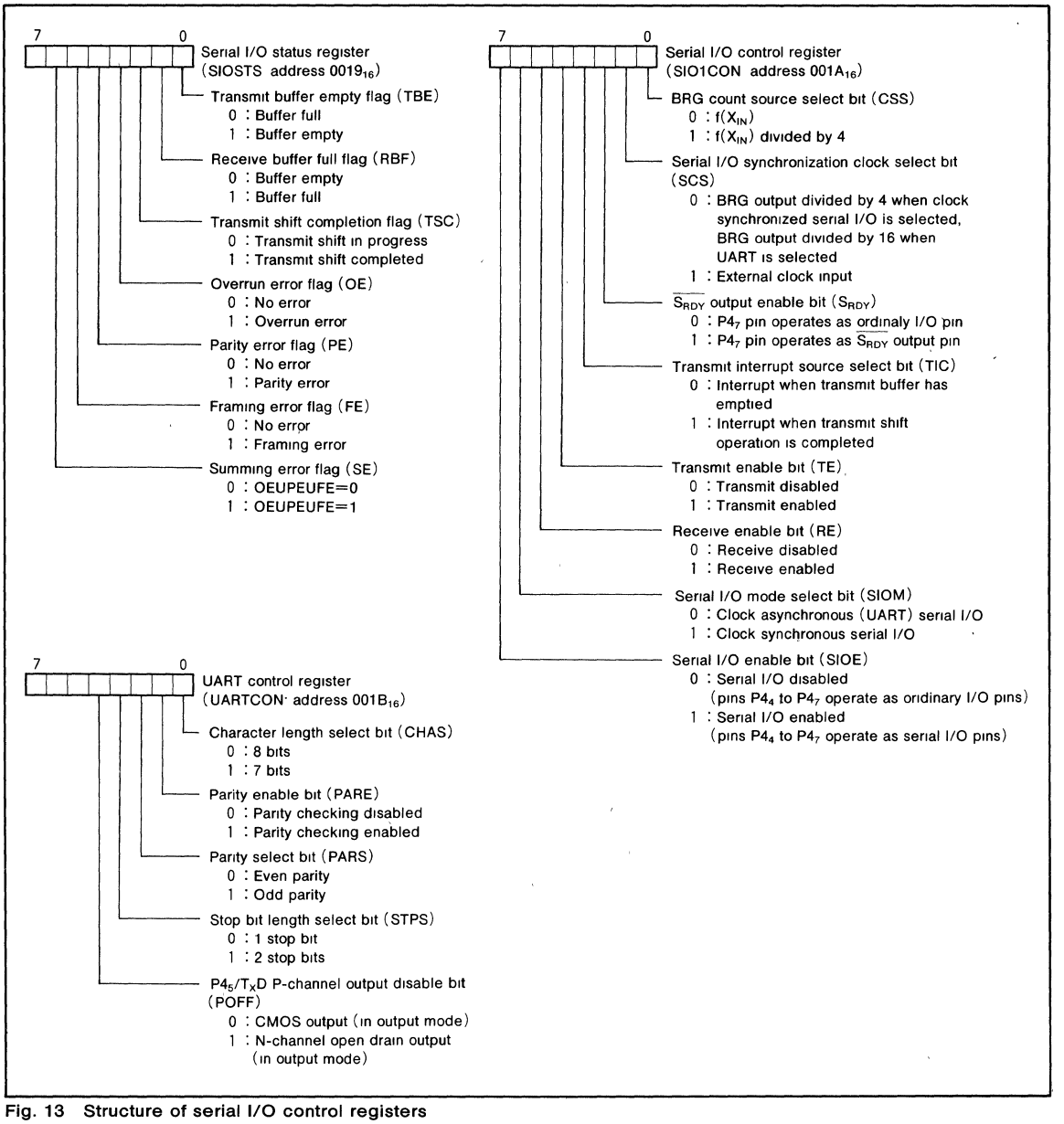


Fig. 13 Structure of serial I/O control registers

RESET CIRCUIT

A microcomputer in the M3800x group is reset if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least 2μs then is returned to a "H" level (the power supply voltage should be between 4.0V and 5.5V). In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 8 to 12 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
Make sure that the reset input voltage is no more than 0.8V for a power supply voltage of 4.0V.

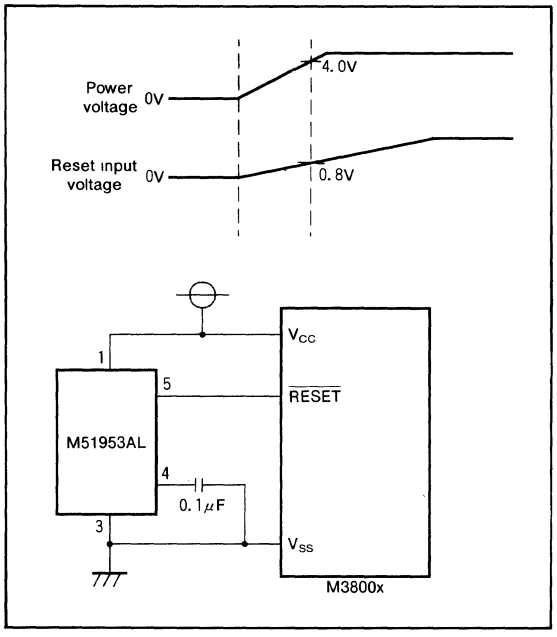


Fig. 14 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	$(0001_{16})\cdots$	00_{16}
(2) Port P1 direction register	$(0003_{16})\cdots$	00_{16}
(3) Port P2 direction register	$(0005_{16})\cdots$	00_{16}
(4) Port P3 direction register	$(0007_{16})\cdots$	00_{16}
(5) Port P4 direction register	$(0009_{16})\cdots$	00_{16}
(6) Port P5 direction register	$(000B_{16})\cdots$	00_{16}
(7) Port P6 direction register	$(000D_{16})\cdots$	00_{16}
(8) Port P7 direction register	$(000F_{16})\cdots$	00_{16}
(9) Serial I/O status register	$(0019_{16})\cdots$	1 0 0 0 0 0 0 0
(10) Serial I/O control register	$(001A_{16})\cdots$	00_{16}
(11) UART control register	$(001B_{16})\cdots$	1 1 1 0 0 0 0 0
(12) Prescaler 12	$(0020_{16})\cdots$	FF_{16}
(13) Timer 1	$(0021_{16})\cdots$	01_{16}
(14) Timer 2	$(0022_{16})\cdots$	FF_{16}
(15) Timer XY mode register	$(0023_{16})\cdots$	00_{16}
(16) Prescaler X	$(0024_{16})\cdots$	FF_{16}
(17) Timer X	$(0025_{16})\cdots$	FF_{16}
(18) Prescaler Y	$(0026_{16})\cdots$	FF_{16}
(19) Timer Y	$(0027_{16})\cdots$	FF_{16}
(20) Interrupt edge selection register	$(003A_{16})\cdots$	00_{16}
(21) CPU mode register	$(003B_{16})\cdots$	0 0 0 0 0 0 ※ 0
(22) Interrupt control register 1	$(003E_{16})\cdots$	00_{16}
(23) Interrupt control register 2	$(003F_{16})\cdots$	00_{16}
(24) Processor status register	(PS)···	X X X X X 1 X X
(25) Program counter	$(PC_H)\cdots$	Contents of address $FFFD_{16}$
	$(PC_L)\cdots$	Contents of address $FFFC_{16}$

Note : X : Undefined
※ : The initial values of CM_1 are determined by the level at the CNV_{SS} pin
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software

Fig. 15 Internal status of microcomputer after reset

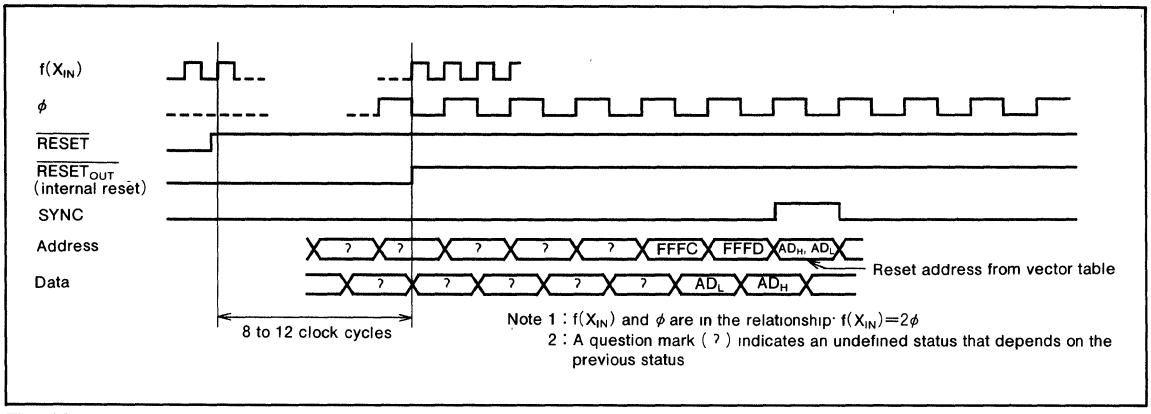


Fig. 16 Timing of reset

CLOCK GENERATION CIRCUIT

An oscillation circuit can be created by connecting a resonator between X_{IN} and X_{OUT}. When using an external clock signal, input the clock signal to the X_{IN} pin and leave the X_{OUT} pin open.

Oscillation Control

(1) Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H". Timer 1 is set to "FF_{16}" and prescaler 12 is set to "01_{16}".

Oscillation restarts when an external interrupt is received, but the internal clock ϕ remains at "H" until timer 1 overflows.

This allows time for the clock circuit oscillation to stabilize. If oscillation is restarted by a reset, no wait time is generated, so keep the $\overline{RESET}$ pin at "L" level until oscillation has stabilized.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at a "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 overflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

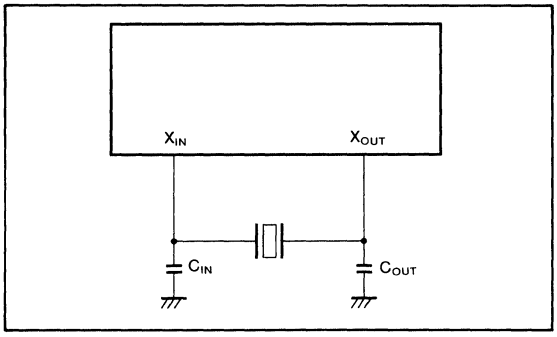


Fig. 17 Ceramic resonator circuit

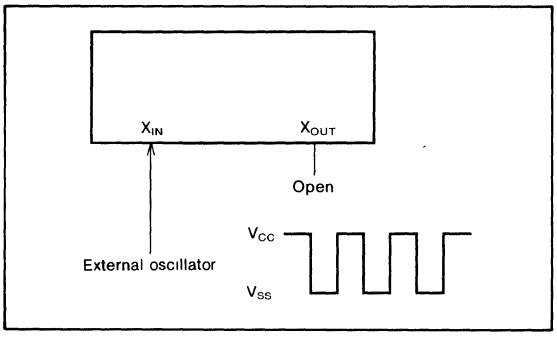


Fig. 18 External clock input circuit

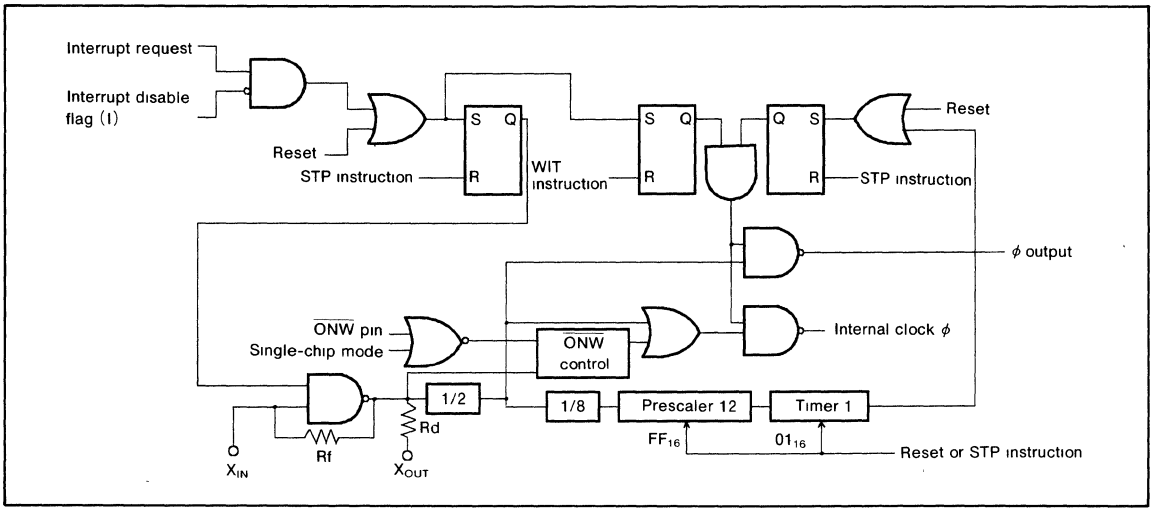


Fig. 19 Block diagram of clock generation circuit

PROCESSOR MODES

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM_0 and CM_1 (bits 0 and 1 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 2 Functions of ports in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs lower byte of address
Port P1	Outputs upper byte of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction codes)
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read) $P3_2$ is the $\overline{ONW}$ input pin $P3_3$ is the $\overline{RESET_{OUT}}$ output pin. (Note) $P3_4$ is the ϕ output pin $P3_5$ is the SYNC output pin $P3_6$ is the $\overline{WR}$ output pin, and $P3_7$ is the $\overline{RD}$ output pin.

Note : If CNV_{SS} is connected to V_{SS}, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $\overline{RESET_{OUT}}$ output pin

- **Single-Chip Mode**
  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS}.
- **Memory Expansion Mode**
  Select this mode by setting the processor mode bits to "01" in software with CNV_{SS} connected to V_{SS}. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.
- **Microprocessor Mode**
  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC}, or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS}. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.

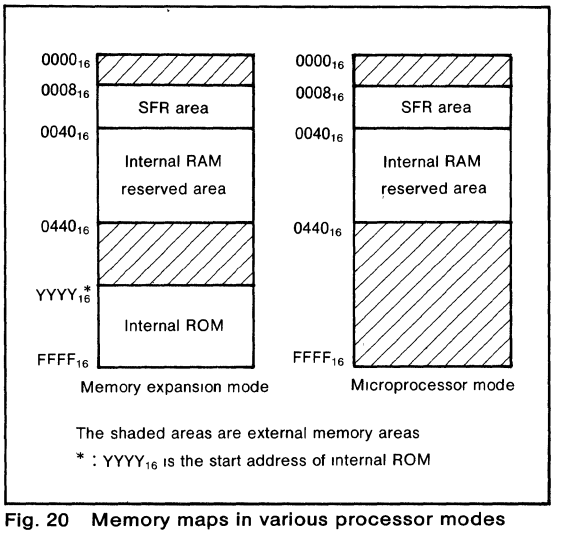


Fig. 20 Memory maps in various processor modes

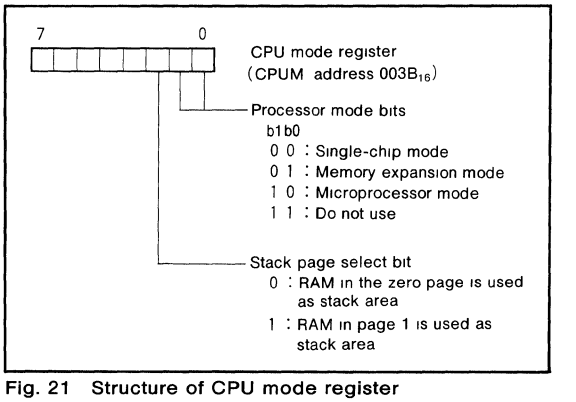
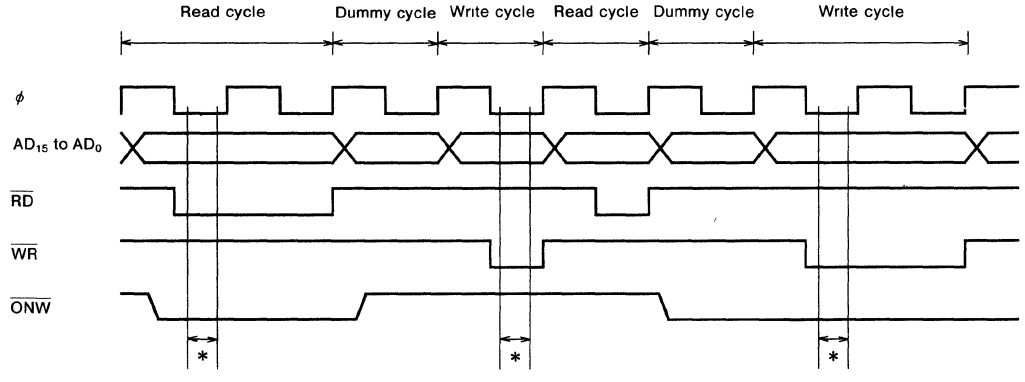


Fig. 21 Structure of CPU mode register

Bus Control with Memory Expansion

Microcomputers of the M3800x group have a built-in $\overline{ONW}$ function to facilitate access to extra memory and I/O functions in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the $\overline{ONW}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{RD}$ or $\overline{WR}$ signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to $FFFF_{16}$, and only read and write cycles are extended.



* : Period during which $\overline{ONW}$ input signal is received
During this period, the $\overline{ONW}$ signal must be fixed at either "H" or "L" At all other times, the input level of the $\overline{ONW}$ signal has no affect on operations
The bus cycles is not extended for an address in the area 0008_{16} to $043F_{16}$, regardless of whether the $\overline{ONW}$ signal is received

Fig. 22 $\overline{ONW}$ function timing

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset

In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the T_XD pin after transmission is completed.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency.

When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
64P4B, 64S1B	PCA4738S-64
64P6N	PCA4738F-64
64D0	PCA4738L-64

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 23 is recommended to verify programming.

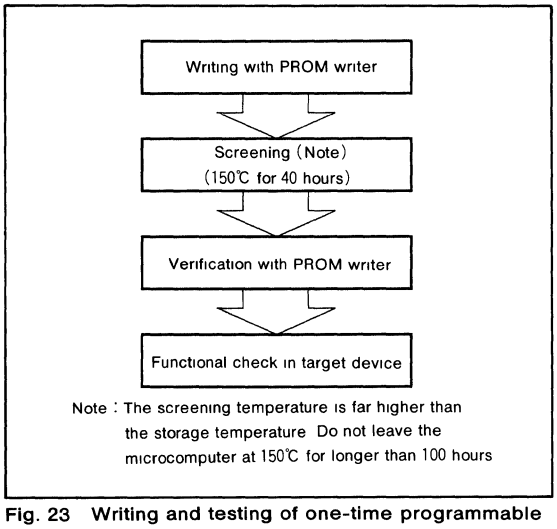


Fig. 23 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured with reference to the V_{SS} pin, output transistors isolated	−0.3 to 7.0	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$, X_{OUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25°C	1000 (Note)	mW
T_{opr}	Operating temperature		−20 to 85	°C
Tstg	Storage temperature		−40 to 125	°C

Note : 300mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 3.0 to 5.5V, T_a = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage (f (X_{IN}) ≦ 2MHz)	3.0	5.0	5.5	V
	Supply voltage (f (X_{IN}) > 2MHz)	4.0	5.0	5.5	
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS}	0		0.2V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$ (Note 1)			−80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 1)			−80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$ (Note 1)			−40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 1)			−40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 1)			40	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 2)			−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 3)			−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC}=4.0~5.5V)			8	MHz
	Internal clock oscillation frequency (V_{CC}=3.0~5.5V)			2	

Note 1 The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms The total peak current is the peak value of all the currents

2 The peak output current is the peak current flowing in each port

3 The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100ms

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$ (Note)	I_{OH}=−10mA, V_{CC}=4.0~5.5V		V_{CC}−2.0			V
		I_{OH}=−10mA, V_{CC}=3.0~5.5V		V_{CC}−1.0			
V_{OL}	"L" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$	I_{OL}=10mA, V_{CC}=4.0~5.5V				2.0	V
		I_{OL}=1.0mA, V_{CC}=3.0~5.5V				1.0	
V_{T+}−V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0−INT_5				0.4		V
V_{T+}−V_{T-}	Hysteresis R_XD, S_{CLK}				0.5		V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$				0.5		V
I_{IH}	"H" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$	V_I=V_{CC}				5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{CC}				5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}			4		μA
I_{IL}	"L" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_7$, $P6_0$−$P6_7$, $P7_0$, $P7_1$, $\overline{RESET}$, CNV_{SS}	V_I=V_{SS}				−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}			−4		μA
V_{RAM}	RAM hold voltage	With clock stopped		2.0		5.5	V
I_{CC}	Supply current	f(X_{IN})=8MHz, V_{CC}=5V			6.4	13	mA
		f(X_{IN})=5MHz, V_{CC}=5V			4	8	
		f(X_{IN})=2MHz, V_{CC}=3V			0.8	2.0	
		When WIT instruction is executed with f(X_{IN})=8MHz, V_{CC}=5V			1.5		
		When WIT instruction is executed with f(X_{IN})=5MHz, V_{CC}=5V			1		
		When WIT instruction is executed with f(X_{IN})=2MHz, V_{CC}=3V			0.2		
		When STP instruction is executed with clock stopped, output transistors isolated	T_a=25℃		0.1	1	μA
			T_a=85℃			10	

Note : $P4_5$ is measured when the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"

TIMING REQUIREMENTS 1 (V_{CC} =4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	125			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	50			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	80			ns
$t_{WH(INT)}$	INT_0 to INT_5 input "H" pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	80			ns
$t_{WL(INT)}$	INT_0 to INT_5 input "L" pulse width	80			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "0"

TIMING REQUIREMENTS 2 (V_{CC} =3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	500			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	200			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	200			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	230			ns
$t_{WH(INT)}$	INT_0 to INT_5 input "H" pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	230			ns
$t_{WL(INT)}$	INT_0 to INT_5 input "L" pulse width	230			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	950			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	950			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	200			ns

Note : When $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "0"

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			140	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rise time			30	ns
$t_{f(S_{CLK})}$	Serial I/O clock output fall time			30	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		10	30	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded

SWITCHING CHARACTERISTICS 2 (V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			350	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rise time			50	ns
$t_{f(S_{CLK})}$	Serial I/O clock output fall time			50	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		20	50	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded

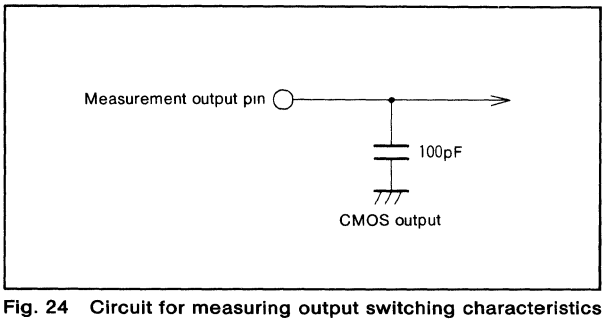


Fig. 24 Circuit for measuring output switching characteristics (1)

TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su(\overline{ONW}-\phi)}$	$\overline{ONW}$ input set up time	−20			ns
$t_{h(\phi-\overline{ONW})}$	$\overline{ONW}$ input hold time	−20			ns
$t_{su(DB-\phi)}$	Data bus set up time	60			ns
$t_{h(\phi-DB)}$	Data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{C(\phi)}$	ϕ clock cycle time		$2\times t_{C(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock "H" pulse width	$t_{C(X_{IN})}-10$			ns
$t_{WL(\phi)}$	ϕ clock "L" pulse width	$t_{C(X_{IN})}-10$			ns
$t_{d(\phi-AH)}$	AD_{15} to AD_8 delay time		20	40	ns
$t_{v(\phi-AH)}$	AD_{15} to AD_8 valid time	6	10		ns
$t_{d(\phi-AL)}$	AD_7 to AD_0 delay time		25	45	ns
$t_{v(\phi-AL)}$	AD_7 to AD_0 valid time	6	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time		20		ns
$t_{v(\phi-SYNC)}$	SYNC valid time		10		ns
$t_{d(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ delay time		10	20	ns
$t_{v(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ valid time	3	5	10	ns
$t_{d(\phi-DB)}$	Data bus delay time		20	70	ns
$t_{v(\phi-DB)}$	Data bus valid time	15			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output delay time (Note)			200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET_{OUT}}$ output valid time (Note)	0		200	ns

Note : The $\overline{RESET_{OUT}}$ output goes "H" in sync with the rise of the ϕ clock that is anywhere between about 1 cycle and 19 cycles after the RESET input goes "H"

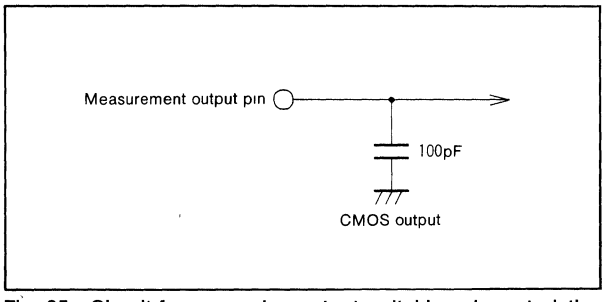
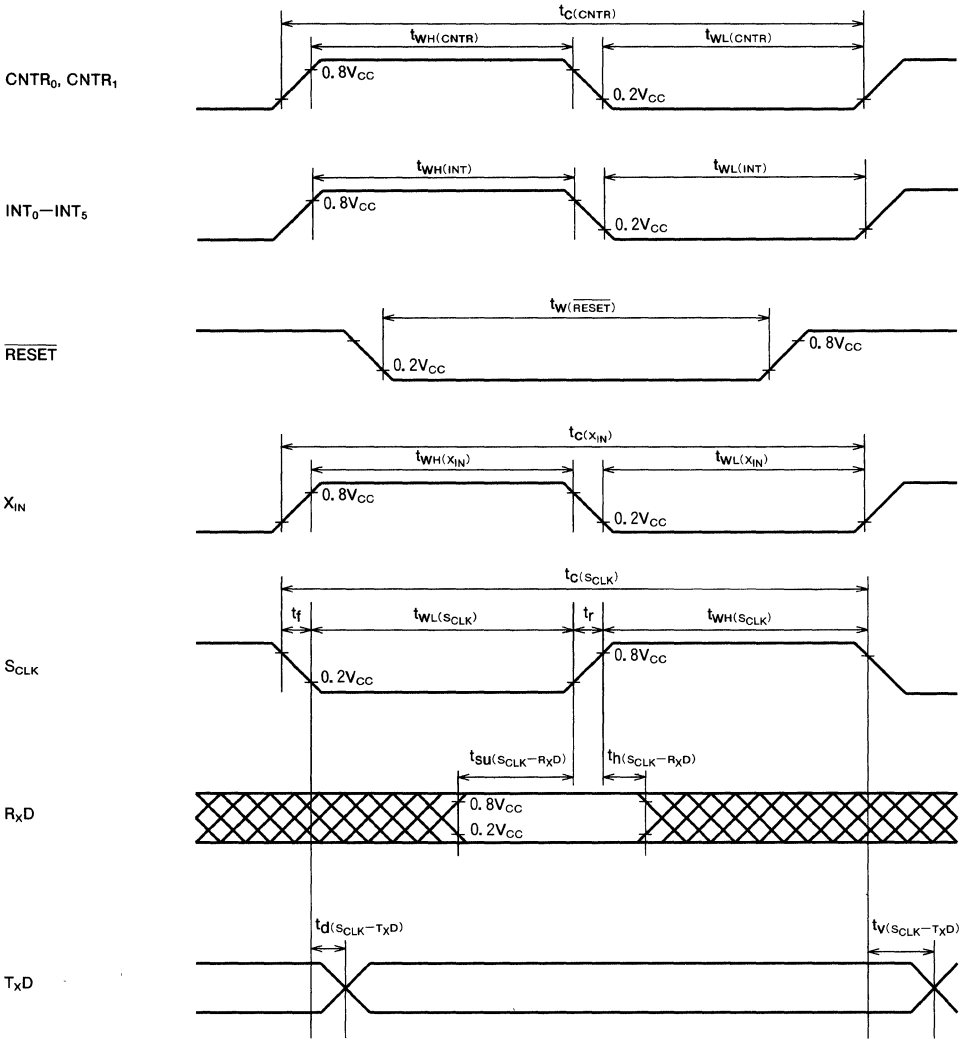


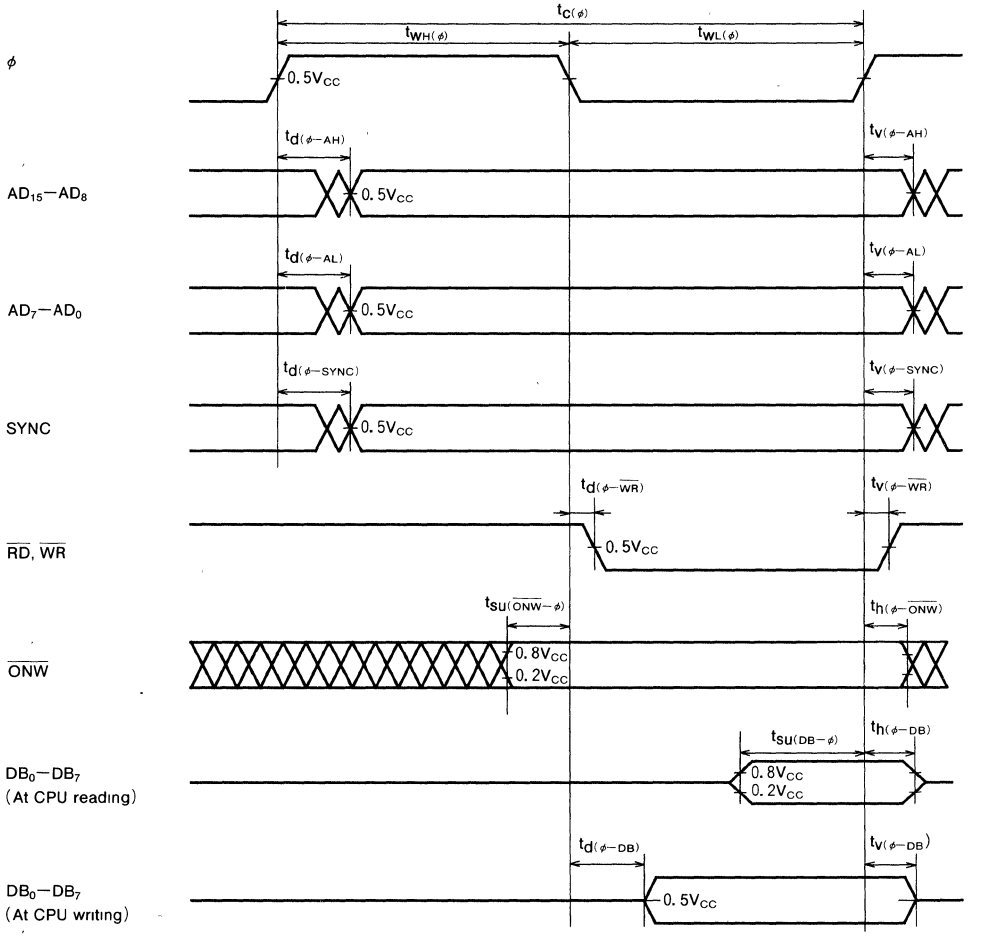
Fig. 25 Circuit for measuring output switching characteristics (2)

TIMING DIAGRAM

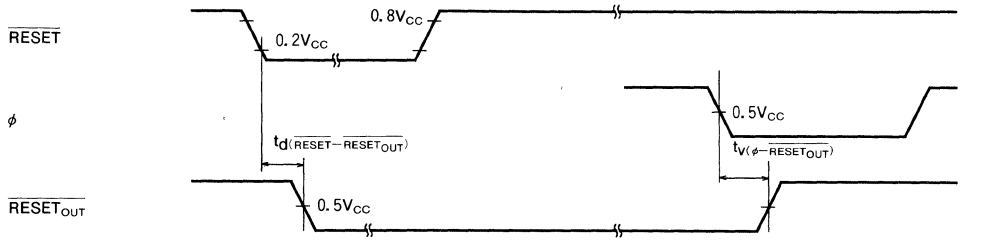
(1) Timing diagram



(2) Timing diagram in memory expansion mode and microprocessor mode



(3) Timing diagram in microprocessor mode



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