MITSUBISHI MICROCOMPUTERS

M37451E4-XXXSP/FP/GP,M37451E4SS/FS
M37451E8-XXXSP/FP/GP,M37451E8SS/FS
M37451EC-XXXSP/FP/GP,M37451ECSS/FS

PROM Version of M37451 Group

DESCRIPTION

The M37451E4-XXXSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm-pitch or 0.65mm-pitch 80-pin plastic molded QFP.

The features of this chip are similar to those of the M37451M4-XXXSP/FP/GP except that this chip has a 8192 bytes PROM built in.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices. The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences among M37451E4-XXXSP/FP/GP, M37451 E8-XXXSP/FP/GP and M37451EC-XXXSP/FP/GP are as shown below. The M37451E4SS/FS, M37451E8SS/FS and M37451ECSS/FS are the window type. The descriptions that follow describe the M37451E4-XXXSP/FP/GP unless otherwise noted.

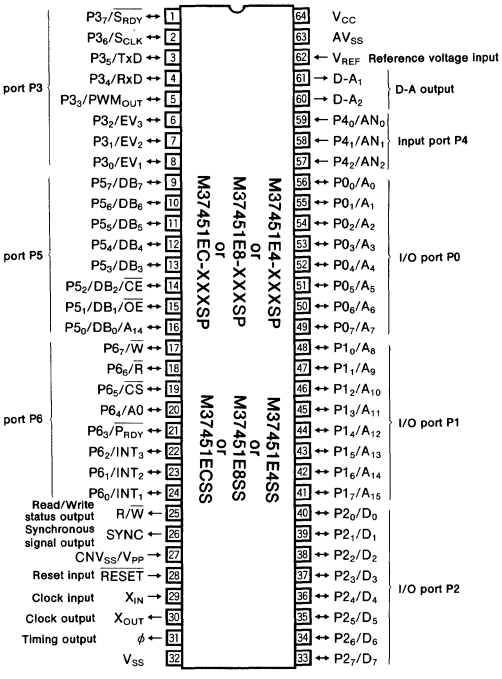
Type name	ROM size	RAM size	Built-in PROM
M37451E4SS/FS	8192 bytes	256 bytes	EPROM (Window type)
M37451E4-XXXSP/FP/GP			One-time programmable
M37451E8SS/FS	16384 bytes	384 bytes	EPROM (Window type)
M37451E8-XXXSP/FP/GP			One-time programmable
M37451ECSS/FS	24576 bytes	512 bytes	EPROM (Window type)
M37451EC-XXXSP/FP/GP			One-time programmable

The number of analog input pins for the 80-pin model (FP, GP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5MHz frequency) 0.64μs
- Single power supply ..... 5V$\pm$10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) 40mW
- Subroutine nesting ..... 96 levels max.(M37451E4)
  96 levels max.(M37451E8)
  128 levels max.(M37451EC)
- Interrupt ..... 15 events

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

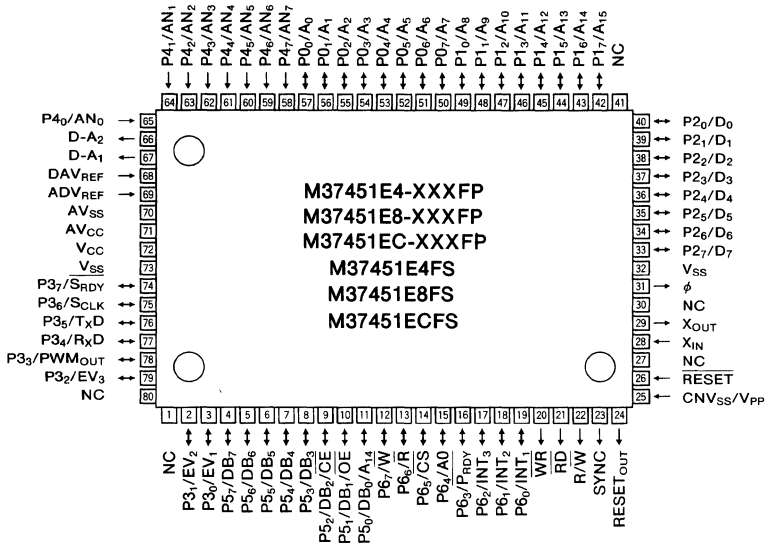
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFP, QFN)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8 bit or 16 bit is software selectable) ... 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input port (Port P4) ..... 3(DIP), 8(QFP, QFN)
- Output ports (Ports D-A_1, D-A_2) 2
- PROM (equivalent to the M5L27256)
  Program voltage 12.5V

APPLICATION

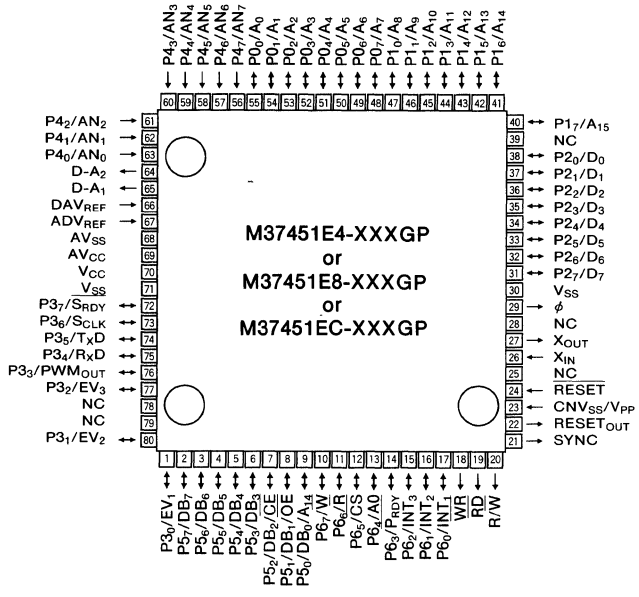
Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

MITSUBISHI ELECTRIC

PIN CONFIGURATION (TOP VIEW)



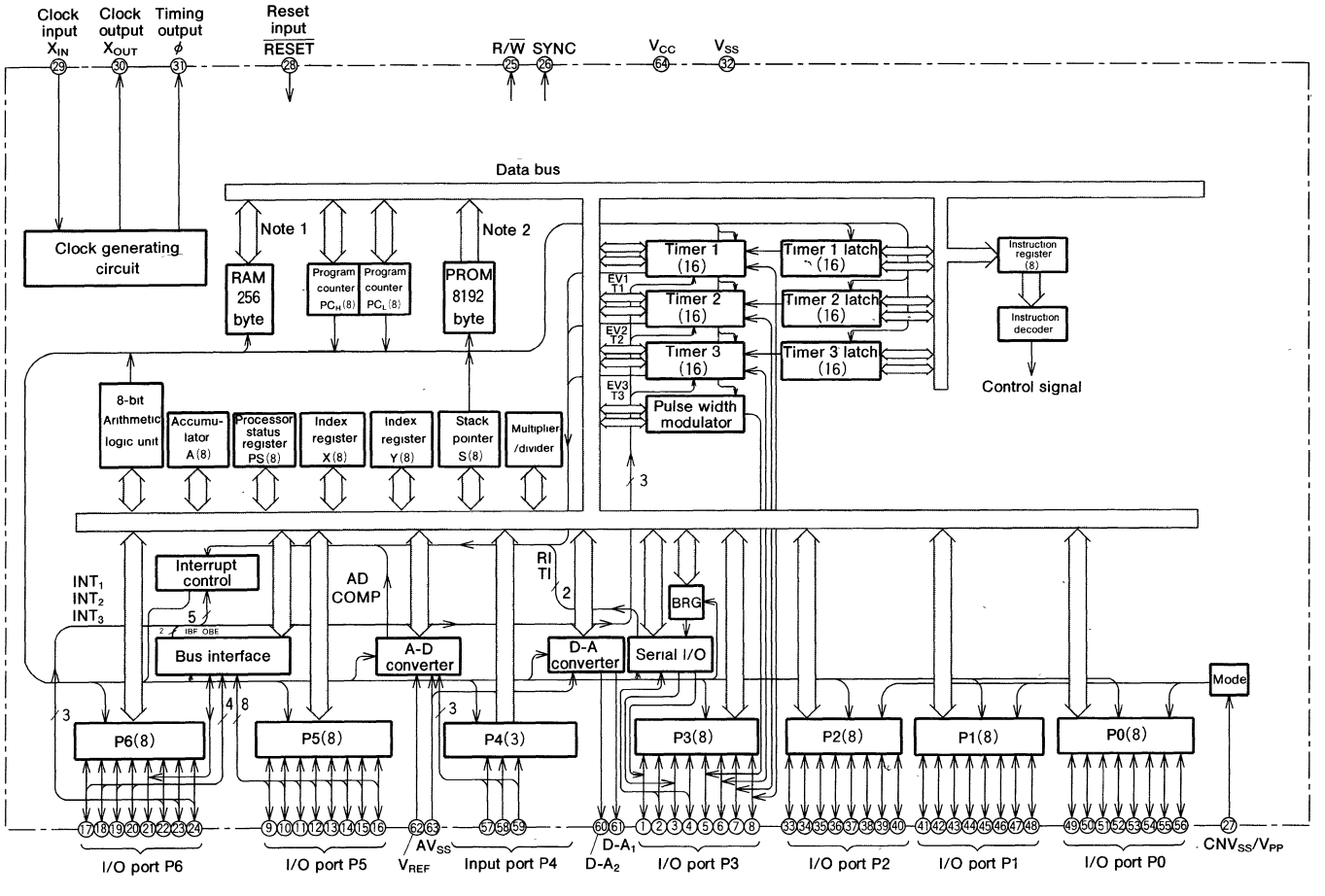
Outline 80P6N (OTP)
80D0 (Window)



Outline 80P6S

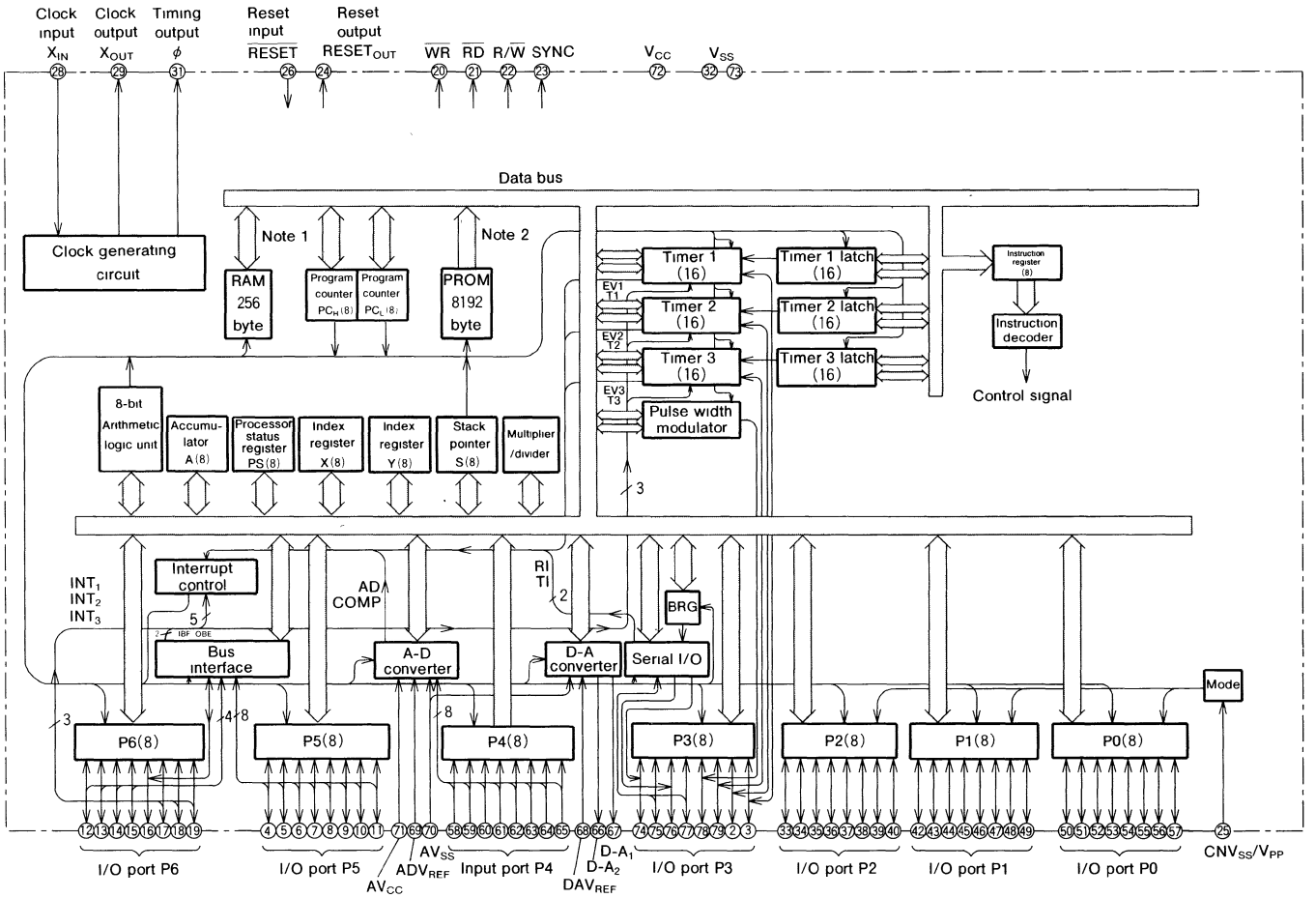
NC : No connection

M37451E4-XXXSP/M37451E4SS BLOCK DIAGRAM



Note 1 : 384 bytes for M37451E8-XXXSP/M37451E8SS and 512 bytes for M37451EC-XXXSP/M37451ECSS.
2 : 16384 bytes for M37451E8-XXXSP/M37451E8SS and 24576 bytes for M37451EC-XXXSP/M37451ECSS

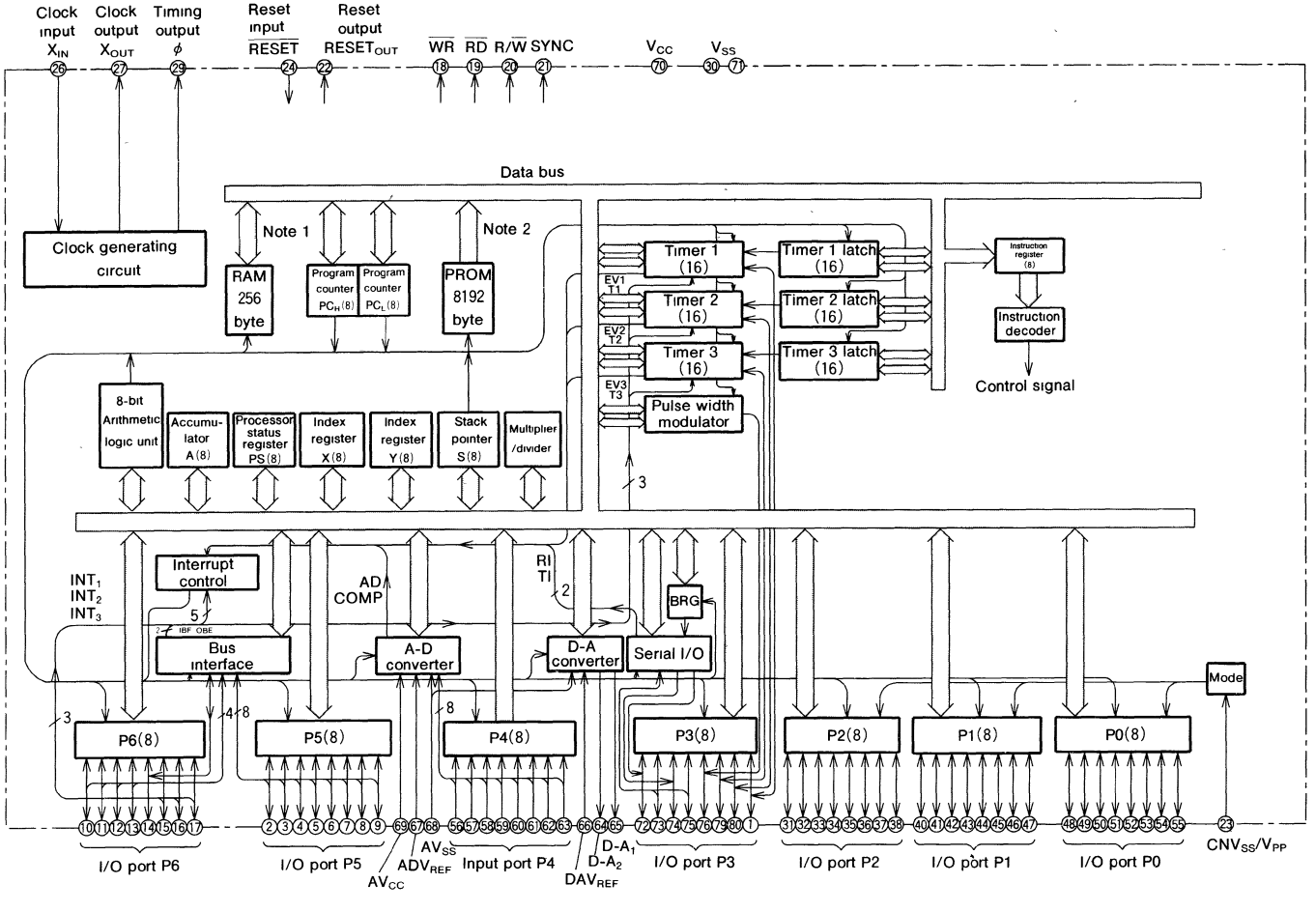
M37451E4-XXXFP/M37451E4FS BLOCK DIAGRAM



Note 1 : 384 bytes for M37451E8-XXXFP/M37451E8FS and 512 bytes for M37451EC-XXXFP/M37451ECFS
2 : 16384 bytes for M37451E8-XXXFP/M37451E8FS and 24576 bytes for M37451EC-XXXFP/M37451ECFS

MITSUBISHI ELECTRIC

M37451E4-XXXGP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451E8-XXXGP and 512 bytes for M37451EC-XXXGP
2 : 16384 bytes for M37451E8-XXXGP and 24576 bytes for M37451EC-XXXGP.

MITSUBISHI ELECTRIC

M37451E4-XXXSP/FP/GP,M37451E4SS/FS
M37451E8-XXXSP/FP/GP,M37451E8SS/FS
M37451EC-XXXSP/FP/GP,M37451ECSS/FS

PROM Version of M37451 Group

FUNCTIONS OF M37451E4-XXXSP/FP/GP, M37451E8-XXXSP/FP/GP, M37451EC-XXXSP/FP/GP, M37451E4SS/FS, M37451E8SS/FS, M37451ECSS/FS

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.64μs (minimum instructions, at 12.5MHz frequency)
Clock frequency			12.5MHz (max.)
Memory size	M37451E4-XXXSP/FP/GP	PROM	8192 bytes
	M37451E4SS/FS	RAM	256 bytes
	M37451E8-XXXSP/FP/GP	PROM	16384 bytes
	M37451E8SS/FS	RAM	384 bytes
	M37451EC-XXXSP/FP/GP	PROM	24576 bytes
	M37451ECSS/FS	RAM	512 bytes
Input/Output port	P0 to P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels max. (M37451E4, M37451E8) 128-levels max. (M37451EC)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW (at 12.5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible (64K bytes max.)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37451E4-XXXSP		64-pin shrink plastic molded DIP
	M37451E8-XXXSP		
	M37451EC-XXXSP		
	M37451E4-XXXFP		80-pin plastic molded QFP (0.8mm-pitch)
	M37451E8-XXXFP		
	M37451EC-XXXFP		
	M37451E4-XXXGP		80-pin plastic molded QFP (0.65mm-pitch)
	M37451E8-XXXGP		
	M37451EC-XXXGP		
	M37451E4SS		64-pin shrink ceramic DIP
	M37451E8SS		
	M37451ECSS		
	M37451E4FS		80-pin ceramic QFN (LCC)
	M37451E8FS		
	M37451ECFS		

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}	Input	Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$—$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$—$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$—$P4_2$ ($P4_0$—$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$—$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$—$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$—$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$—$P6_2$ may be programmed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only. Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components. This pin is for 80-pin model only

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
R/$\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$—$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$—$P1_7$	I/O port P1	Input	$P1_0$—$P1_5$ work as the higher 6-bit address input $P1_6$ and $P1_7$ connect to V_{CC}
$P2_0$—$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus
$P3_0$—$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$—$P4_7$ ($P4_0$—$P4_2$)	Input port P4	Input	Connect to V_{SS} The 64-pin model has only three pins $P4_0$—$P4_2$
$P5_0$—$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as A_{14}, $\overline{OE}$, and $\overline{CE}$ inputs respectively Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$—$P5_7$ to V_{SS}
$P6_0$—$P6_7$	I/O port P6	Input	Connect to V_{SS}
D-A_1, D-A_2	D-A output	Output	Kept to open
V_{REF}	Reference voltage input	Input	Connect to V_{SS}. This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS} This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS} This pin is for 80-pin model only
AV_{SS}	Analog power	Input	Connect to V_{SS}
AV_{CC}	Analog power	Input	Connect to V_{CC} or V_{SS} This pin is for 80-pin model only
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only

EPROM MODE

The M37451E4-XXXSP/FP/GP, M37451E4SS/FS features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, 2 and 3 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, $P1_0$—$P1_5$, P2, $P5_0$—$P5_2$ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37451E4-XXXSP/FP/GP, M37451E4SS/FS	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$—$P1_5$, $P5_0$	A_0—A_{14}
Data I/O	Port P2	D_0—D_7
$\overline{CE}$	$P5_2/DB_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/DB_1/\overline{OE}$	$\overline{OE}$

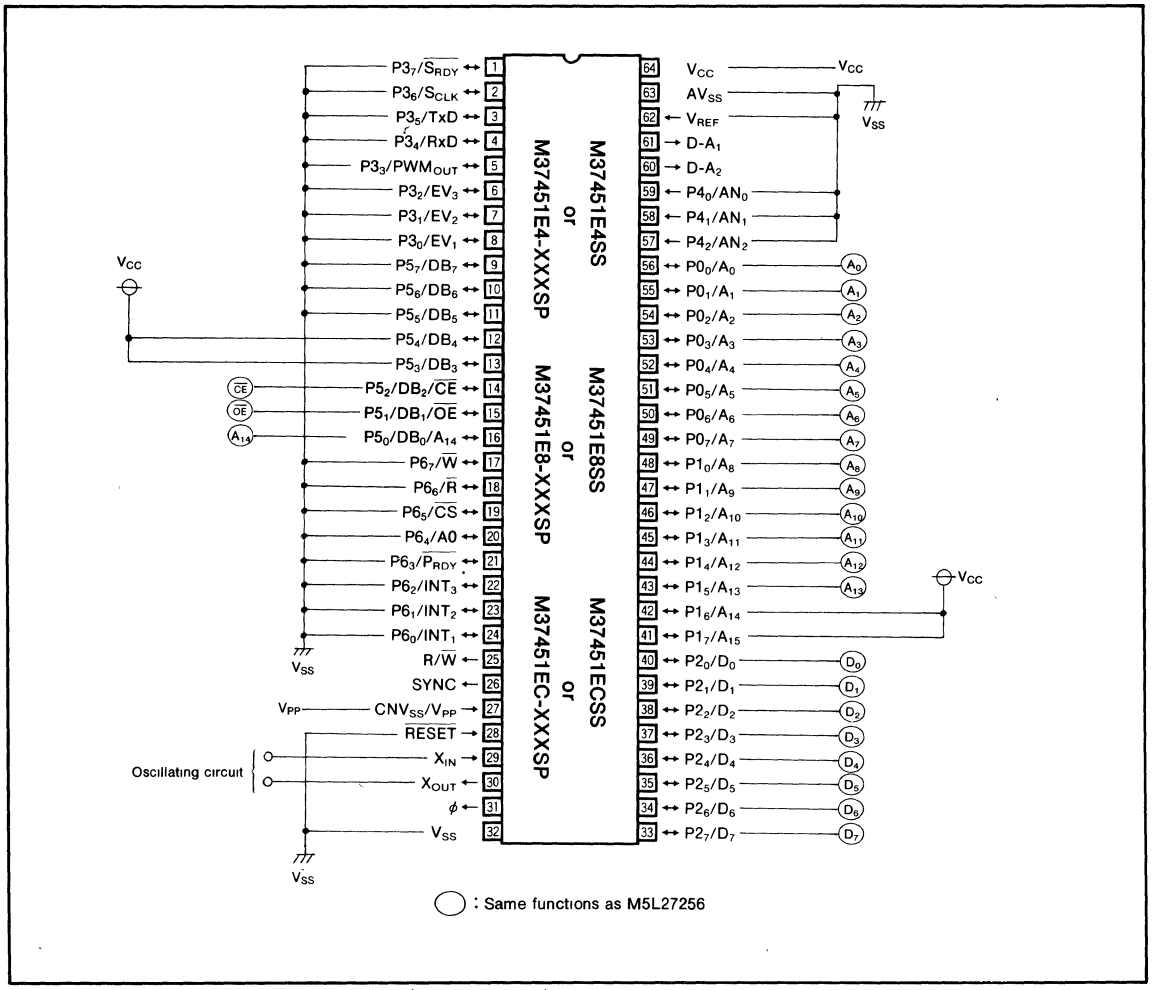


Fig. 1 Pin connection in EPROM mode (64-pin model)

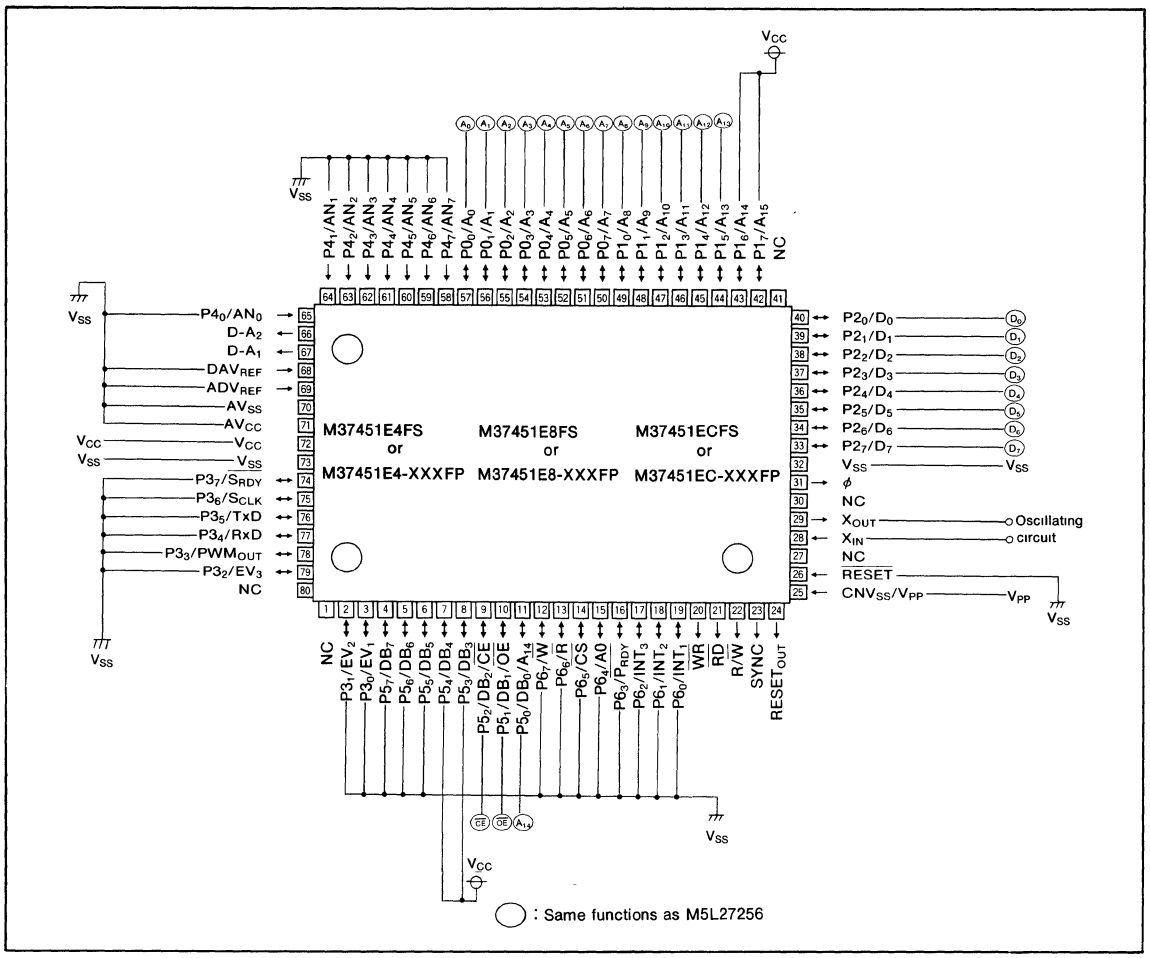


Fig. 2 Pin connection in EPROM mode (0.8mm pitch 80-pin model)

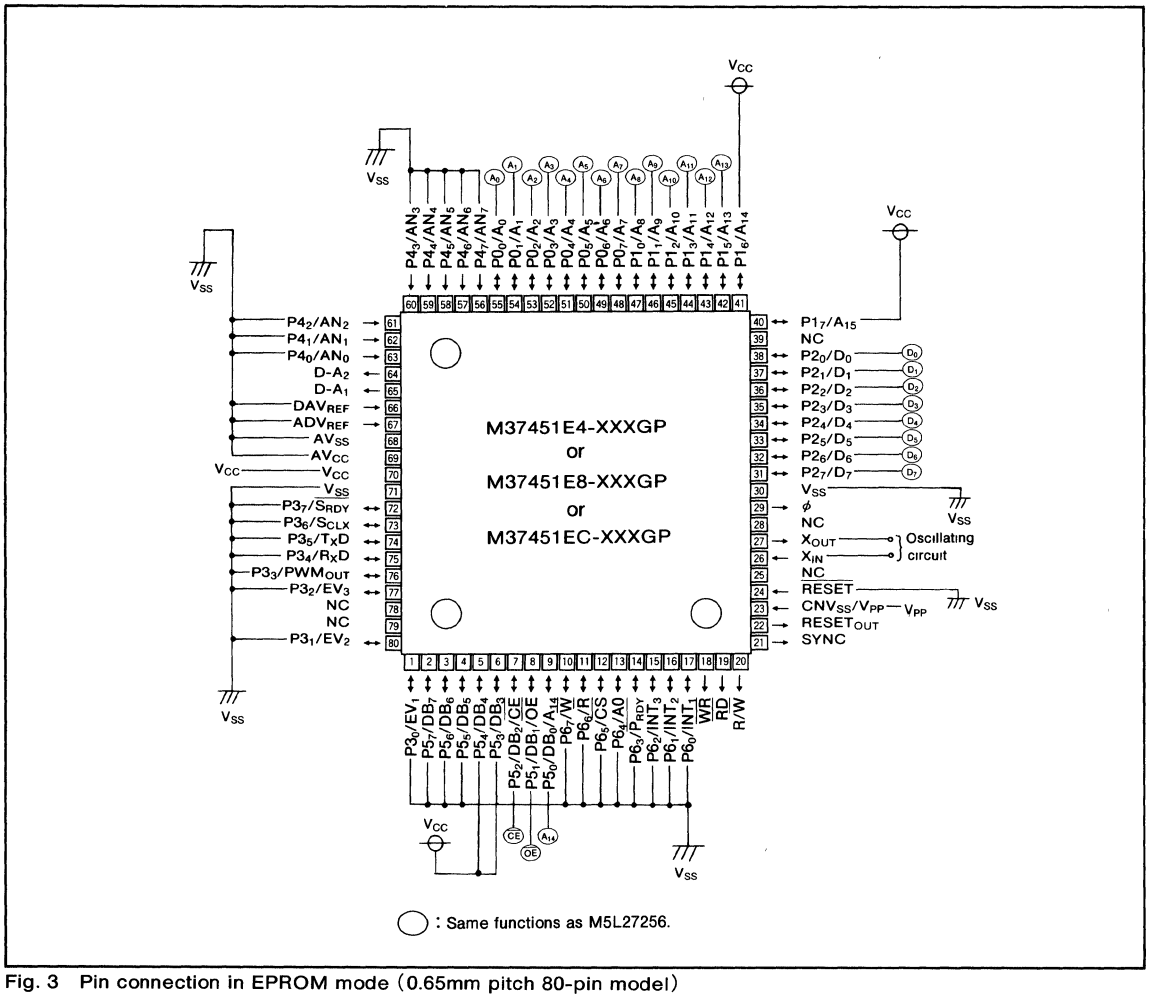


Fig. 3 Pin connection in EPROM mode (0.65mm pitch 80-pin model)

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and supply 0V to the $\overline{RESET}$ pin, 5V to the V_{CC} pin and the CNV_{SS} (V_{PP}) pin. Input the address of the data (A_0—A_{14}) to be read and the data will be output to the I/O pins D_0—D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to an "H" level, and supply 0V to the $\overline{RESET}$ pin, 6V to the V_{CC} pin and 12.5V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0—A_{14}, and the data to be written is input to pins D_0—D_7. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Erasing

Data can only erased on the M37451E4SS/FS, M37451E8SS/FS and M37451ECSS/FS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W·s/cm^2.

NOTES ON HANDLING

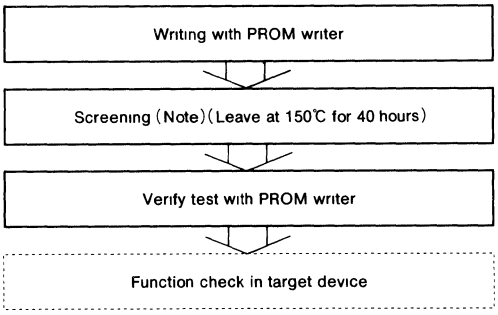
(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.

(5) In EPROM mode, address A_{15} is set to "H" automatically.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	5V	5V	Output
Programming	V_{IL}	V_{IH}	12.5V	6V	Input
Programming verify	V_{IH}	V_{IL}	12.5V	6V	Output
Program disable	V_{IH}	V_{IH}	12.5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
2 : An X indicates either V_{IL} or V_{IH}