M37450E4TXXXSP/J

PROM VERSION of M37450M4TXXXSP/J

DESCRIPITION

The M37450E4TXXXSP/J is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or 84-pin plastic molded QFJ (PLCC). The features of this chip are similar to those of the M37450M4-XXXSP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It also has a unique feature that enables it to be used as a slave microcomputer.

The difference between the M37450E4TXXXSP and the M37450E4TXXXJ is the package outline.

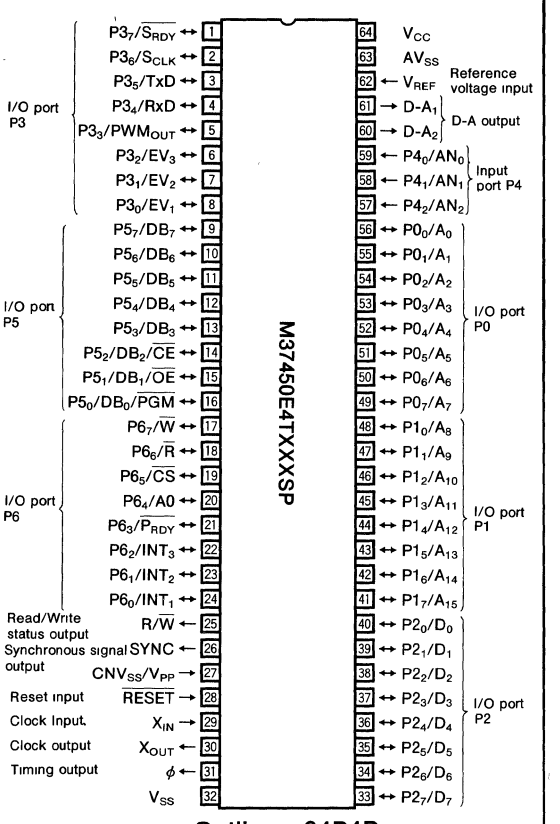
FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size PROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  (minimum instructions at 10 MHz frequency) 0.8μs
- Single power supply ..... 5V$\pm$5%
- Power dissipation normal operation mode
  (at 10 MHz frequency) 30mW
- Subroutine nesting ..... 96 levels max.
- Interrupt ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFJ)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8-bit or 16-bit) 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input port (Port P4) ..... 3 (DIP), 8 (QFJ)
- Output ports (Ports D-A_1, D-A_2) 2
- PROM (equivalent to the M5L2764)
  program voltage 21V

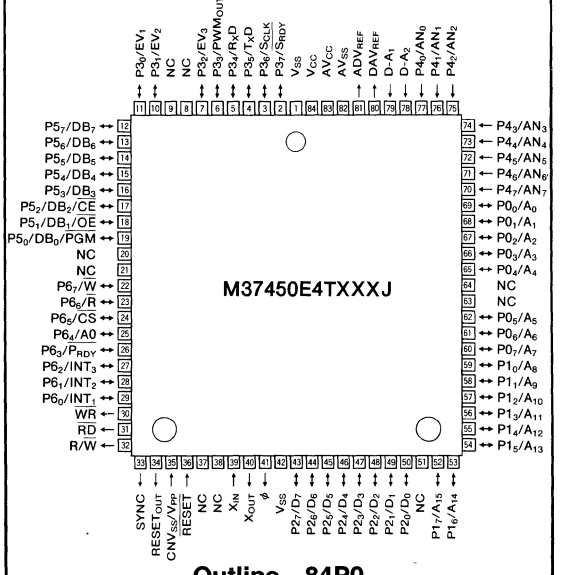
APPLICATION

Slave controller for PPCs, facsimiles, and page printers
HDD, optical disk, inverter, and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

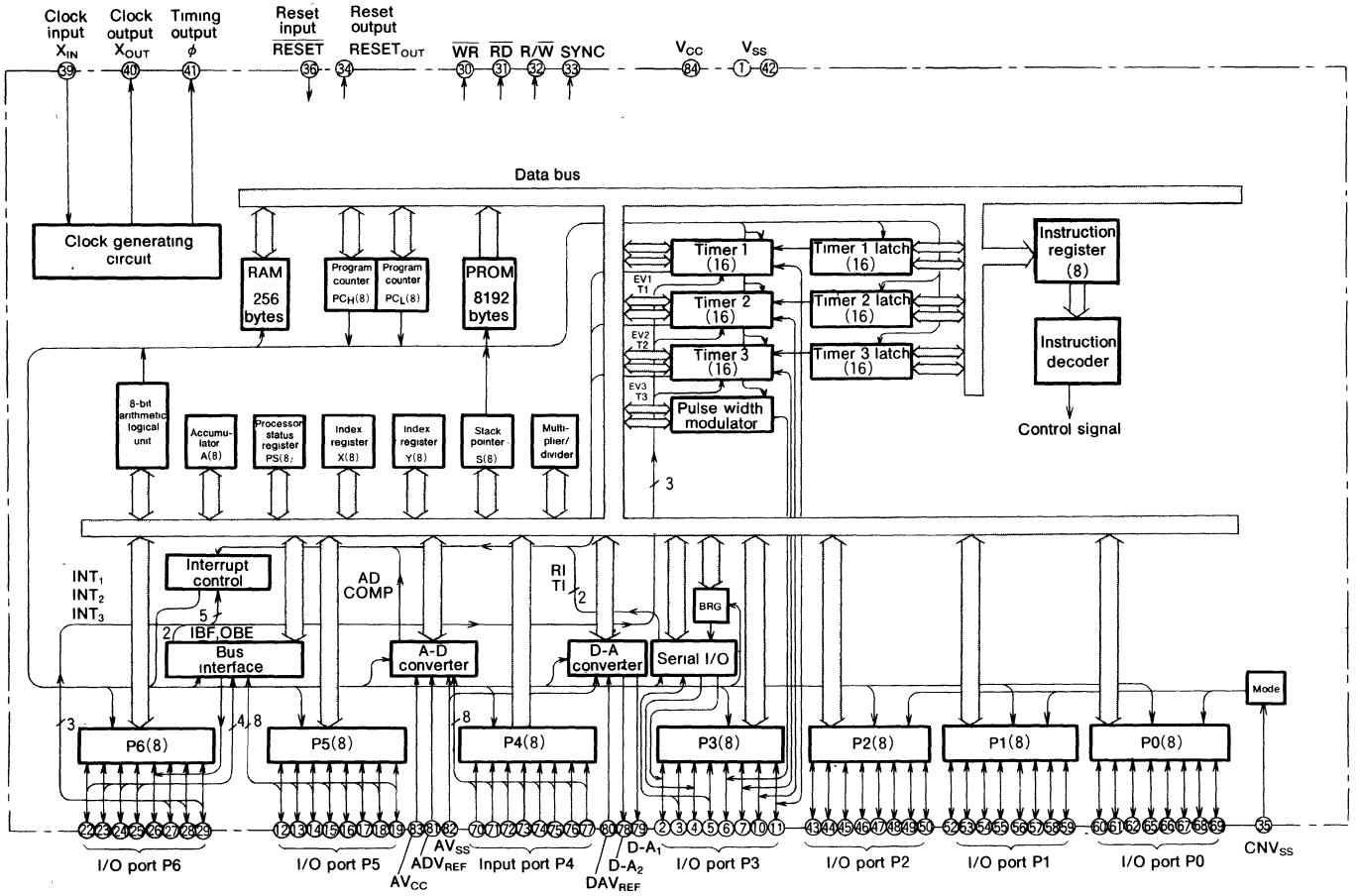


Outline 84P0

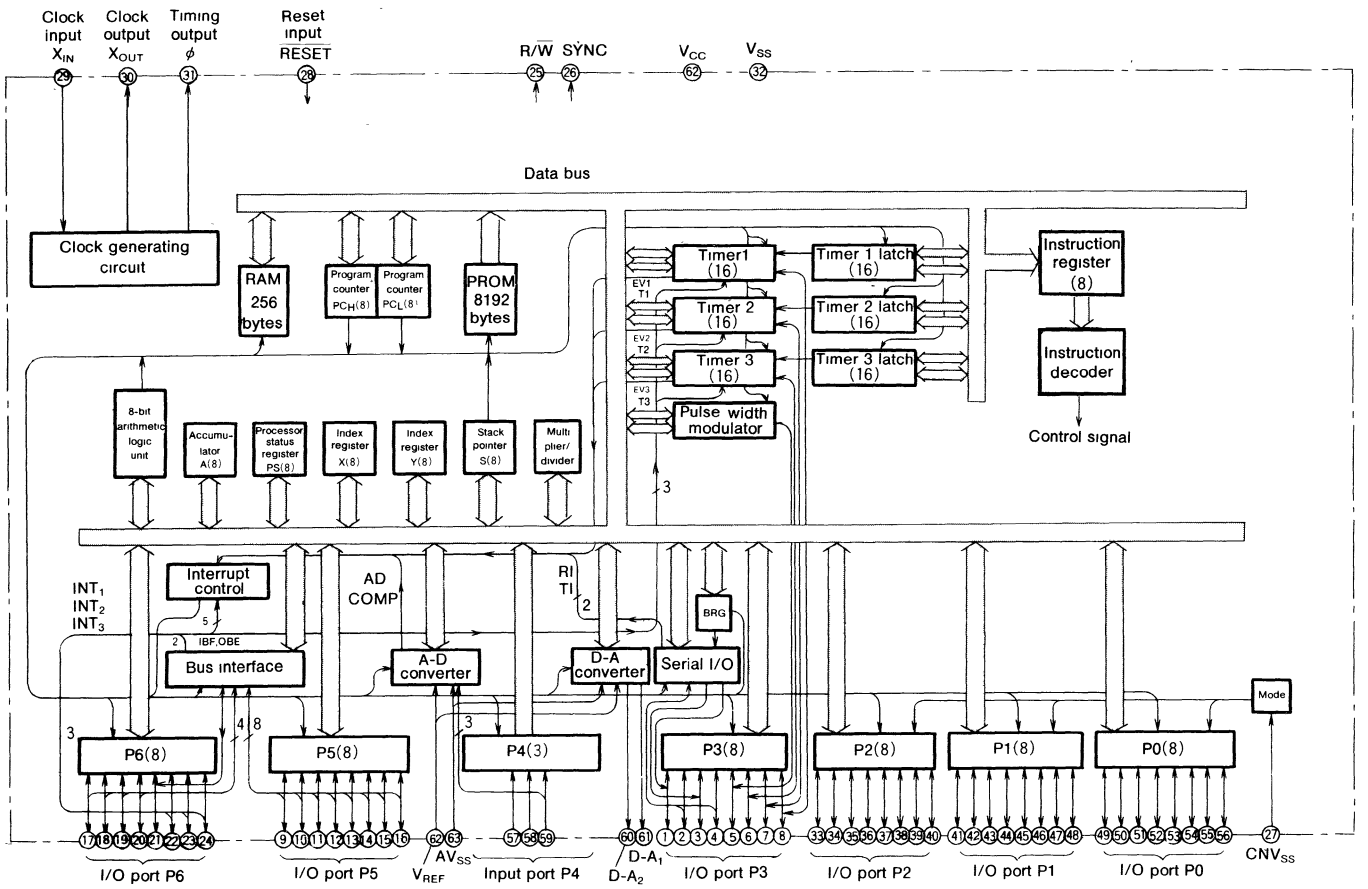
NC : No connection

MITSUBISHI ELECTRIC

M37450E4TXXXJ BLOCK DIAGRAM



M37450E4TXXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37450E4TXXXSP/J

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz (max.)
Memory size	PROM		8192 bytes
	RAM		256 bytes
Input/Output port	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 84-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 84-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels
Interrupt			6 external interrupts, 8 internal interrupts One software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−40 to 85℃
Device structure			CMOS silicon gate
Package	M37450E4TXXXSP		64-pin shrink plastic molded DIP
	M37450E4TXXXJ		84-pin plastic molded QFJ (PLCC)

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. Used as data bus except in single-chip mode.
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program.
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 84-pin model has eight pins. They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 84-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 84-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 84-pin model only. Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 84-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 84-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components. This pin is for 84-pin model only.

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
R/$\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$-$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$-$P1_7$	I/O port P1	Input	P1 works as the higher 8-bit address input.
$P2_0$-$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus
$P3_0$-$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Connect to V_{SS} (The 80-pin model has eight pins $P4_0$ to $P4_7$).
$P5_0$-$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as $\overline{PGM}$, $\overline{OE}$, and $\overline{CE}$ inputs respectively Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$ to $P5_7$ to V_{SS}
$P6_0$-$P6_7$	I/O port P6	Input	Connect to V_{SS}.
D-A_1, D-A_2	D-A output	Output	Kept to open
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS}
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS}.
AV_{SS}	Analog power	Input	Connect to V_{SS}
AV_{CC}	Analog power	Input	Connect to V_{SS}
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output)
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output).
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output)

EPROM MODE

The M37450E4TXXXSP/J features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P5_0$ to $P5_2$ and CNV_{SS} are used for the PROM (equivalent to the M5L2764). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37450E4TXXXSP/J	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$-$P1_4$	A_0-A_{12}
Data I/O	Port P2	D_0-D_7
$\overline{CE}$	$P5_2/DB_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/DB_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P5_0/DB_0/\overline{PGM}$	$\overline{PGM}$

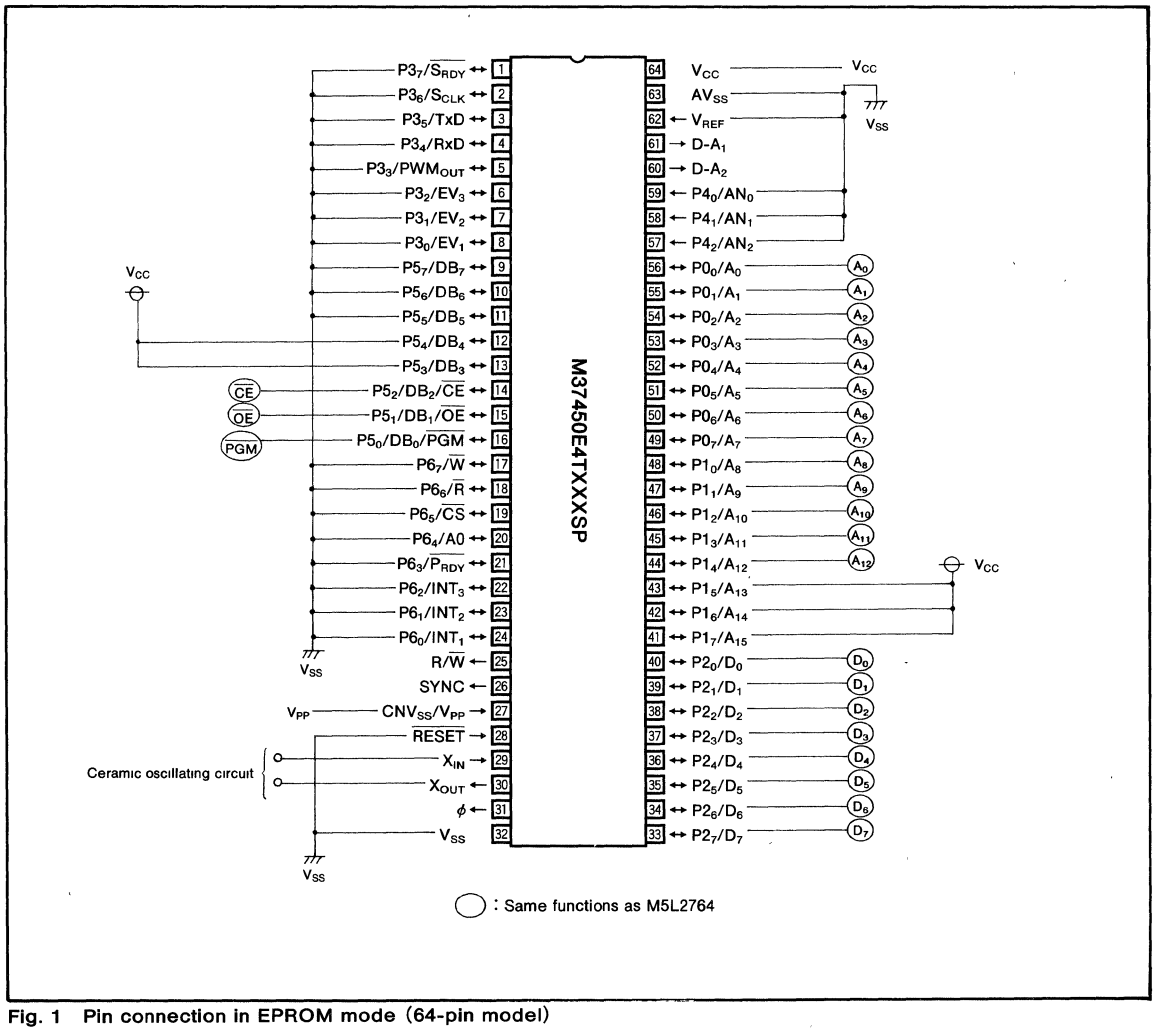


Fig. 1 Pin connection in EPROM mode (64-pin model)

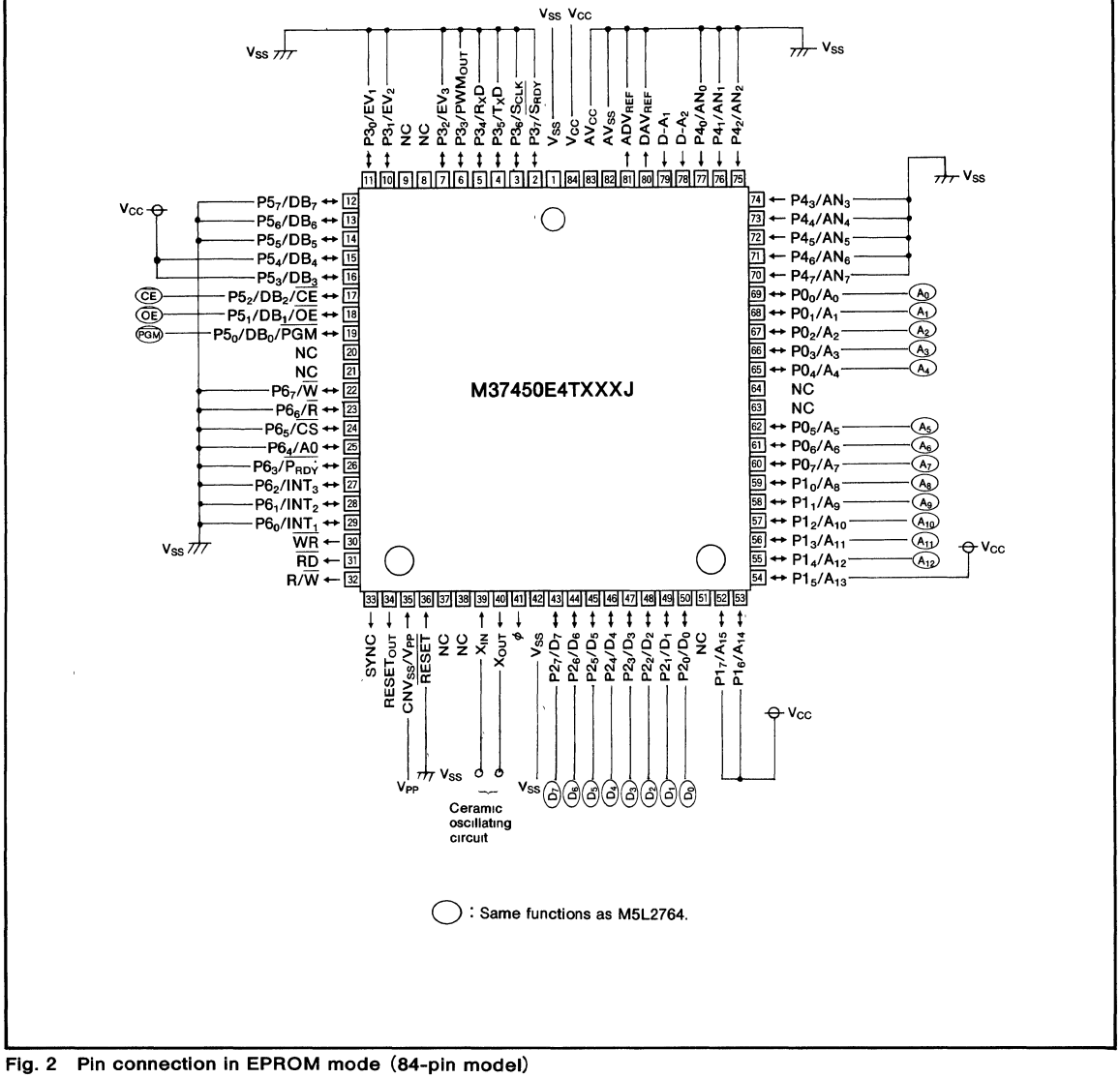


Fig. 2 Pin connection in EPROM mode (84-pin model)

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address (A_0 to A_{12}) to be read and the data will be output to the I/O pins D_0 to D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

The PROM is programmed at the factory already and do not use the writing mode.

NOTES ON HANDLING

(1) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH}\rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13(Note 1)	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−40 to 85	℃
Tstg	Storage temperature		−65 to 150	℃

Note 1 : In PROM programming mode, CNV_{SS} is 22.0V.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±5%, Ta=−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_xD($P3_4$) and S_{CLK}($P3_6$)
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms
3 : The total of "L" output current $I_{OL(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = −40 to 85℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
V_{T+}−V_{T-}	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
V_{T+}−V_{T-}	Hysterisis $\overline{RESET}$				0.7	V
V_{T+}−V_{T-}	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open. The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6)

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V±5%, V_{SS} = AV_{SS} = 0V, T_a = −40 to 85℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±5%		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = AV_{SS} = 0V, T_a = −40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 5	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig 5			150	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

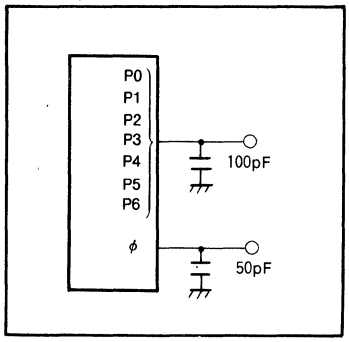


Fig. 3 Test circuit in single-chip mode

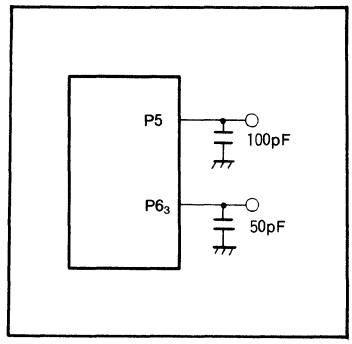


Fig. 4 Master CPU bus interface test circuit

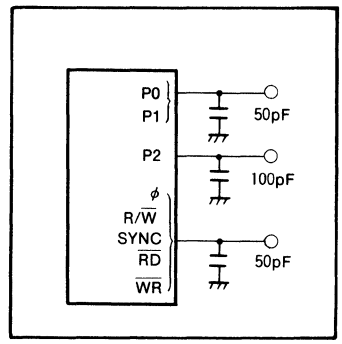


Fig. 5 Local bus test circuit

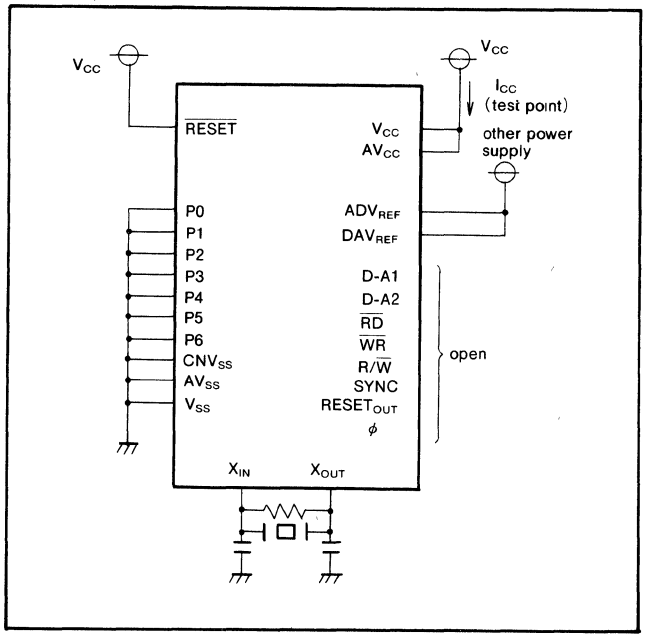


Fig. 6 I_{CC} (at STOP mode) test condition

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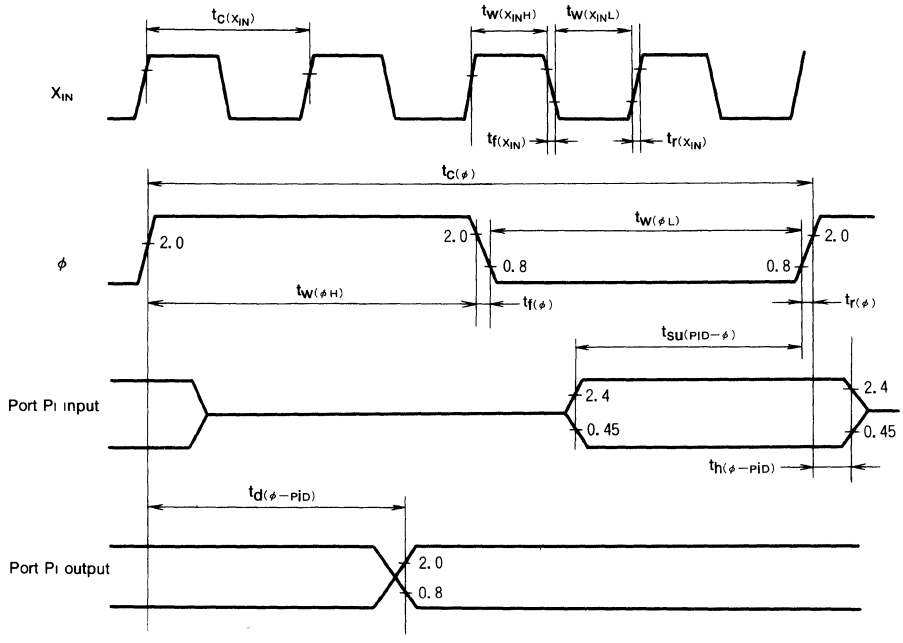
TIMING DIAGRAM

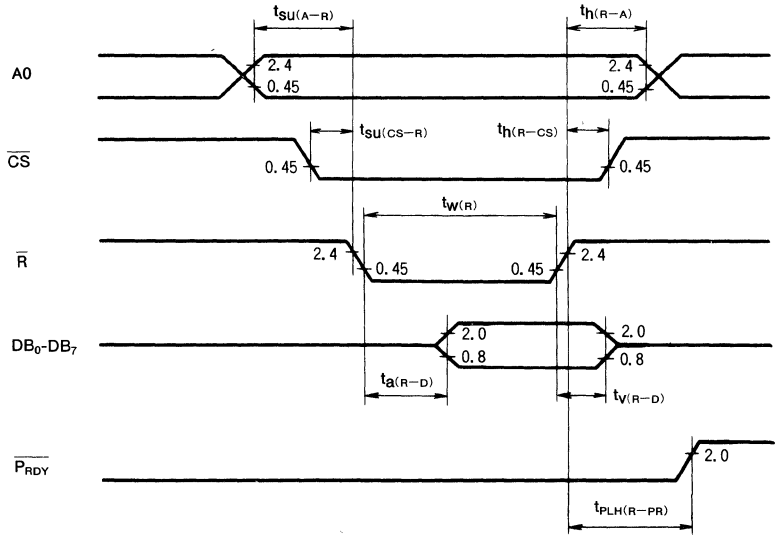
Port/single-chip mode timing diagram



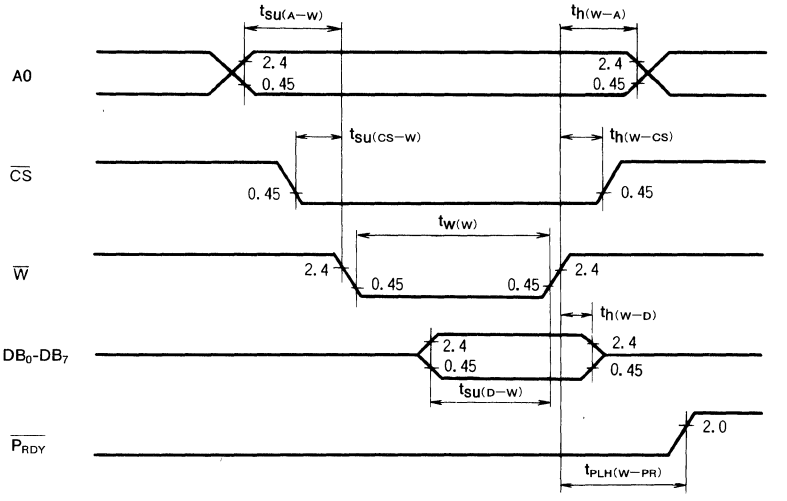
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

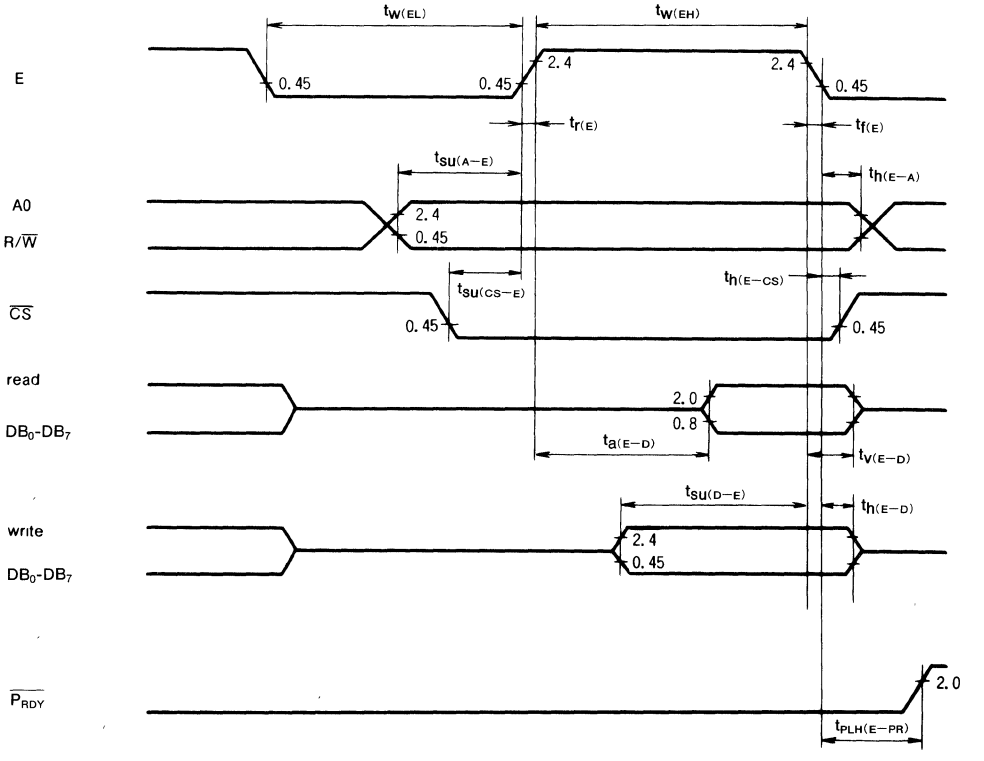
Read



Write



Master CPU interface/ R/W type timing diagram



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Local bus timing diagram