M37420E6-XXXSP
M37420E6SS

PROM VERSION of M37420M6-XXXSP

DESCRIPTION

The M37420E6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP. The features of this chip are similar to those of the M37420M6-XXXSP except that this chip has a 12288 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The M37420E6SS is the window type.

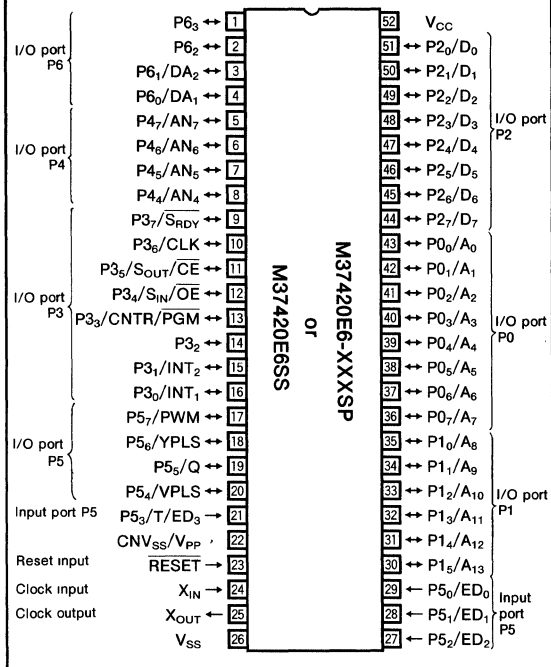
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 12288 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1μs (minimum instructions at 8MHz frequency)
- Single power supply ..... 5V$\pm$5%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4, P5, P6) 42
- Input port (Port P5) 4
- Serial I/O (8/16-bit) 1
- A-D converter (8-bit) 4
- D-A converter (8-bit) 2
- 14-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)
  program voltage 21V

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B (OTP)
52S1 (Window)

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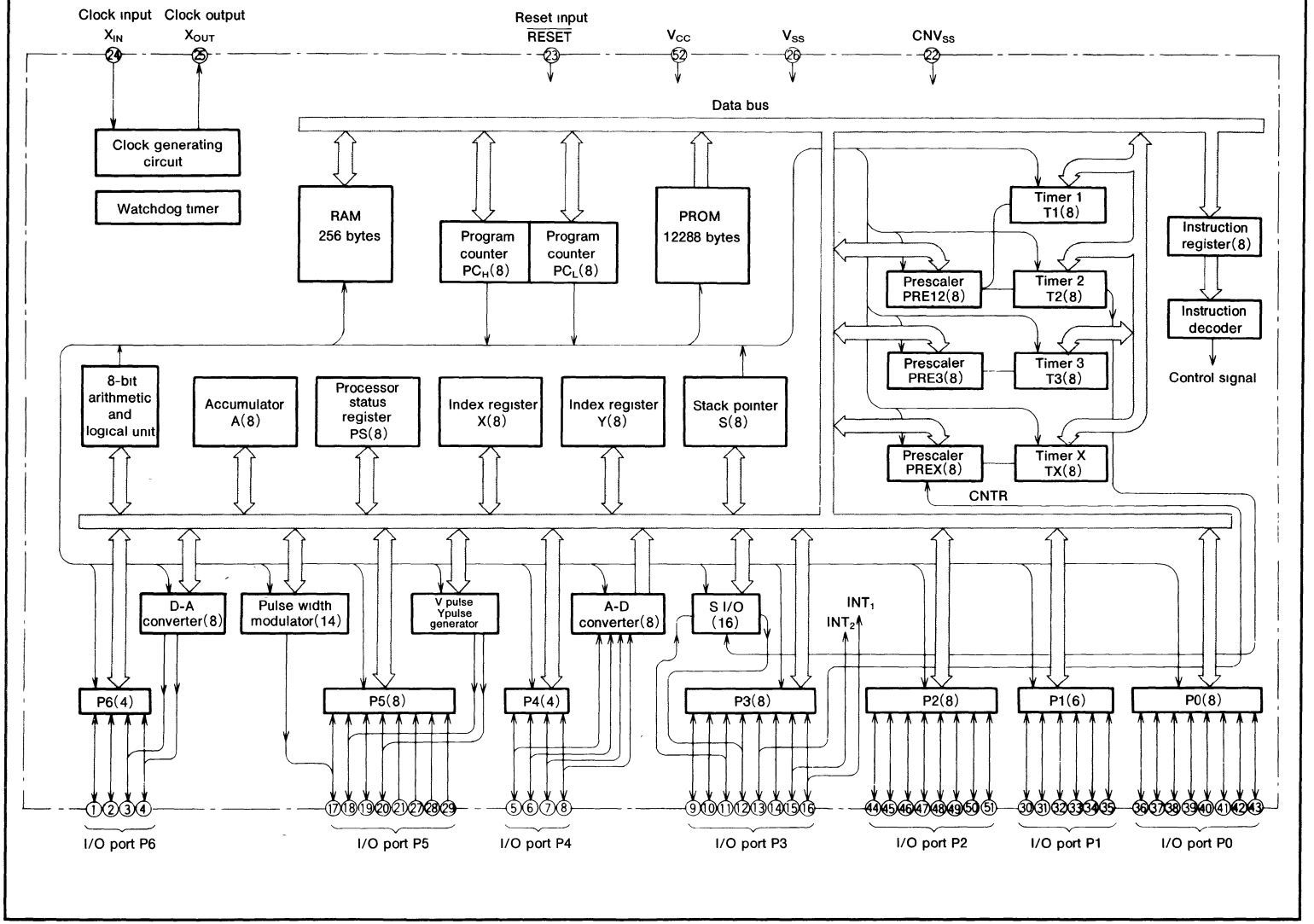
M37420E6-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M37420E6-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	PROM		12288 bytes (Note 1)
	RAM		256 bytes
Input/Output ports	P0, P1, P2, P3, P4, $P5_4$~$P5_7$, P6	I/O	8-bitX3, 6-bitX1, 4-bitX3
	$P5_0$~$P5_3$	Input	4-bitX1
Serial I/O			8-bitX1 or 16-bitX1
Timers			8-bit prescalerX3+8-bit timerX4
A-D conversion			8-bitX1 (4 channels)
D-A conversion			8-bitX2
Pulse width modulator			14-bitX1
Watchdog timer			15-bitX1
Subroutine nesting			96 levels (max)
Interrupt			Two external interrupts, three internal timer interrupts (or timerX2, S I/OX1)
Clock generating circuit			built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M37420E6-XXXSP		52-pin shrink plastic molded DIP
	M37420E6SS		52-pin shrink ceramic DIP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS} This voltage can be used as reference voltage for A-D or D-A converter
CNV_{SS} /V_{PP}	Single-chip	CNV_{SS} input	Input	Connect to 0V
	EPROM	V_{PP} input		Connect to V_{PP} when programming or verifing
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM	RESET input		Connect to V_{SS}
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output It is set to input mode at reset The output format is N-ch open drain
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7)
$P1_0$~$P1_5$	Single-chip	I/O port P1	I/O	Port P1 is an 6-bit I/O port which has the same function as port P0
	EPROM	Address input A_8~A_{13}	Input	$P1_0$~$P1_5$ works as the higher 6 bit address inputs (A_8~A_{13})
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as port P0 The output format is CMOS
	EPROM	Data input/output D_0~D_7	I/O	Port 2 works as an 8 bit data bus (D_0~D_7)
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$, $P3_1$ and $P3_0$ work as CNTR pin, INT_2 and INT_1 respectively The output format is N-ch open drain
	EPROM	Input Port P3	Input	$P3_5$, $P3_4$ and $P3_3$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs respectively Connect $P3_0$~$P3_2$ to 0V and $P3_7$ and $P3_6$ to V_{CC}
$P4_4$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 4-bit I/O port which has the same function as port P0 Ports $P4_7$~$P4_4$ are common with analog inputs AN_7~AN_4 The output format is N-ch open drain
	EPROM	Select mode	Input	Connect to 0V
$P5_0$~$P5_3$	Single-chip	Input port P5	Input	$P5_0$~$P5_3$ are input port These port can be used as edge-sence input $P5_0$~$P5_2$ detects rising edge, and $P5_3$ detects both rising and falling edge $P5_3$ is also common with external trigger output and V pulse, Y pulse generator trigger input
	EPROM		Input	Connect to 0V
$P5_4$~$P5_7$	Single-chip	I/O port P5	I/O	$P5_4$~$P5_7$ is I/O port and has basically the same function as port P0 $P5_7$ is common with PWM The output format is CMOS output
	EPROM		Input	Connect to 0V
$P6_0$~$P6_3$	Single-chip	I/O port P6	I/O	Port P6 is 4-bit I/O port and has basically the same function as port P0 $P6_0$ and $P6_1$ are common with DA_1 and DA_2 respectively The output format is CMOS output
	EPROM		Input	Connect to 0V

EPROM MODE

The M37420E6-XXXSP or M37420E6SS features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P3_3 \sim P3_5$, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37420E6-XXXSP, M37420E6SS	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1	$A_0 \sim A_{13}$
Data I/O	Port P2	$D_0 \sim D_7$
$\overline{CE}$	$P3_5/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P3_4/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P3_3/CNTR/\overline{PGM}$	$\overline{PGM}$

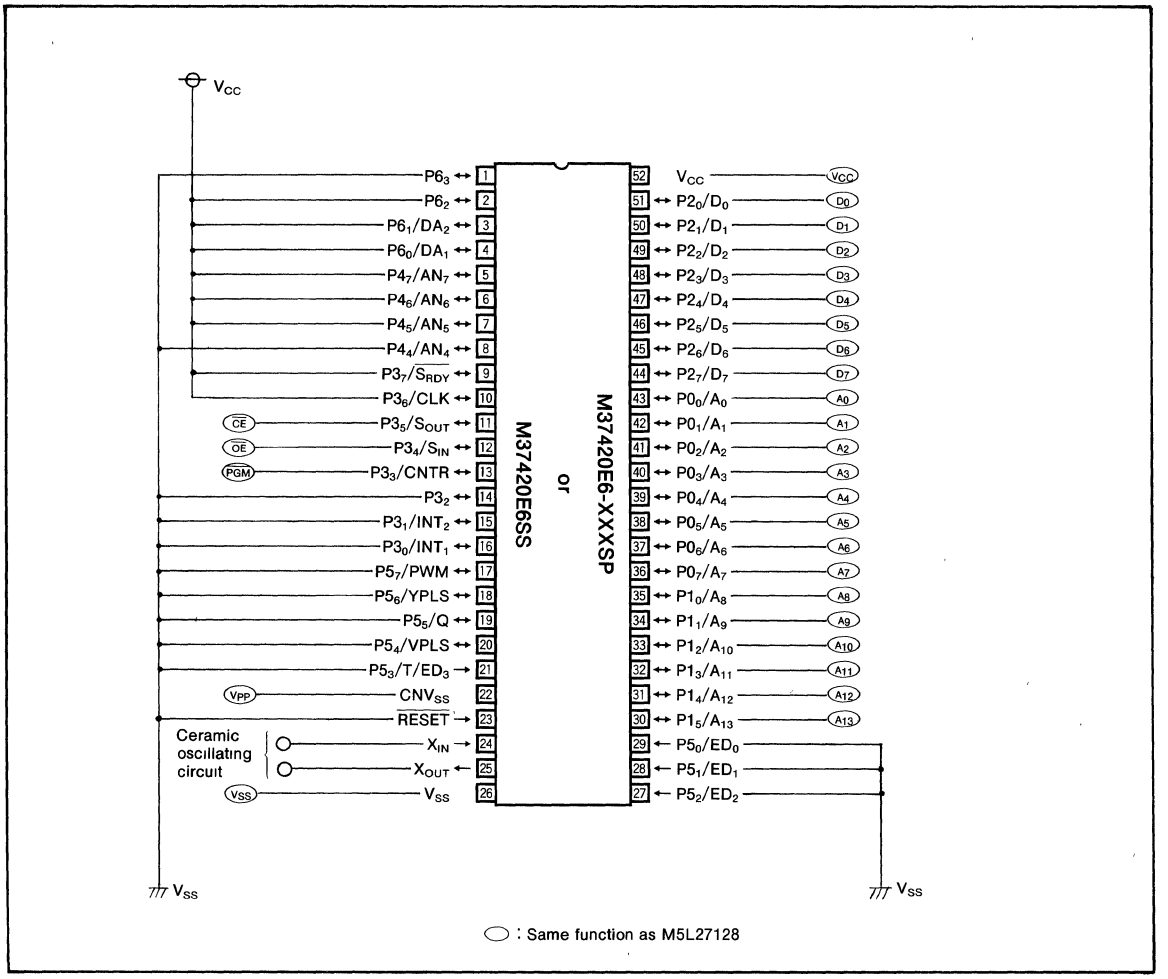


Fig. 1 Pin connection in EPROM mode

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PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{13}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only be erased on the M37420E6SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

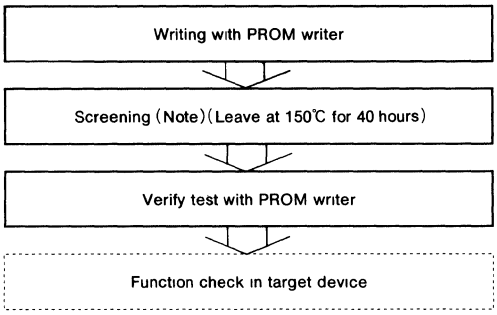
NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$(11)	$\overline{OE}$(12)	$\overline{PGM}$(13)	V_{PP}(22)	V_{CC}(52)	Data I/O (44~51)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
2 : An X indicates either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$, $P5_4$∼$P5_7$, $P6_0$∼$P6_3$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$		−0.3∼13	V
V_I	Input voltage CNV_{SS}		−0.3∼13 (Note 1)	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_4$∼$P5_7$, $P6_0$∼$P6_3$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P3_0$∼$P3_7$		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_4$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_3$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_5$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_4$∼$P4_7$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$, $P5_4$∼$P5_7$, $P6_0$∼$P6_3$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$, $P5_4$∼$P5_7$, $P6_0$∼$P6_3$ (Note 1)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
2 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4 and P6 to exceed 80mA
Do not allow the combined high- level output current of port P2, P5 and P6 to exceed 50mA

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
V_{OH}	"H" output voltage $P2_0$~$P2_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	I_{OH}=−10mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	I_{OL}=10mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_0$, $P3_1$	When used as INT input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P5_3$	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P3_0$~$P3_7$, $P5_0$~$P5_3$	V_I=12V			12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	V_I=5V			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	φ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition; f(X_{IN})=8MHz Square wave		6	15	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				25	μs
V_{IA}	Analog input voltage		0		V_{CC}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±2	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}	1	2	4	kΩ