M37415M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37415M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

This microcomputer is also suitable for applications which require controlling LCDs and generating DTMF.

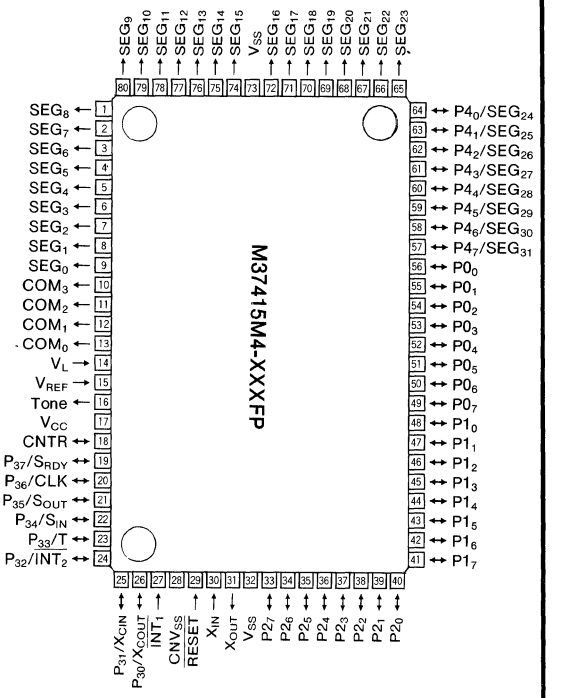
FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ..... 8192 bytes
  - RAM ..... 512 bytes
  - RAM for display LCD ..... 16 bytes
- Instruction execution time
  - ... 2.5 μs (minimum instructions at 3.2MHz frequency)
  - ..... 5μs (minimum instructions at 1.6MHz frequency)
  - .... 10 μs (minimum instructions at 800kHz frequency)
  - ..... 20μs (minimum instructions at 400kHz frequency)
- Single power supply
  - f(X_{IN})=400kHz, or 800kHz ..... $2.5 \leqq V_{CC} \leqq 5.5V$
  - f(X_{IN})=1.6MHz, or 3.2MHz ..... $4.5V \leqq V_{CC} \leqq 5.5V$
- Power dissipation
  - normal operation mode (at 3.2MHz frequency)
    - ..... 20mW (DTMF output V_{CC}=5.0V typ.)
    - ..... 15mW (DTMF off V_{CC}=5.0V typ.)
  - low-speed operation mode
    (at 32kHz frequency for clock function)
    - ..... 225μW (V_{CC}=5.0V typ.)
  - stop mode (at 25℃) ..... 5μW (V_{CC}=5.0V max.)
- RAM retention voltage (stop mode) ..... $2V \leqq V_{RAM} \leqq 5.5V$
- Subroutine nesting ..... 64 levels (max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers makes one set)
- Programmable I/O ports
  (Ports P0, P1, P2, P3) 32
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- DTMF (Dual-Tone Multi-Frequency) generator ... Built-in
- LCD controller/driver
  (1/2, 1/3, bias, 1/2, 1/3, 1/4 duty)
  - segment output 32
  - common output 4
  - resistor for LCD power supply ..... Built-in
- Two clock generator circuits
  (One is for main clock, the other is for clock function.)

APPLICATION

Home telephone, Multi function telephone

PIN CONFIGURATION (TOP VIEW)



Outline 80P6

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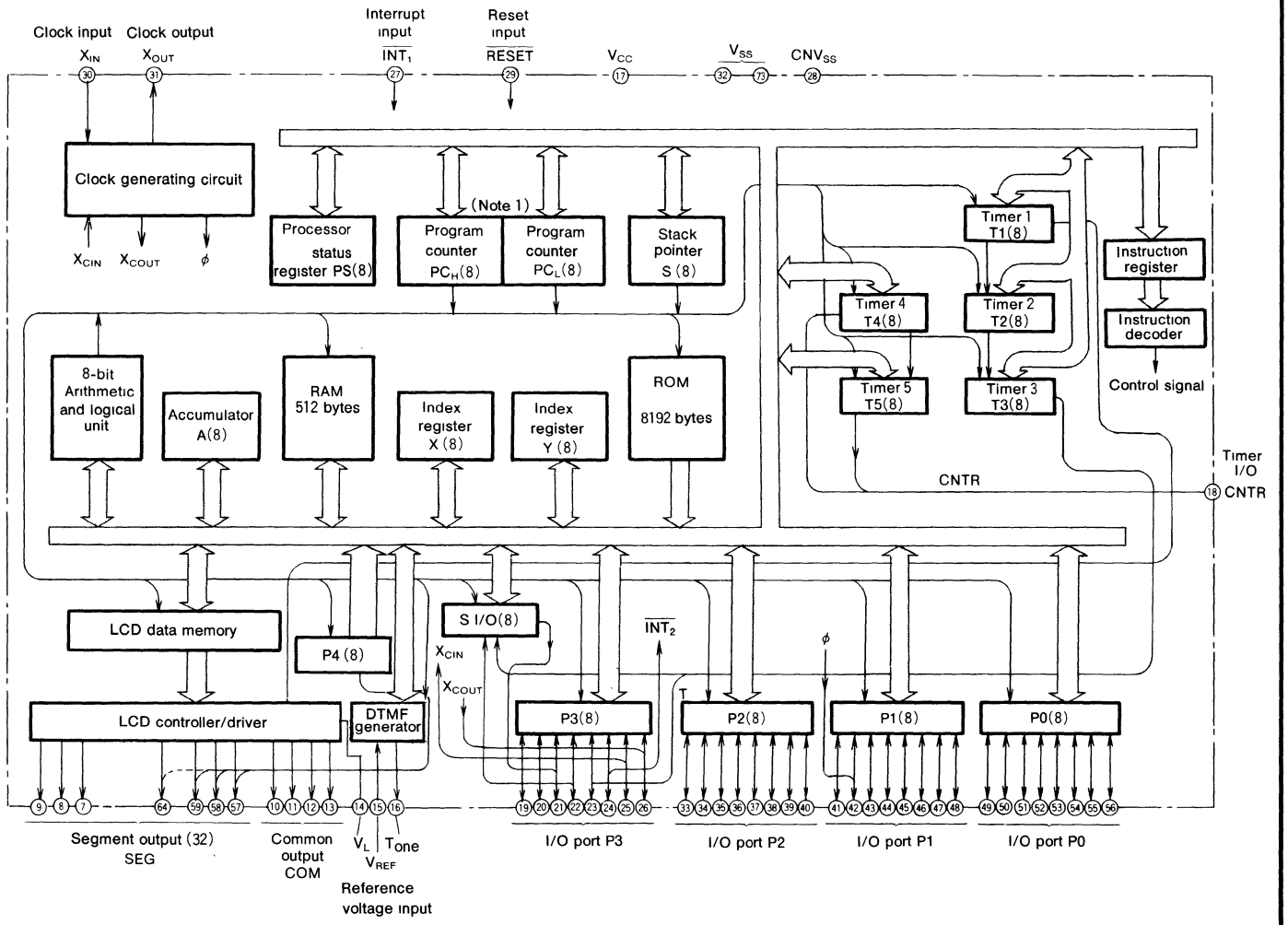
M37415M4-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 6 bits long

FUNCTIONS OF M37415M4-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2.5μs (minimum instructions, at 3.2MHz frequency) 5μs (minimum instructions, at 1.6MHz frequency) 10μs (minimum instructions, at 800kHz frequency) 20μs (minimum instructions, at 400kHz frequency)
Clock frequency			3.2MHz, 1.6MHz, 800kHz, 400kHz
Memory size	ROM		8192 bytes
	RAM		512 bytes
	RAM for display LCD		16 bytes
Input/Output port	P0, P1, P2, P3	I/O	8-bit×4
	P4	Input	8-bit×1 (Port P4 are in common with SEG)
	SEG	LCD output	32-bit×1
	COM	LCD output	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when serial I/O is used)
			16-bit timer×1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3, bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		32(SEG_{24}~SEG_{31} are in common with port P4)
Subroutine nesting			64 (max.)
Interrupt			Two external interrupts, Three timer internal interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			2.5~5.5V(at 400kHz or 800kHz frequency) 4.5~5.5V(at 1.6MHz or 3.2MHz frequency) RAM retention voltage at clock stop is 2~5.5V
Power dissipation	DTMF output	At high-speed operation V_{CC}=5V	20mW (at clock frequency f(X_{IN})=3.2MHz)
	DTMF off	At high-speed operation V_{CC}=5V	15mW (at clock frequency f(X_{IN})=3.2MHz)
		At low-speed operation V_{CC}=5V	225μW (at clock frequency f(X_{CIN})=32kHz)
		At stop mode	1μA (max. 25℃)
Input/Output characteristics	Input/Output voltage		5V
	Output current		I_{OH}=−2mA(V_{OH}=3V)
			I_{OL}=10mA(V_{OL}=2V)
			Pull-up current : Min −30μA, Max −140μA, Typ −70μA (V_{CC}=5V input voltage 0V)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage input		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}
CNV_{SS}	CNV_{SS} input		Connect to V_{SS}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin It can be measured input voltage level
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively
$P4_0$~$P4_7$	Input port P4	Input	Port P4 is an 8-bit input port and can be used as segment output pins
V_L	Voltage input for LCD	Input	This is a voltage input pin for LCD Supply voltage is $0V \leqq V_L \leqq V_{CC}$ 0V~V_{LV} is supplied to LCD
COM_0~ COM_3	Common output	Output	These are the LCD common output pins At 1/2 duty, COM_2 and COM_3 pins are not use At 1/3 duty, COM_3 pin is not used
SEG_0~ SEG_{23}	Segment output	Output	These are LCD segment output pins
CNTR	Counter I/O	I/O	This is an output pin for timer 4 and 5 It can be measured input voltage level
V_{REF}	D-A convert power supply for DTMF		Reference voltage input for A-D converter of DTMF
Tone	DTMF output	Output	This is DTMF output pin

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37415 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

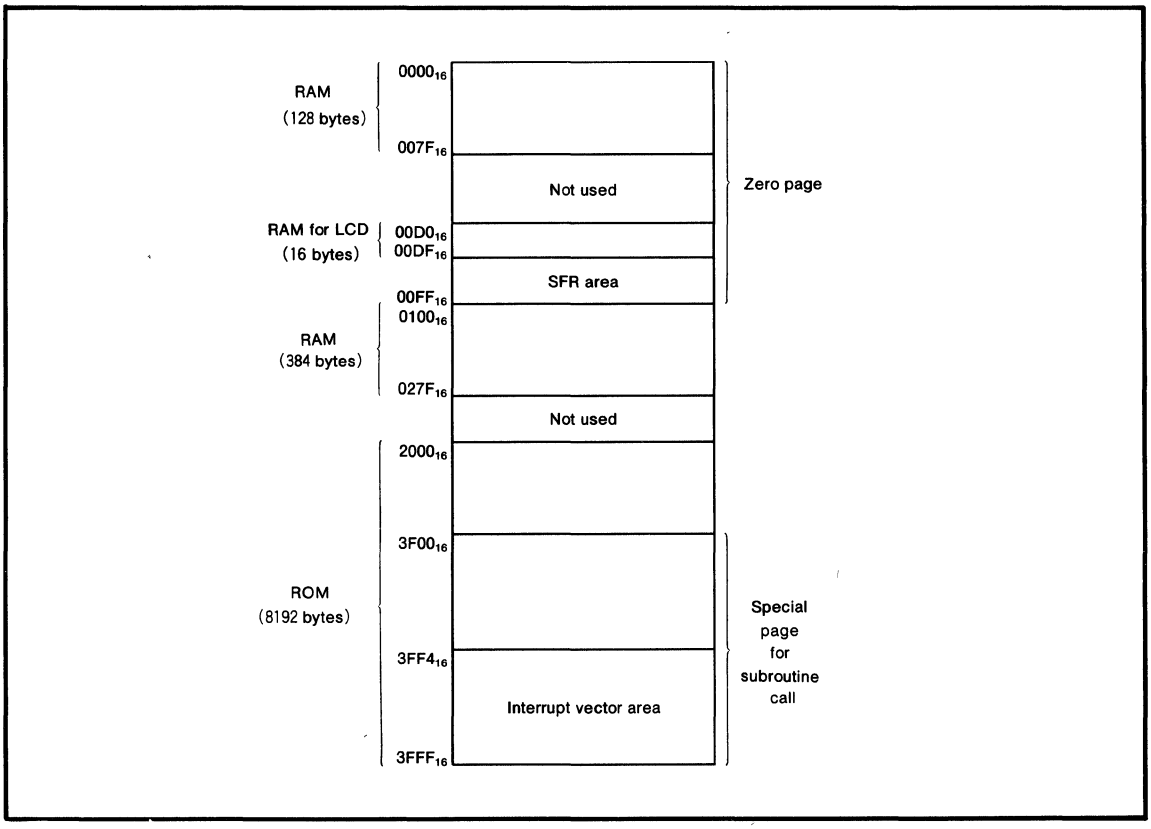


Fig.1 Memory map

$00E0_{16}$	Port P0	$00F0_{16}$	
$00E1_{16}$	Port P0 directional register	$00F1_{16}$	
$00E2_{16}$	Port P1	$00F2_{16}$	
$00E3_{16}$	Port P1 directional register	$00F3_{16}$	
$00E4_{16}$	Port P2	$00F4_{16}$	DTMF register
$00E5_{16}$	Port P2 directional register	$00F5_{16}$	LCD mode register
$00E6_{16}$		$00F6_{16}$	Serial I/O mode register
$00E7_{16}$		$00F7_{16}$	Serial I/O register
$00E8_{16}$	Port P3	$00F8_{16}$	Timer 4, 5 mode register
$00E9_{16}$	Port P3 directional register	$00F9_{16}$	Timer 1
$00EA_{16}$	Port P4	$00FA_{16}$	Timer 2
$00EB_{16}$		$00FB_{16}$	Timer 3
$00EC_{16}$		$00FC_{16}$	Timer 4
$00ED_{16}$		$00FD_{16}$	Timer 5
$00EE_{16}$		$00FE_{16}$	Interrupt control register
$00EF_{16}$		$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

INTERRUPT

The M37415M4-XXXFP can be interrupted from eight sources; $\overline{INT_1}$, Timer 1, Timer 2, Timer 3 or Serial I/O, $\overline{INT_2}$ or key on wake up, and BRK inctruction.

The value of bit 2 of the serial I/O register (address $00F6_{16}$) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from $\overline{INT_2}$ or from "key on wake up". When bit 7 is "0", the interrupt is from $\overline{INT_2}$. When bit 7 is "1" the interrupt is from "key on wake up". "Key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as interrupt.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$3FFF_{16}$, $3FFE_{16}$
$\overline{INT_1}$	2	$3FFD_{16}$, $3FFC_{16}$
Timer 1	3	$3FFB_{16}$, $3FFA_{16}$
Timer 2	4	$3FF9_{16}$, $3FF8_{16}$
Timer 3 or serial I/O	5	$3FF7_{16}$, $3FF6_{16}$
$\overline{INT_2}$ or key on wake up(BRK)	6	$3FF5_{16}$, $3FF4_{16}$

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Expect for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts except key on wake up function can further be controlled individually via the interrupt control register shown in Figure 3 An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins goes from "H" to "L"
(2) When the levels any pin of P2 goes "L" (at power down mode)
(3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O goes to "0"

These request bits can be clear by a program but can not be set. The interrupt enable bit can be set and clear by a program.

Since the BRK instruction interrupt and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt of if $\overline{INT_2}$ generated the interrupt.

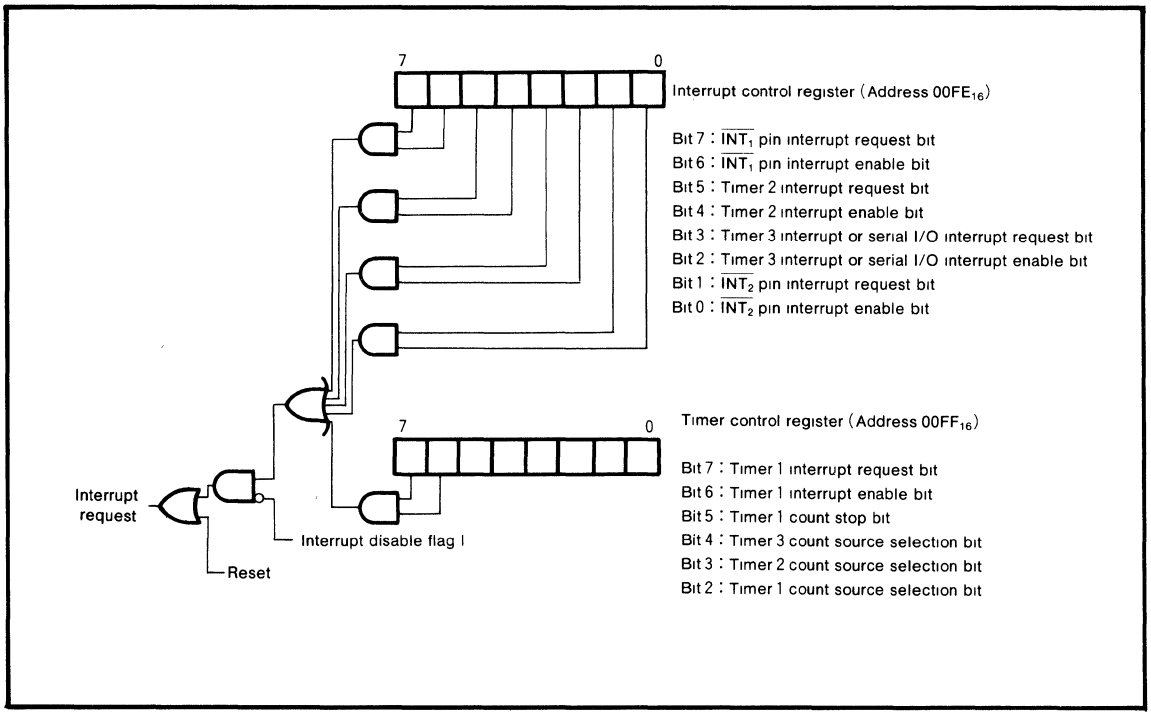


Fig.3 Interrupt control

TIMER

The M37415M4-XXXFP has five timers; timer 1, timer 2, timer 3, timer 4, and timer 5. The interrupt of timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for timer 1, timer 2, timer 3 can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5. A block diagram of timer 1 through 5 is shown in Figure 4. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is $1/(n+1)$, where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$, and $00FF_{16}$, respectively (see interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 though 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

TIMER 4 AND TIMER 5 MODES

(1) Timer mode [00].
The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.

(2) Pulse output mode [01].
The output level of the CNTR pin inverts each timer the timer contents to zero.

(3) Event counter mode [10].
The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decreased each time the CNTR input goes from "L" to "H".

(4) Pulse width measurement mode [11].
This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address $00F8_{16}$.
The structure of timer 4, 5 mode register is shown in Figure 6.

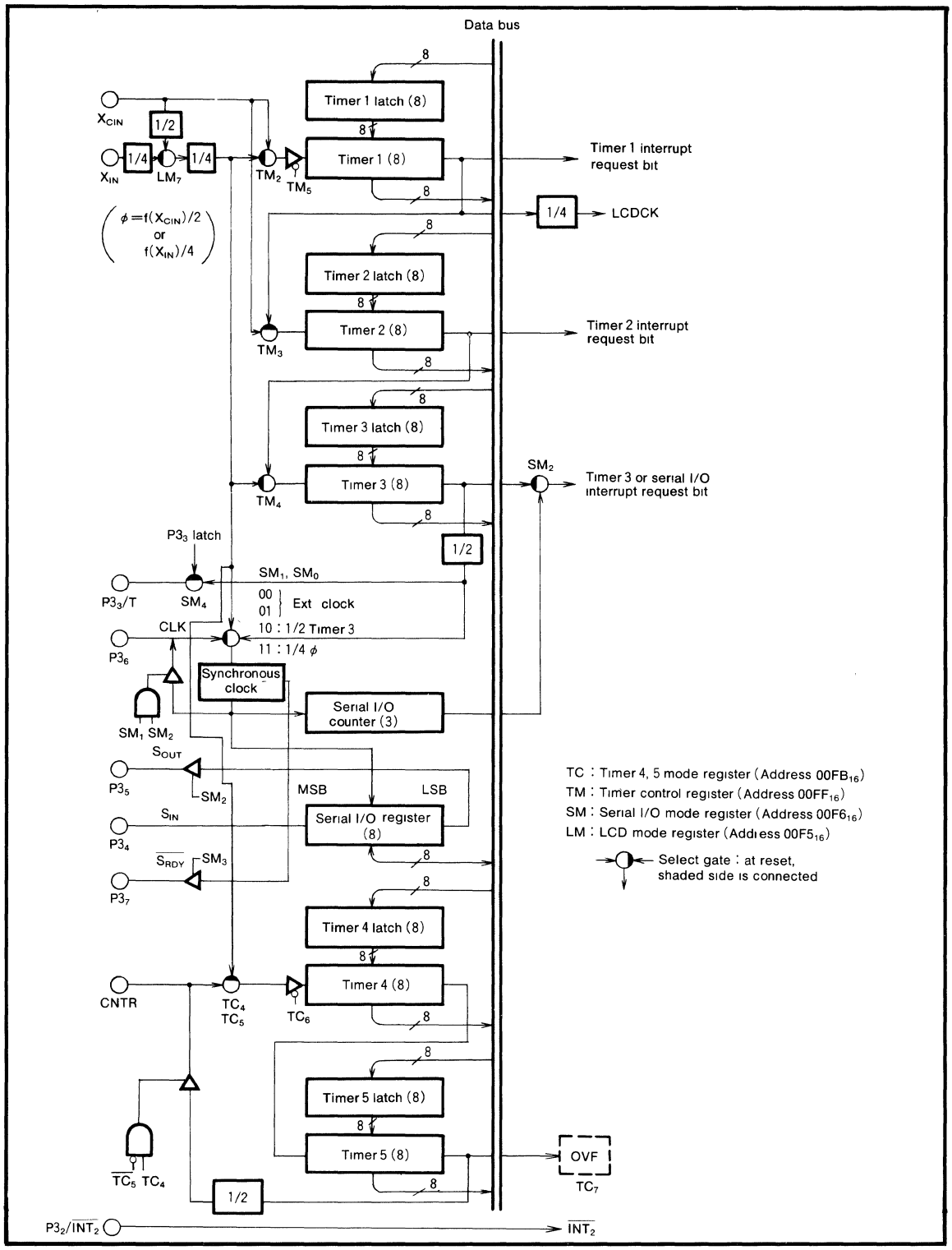


Fig.4 Block diagram of timers 1 through 5

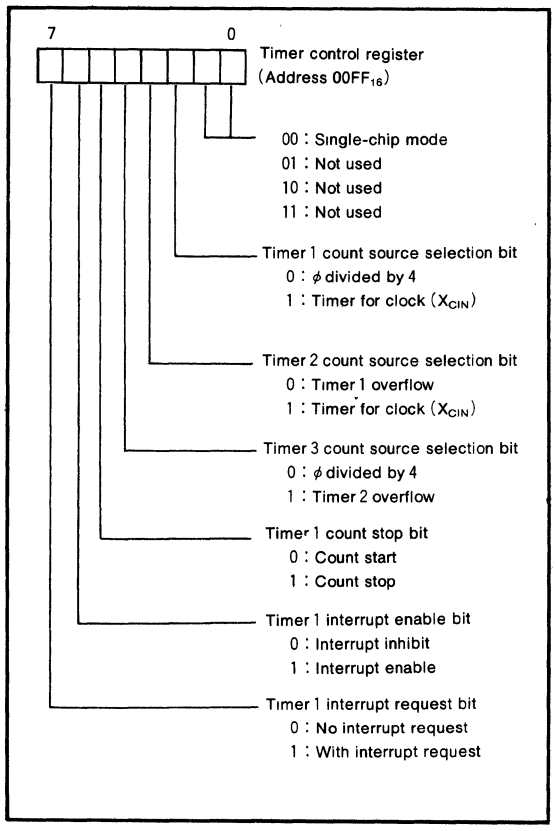


Fig.5 Structure of timer control register

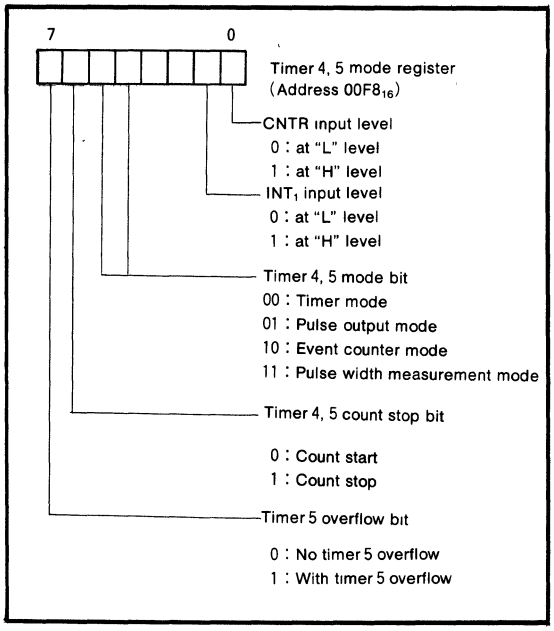


Fig.6 Structure of timer 4, 5 mode register

PORT $P3_3$/TIMER 3 OUTPUT

The signal that timer 3 is divided by 2 is output from $P3_3$ (T), at the contents of bit 4 of the serial I/O mode register (address $00F6_{16}$) is "1"

WATCHDOG TIMER FUNCTION

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the $\overline{\text{RESET}}$ pin as shown in Figure 7, and by setting bit 4 and 5 of address $00F8_{16}$ to "01". At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 12.5 to 15.0μs (at $f(X_{IN})$ =800kHz) after the reset is input, bits 4,5 and 6 of the timer 4,5 mode register are initialized to "0". The initialization program to set the watchdog timer mode should have the following sequence;

(1) Set the pulse output mode after writing a value to timer 4 and 5 registers.
(2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the reset is executed.
(3) 12.5 to 17.5μs (at $f(X_{IN})=800$kHz) after a reset, the CNTR pin will be in high impedance state.

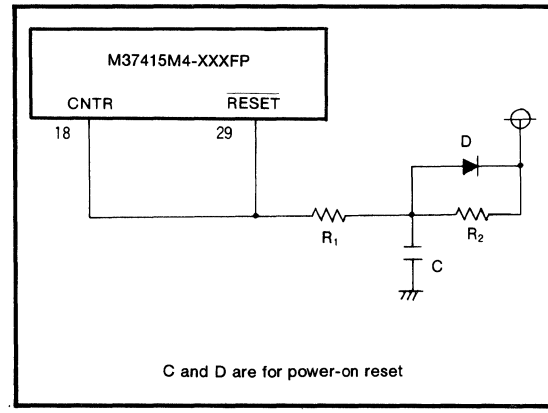


Fig.7 Reset circuit with the watchdog timer

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

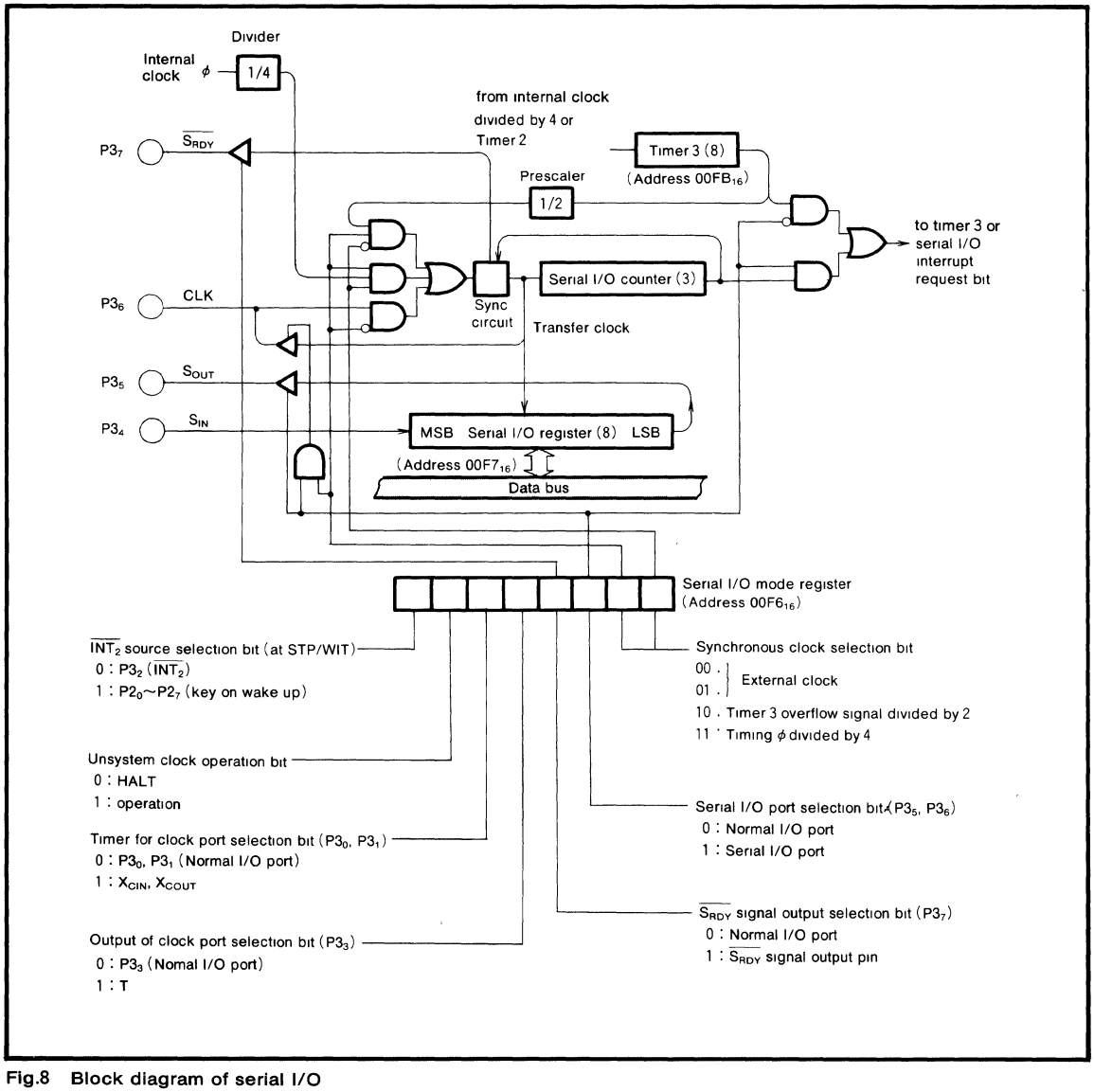


Fig.8 Block diagram of serial I/O

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output, and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the faling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37415M4-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 50kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M37415M4-XXXFP's are shown in Figure 10.

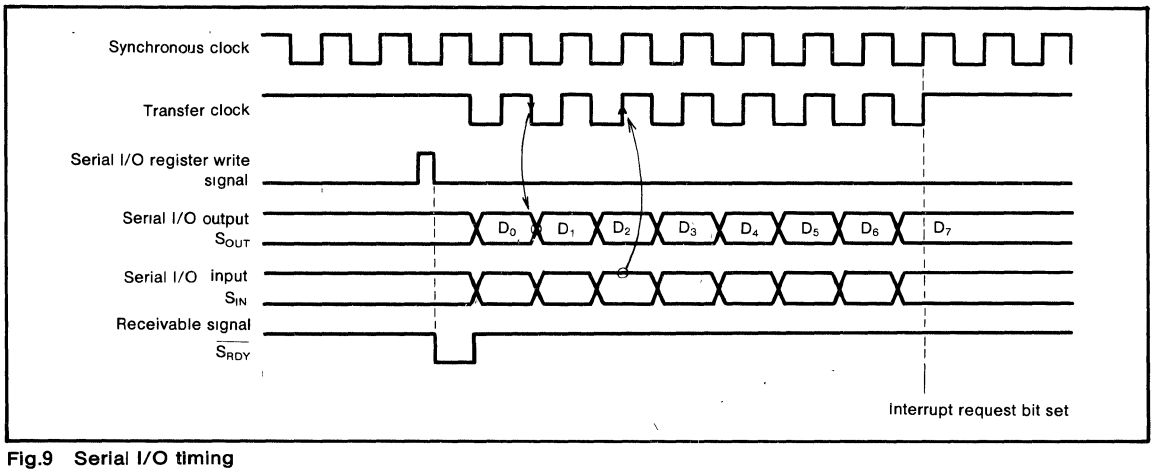


Fig.9 Serial I/O timing

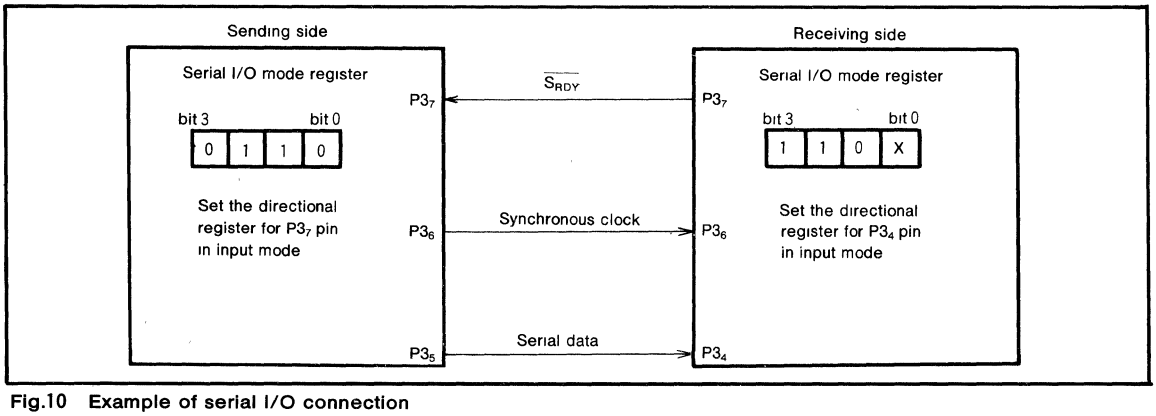


Fig.10 Example of serial I/O connection

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DTMF FUNCTION

The M37415M4-XXXFP has the DTMF (Dual-Tone Multi-Frequency) output and control function. The value of bit 0, and bit 1 of DTMF register (address $00F4_{16}$) determines the low frequency band value. And the value of bit 2, and bit 3 of DTMF register determines the high frequency band value. The DTMF output can be controlled by the value of bit 4, and bit 5 of the DTMF register. When bit 4 is "1" the low frequency band is output to Tone, and when bit 4 is "0" the output of low frequency band is stopped. When bit 5 is "1" the high frequency band is output to Tone, and when bit 5 is "0" the output of high frequency band is stopped.

The value of bit 6, and 7 of DTMF register determines the basic frequency. The structure of the DTMF register is shown in Figure 11. The accuracy of DTMF output value is shown in Table 2 and 3.

Table 2. Accuracy of DTMF output (at low frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
697	694.44	−2.555	−0.367
770	769.23	−0.769	−0.1
852	854.7	2.7	0.317
941	938.97	−2.033	−0.216

Table 3. Accuracy of DTMF output (at high frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
1209	1204.8	−4.181	−0.346
1336	1333.3	−2.667	−0.2
1477	1470.6	−6.412	−0.434
1633	1639.3	6.344	0.389

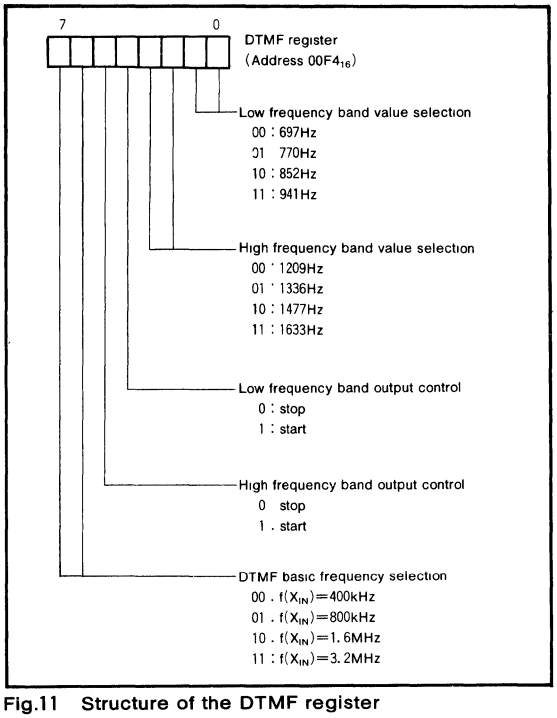


Fig.11 Structure of the DTMF register

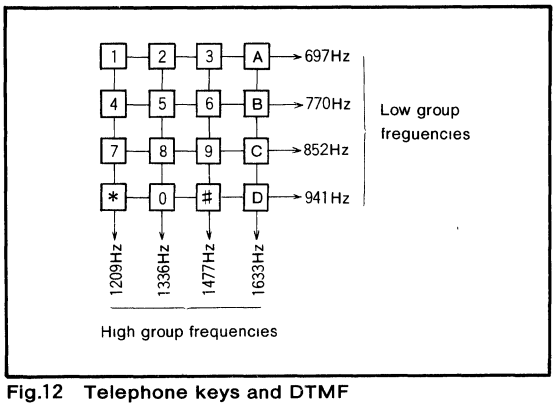


Fig.12 Telephone keys and DTMF

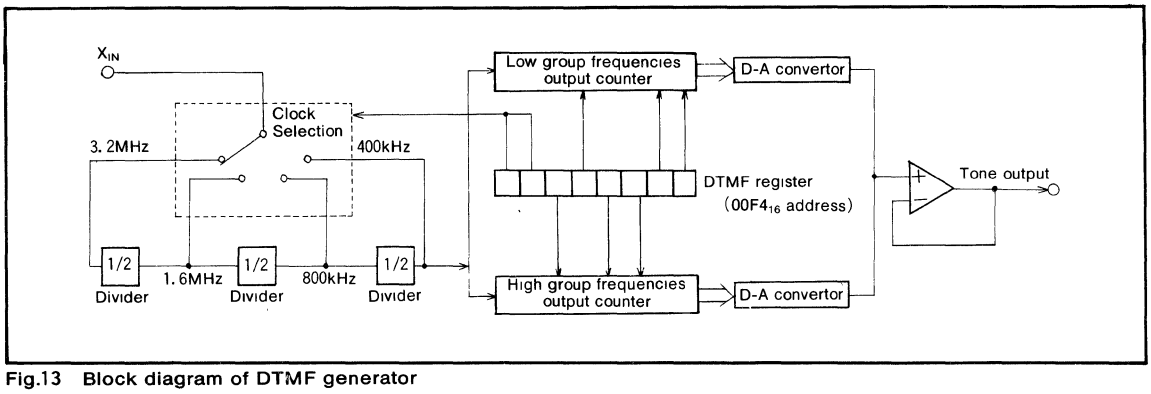


Fig.13 Block diagram of DTMF generator

LCD CONTROLLER/DRIVER

The M37415M4-XXXFP has internal LCD controllers and drivers. A block diagram of LCD circuit is shown in Figure 17.

The terminals for LCD consist of 4 common-pin and 32 segments pin. SEG_{24}~SEG_{31} are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM_4, address $00F5_{16}$). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM_0, LM_1) is n, the duty ratio is 1/(n+1).

Address $00D0_{16}$ ~ $00DF_{16}$ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 15. The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM_3). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off. An example circuit for each bias is shown in Figure 18 and Figure 19 describes the LCD driver waveforms for each bias and duty cycle.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of timer 1 count source)}}{\text{((timer 1 setting}+1)\times 4)}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{n} \quad ; \text{at 1/n duty}$$

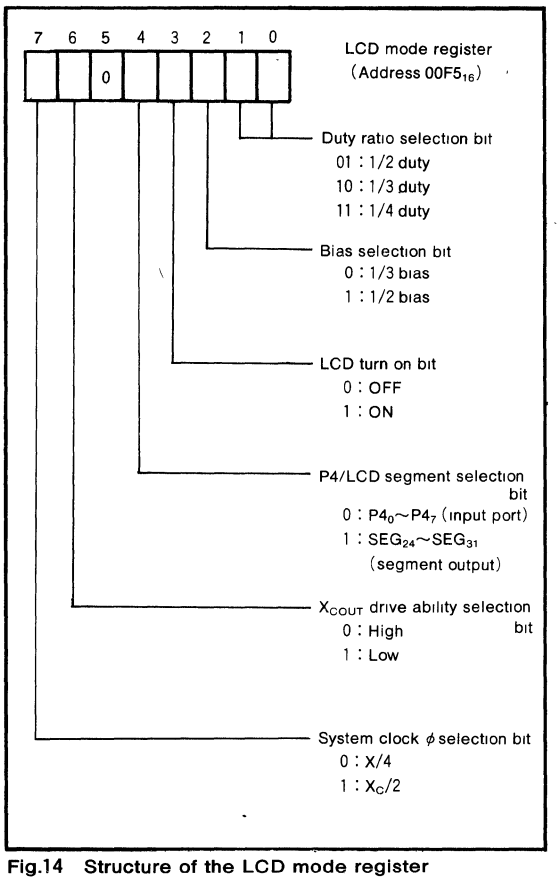


Fig.14 Structure of the LCD mode register

Bit / Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

*Number in data memory area indicates corresponding segment.

Fig. 15 Map of RAM for LCD segment

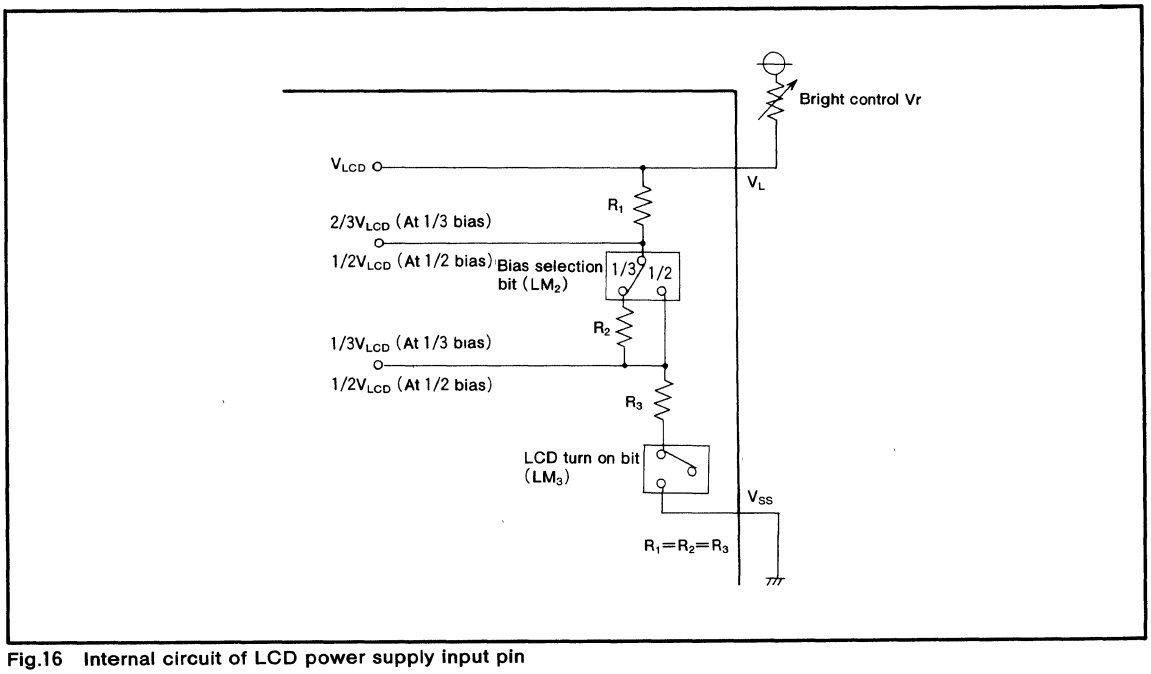


Fig.16 Internal circuit of LCD power supply input pin

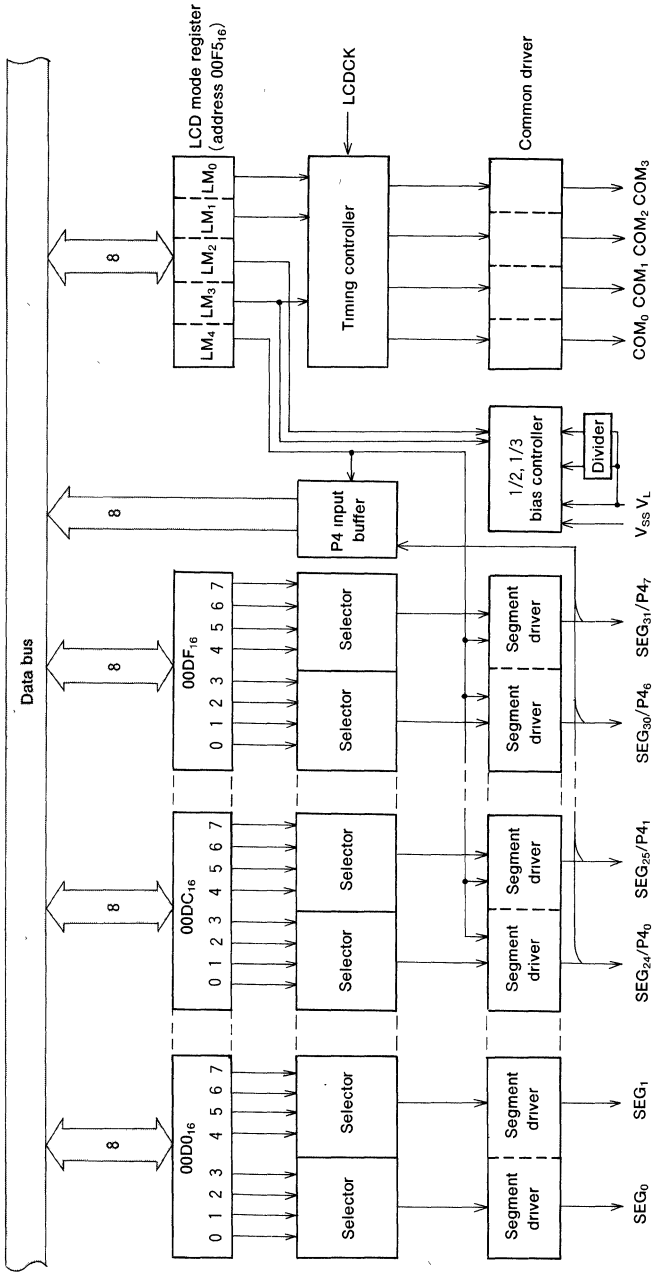


Fig.17 Block diagram of LCD control circuit

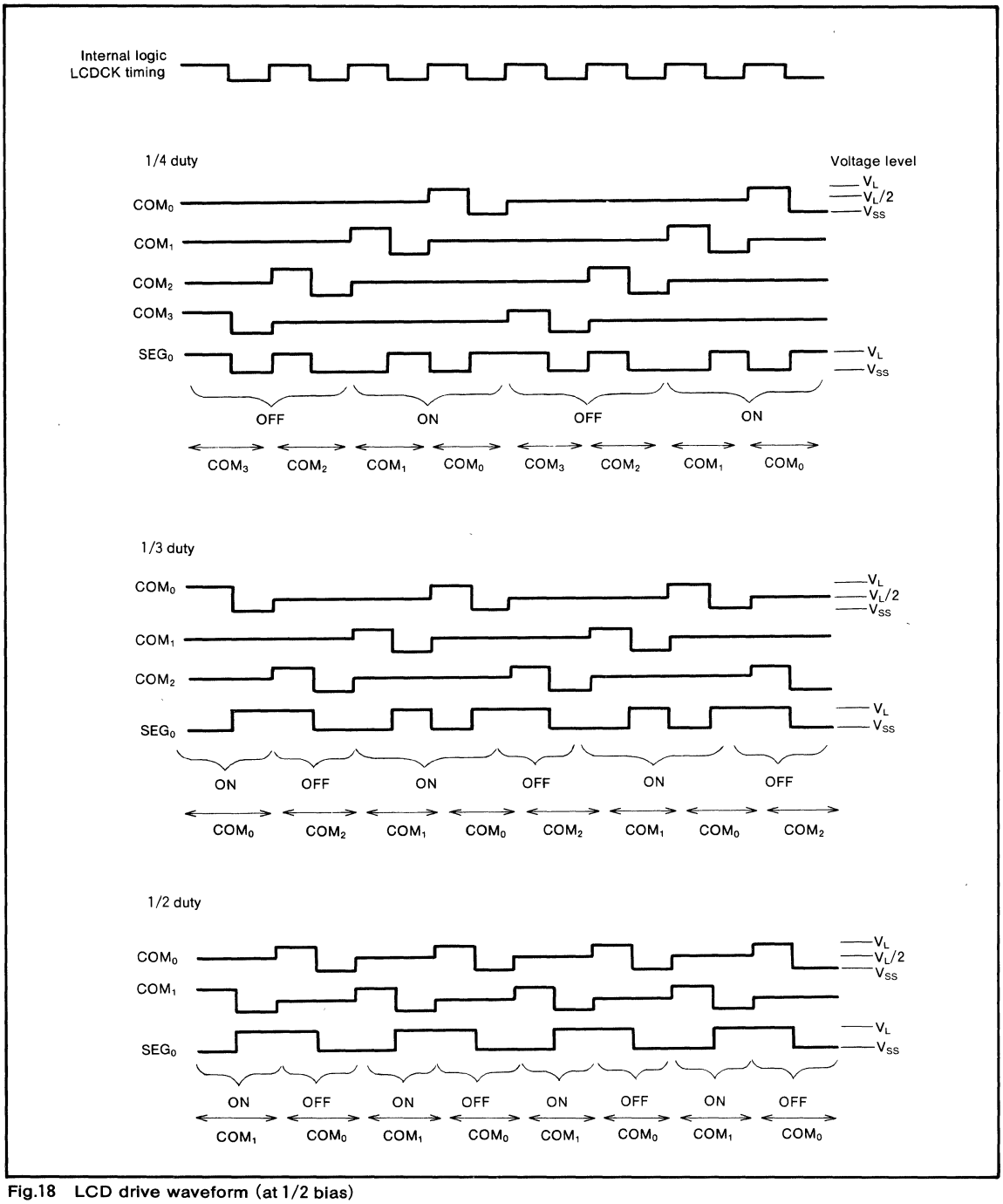


Fig.18 LCD drive waveform (at 1/2 bias)

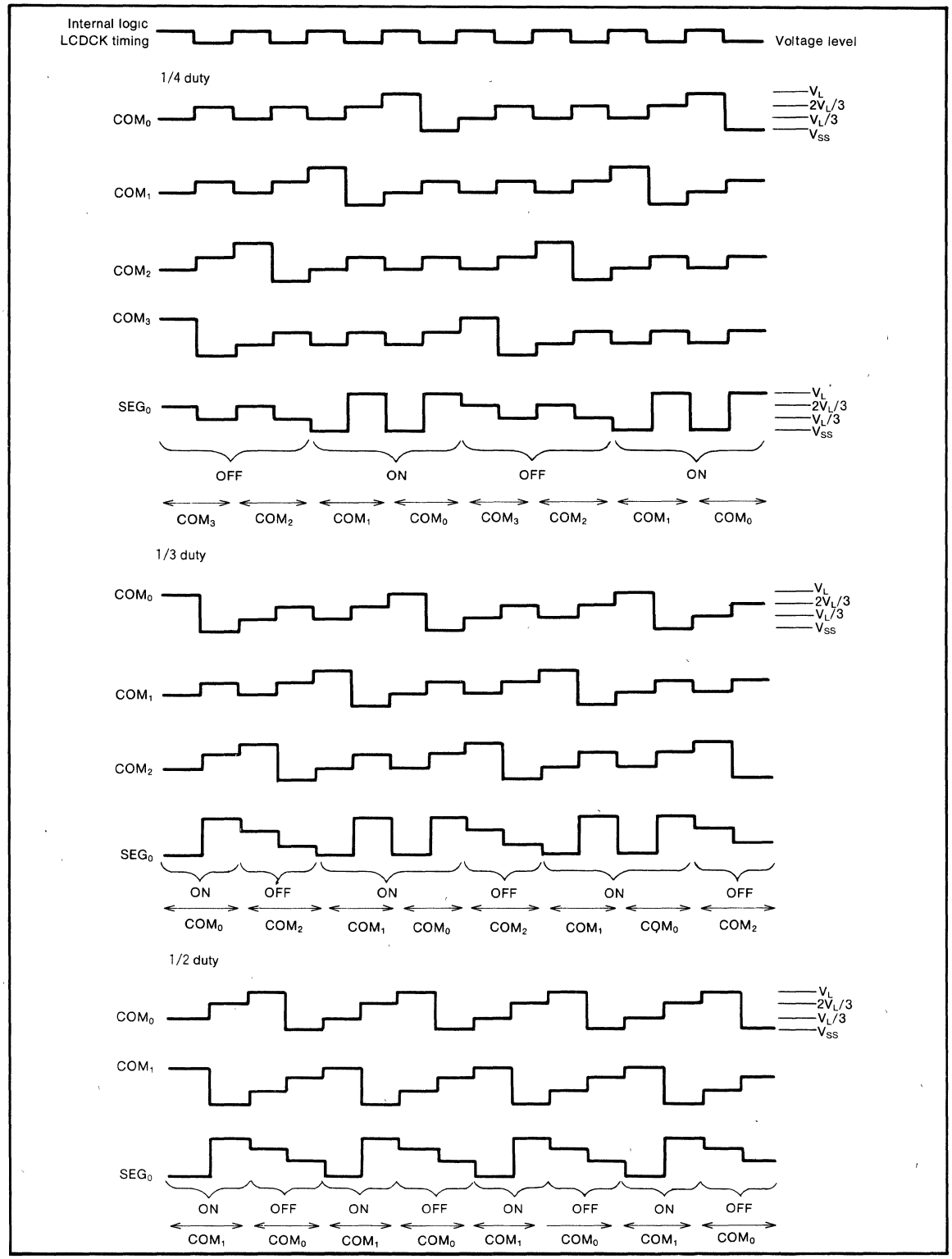


Fig.19 LCD drive waveform (at 1/3 bias)

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register (SM_7) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 20, a key matrix can be connected to port P2 and the microcomputer can be retuned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_2}$ interrupt. When SM_7 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_2}$ are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and SM_7 is "1", all of port P2 must be input "H"

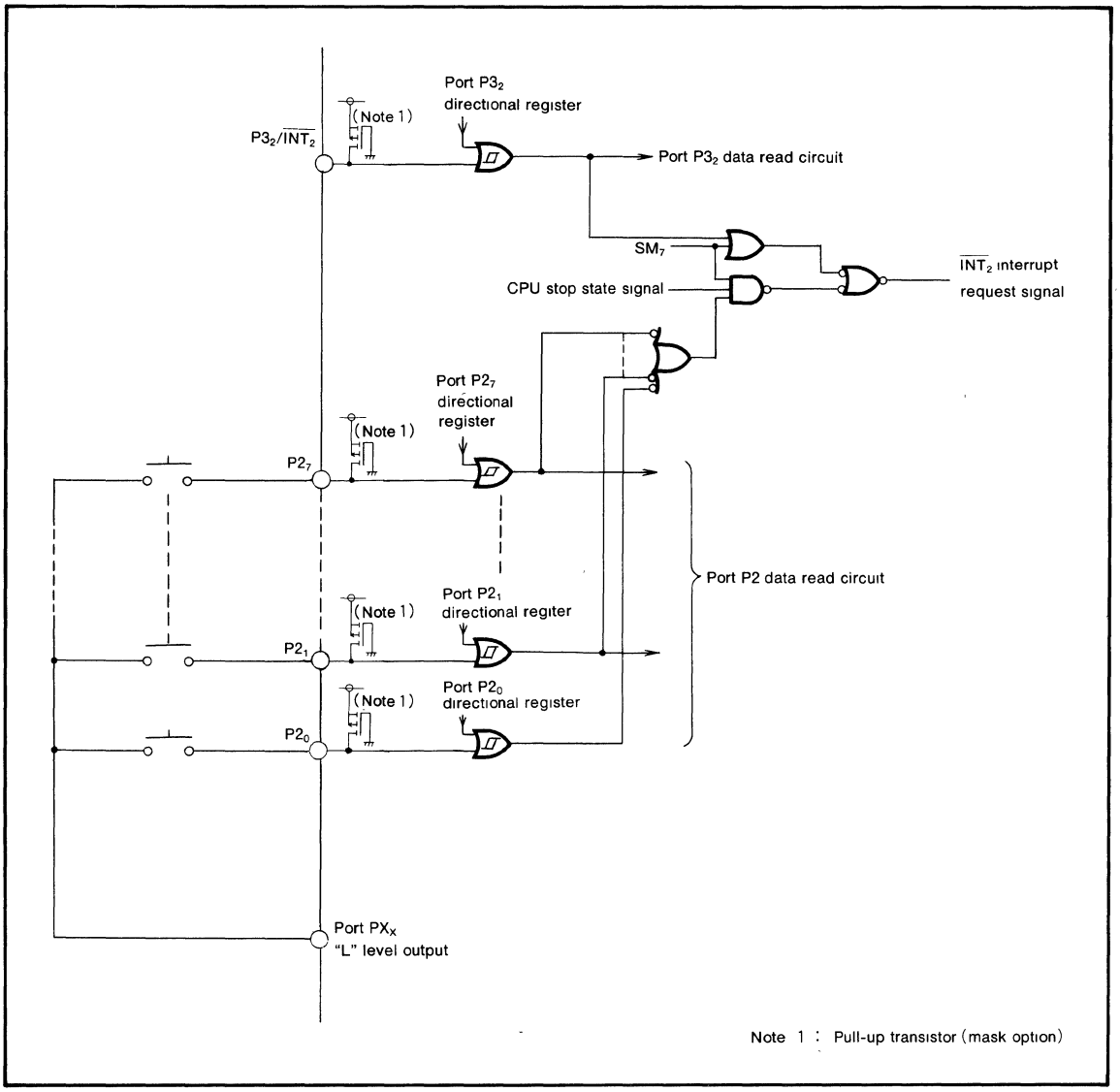


Fig.20 Block diagram of port P2 and $P3_2$, and example of wired at used key on wake up

RESET CIRCUIT

The M37415M4-XXXFP is reset according to the sequence shown in Figure 23. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for at least 8 rising edges of X_{IN} while the power voltage is in the recommended oprating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are as shown in Figure 21, regardless of the status before reset (including stop mode or wait mode).

An example of the reset circuit is shown in Figure 22.

When the power on reset is used and the reset is used while the X_{IN} clock is stopped, the $\overline{RESET}$ pin must be held "L" unitil the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	($00E1_{16}$)	00_{16}
(2)	Port P1 directional register	($00E3_{16}$)	00_{16}
(3)	Port P2 directional register	($00E5_{16}$)	00_{16}
(4)	Port P3 directional register	($00E9_{16}$)	00_{16}
(5)	DTMF register	($00F4_{16}$)	0 0 0 0
(6)	LCD mode register	($00F5_{16}$)	00_{16}
(7)	Serial I/O mode register	($00F6_{16}$)	00_{16}
(8)	Timer 4, 5 mode register	($00F8_{16}$)	0 0 0 0
(9)	Interrupt control register	($00FE_{16}$)	00_{16}
(10)	Timer control register	($00FF_{16}$)	00_{16}
(11)	Interrupt disable flag for processor status register	(PS)	1
(12)	Program counter	(PC_H)	Contents of address $3FFF_{16}$
		(PC_L)	Contents of address $3FFE_{16}$

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig.21 Internal state of microcomputer at reset

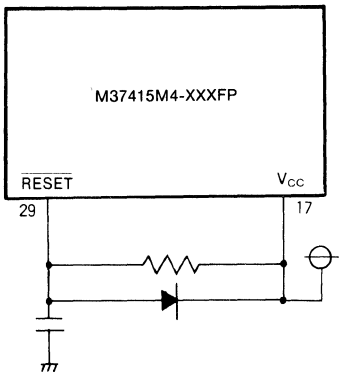
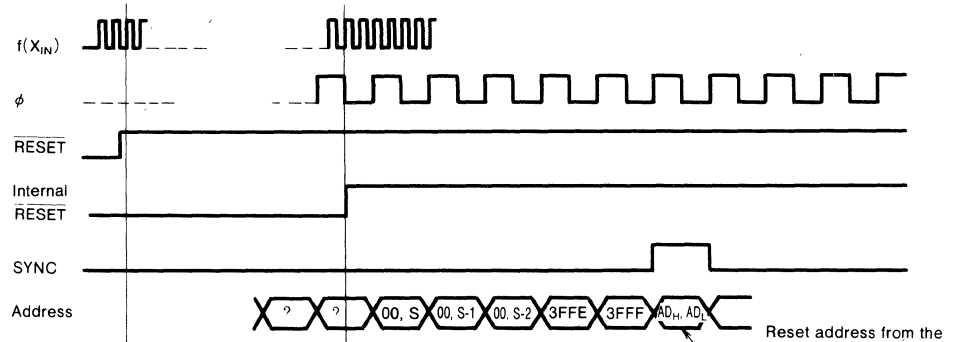


Fig.22 Example of reset circuit



Note 1 : Frequency relation of f(X_{IN}) and φ is f(X_{IN}) = 4·φ
2 : The mark "?" means that the address is changeable depending upon the previous state

Fig.23 Timing diagram at reset

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction. P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal oprating mode after being in the power-down mode.

(4) Port P3

Port P3 has the same function as P0 execept that part of P3 is common with the serial I/O lines (ie output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment output (SEG_0~SEG_{23})

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM_0~COM_3)

These port provides output drive and control for the LCD common lines.

(8) Power supply for LCD (V_L)

Supplies power to the LCD terminals.

(9) $\overline{INT_1}$

The $\overline{INT_1}$ pin is an interrupt pin. The $\overline{INT_1}$ interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address $00F8_{16}$).

(10) $\overline{INT_2}$ ($\overline{INT_2}$/$P3_2$)

The $\overline{INT_2}$ pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The $\overline{INT_2}$ interrupt request bit (bit 1 of address $00FE_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timer 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address $00F8_{16}$).

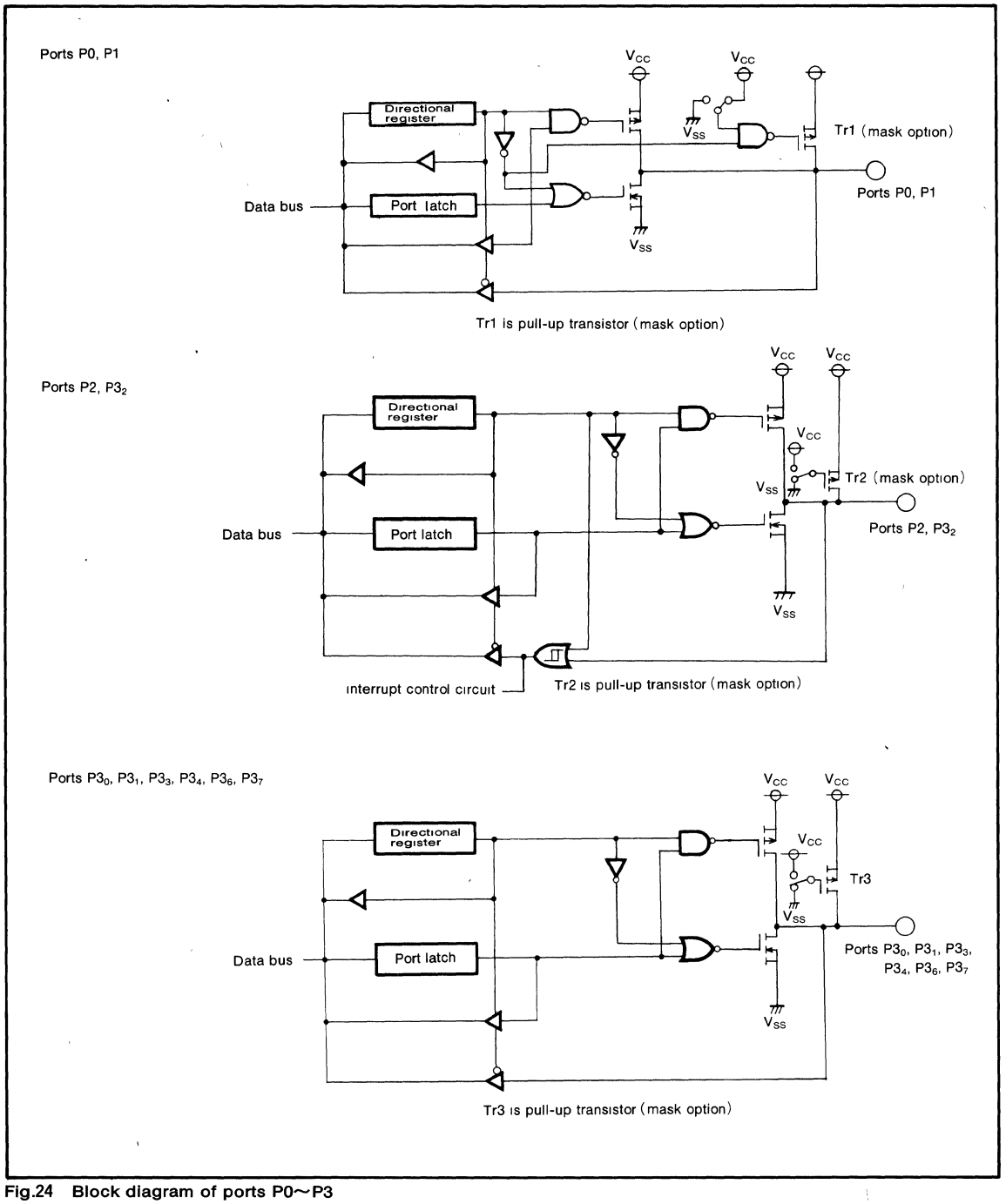


Fig.24 Block diagram of ports P0~P3

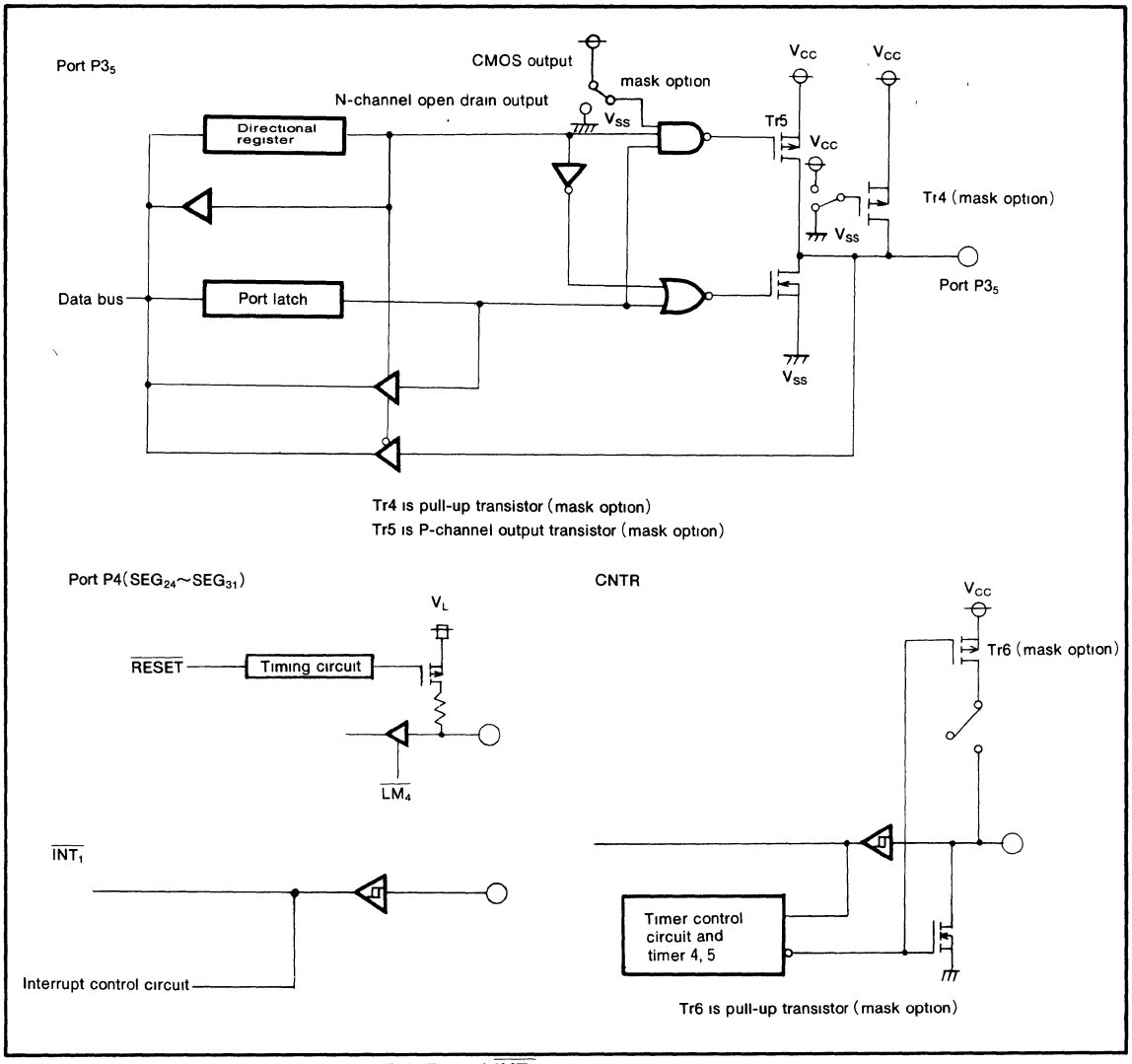


Fig.25 Block diagram of ports P3, P4, CNTR, and $\overline{INT_1}$

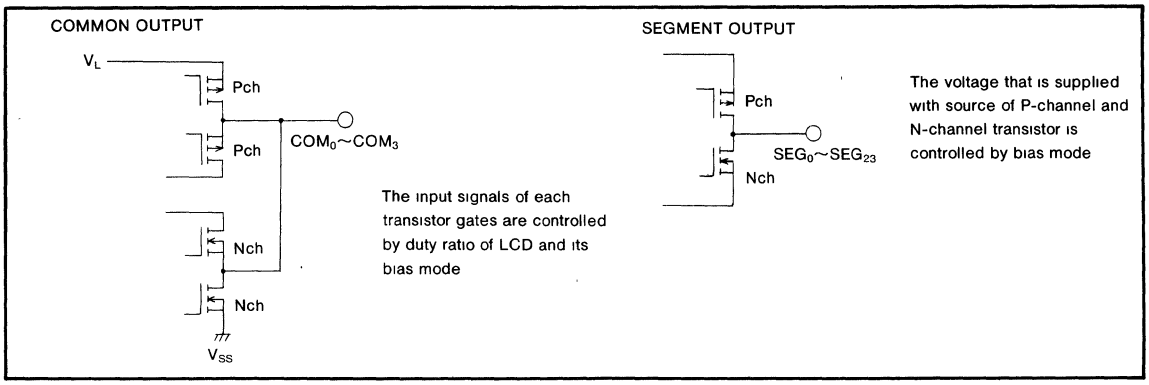


Fig.26 Block diagram of COM, SEG

CLOCK GENERATING CIRCUIT

The M37415M4-XXXFP has two internal clock generating circuit. Figure 29 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of LCD mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 27 shows a circuit example using a ceramic (or cystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 28.

The M37415M4-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enablb bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1 INT_2, key on wake up or serial I/O interrupt is received. The interrupt enaable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" unitil timer 2 overflows and is not supplied to the CPU.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) the microcomputer receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power disspation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock. X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restaring. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 30 shows the transition states for the system clock.

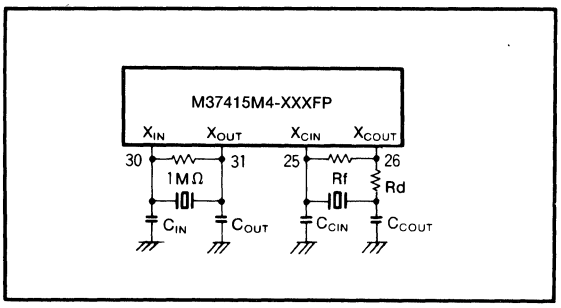


Fig.27 External ceramic resonator circuit

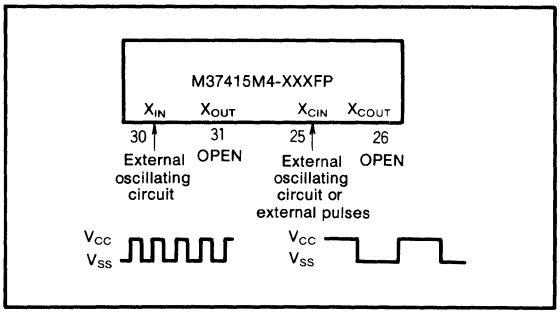


Fig.28 External clock input circuit

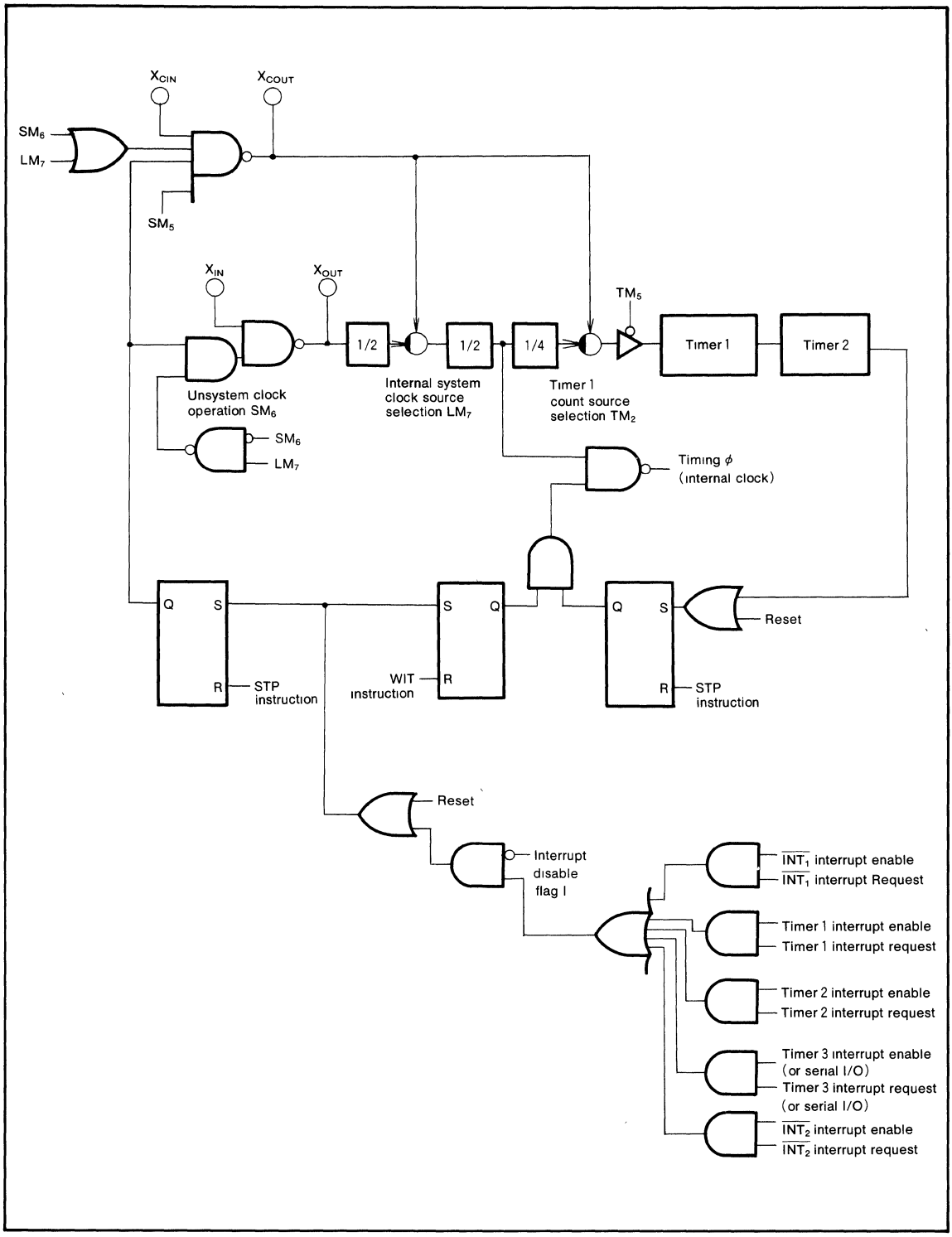
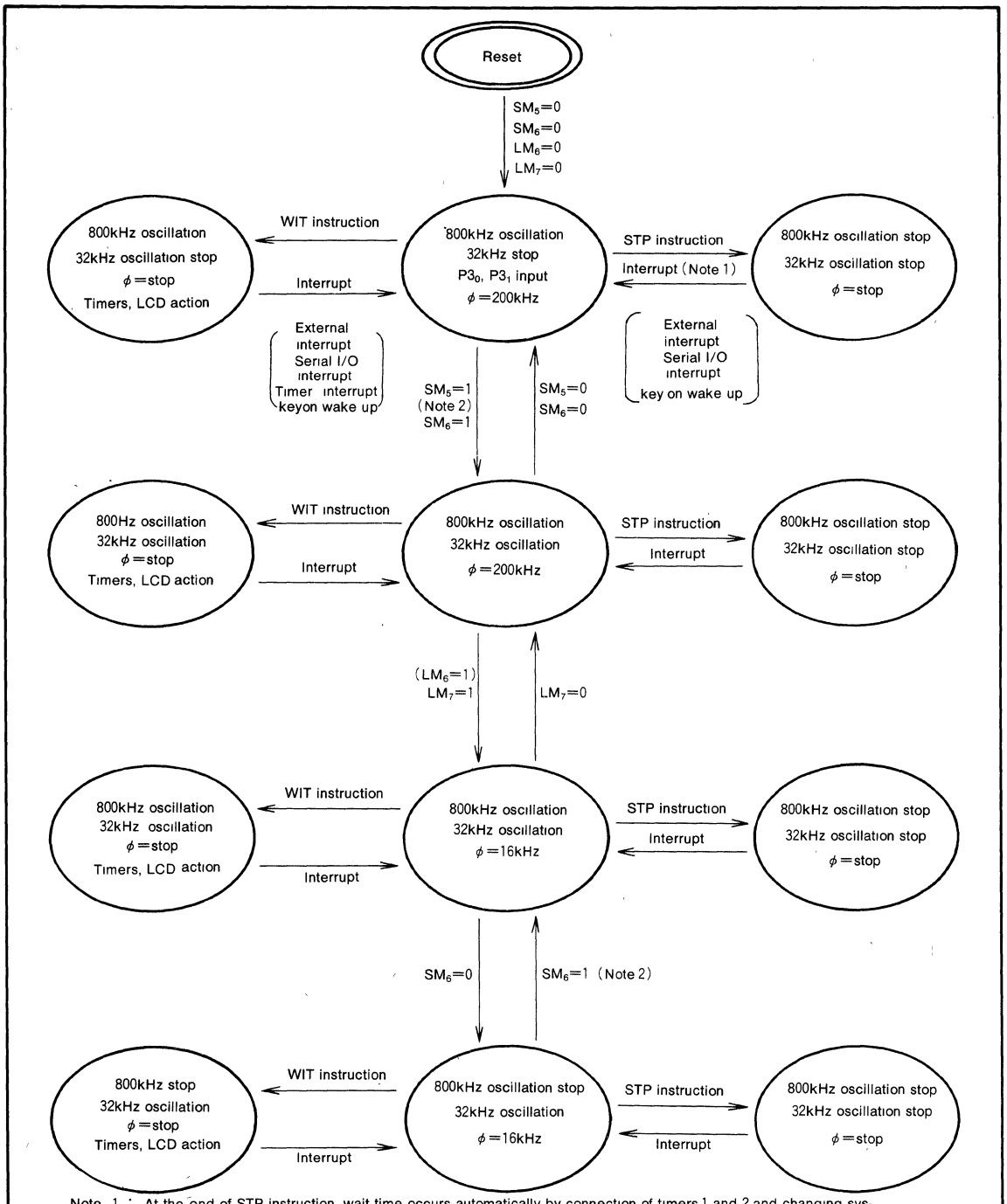


Fig.29 Block diagram of clock generating circuit



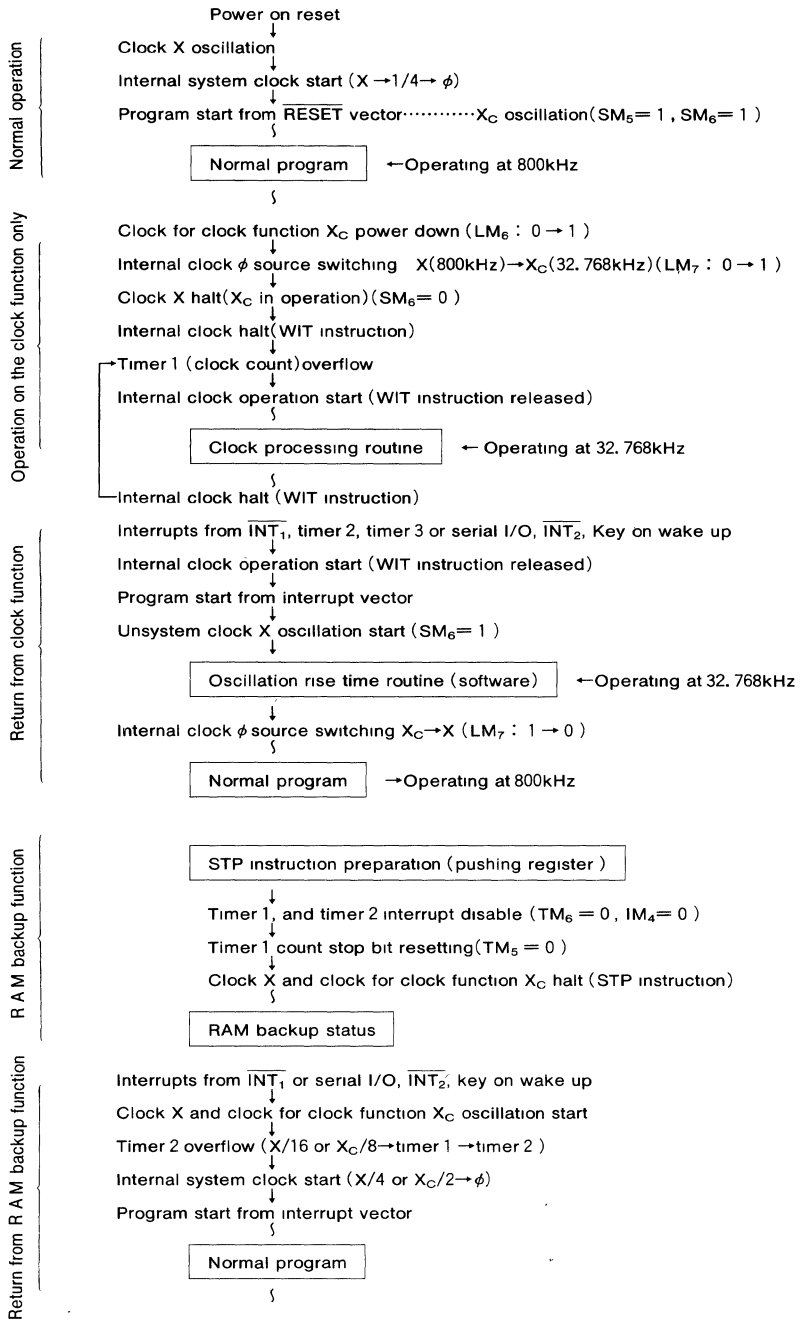
Note 1 : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.

2 : When $SM_6 = 1$ and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.

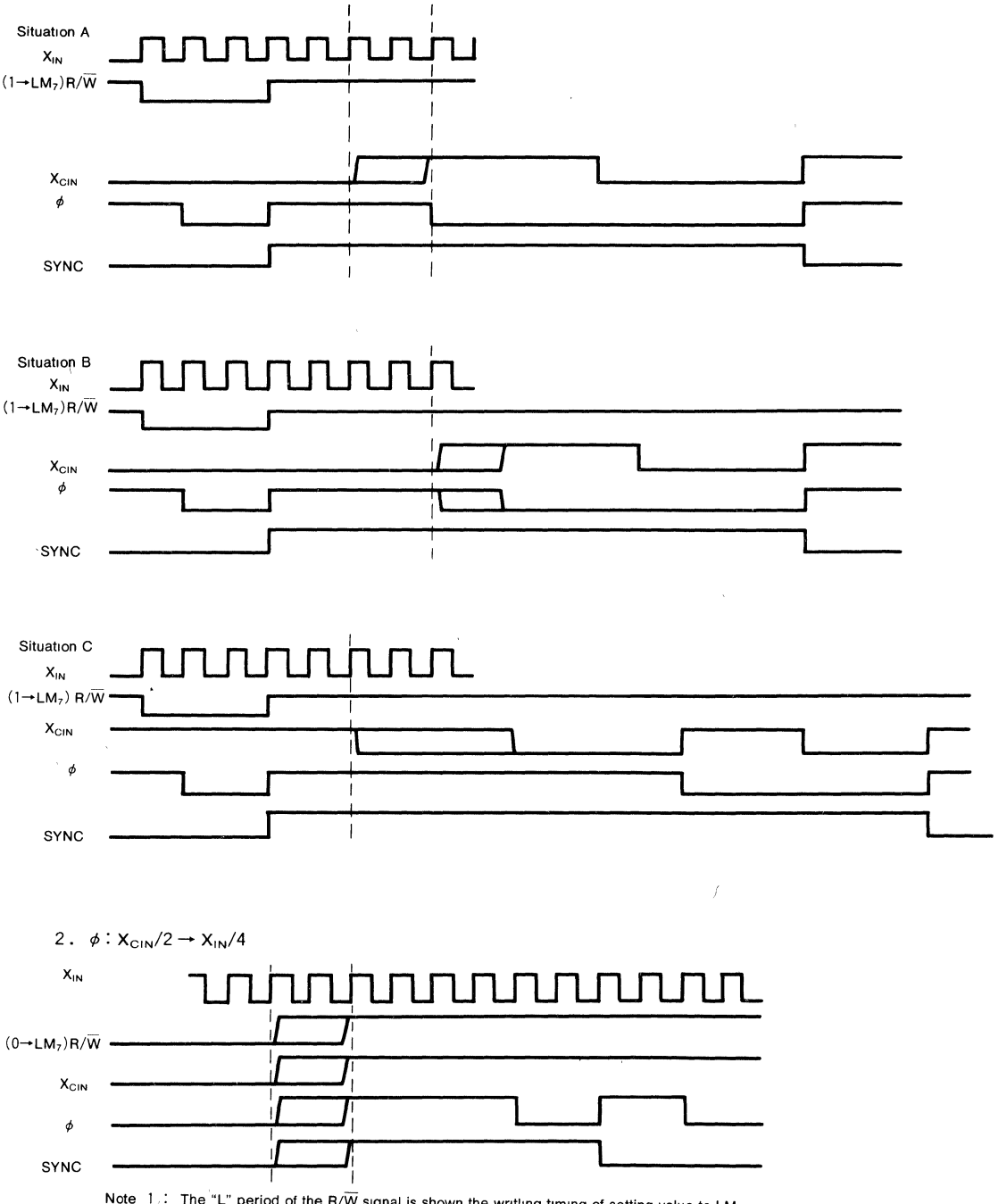
3 : The case of example clock X=800kHz, clock X_C=32kHz

Fig.30 External clock input circuit

≪An example of flow for system≫



1. ϕ : $X_{IN}/4 \rightarrow X_{CIN}/2$ (timing diagrams are shown situation A~C, because there are three kinds of waveform by the timing)



2. ϕ : $X_{CIN}/2 \rightarrow X_{IN}/4$

Note 1. : The "L" period of the R/$\overline{W}$ signal is shown the writing timing of setting value to LM_7
2 : The delay of timing is ignored

Fig.31 Timing diagram of the changing system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modifications are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(8) Notes on controlling the clock generation circuit
① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM_7 to "1" after oscillation is stable by the software in side of clock X_C.
② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM_7 to "0" after oscillation is stable by the software in side of clock X.
③ When SM_5 is "0" or when LM_7 is "0" and SM_6 is "0", LM_6 is automatically set to "0" by the hardware.
④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set SM_5 to "0".

Just for reference, timing diagram of the changing system clock are shown in Figure 31.

(9) In order to avoid noise and latch-up, connect the following external circuit.
① Connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.
② Connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{REF} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation from

(2) mark specification from

(3) ROM data ..... EPROM 3 sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit (see the confirmation form)
- Port P1 pull-up transistor bit (see the confirmation form)
- Port P2 pull-up transistor bit (see the confirmation form)
- Port P3 pull-up transistor bit (see the confirmation form)
- Port $P3_5/S_{OUT}$ output type (see the confirmation form)
- CNTR pin pull up transistor (see the confirmation form)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3∼7	V
V_I	Input voltage for LCD V_L		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, SEG_{24}∼SEG_{31}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}, V_{REF}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
P_d	Power dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7∼5.5V, V_{SS} = 0V, T_a = −10∼70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage(Note 1)	f(X_{IN})=3.2MHz	4.5		5.5	V
		f(X_{IN})=800kHz	2.5		5.5	
V_{SS}	Supply voltage			0		V
V_{REF}	Supply voltage for DTMF	R_L≧20kΩ	1.5		V_{CC}−0.5	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$(Note 2), $P3_3$∼$P3_7$(Note 3), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$(Note 4), $\overline{INT_1}$, CNTR		0.74V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$(Note 2), $P3_3$∼$P3_7$(Note 3), $P4_0$∼$P4_7$, CNV_{SS}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$(Note 4), $\overline{INT_1}$, CNTR		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$(Note 5), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 7)				5	mA
f(X_{IN})	Clock oscillating frequency(Note 8)	V_{CC}=4.5∼5.5V	380		3300	kHz
		V_{CC}=2.5∼5.5V	380		1000	
f(X_{CIN})	Clock oscillating frequency for clock function		32		50	kHz

Note 1 : When only maintaining the RAM data minimum value of V_{CC} is 2V
2 : When using port $P3_1$ as X_{CIN}, 0.85V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.15V_{CC} for port $P3_1$
3 : In this case of using port $P3_6$ as normal input.
4 : In this case of using port $P3_6$ as CLK input Especially when the input oscillation frequency is more than 50kHz, recommend the following : 0.8V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.2V_{CC}.
5 : The total of I_{OH} of port P0, P1, P2, P3, X_{OUT} should be 35mA max
6 : The total of $I_{OL(peak)}$ of port P0, P1, P2, P3 should be 55mA max, and the total of $I_{OL(peak)}$ of port P3, CNTR and X_{OUT} should be 45mA max
7 : $I_{OL(avg)}$ is the average current in 100ms
8 : When using DTMF function, f(X_{IN}) should be 400kHz, 800kHz, 1.6MHz, or 3.2MHz

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ (Note 1) (Note 2)	V_{CC}=5V, I_{OH}=−2mA		3			V
		V_{CC}=3V, I_{OH}=−0.7mA		2			
V_{OH}	"H" output voltage X_{OUT}	V_{CC}=5V, I_{OH}=−1.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ (Note 2), CNTR	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}	V_{CC}=5V, I_{OL}=1.5mA				2	V
		V_{CC}=3V, I_{OL}=0.3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, CNTR	V_{CC}=5V		0.25		1	V
		V_{CC}=3V		0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.4		
$V_{T+}-V_{T-}$	Hysteresis $P3_1$	When used as X_{CIN} input	V_{CC}=5V		0.7		V
			V_{CC}=3V		0.5		
$V_{T+}-V_{T-}$	Hysteresis $P2_0$~$P2_7$, $P3_2$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.4		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.35		
I_{IL}	"L" input current SEG_{24}~SEG_{31} (Except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$} Without pull-up Tr $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=0V				−5	μA
		V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR} With pull-up Tr	V_{CC}=5V, V_I=0V		−30	−70	−140	μA
		V_{CC}=3V, V_I=0V		−6	−25	−45	
I_{IL}	"L" input current SEG_{24}~SEG_{31} (at reset state)	V_{CC}=5V, V_L=5V, V_I=0V		−30		−140	μA
		V_{CC}=3V, V_L=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current SEG_{24}~SEG_{31} (Except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current SEG_{24}~SEG_{31} (at reset state)	V_{CC}=5V, V_L=5V, V_I=5V				5	μA
		V_{CC}=3V, V_L=3V, V_I=3V				4	
I_{CC}	Supply current (Output pins are opened $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are connected to V_{CC}. Except the above pins are connected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions)	At operation: $f(X_{IN})$=3.2MHz, V_{CC}=5V	at DTMF wave form output		4	8	mA
			at DTMF wave form stop		3	6	
		At operation: $f(X_{IN})$=800kHz, V_{CC}=3V	at DTMF wave form output		0.8	1.5	
			at DTMF wave form stop		0.5	1.0	
		At operation: T_a=25℃, X_{IN}=0V, $f(X_{CIN})$=32.8kHz, at low power mode (LM6=1)	V_{CC}=5V		45		μA
			V_{CC}=3V		18		
		At wait state: $f(X_{IN})$=3.2MHz, V_{CC}=5V			1		mA
		At wait state: $f(X_{IN})$=800kHz, V_{CC}=3V			0.3		
		At wait state: T_a=25℃, X_{IN}=0V, $f(X_{CIN})$=32.8kHz, at low power mode (LM6=1)	V_{CC}=5V		20	60	μA
			V_{CC}=3V		4	12	
		At stop state: $f(X_{IN})$=0, $f(X_{CIN})$=0, V_{CC}=5V	T_a=25℃		0.1	1	
			T_a=70℃			10	
I_L	V_L current	V_{CC}=V_L=5V, 1/3 bias			10	25	μA
		V_{CC}=V_L=3V, 1/3 bias			6	15	
I_{REF}	V_{REF} current	V_{CC}=5V, V_{REF}=4.5V			100	200	μA
		V_{CC}=3V, V_{REF}=2.5V			60	120	
V_{RAM}	RAM retention voltage	$f(X_{IN})$=0, $f(X_{CIN})$=0		2		5.5	V

Note 1 : Except when the output type of $P3_5$ is N-channel open drain (mask option)
2 : If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above

DTMF CHARACTERISTICS (V_{SS} = 0V, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max.	
V_{OT}	Output voltage T_{one}	High frequency band group	V_{CC}=5V, V_{REF}=4.5V, R_L=20kΩ	470	490	510	mVrms
			V_{CC}=3V, V_{REF}=2.5V, R_L=20kΩ	257	270	283	
		Low frequency band group	V_{CC}=5V, V_{REF}=4.5V, R_L=20kΩ	325	345	365	
			V_{CC}=3V, V_{REF}=2.5V, R_L=20kΩ	177	190	203	
dB_{CR}	Output ratio of high frequency band to low frequency band		R_L=20kΩ	2.5	3	3.5	dB
DIS	Disportional percentage		R_L=20kΩ, T_a=25℃		13		%