M37250M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37250M6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs and VCRs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

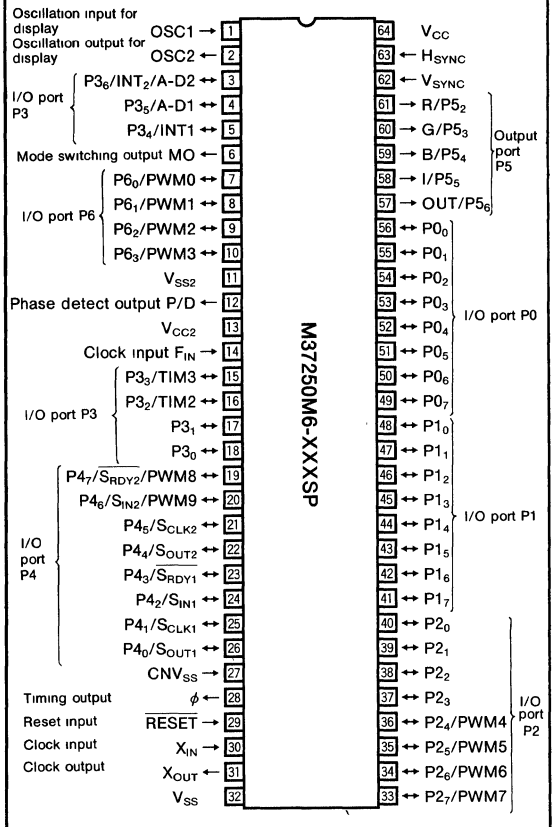
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 24576 bytes
  RAM ..... 384 bytes
- Instruction execution time
  ..... 1μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V$\pm$10%
- Power dissipation
  Normal operation mode (at 4MHz frequency)
  ..... 137.5mW (V_{CC}=5.5V, CRT display, PLL operating)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt 15types, 15vectors
- 8-bit timer 6
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4, P6) 43
- Output port (Port P5) 5
- PLL function
  Programmable divider 14-bit
  Swallow counter 5-bit
- Serial I/O (8-bit) 2
- Special serial I/O for master transfer* 1
- PWM function ..... 8-bit$\times$10
- A-D converter (4-bit resolution) ..... 2 channels
- 72-character on screen display function
  Number of character ..... 24 characters$\times$3 lines
  Kinds of character 126

APPLICATION

TV, VCR

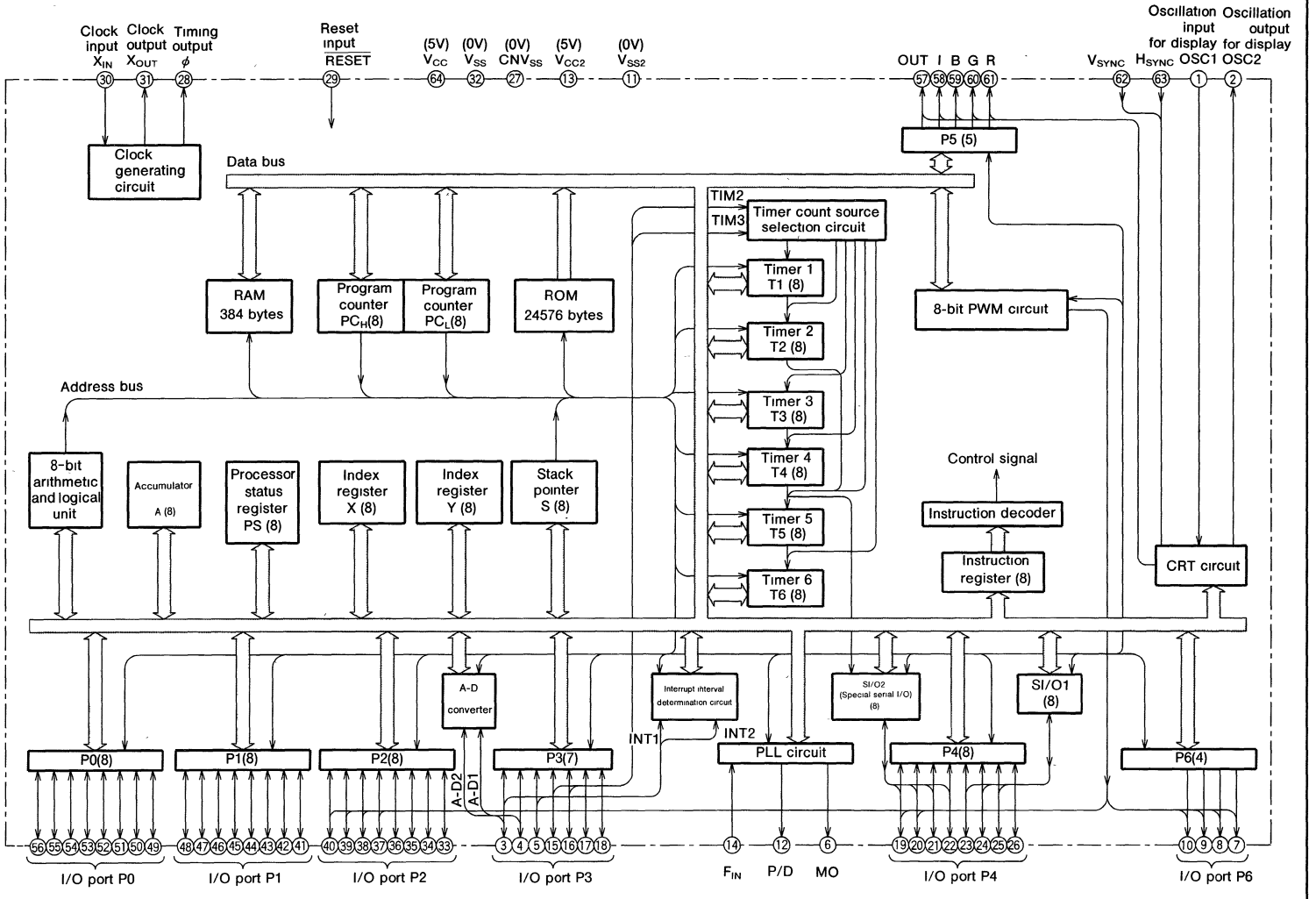
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

* : Purchase of Mitsubishi Electric Corporation's I^{2}C components converys a license under the Philips I^{2}C Patent Rights to use these components in an I^{2}C system, provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

M37250M6-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS OF M37250M6-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		24576 bytes
	RAM		384 bytes
Input/Output ports	P0, P1	I/O	8-bit×2 (CMOS output)
	P2	I/O	8-bit×1 (CMOS output, can be used as PWM output pins)
	$P3_0$, $P3_1$	I/O	2-bit×1 (CMOS output)
	$P3_2$ to $P3_6$	I/O	5-bit×1 (CMOS output, can be used as timer input pins, INT1, INT2 input pins and A-D input pins)
	P4	I/O	8-bit×1 (CMOS output, can be used as serial I/O function pins and PWM output pins)
	P5	Output	5-bit×1 (N-channel open drain output, can be used as R, G, B, I, OUT pins)
	P6	I/O	4-bit×1 (N-channel open drain output, can be used as PWM output pins)
Serial I/O			8-bit×2 (Special serial I/O (8-bit)×1)
Timers			8-bit timer×6
PLL function			Fixed dividing mode and swallow mode can be selected
Subroutine nesting			96 levels (max.)
Interrupt			Three external interrupts, ten internal interrupts, one software interrupt
Clock generating circuit			One built-in circuits (externally connected quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at CRT display ON and PLL operating		137.5mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at CRT display OFF and PLL stopped		55mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at wait mode		4mW (V_{CC}=5V, Max.)
	at stop mode		0.05mW (V_{CC}=5V, Max.)
Input/Output characteristics	Input/Output voltage		12V (Port $P4_6$, $P4_7$, $P6_0$ to $P6_3$)
	Output current		10mA (Port $P2_4$ to $P2_7$)
Operating temperature range			−10 to 70°C
Device structure			CMOS silicon gate process
Package			64-pin shrink plastic molded DIP
CRT display function	Number of character		24 characters×3 lines (maximum 16 lines by software)
	Kinds of character		126 (12×16 dots)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{CC2}, V_{SS}, V_{SS2}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and V_{CC2}, and 0V to V_{SS} and V_{SS2}
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
$P0_0$ to $P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$ to $P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
$P2_0$ to $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 $P2_4$ to $P2_7$ are in common with PWM output port of PWM4 to PWM7
$P3_0$ to $P3_6$	I/O port P3	I/O	Port P3 is an 7-bit I/O port and has basically the same functions as port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output and the output structure of $P3_2$ to $P3_6$ is N-channel open drain $P3_2$, $P3_3$ are in common with external clock input pins of timer 1, 2 and 3 $P3_4$, $P3_6$ are in common with external interrupt input pins INT1 and INT2. $P3_5$, $P3_6$ are in common with analog input pins of A-D converter (A-D1, A-D2)
$P4_0$ to $P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain When serial I/O1 is used,$P4_0$, $P4_1$, $P4_2$ and $P4_3$ work as S_{OUT1}, S_{CLK1}, S_{IN1} and $\overline{S_{RDY1}}$ pins, respectively When serial I/O2 is used, $P4_4$, $P4_5$, $P4_6$ and $P4_7$ work as S_{OUT2}, S_{CLK2}, S_{IN2} and $\overline{S_{RDY2}}$ pins, respectively Also $P4_6$, $P4_7$ are in common with PWM output pins of PWM 8 and 9
OSC1,	Clock input for CRT display	Input	This is the I/O pins of the clock generating circuit for the CRT display function
OSC2	Clock output for CRT display	Output	
H_{SYNC}	H_{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display
V_{SYNC}	V_{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
R, G, B, I, OUT	CRT output	Output	This is an 5-bit output pin for CRT display The output structure is CMOS output This is in common with port $P5_2$ to $P5_6$
$P6_0$ to $P6_3$	I/O port P6	I/O	Port P6 is an 4-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain This port is in common with PWM output pins PWM0 to PWM3
MO	Mode switching output	Output	This pin outputs the mode switching signal of prescaler When fixed dividing mode is selected, this pin can be used as 1-bit output port
P/D	Phase detect output	Output	The phase detector output level is set to "H" when the phase is leading the reference frequency, set to "L" when lagging, and set to the floating state when in-phase
F_{IN}	Clock input	Input	This pin inputs clock from the prescaler

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37250 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

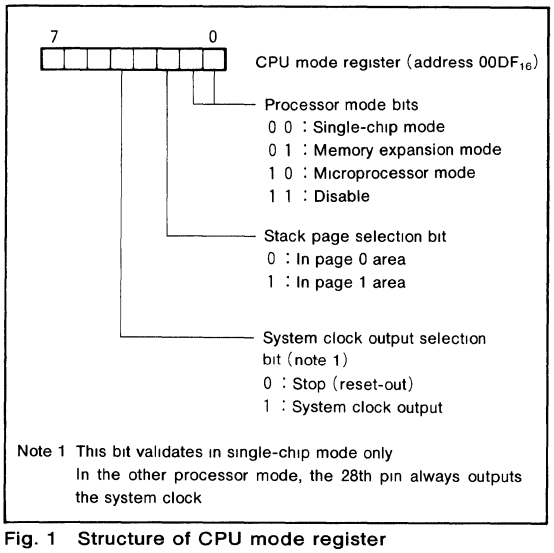


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

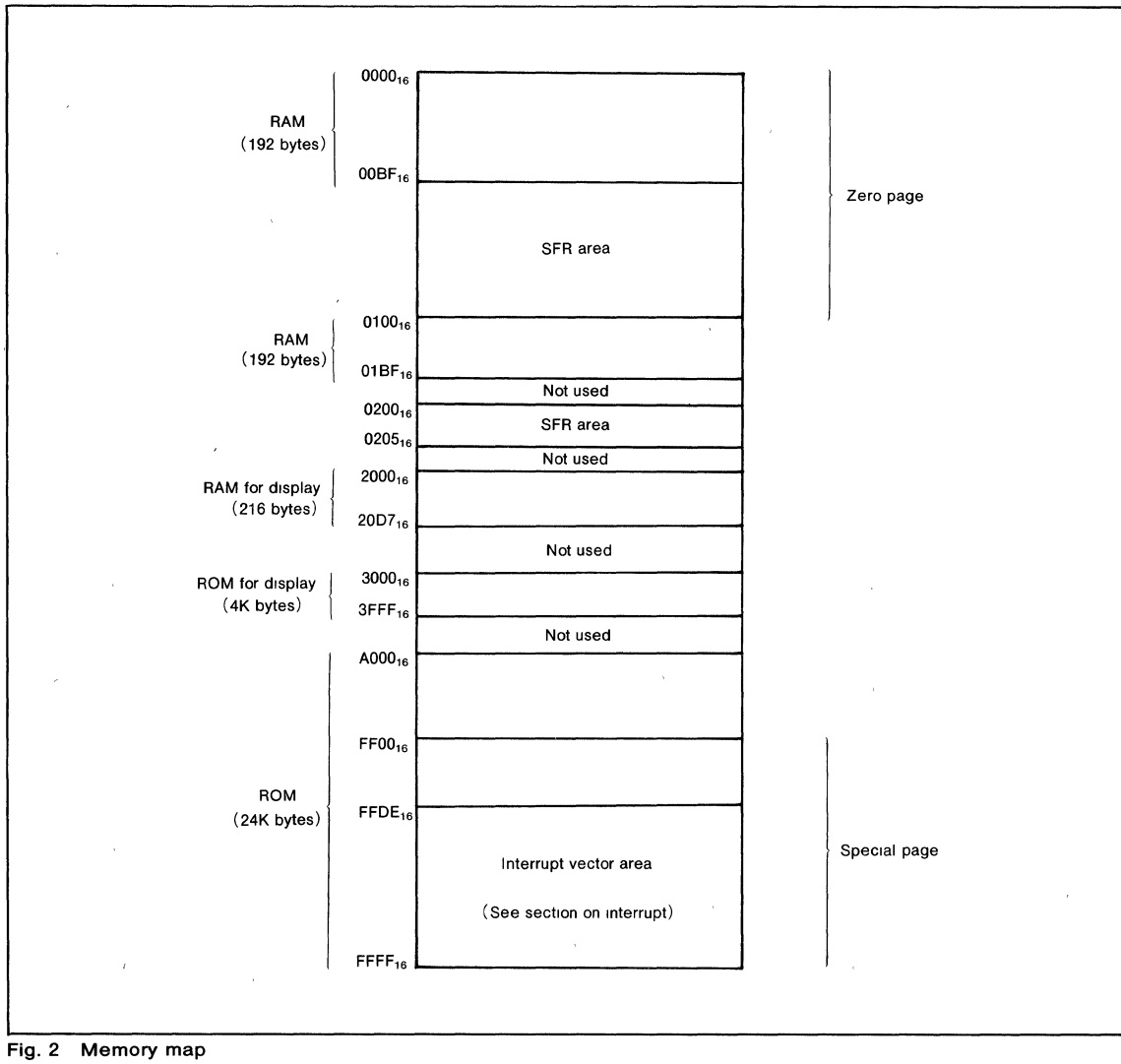


Fig. 2 Memory map

MITSUBISHI ELECTRIC

$00C0_{16}$	Port P0
$00C1_{16}$	Port P0 direction register
$00C2_{16}$	Port P1
$00C3_{16}$	Port P1 direction register
$00C4_{16}$	Port P2
$00C5_{16}$	Port P2 direction register
$00C6_{16}$	Port P3
$00C7_{16}$	Port P3 direction register
$00C8_{16}$	Port P4
$00C9_{16}$	Port P4 direction register
$00CA_{16}$	Port P5
$00CB_{16}$	Port P5 direction register
$00CC_{16}$	Port P6
$00CD_{16}$	Port P6 direction register
$00CE_{16}$	
$00CF_{16}$	
$00D0_{16}$	PWM 0 register
$00D1_{16}$	PWM 1 register
$00D2_{16}$	PWM 2 register
$00D3_{16}$	PWM 3 register
$00D4_{16}$	PWM 4 register
$00D5_{16}$	PWM output control register 1
$00D6_{16}$	PWM output control register 2
$00D7_{16}$	Interrupt interval determination register
$00D8_{16}$	Interrupt interval determination control register
$00D9_{16}$	Special serial I/O register
$00DA_{16}$	Special mode register 1
$00DB_{16}$	Special mode register 2
$00DC_{16}$	Serial I/O1 mode register
$00DD_{16}$	Serial I/O1 register
$00DE_{16}$	Serial I/O2 mode register
$00DF_{16}$	Serial I/O2 register
$00E0_{16}$	Horizontal position register
$00E1_{16}$	Vertical display start position register 1
$00E2_{16}$	Vertical display start position register 2
$00E3_{16}$	Vertical display start position register 3
$00E4_{16}$	Character size register
$00E5_{16}$	Border selection register
$00E6_{16}$	Color register 0
$00E7_{16}$	Color register 1
$00E8_{16}$	Color register 2
$00E9_{16}$	Color register 3
$00EA_{16}$	CRT control register
$00EB_{16}$	Display block counter
$00EC_{16}$	CRT port control register
$00ED_{16}$	
$00EE_{16}$	
$00EF_{16}$	A-D control register

$00F0_{16}$	Timer 1
$00F1_{16}$	Timer 2
$00F2_{16}$	Timer 3
$00F3_{16}$	Timer 4
$00F4_{16}$	Timer mode register 1
$00F5_{16}$	Timer mode register 2
$00F6_{16}$	PWM 5 register
$00F7_{16}$	PWM 6 register
$00F8_{16}$	PWM 7 register
$00F9_{16}$	PWM 8 register
$00FA_{16}$	PWM 9 register
$00FB_{16}$	CPU mode register
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2
0100_{16}	RAM 192 bytes
$01BF_{16}$	
$01C0_{16}$	Not used
$01FF_{16}$	
0200_{16}	PLL control register
0201_{16}	PCH register
0202_{16}	PCL register
0203_{16}	SWC register
0204_{16}	Timer 5
0205_{16}	Timer 6

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 14 different events consisting of three external, ten internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1, 2, interrupt control registers 1, and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0" The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT2 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	
INT1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	
Serial I/O2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 4 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
1 ms interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
V_{SYNC} interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 2 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
Timer 1 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O1 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	
Timer 5 interrupt	13	$FFE7_{16}$, $FFE6_{16}$	
Timer 6 interrupt	14	$FFE5_{16}$, $FFE4_{16}$	
BRK instruction interrupt	15	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

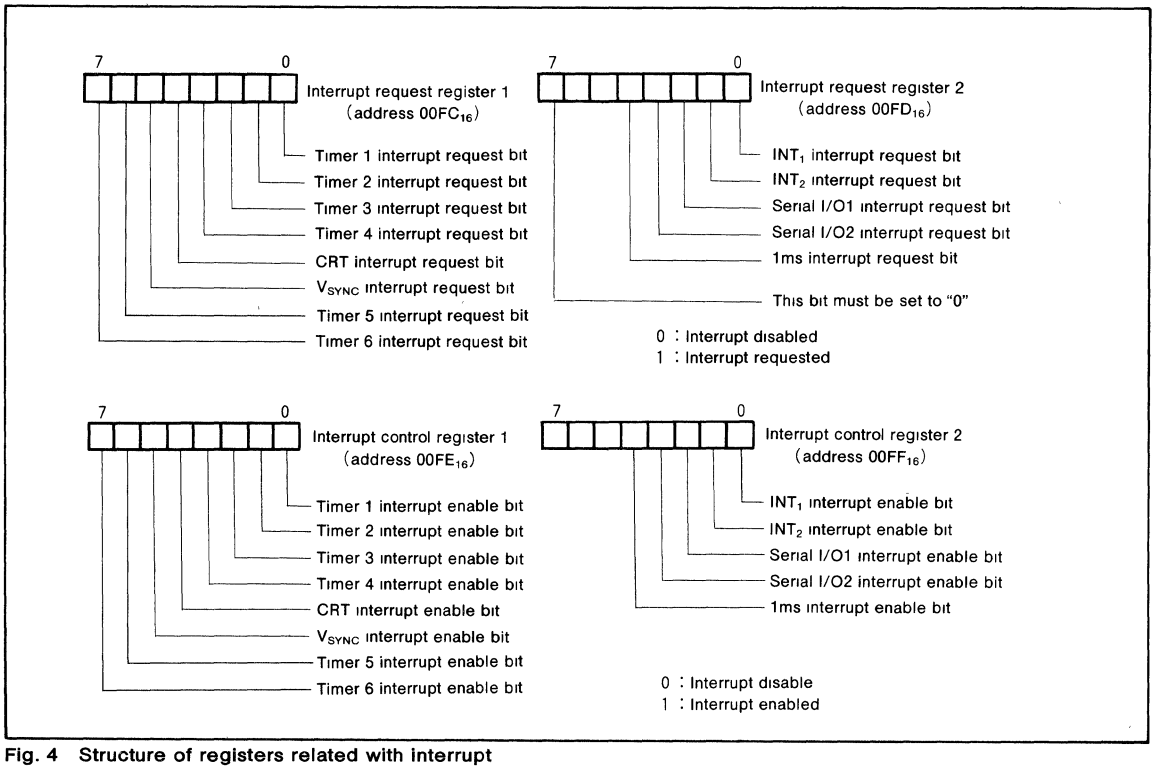


Fig. 4 Structure of registers related with interrupt

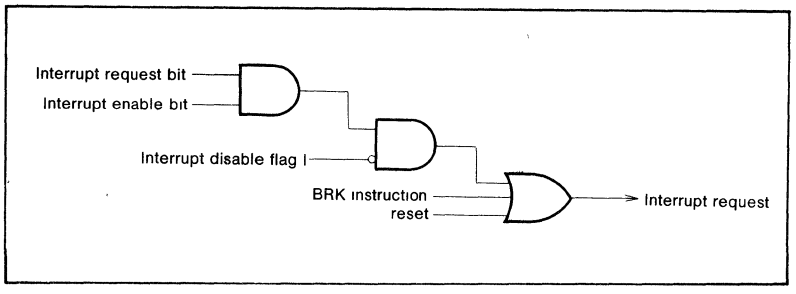


Fig. 5 Interrupt control

TIMER

The M37250M6-XXXSP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer 1 through 6 is shown in Figure 7.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "00_{16}" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch. The timer interrupt request bit is set at the next count pulse after the timer reaches "00_{16}".

(1) Timer 1

The count source of timer 1 is selectable from $f(X_{IN})/16$ and the 1,024μ second clock (by 1ms interrupt; it can be used at PWM count source generating) and external clock from $P3_2$/TIM2 pin by timer mode register 1 (address $00F4_{16}$).

Timer 1 interrupt request is occurred by overflow of timer 1.

(2) Timer 2

The count source of timer 2 is selectable from $f(X_{IN})/16$, timer 1 overflow signal, and external clock from $P3_2$/TIM2 pin by timer mode register 1 (address $00F4_{16}$).

Timer 1 can be used as 8 bits prescaler when timer 1 overflow signal is selected as count source of timer 2.

Timer 2 interrupt request is occurred by overflow of timer 2.

(3) Timer 3

The count source of timer 3 is selectable from $f(X_{IN})/16$ and external clock from $P3_3$/TIM3 pin by timer mode register 2 (address $00F5_{16}$).

Timer 3 interrupt request is occurred by overflow of timer 3.

(4) Timer 4

The count source of timer 4 is selectable from $f(X_{IN})/16$, $f(X_{IN})/2$, and timer 3 overflow signal by timer mode register 2 (address $00F5_{16}$).

Timer 3 can be used as 8 bits prescaler when timer 3 overflow signal is selected as count source of timer 4.

Timer 4 interrupt request is occurred by overflow of timer 4.

(5) Timer 5

The count source of timer 5 is selectable from $f(X_{IN})/16$, timer 2 overflow signal and timer 4 overflow signal by timer mode register 1 (address $00F4_{16}$) and timer mode register 2 (address $00F5_{16}$).

(6) Timer 6

The count source of timer 6 is selectable from $f(X_{IN})/16$ and timer 5 overflow signal by timer mode register 1 (address $00F4_{16}$).

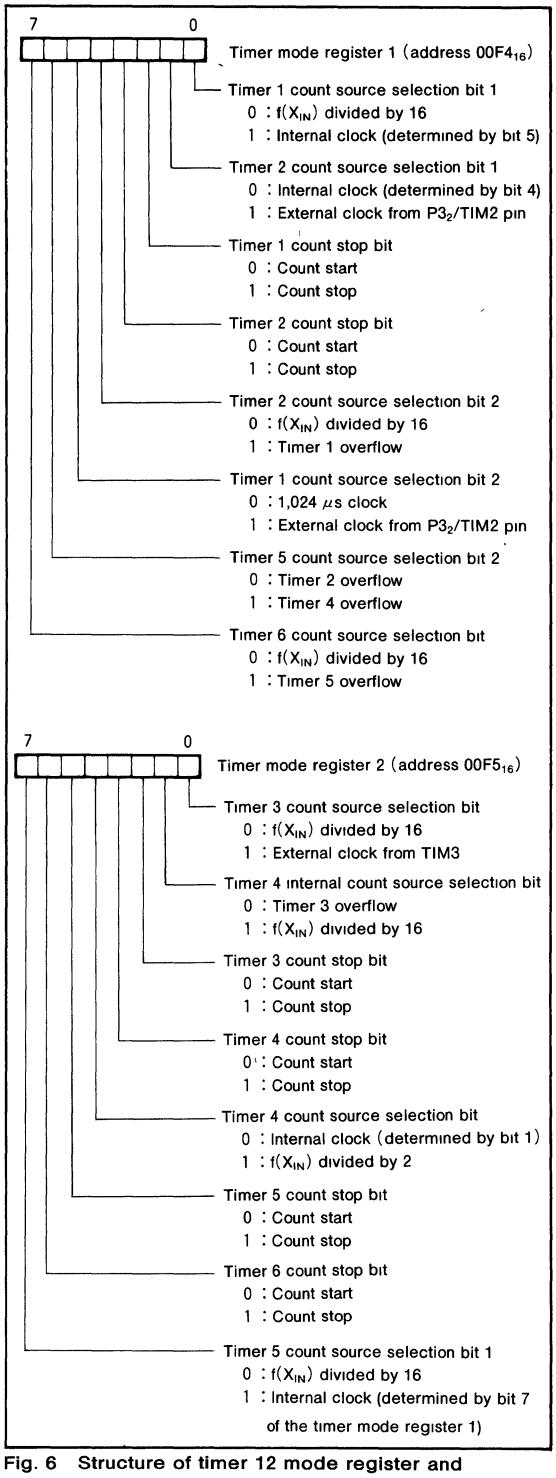


Fig. 6 Structure of timer 12 mode register and timer 34 mode register

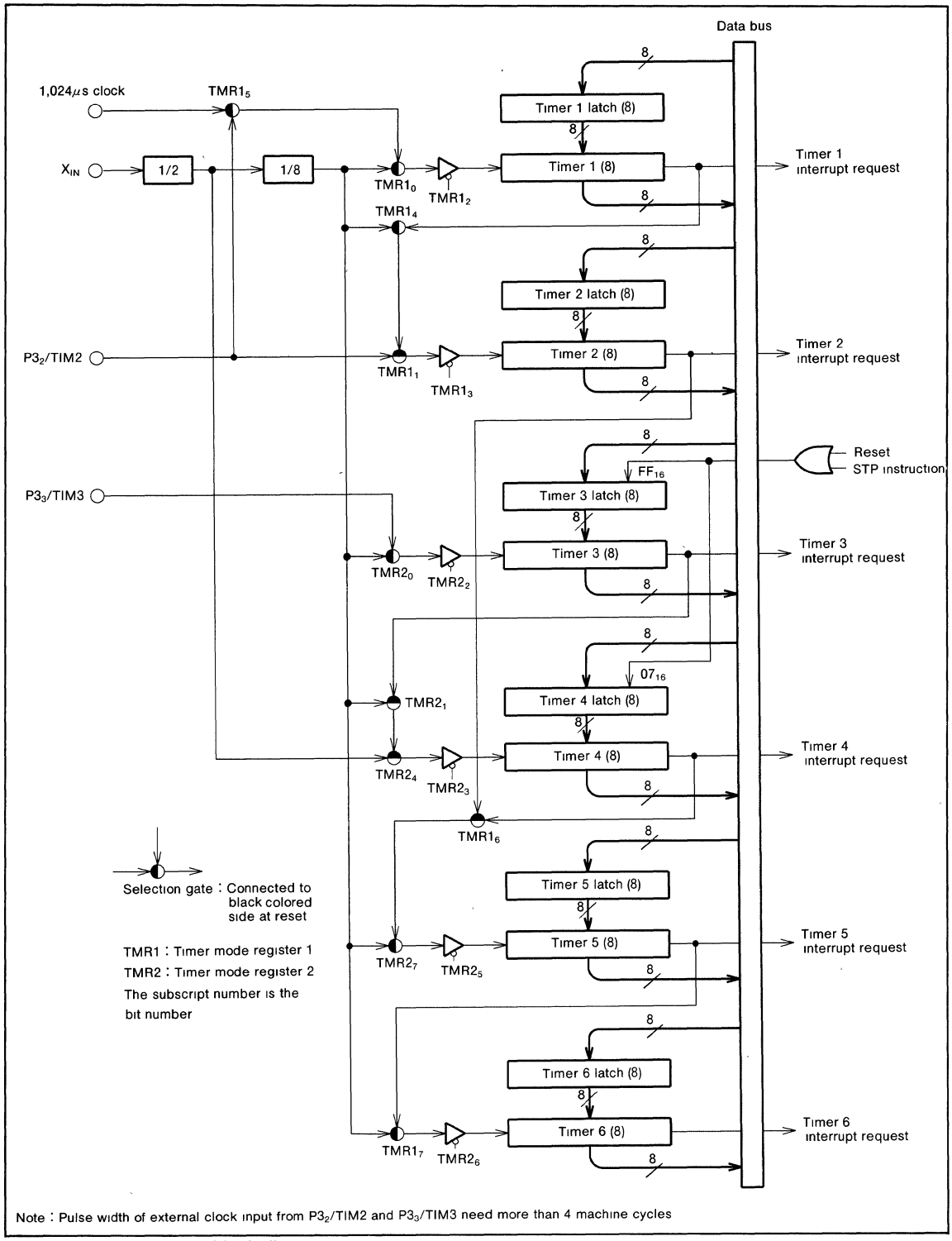


Fig. 7 Timer 1 through 6 block diagram

MITSUBISHI ELECTRIC

SERIAL I/O

M37250M6-XXXSP has two serial I/O (serial I/O1, serial I/O2). Serial I/O1 has the same function as serial I/O2.

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDYi}}$), synchronous input/output clock (CLK_i), and the serial I/O pins (S_{OUTi}, S_{INi}) are used as port P4. The serial I/O_i mode registers (address $00DC_{16}$, $00DE_{16}$) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use $P4_2$ or $P4_6$ as a serial input, set the direction register bit which corresponds to $P4_2$ or $P4_6$ to "0". For more information on the direction register, refer to the I/O pin section.

Also to use internal clock of serial I/O2, bit 1 of special mode register 1 (address $00DA_{16}$) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

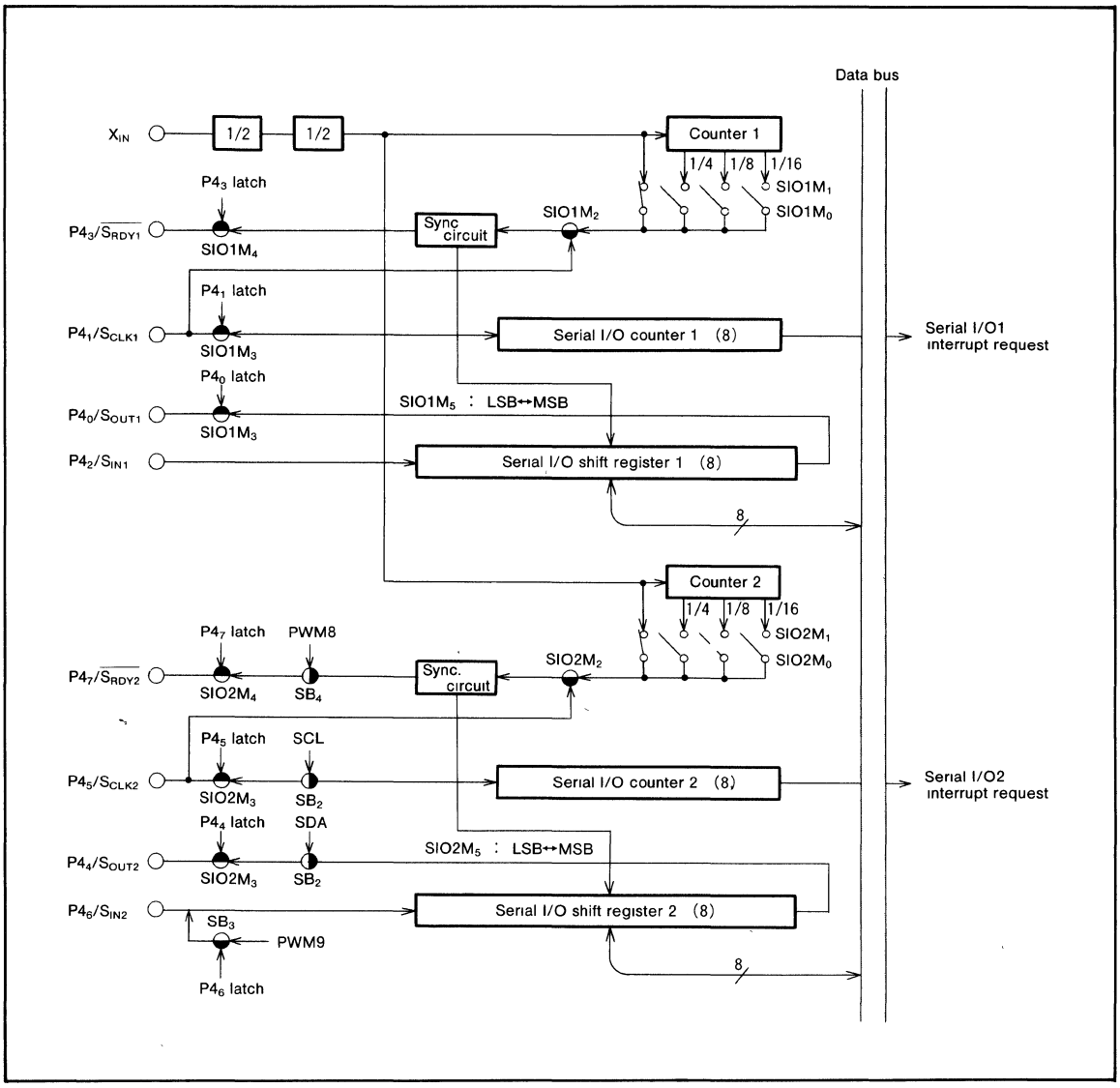


Fig. 8 Serial I/O block diagram

Internal clock — The $\overline{S_{RDYi}}$ signal becomes"H"during transmission or while dummy data is stored in the serial I/O_i register (address $00DD_{16}$, $00DF_{16}$). After the falling edge of the write signal, the $\overline{S_{RDYi}}$ signal becomes low signaling that the M37250M6-XXXSP is ready to receive the external serial data. The $\overline{S_{RDYi}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_i counter is set to 7 when data is stored in the serial I/O_i register. At each falling edge of the fransfer clock, serial data is output to S_{OUTi}. During the rising edge of this clock, data can be input from S_{INi} and the data in the serial I/O_i register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O_i mode register. After the transfer clock has counted 8 times, the serial I/O_i register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O_i counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37250M6-XXXSPs is shown in Figure 10.

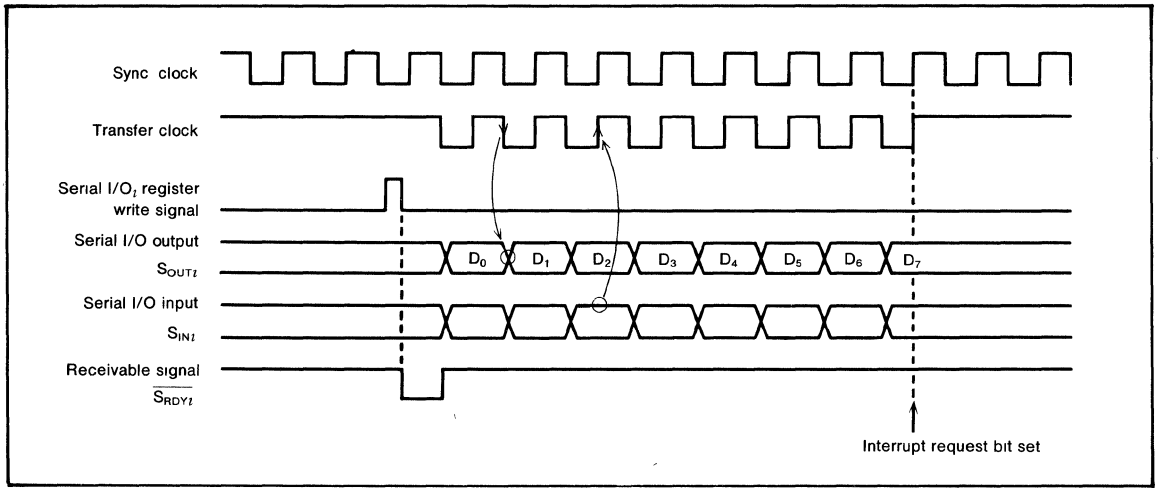


Fig. 9 Serial I/O timing

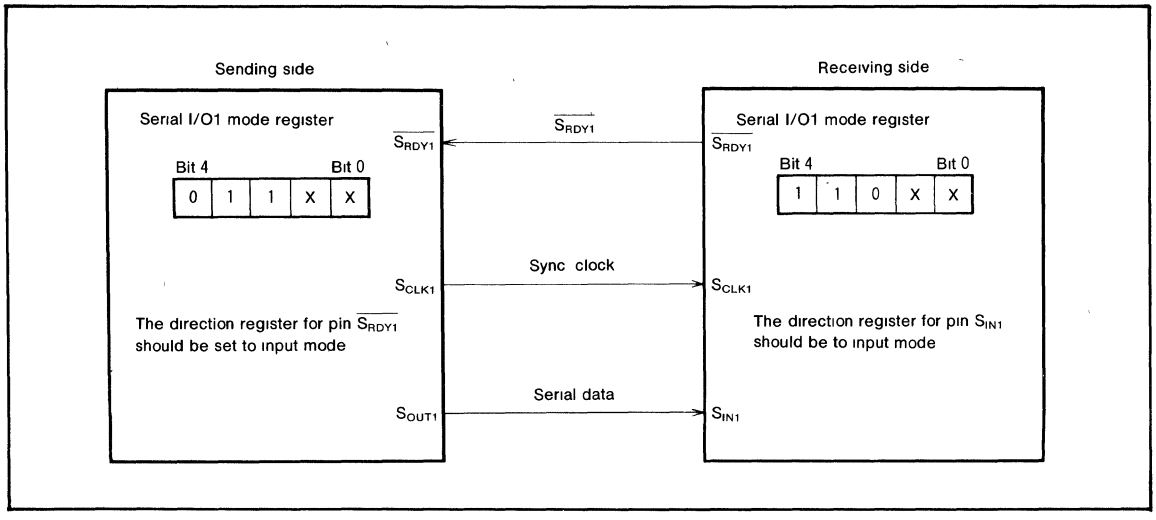


Fig. 10 Example of serial I/O connection

MITSUBISHI ELECTRIC

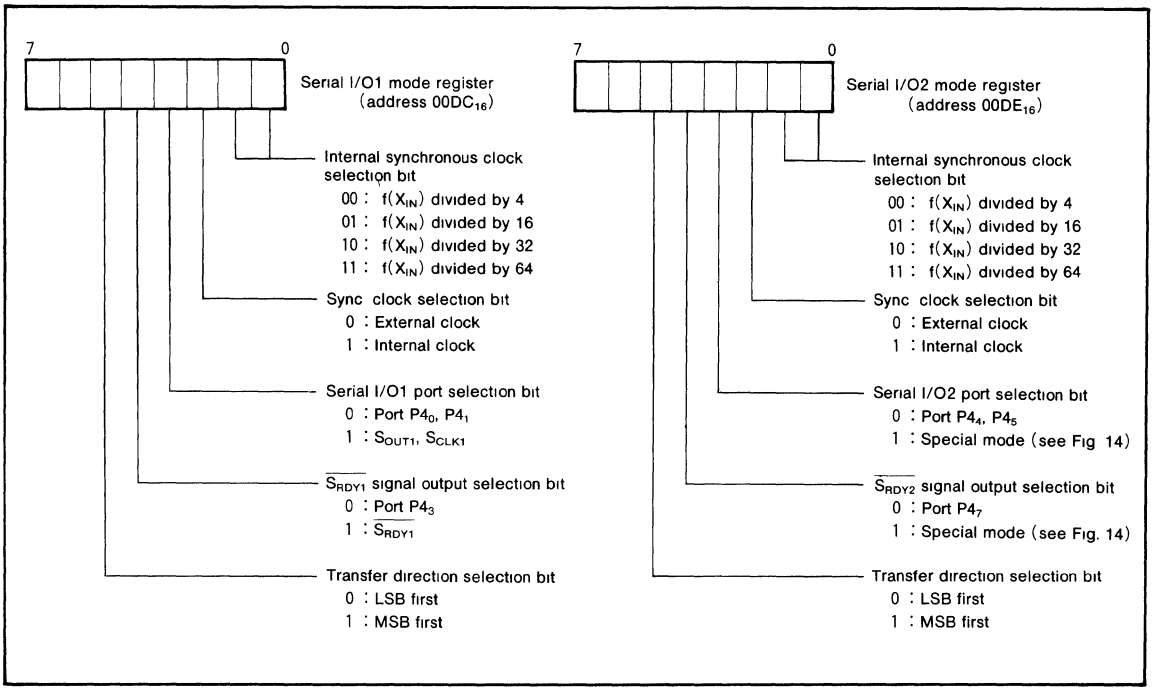


Fig. 11 Structure of serial I/O1 mode register and serial I/O2 mode register

SPECIAL MODE (I^2C BUS MODE)

M37250M6-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (Inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37250M6-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address $00DB_{16}$) to "1" so as to special serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address $00FF_{16}$) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports $P4_4$ and $P4_5$. Set all bits (bits 4 and 5) corresponding to $P4_4$ and $P4_5$ of the port P4 register (address $00C8_{16}$) and the port P4 direction register (address $00C9_{16}$) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and timer mode register 2. (For instance, if $f(X_{IN})/16$ is selected as the clock source of timer 4 and "4" is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address $00DB_{16}$). (Usually, "83_{16}".)

Set the bit 3 of serial I/O2 mode register (address $00DE_{16}$) to "1". After that set the special mode register 1 (address $00DA_{16}$). Figure 15 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O register (address $00D9_{16}$). Immediately after this, clear bits 0 and 1 of special mode regiser 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal.

Figure 13 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided (26_{16}) in the special mode register 1 (address $00DA_{16}$), and write "FF_{16}" in the special serial I/O register (address $00D9_{16}$). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 14 shows master reception timing.

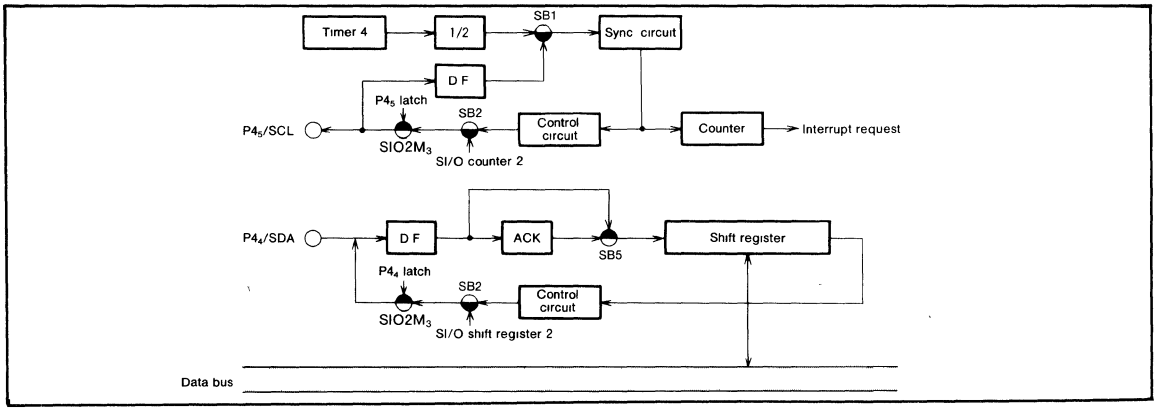


Fig. 12 Block diagram of special serial I/O

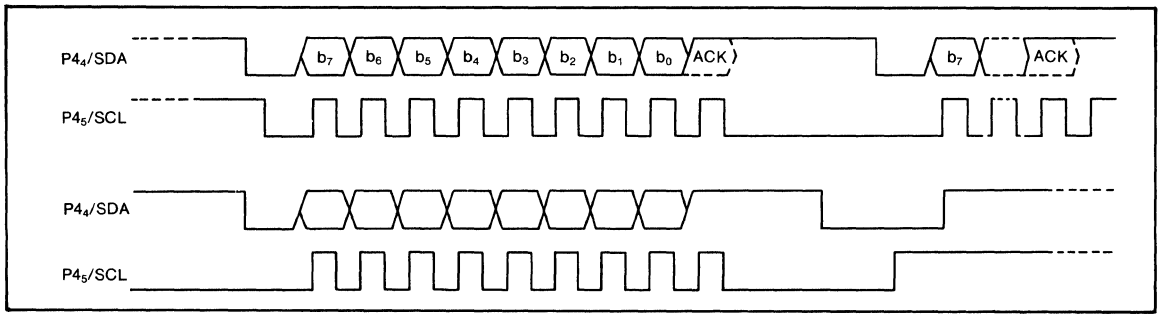


Fig. 13 Master transmission timing

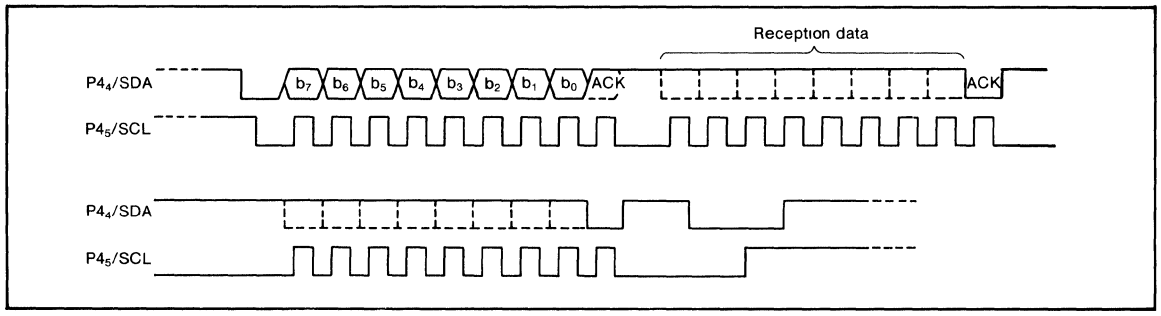


Fig. 14 Master reception timing

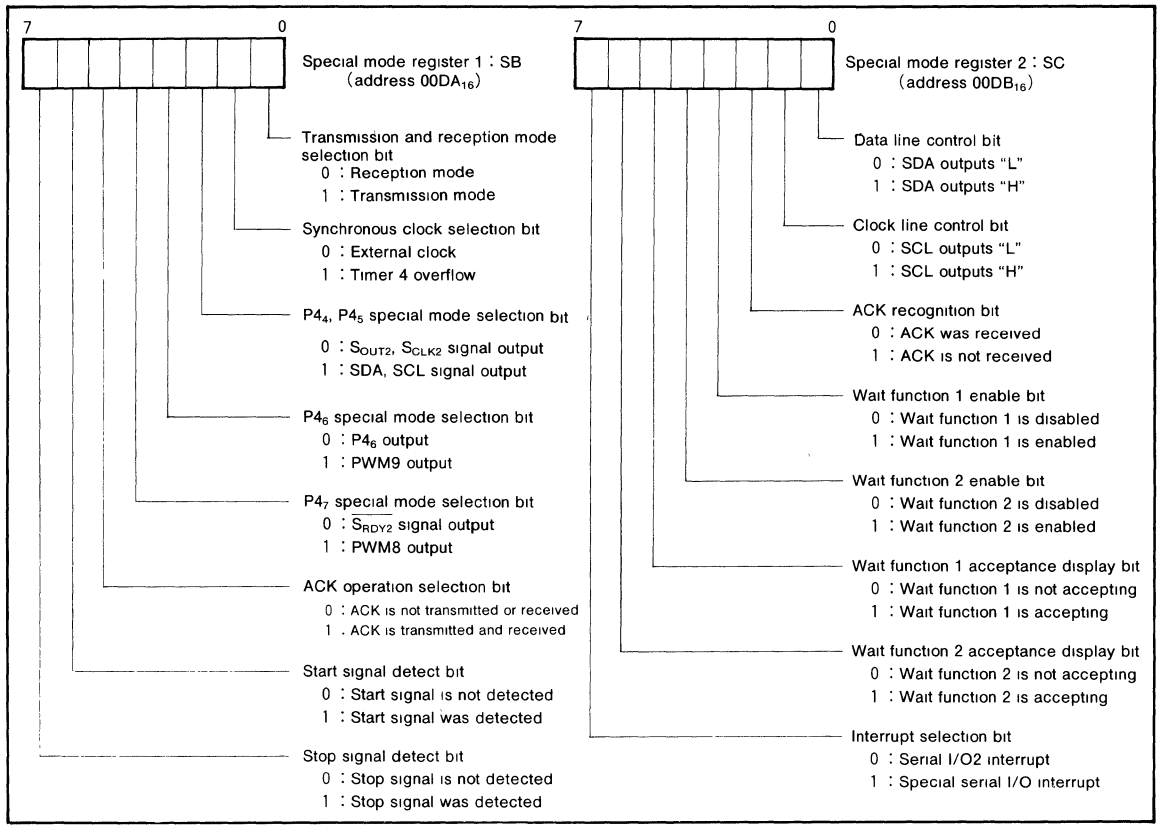


Fig. 15 Structure of special mode registers 1 and 2

(3) Wait function

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate. Reset the internal counter by writing data to the special serial I/O register (address $00D9_{16}$), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data tranfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1 : Clear the START signal detect bit (bit 6) and the STOP signal detect bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

PWM OUTPUT CIRCUIT

(1) Introduction

The M37250M6-XXXSP is equipped with ten 8-bit PWMs (PWM0~PWM9). PWM0 to PWM9 have a 8-bit resolution with minimum resolution bit width of 8μs (for X_{IN}=4MHz) and repeat period of 2048μs.

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to PWM0 to 9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

Set the 8-bit data for output in the PWM$_i$ register (i means 0 to 9; addresses $00D0_{16}$ to $00D4_{16}$ and $00F6_{16}$ to $00FA_{16}$).

(3) Transferring from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed.

(4) Operation of the PWMs

The following is the explain about PWM operation.

At first, clear the bit 0 of PWM output control register 1 (address $00D5_{16}$) to "0" (at reset, this bit already clear to "0" automatically), so that the PWM count source is supplyed.

PWM0 to 3 output pins and PWM4 to 7 output pins are in common with port P6 and port P2 respectively, and PWM8 and 9 output pins are in common with port P4 and serial I/O2 pins.

PWM0 to 7 are selected the pin function by setting of PWM output control register 1 (address $00D5_{16}$) and PWM output control register 2 (address $00D6_{16}$), and PWM8 and 9 are selected the pin function by the bit 3 and 4 of special mode register 1 (address $00DA_{16}$) and bit 4 of serial I/O2 mode register (address $00DE_{16}$). When these pins are set as PWM output pins by these registers, the PWM output can be performed.

Figure 17 shows the timing diagram of PWM0 through 9. One cycle (T) is composed of 256 (2^8) segments. There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one cycle in the circuit internal section. Refer Figure 17 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 17 (b).

Change in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. An length of entirely high-level output cannot be output, i. e. 256/256.

(5) Output after reset

At reset the output of port P2, P4, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, the contents of the latch is undefined until its data is transferred to the latch.

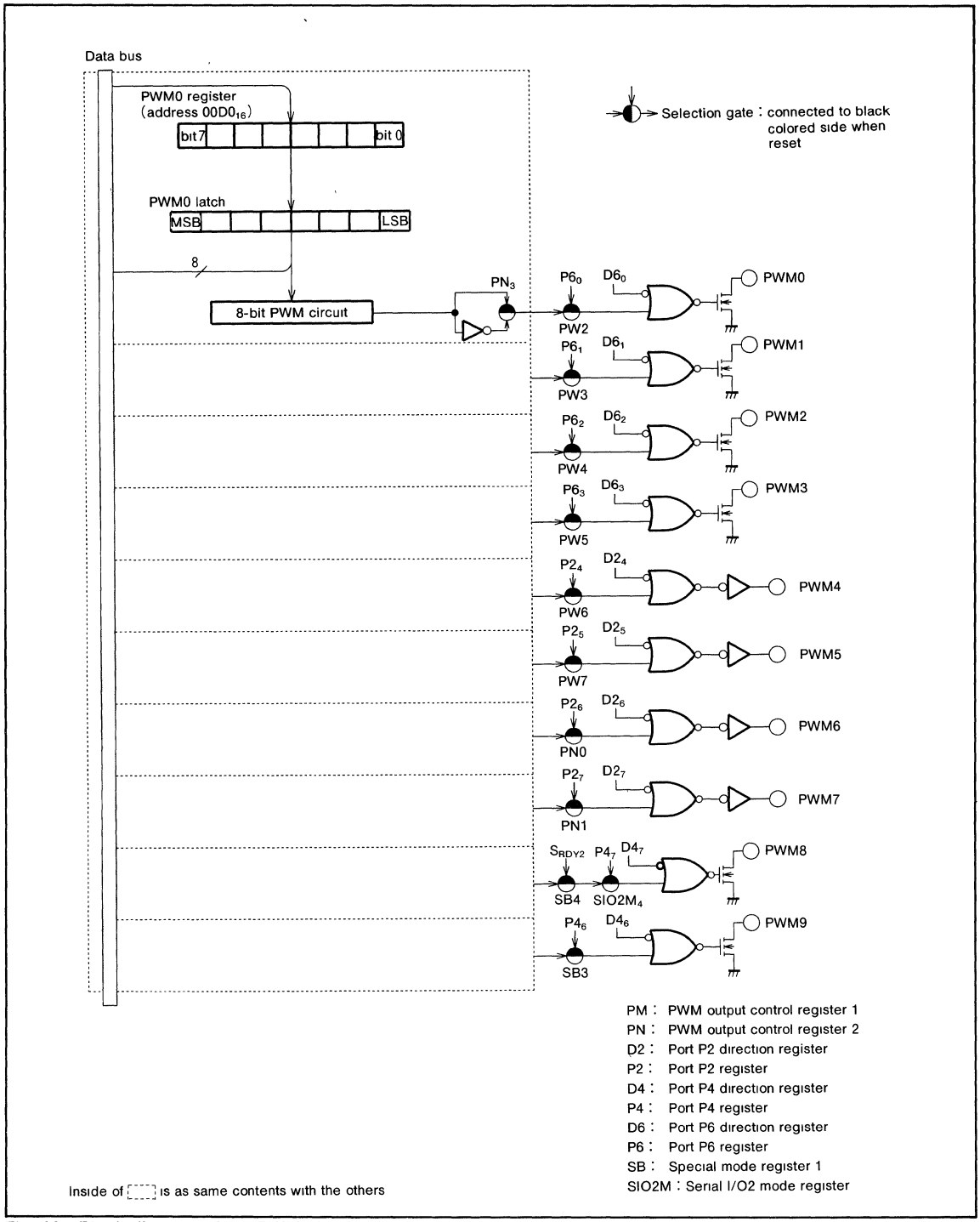


Fig. 16 Block diagram of the PWM circuit

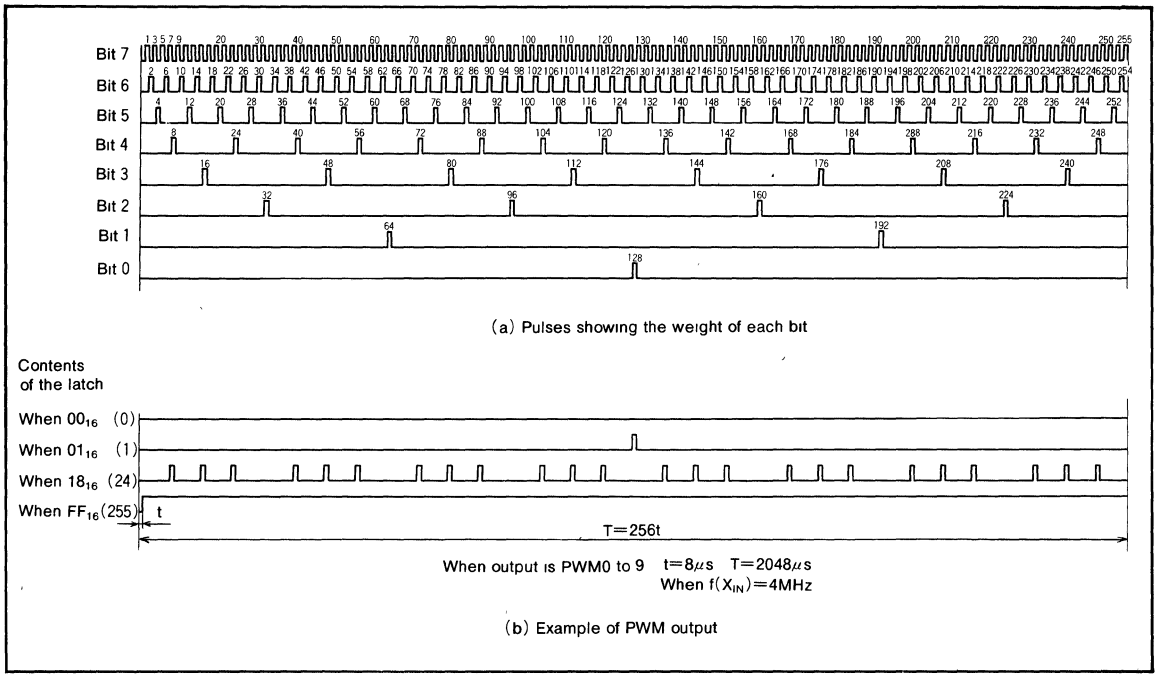


Fig. 17 PWM timing diagram

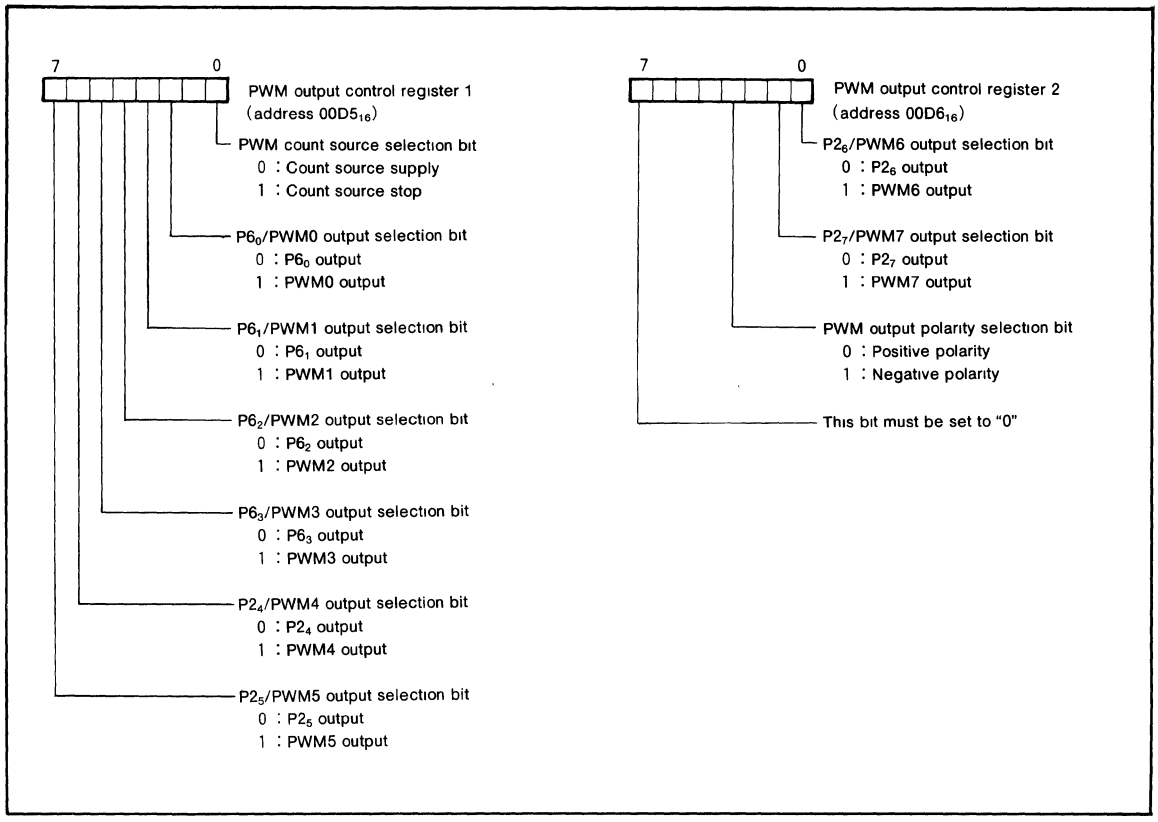


Fig. 18 Structure of PWM output control register 1 and 2

A-D CONVERTER

Block diagram of A-D converter is shown in Figure 19. A-D converter consists of 4-bit D-A converter and comparator. The A-D control register can generate 1/16 V_{CC}-step internal analog voltage based on the settings of bits 0 to 3.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_5$, $P3_6$ to "0" (port $P3_5$, $P3_6$ enters the input mode), to allow port $P3_5$/A-D1, $P3_6$/A-D2 to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 20 machine cycle, the voltage comparison starts.

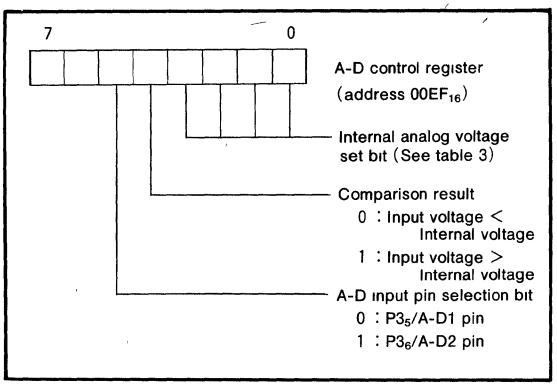


Fig. 20 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and internal analog voltage

A-D control register				Internal analog voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

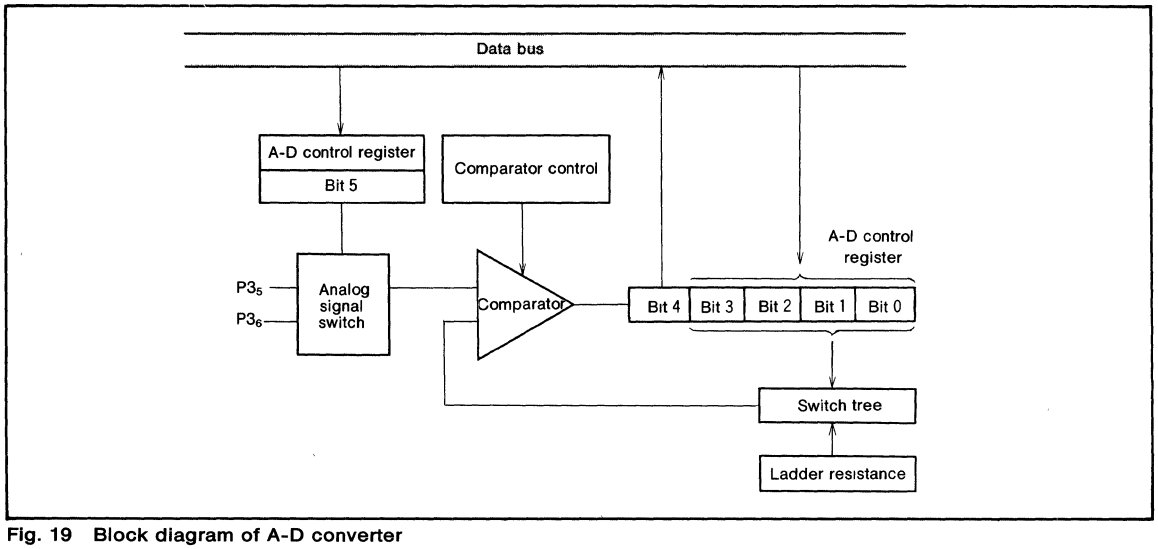


Fig. 19 Block diagram of A-D converter

PLL CIRCUIT

M37250M6-XXXSP has a built-in PLL circuit which is selectable either fixed dividing mode or swallow mode. PLL block diagram is shown in Figure 21.

(1) PLL control register

Switching fixed dividing mode/swallow mode, starting PLL operation, and selection of reference frequency are determined by PLL control register (address 0200_{16})

When fixed dividing mode is selected by setting the bit 6 (PL_6) of PLL control register to "0", MO pin becomes 1-bit general purpose output port. In this case, the output level of MO pin is determined by bit 5 (PL_5) of PLL control register (address 0200_{16}).

(2) Reference frequency generator

Nine kinds reference frequency are generated by built-in reference frequency generator that divides the external clock (4MHz), in both fixed dividing mode and swallow mode.

Reference frequency is determined by bit 0 (PL_0) to bit 4 (PL_4) of PLL control register.

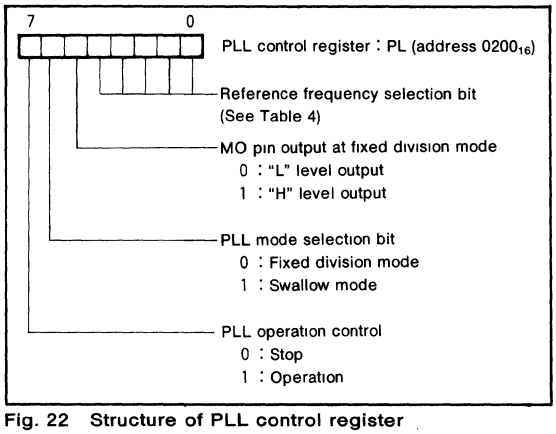


Fig. 22 Structure of PLL control register

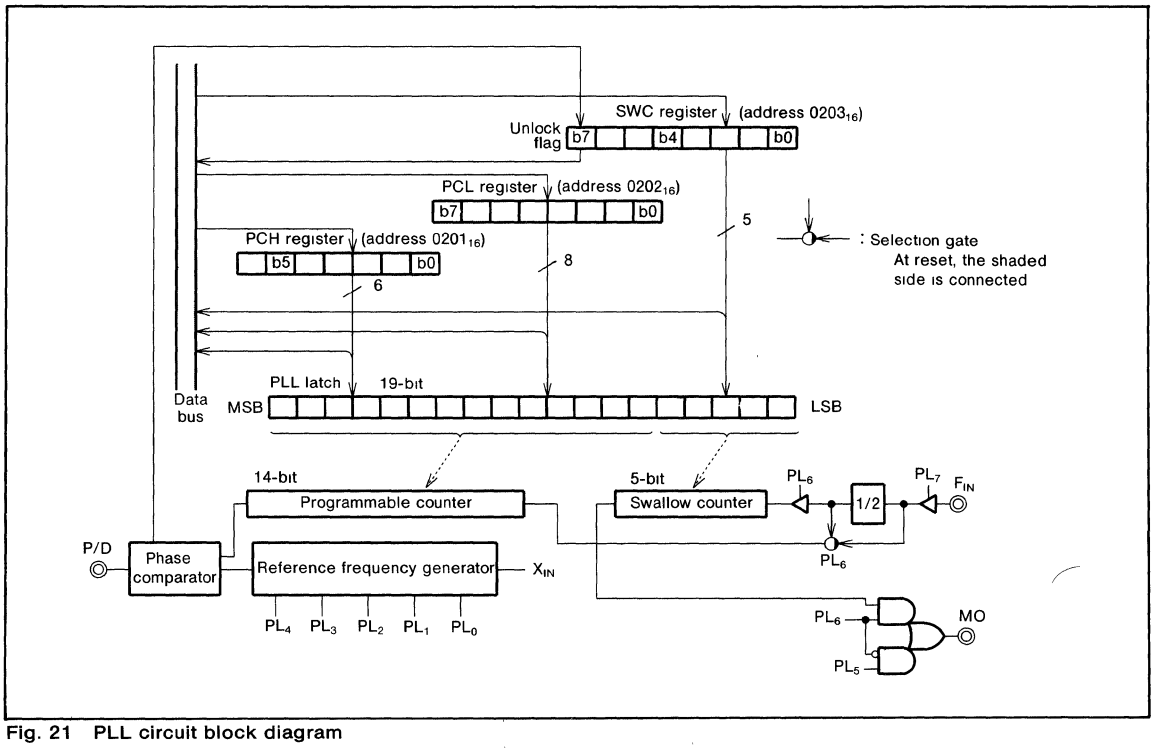


Fig. 21 PLL circuit block diagram

(3) Phase detector

Phase detector is a built-in circuit to detect a phase difference between reference frequency (f_{REF}) and division of VCO output by programmable divider.

Output of phase detector is input into internal charge pump, and outputs the following level from P/D pin.

- "L" level where $f_{REF} > f_{IN}/N$
- "H" level where $f_{REF} < f_{IN}/N$
- Floating where $f_{REF} = f_{IN}/N$

f_{IN} : Oscillation frequency of VCO

N : Division ratio of all PLL system include external prescaler.

Table 4. PLL control register bit mapping about reference frequency

PLL control register (address 0200_{16})					Reference frequency
PL_4	PL_3	PL_2	PL_1	PL_0	
0	0	1	1	1	7.8125kHz
0	1	0	0	1	5.0000kHz
0	1	0	1	0	0.78125kHz
0	1	0	1	1	3.125kHz
0	1	1	1	1	1.953125kHz
1	0	1	0	0	1.5625kHz
1	0	1	1	0	0.9765625kHz
1	0	1	1	1	3.90625kHz

(4) Programmable divider

Programmable divider is a binary down-counter configured by 5-bit swallow counter and 14-bit programmable counter. Lower 5 bits of 19-bit PLL latch data are preset to swallow counter and higher 14 bits of 19-bit PLL latch data are preset to programmable counter at a time, and it is down-counted.

(5) PLL latch

Data is set to programmable counter through PLL latch.

Contents of PLL latch is determinated by following sequence.

- Writing contents of swallow counter to SWC register (address 0203_{16})
- Writing lower 8-bit of programmable counter to PCL register (address 0202_{16})
- Writing higher 6-bit of programmable counter to PCH register (address 0201_{16})

Each register data is transferred to PLL latch, after writing to PCH register. Even when only lower 8-bit of programmable counter or contents of swallow counter need to change, be sure to write to PCH register again.

When reading the addresses 0201_{16} to 0203_{16} assigned PCH register, PCL register, and SWC register, the contents of PLL latch is read

The contents of PLL latch is indeterminate during reset. And this PLL latch contents is indeterminated till the transfer is completed, even though data are set to PCH, PLL, and SWC registers.

(6) Unlock flag

When PLL system is unlock, namely when reference frequency f_{REF} is difficult from division output frequency of VCO, the pulse is output synchronized f_{REF} from phase detecter. Unlock flag is assigned in bit 7 of SWC register, and it is set to "1" by this pulse, and this flag is set to "0" by reading. So, reading cycle is necessary to be longer than f_{REF} cycle. If the reading cycle is shorter than f_{REF} cycle, unlocked PLL system is regard as locking, so that this microcomputer may be missing operation. More time than f_{REF} cycle need to read unlock flag at first, after PLL operation starts.

(7) Programmable divider determination method

When M54470L (division ratio is 1/128 or 1/136) is used as prescaler at swallow mode, determination method of programmable divider division value is as following.

$$fo = 8 \cdot f_{REF}(32N_P + A)$$

fo : Partial oscillation frequency

f_{REF} : Reference frequency

N_P : Division ratio of programmable counter

$2^{14} \geqq N_P \geqq 16$ and $N_P > A$

A : Division ratio of swallow counter

$31 \geqq A \geqq 0$

When fixed prescaler (division ratio 1/K) is used at fixed dividing mode, determination method of programmable divider division value is as following.

$$fo = f_{REF} \cdot K \cdot N_P$$

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 5 outlines the CRT display functions of the M37250M6-XXXSP. The M37250M6-XXXSP incorporates a 24 columns×3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12×16 dot configuration to obtain smooth character patterns. (See Figure 23)

The following shows the procedure how to display characters on the CRT screen.

Table 5. Outline of CRT display functions

Parameter		Functions
Number of display character		24 characters×3 lines
Character configuration		12×16 dots (See Figure 23)
Kinds of character		126
Character size		4 size selectable
Color	Kinds of color	15 (max.)
	Coloring unit	a character
Display expansion		Possible (multiple lines)

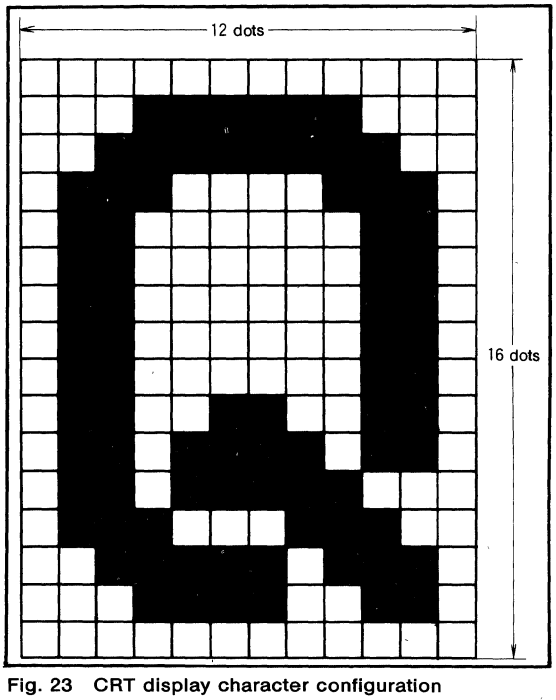


Fig. 23 CRT display character configuration

① Set the character to be displayed in display RAM.
② Set the display color by using the color register.
③ Specify the color register in which the display color is set by using the display RAM.
④ Specify the vertical position and character size by using the vertical position register and the character size register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 25 shows a block diagram of the CRT display control circuit. Figure 24 shows the structure of the CRT display control register.

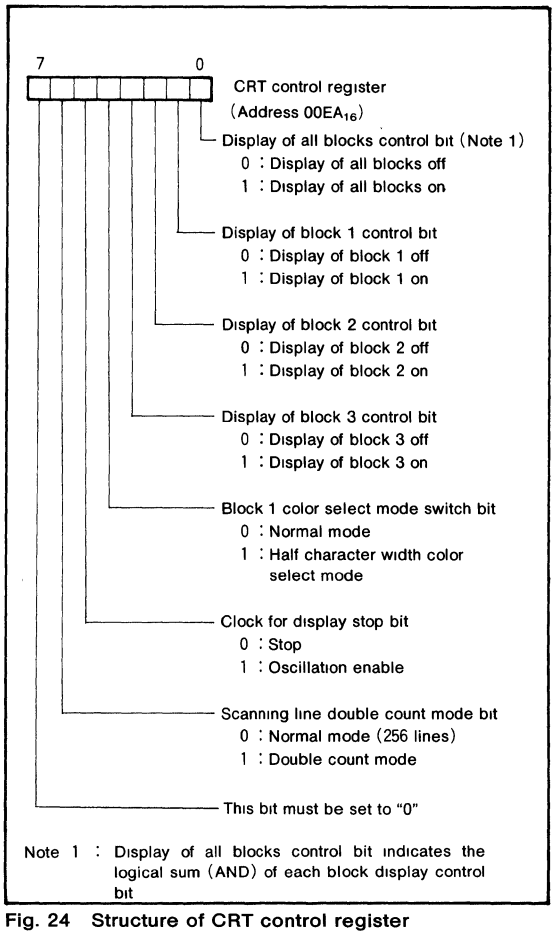


Fig. 24 Structure of CRT control register

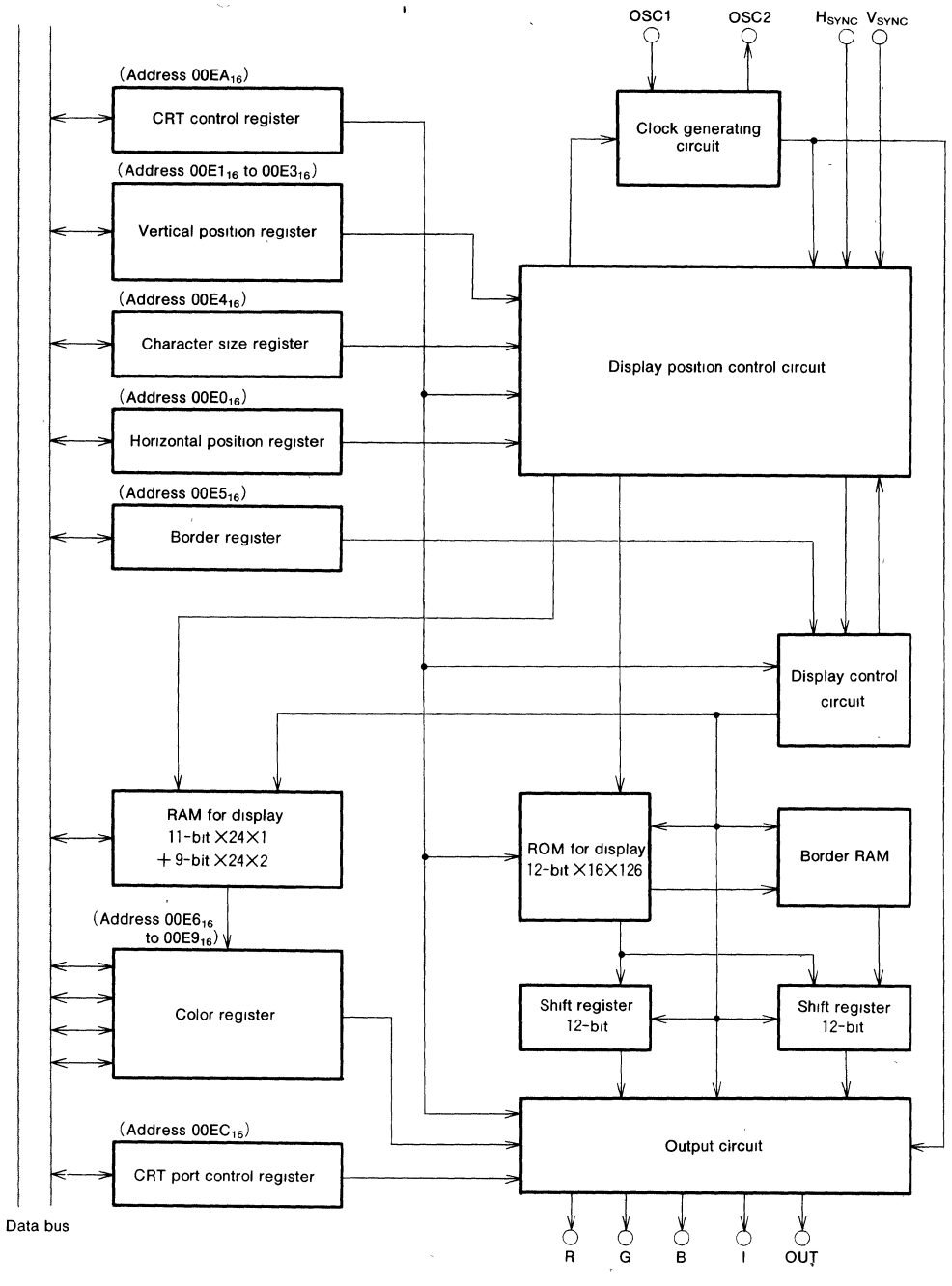


Fig. 25 Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc =oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 28), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 28), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 26 shows the structure of the vertical position register.

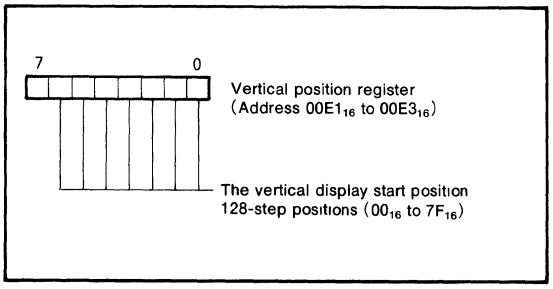


Fig. 26 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc=oscillation cycle for display) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 27 shows the structure of the horizontal position register.

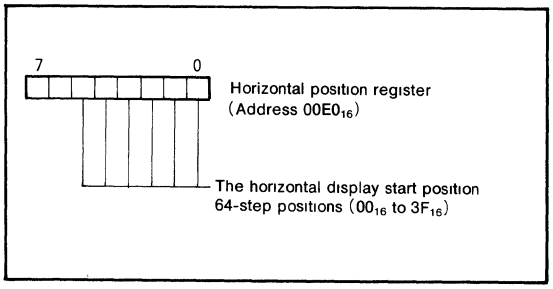
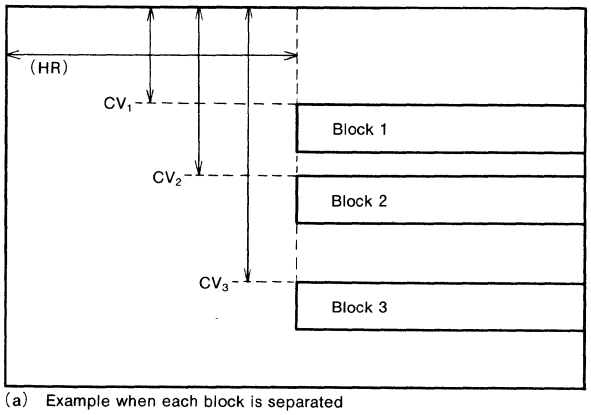
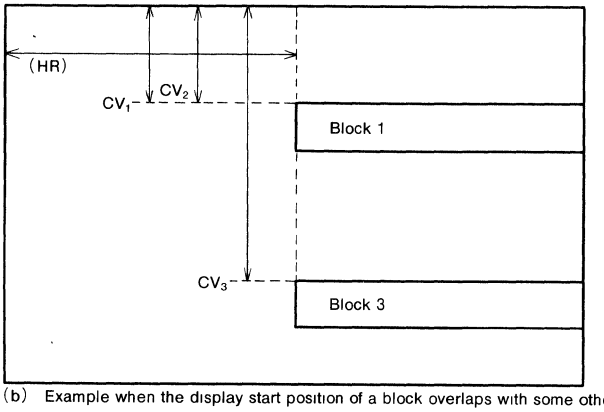


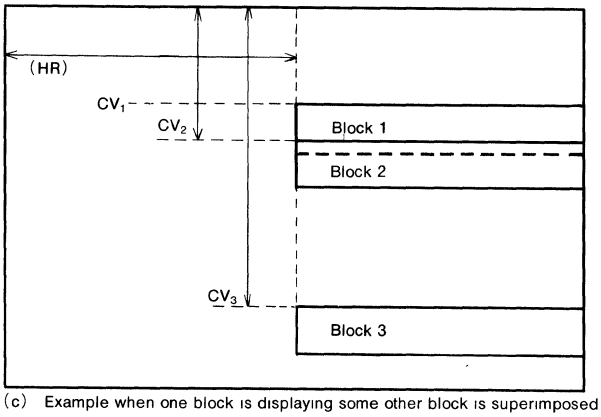
Fig. 27 Structure of horizontal position register



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 28 Display position

(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address $00E4_{16}$) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 29 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=Tc) in the width (horizontal) direction.

The small size consists of [one scanning line] × [1 Tc]; the medium size consists of [two scanning lines] × [2 Tc]; the large size consists of [three scanning lines] × [3 Tc]; and the extra large size consists of [four scanning lines] × [4 Tc]. Table 6 shows the relationship between the set values in the character size register and the character sizes.

Table 6. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction	Height (vertical) direction
CS_{n1}	CS_{n0}			
0	0	Small	1 T_C	1
0	1	Medium	2 T_C	2
1	0	Large	3 T_C	3
1	1	Extra large	4 T_C	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block (See Figure 30)

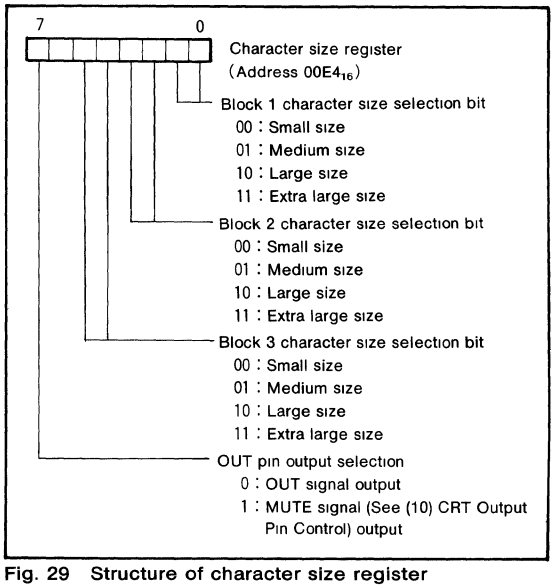


Fig. 29 Structure of character size register

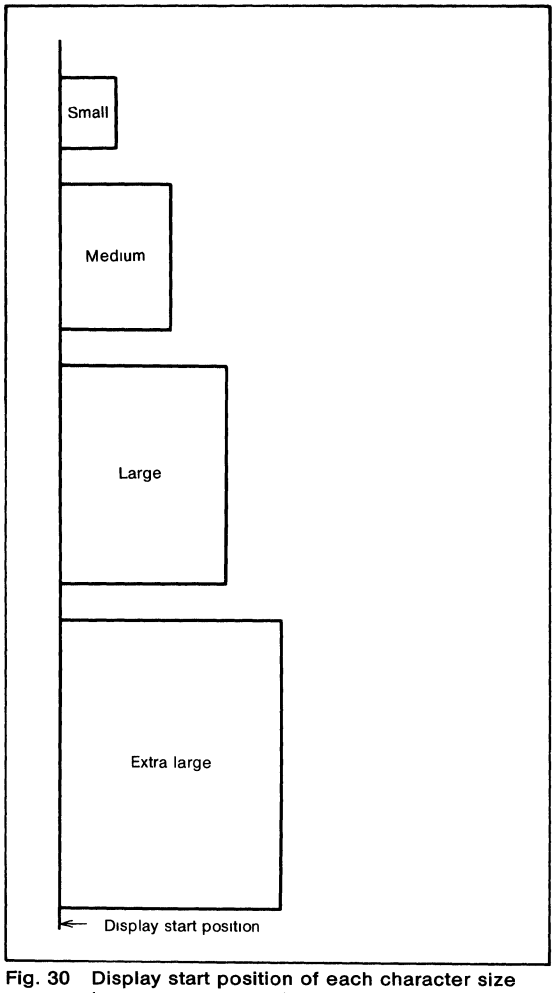


Fig. 30 Display start position of each character size (horizontal direction)

(4) Display Memory

There are two types of display memory: ROM of CRT display (3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and display RAM (2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (3000_{16} to $3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$. (See Figure 31) Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX_{16}".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) address (3000_{16} to $37FF_{16}$) where data for that character is stored.

Table 7 lists the character codes.

Table 7. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16} : 10_{16}	3030_{16} to $303F_{16}$: 3100_{16} to $310F_{16}$	3830_{16} to $383F_{16}$: 3900_{16} to $390F_{16}$
11_{16} : $4F_{16}$	3110_{16} to $311F_{16}$: $34F0_{16}$ to $34FF_{16}$	3910_{16} to $391F_{16}$: $3CF0_{16}$ to $3CFF_{16}$
50_{16} : $7D_{16}$	3500_{16} to $350F_{16}$: $37D0_{16}$ to $37DF_{16}$	$3D00_{16}$ to $3D0F_{16}$: $3FD0_{16}$ to $3FDF_{16}$
$7E_{16}$*	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}$*	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

※ : The test pattern are stored

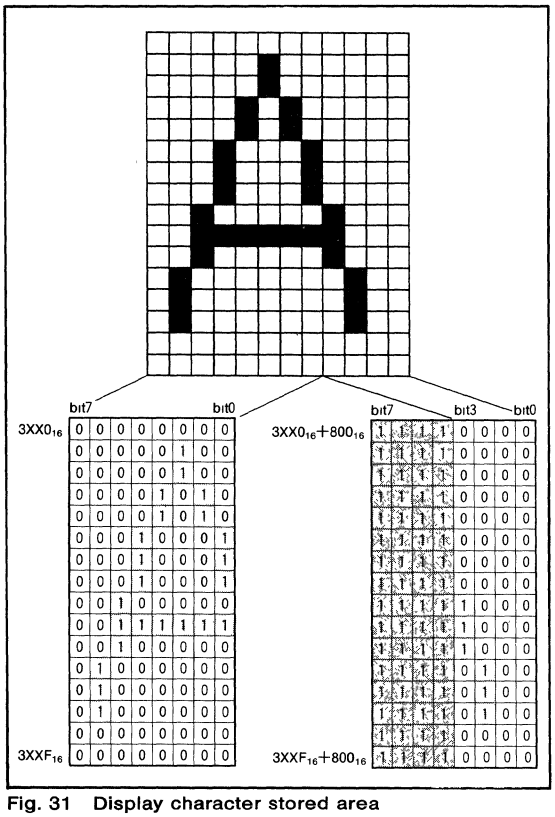


Fig. 31 Display character stored area

② CRT display RAM (2000_{16} to $20D7_{16}$)

The CRT display RAM is allocated at addresses 2000_{16} to $20D7_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 8 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16}. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 32. Write the character patterns at Table 9 and 10 as test pattern, when M37250M6-XXXSP is mask-ordered.

Table 8. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000_{16}	2080_{16}
	2nd column	2001_{16}	2081_{16}
	3rd column	2002_{16}	2082_{16}
	:	:	:
	22th column	2015_{16}	2095_{16}
	23th column	2016_{16}	2096_{16}
	24th column	2017_{16}	2097_{16}
Not used		2018_{16} ~ $201F_{16}$	2098_{16} ~ $209F_{16}$
Block 2	1st column	2020_{16}	$20A0_{16}$
	2nd column	2021_{16}	$20A1_{16}$
	3rd column	2022_{16}	$20A2_{16}$
	:	:	:
	22th column	2035_{16}	$20B5_{16}$
	23th column	2036_{16}	$20B6_{16}$
	24th column	2037_{16}	$20B7_{16}$
Not used		2038_{16} ~ $203F_{16}$	$20B8_{16}$ ~ $20BF_{16}$
Block 3	1st column	2040_{16}	$20C0_{16}$
	2nd column	2041_{16}	$20C1_{16}$
	3rd column	2042_{16}	$20C2_{16}$
	:	:	:
	22th column	2055_{16}	$20D5_{16}$
	23th column	2056_{16}	$20D6_{16}$
	24th column	2057_{16}	$20D7_{16}$
Not used		2058_{16} ~ $207F_{16}$	

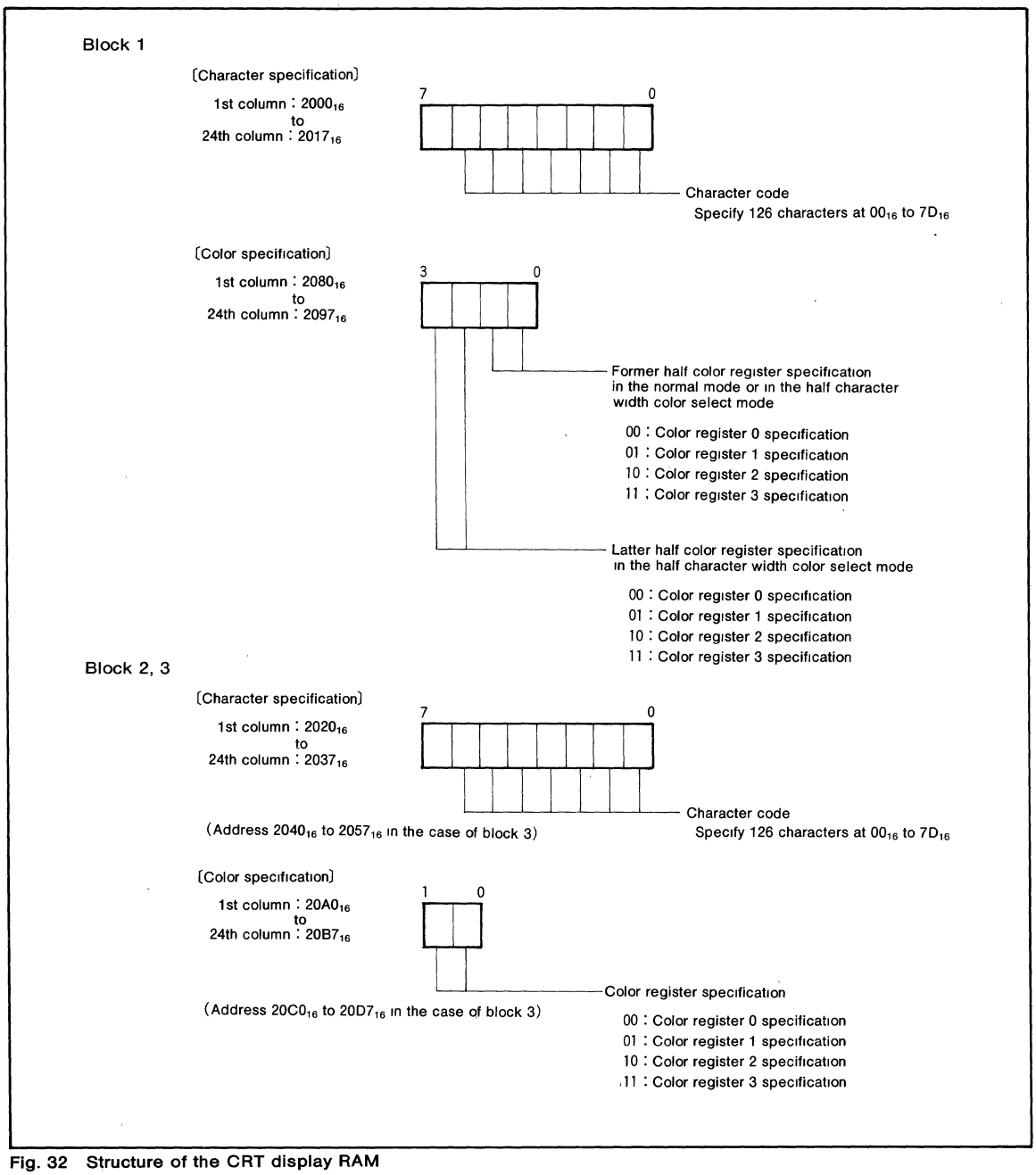


Fig. 32 Structure of the CRT display RAM

Table 9. Test character patterns 1

Address	Data	Address	Data
$37E0_{16}$	40_{16}	$3FE0_{16}$	$F0_{16}$
$37E1_{16}$	04_{16}	$3FE1_{16}$	$F0_{16}$
$37E2_{16}$	00_{16}	$3FE2_{16}$	$F4_{16}$
$37E3_{16}$	20_{16}	$3FE3_{16}$	$F0_{16}$
$37E4_{16}$	02_{16}	$3FE4_{16}$	$F0_{16}$
$37E5_{16}$	00_{16}	$3FE5_{16}$	$F2_{16}$
$37E6_{16}$	10_{16}	$3FE6_{16}$	$F0_{16}$
$37E7_{16}$	01_{16}	$3FE7_{16}$	$F0_{16}$
$37E8_{16}$	80_{16}	$3FE8_{16}$	$F0_{16}$
$37E9_{16}$	08_{16}	$3FE9_{16}$	$F0_{16}$
$37EA_{16}$	00_{16}	$3FEA_{16}$	$F8_{16}$
$37EB_{16}$	40_{16}	$3FEB_{16}$	$F0_{16}$
$37EC_{16}$	04_{16}	$3FEC_{16}$	$F0_{16}$
$37ED_{16}$	00_{16}	$3FED_{16}$	$F4_{16}$
$37EE_{16}$	20_{16}	$3FEE_{16}$	$F0_{16}$
$37EF_{16}$	02_{16}	$3FEF_{16}$	$F0_{16}$

Table 10. Test character patterns 2

Address	Data	Address	Data
$37F0_{16}$	00_{16}	$3FF0_{16}$	$F0_{16}$
$37F1_{16}$	00_{16}	$3FF1_{16}$	$F0_{16}$
$37F2_{16}$	00_{16}	$3FF2_{16}$	$F0_{16}$
$37F3_{16}$	00_{16}	$3FF3_{16}$	$F0_{16}$
$37F4_{16}$	00_{16}	$3FF4_{16}$	$F0_{16}$
$37F5_{16}$	00_{16}	$3FF5_{16}$	$F0_{16}$
$37F6_{16}$	00_{16}	$3FF6_{16}$	$F0_{16}$
$37F7_{16}$	00_{16}	$3FF7_{16}$	$F0_{16}$
$37F8_{16}$	00_{16}	$3FF8_{16}$	$F0_{16}$
$37F9_{16}$	00_{16}	$3FF9_{16}$	$F0_{16}$
$37FA_{16}$	00_{16}	$3FFA_{16}$	$F0_{16}$
$37FB_{16}$	00_{16}	$3FFB_{16}$	$F0_{16}$
$37FC_{16}$	00_{16}	$3FFC_{16}$	$F0_{16}$
$37FD_{16}$	00_{16}	$3FFD_{16}$	$F0_{16}$
$37FE_{16}$	00_{16}	$3FFE_{16}$	$F0_{16}$
$37FF_{16}$	00_{16}	$3FFF_{16}$	$F0_{16}$

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses $00E6_{16}$ to $00E9_{16}$) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 33 shows the structure of the color register.

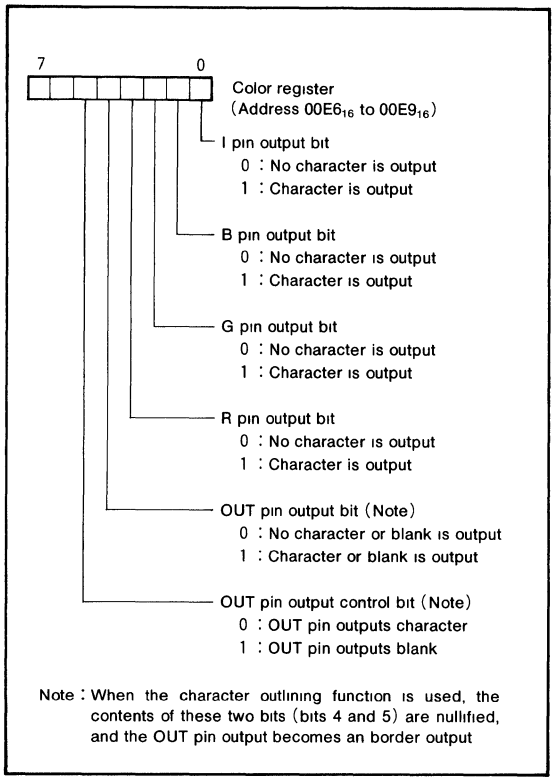


Fig. 33 Structure of color registers

(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address $00EA_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

①The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

②The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

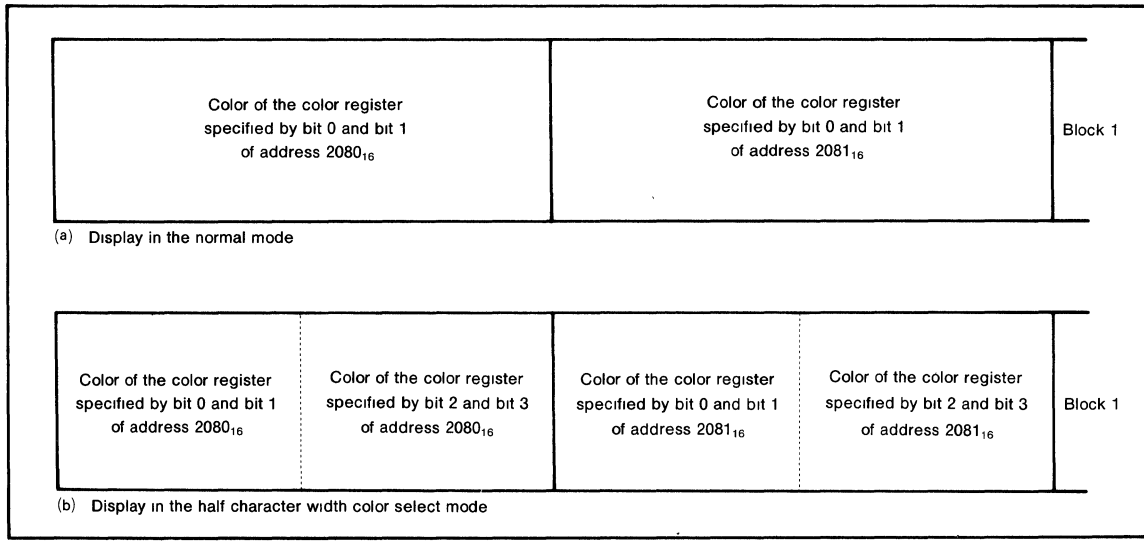


Fig. 34 Difference between normal color select mode and half character width color select mode

(7) Multiline Display

The M37250M6-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit=bit 4 at address $00FE_{16}$) to "1"), then execute the following processing in the CRT interrupt handling routine.

①Read the value of the display block counter.

②The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.

③Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 36 shows the structure of the display block counter.

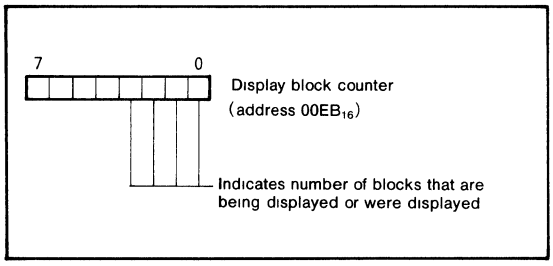


Fig. 36 Structure of display block counter

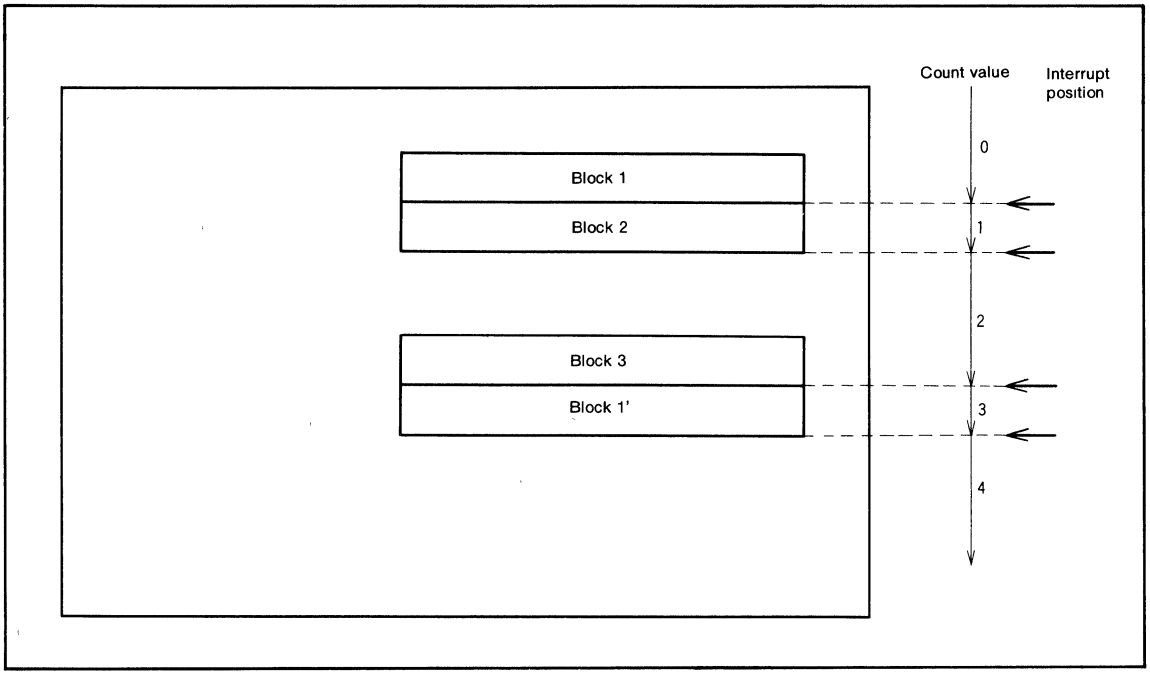


Fig. 35 Timing of CRT interrupt and count value of display block counter

(8) Scanning Line Double Count Mode

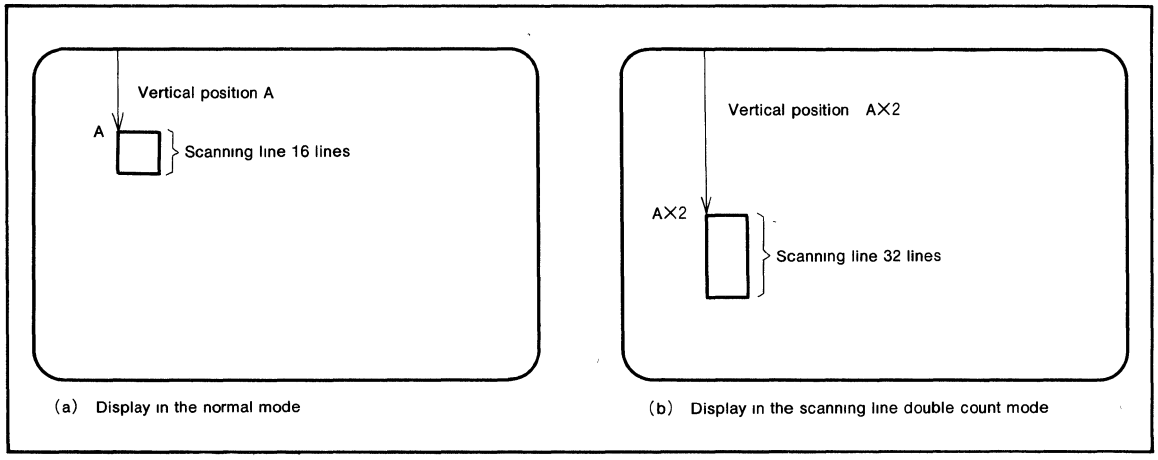
One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.



(a) Display in the normal mode

(b) Display in the scanning line double count mode

Fig. 37 Display in the normal mode and in the scanning line double count mode

(9) Character Border Function

A border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address $00E5_{16}$). Table 11 shows the relationship between the values set in the border select register and the character border function. Figure 39 shows the structure of the border select register.

Table 11. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

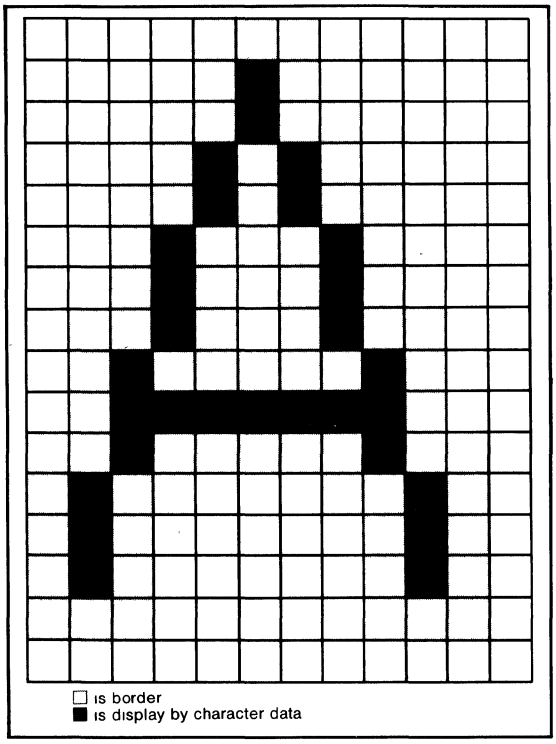


Fig. 38 Example of border

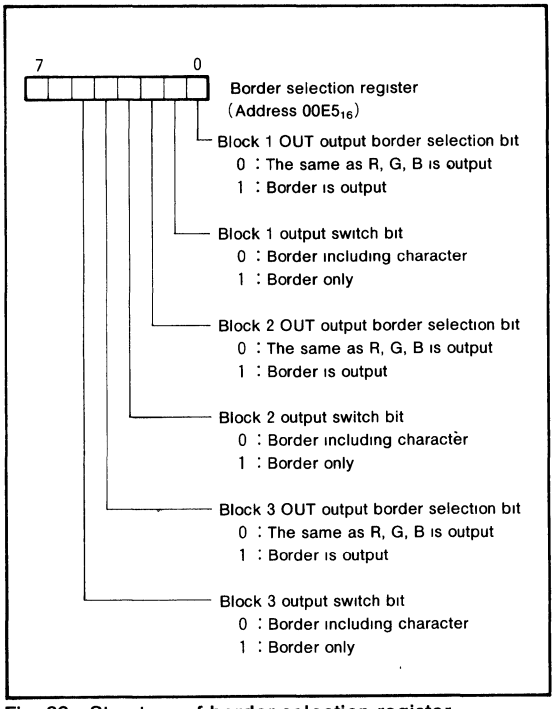


Fig. 39 Structure of border selection register

(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port $P5_2$, $P5_3$, $P5_4$, $P5_5$, and $P5_6$. The output signal can control by port P5 direction register (address $00CB_{16}$) for each port. At reset, because the port P5 direction register is reset, CRT output pins R, G, B, I, and OUT become CRT signal (R, G, B, I, and OUT) output polarity. Bits 0 to 4 of CRT port control register (address $00EC_{16}$) can determine H_{SYNC} and V_{SYNC} input polarity and R, G, B, I, and OUT output polarity.

R, G, B, and OUT signal output can be switched to MUTE signal output. MUTE signal can color all displaying area of CRT.

The following is the explain of MUTE signal at MUTE signal output from B output pin for example (refer to Figure 40).

When the MUTE signal is output from B output pin, the all displaying area of CRT is colored blue. Then, a character data is output from R output pin, for example. If B output pin and R output pin are set to "Character is output" by color register at the character "I" output, the output character is colored "RED" mixed "BLUE"

In this case, OUT pin output is not influenced.

At the character "O" output, if only R output pin is set to "Character is output", the output character is colored "RED" only that is not mixed "BLUE".

However at above case, the OUT output pin is necessary to set "Character is output".

The display screen can be also clear by setting the OUT pin to MUTE output. In this case, the MUTE signal is output from OUT pin, that is not influence the setting about OUT pin by CRT display RAM.

R, G, and B output signals are controlled by bits 5 to 7 of CRT port control register, and OUT output signal is controlled by bit 7 (CS7) of character size register. Then, I output pin don't have MUTE output function.

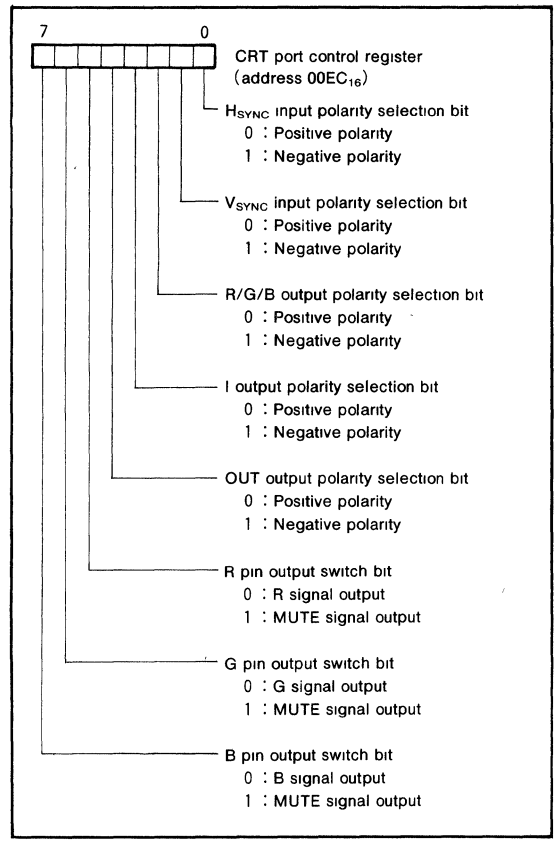


Fig. 41 Structure of CRT port control register

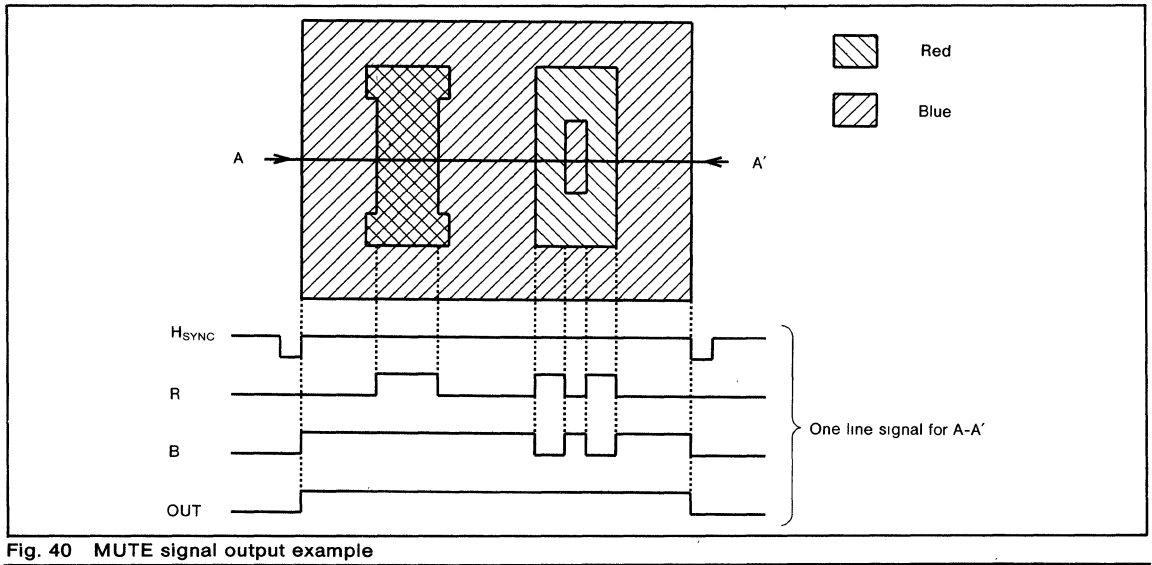


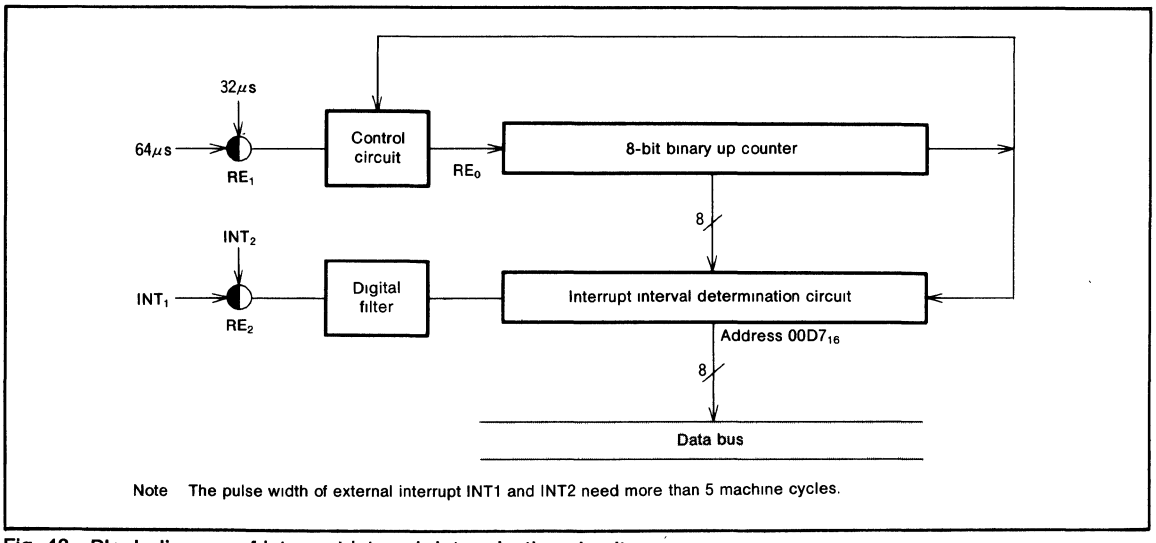
Fig. 40 MUTE signal output example

INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37250M6-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 42. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT1 or INT2 to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address $00D8_{16}$). When this bit is cleared to "0", the INT1 input is selected; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT2 input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).
3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64μs clock is selected; when the bit is set to "1", a 32μs clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary counter starts counting up with the selected reference clock (64μs or 32 μs).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address $00D7_{16}$) and the counter is immediately reset (00_{16}). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00_{16}"
6. When count value "FE_{16}" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF_{16}" to the determination register.



Note The pulse width of external interrupt INT1 and INT2 need more than 5 machine cycles.

Fig. 42 Block diagram of interrupt interval determination circuit

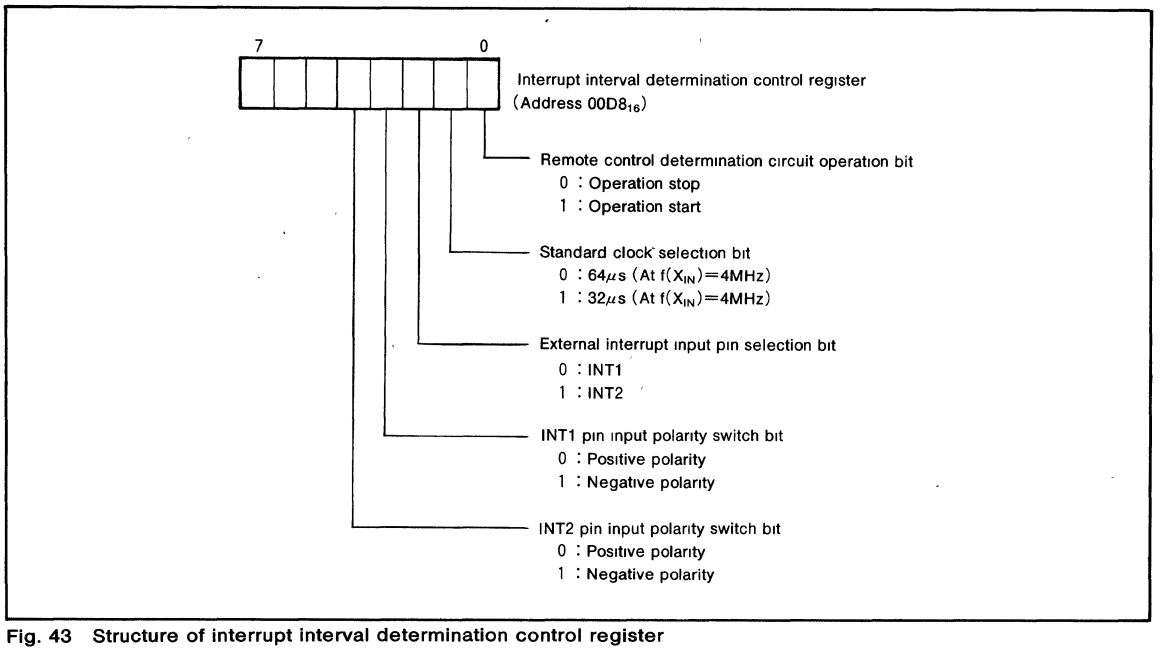


Fig. 43 Structure of interrupt interval determination control register

RESET CIRCUIT

The M37250M6-XXXSP is reset according to the sequence shown in Figure 46. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V$\pm$10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 44.

An example of the reset circuit is shown in Figure 45. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

		Address	Contents
(1)	Port P0 direction register	($00C1_{16}$)	00_{16}
(2)	Port P1 direction register	($00C3_{16}$)	00_{16}
(3)	Port P2 direction register	($00C5_{16}$)	00_{16}
(4)	Port P3 direction register	($00C7_{16}$)	00_{16}
(5)	Port P4 direction register	($00C9_{16}$)	00_{16}
(6)	Port P5 direction register	($00CB_{16}$)	0 0 0 0 0
(7)	Port P6 direction register	($00CD_{16}$)	0 0 0 0
(8)	PWM output control register 1	($00D5_{16}$)	00_{16}
(9)	PWM output control register 2	($00D6_{16}$)	00_{16}
(10)	Interrupt interval determination control register	($00D8_{16}$)	00_{16}
(11)	Special mode register 1	($00DA_{16}$)	00_{16}
(12)	Special mode register 2	($00DB_{16}$)	00_{16}
(13)	Serial I/O1 mode register	($00DC_{16}$)	00_{16}
(14)	Serial I/O2 mode register	($00DE_{16}$)	00_{16}
(15)	Horizontal position register	($00E0_{16}$)	0 0 0 0 0 0
(16)	Color register 0	($00E6_{16}$)	0 0 0 0 0 0
(17)	Color register 1	($00E7_{16}$)	0 0 0 0 0 0
(18)	Color register 2	($00E8_{16}$)	0 0 0 0 0 0
(19)	Color register 3	($00E9_{16}$)	0 0 0 0 0 0
(20)	CRT control register	($00EA_{16}$)	00_{16}
(21)	Display block counter	($00EB_{16}$)	0 0 0 0
(22)	CRT port control register	($00EC_{16}$)	0 0 0 0 0 0
(23)	A-D control register	($00EF_{16}$)	0 0 0 0 0 0
(24)	Timer 1	($00F0_{16}$)	FF_{16}
(25)	Timer 2	($00F1_{16}$)	07_{16}
(26)	Timer 3	($00F2_{16}$)	FF_{16}
(27)	Timer 4	($00F3_{16}$)	07_{16}
(28)	Timer mode register 1	($00F4_{16}$)	00_{16}
(29)	Timer mode register 2	($00F5_{16}$)	00_{16}
(30)	CPU mode register	($00FB_{16}$)	1 1 1 1 1 0 0
(31)	Interrupt request register 1	($00FC_{16}$)	00_{16}
(32)	Interrupt request register 2	($00FD_{16}$)	0 0 0 0 0
(33)	Interrupt control register 1	($00FE_{16}$)	00_{16}
(34)	Interrupt control register 2	($00FF_{16}$)	0 0 0 0 0
(35)	PLL control register	(0200_{16})	00_{16}
(36)	Timer 5	(0204_{16})	FF_{16}
(37)	Timer 6	(0205_{16})	07_{16}
(38)	Processor status register	(PS)	1
(39)	Program counter	(PC_H)	Contents of address $FFFF_{16}$
		(PC_L)	Contents of address $FFFE_{16}$

Note Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
At reset, "0" is read from all bits which is not used

Fig. 44 Internal state of microcomputer at reset

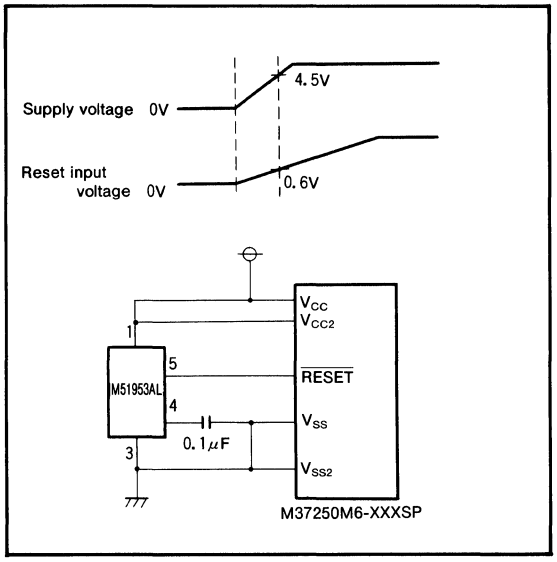
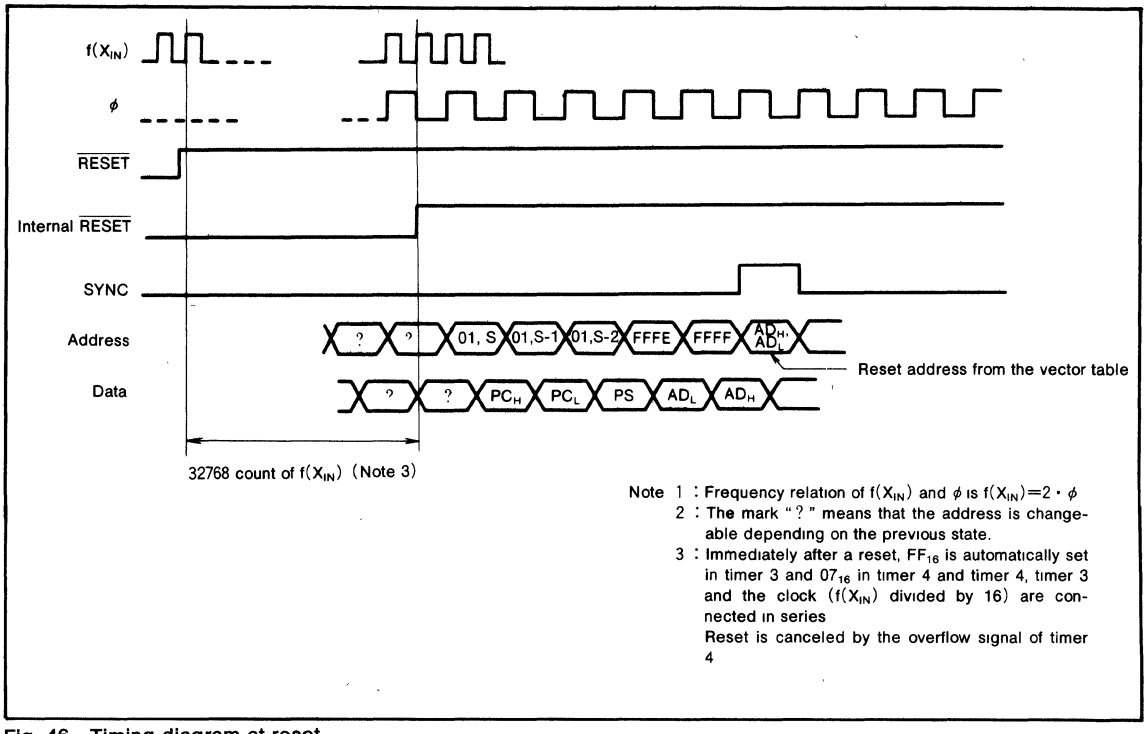


Fig. 45 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=2 \cdot \phi$
2 : The mark "?" means that the address is changeable depending on the previous state.
3 : Immediately after a reset, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4, timer 3 and the clock ($f(X_{IN})$ divided by 16) are connected in series
Reset is canceled by the overflow signal of timer 4

Fig. 46 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the SFR memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a direction register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address $00FB_{16}$), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A_7 to A_0) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15} to A_8) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. Port $P2_4$ to $P2_7$ are in common with PWM output pins PWM4 to 7. In other modes, it functions as data (D_0 to D_7) input/output port. Refer to the section on processor modes for details

(4) Port P3

Port P3 is a 7-bit I/O port with function similar to port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output and $P3_2$ to $P3_6$ is N-channel open drain.

$P3_2$, $P3_3$ are in common with the external clock input pins of timer 2 and 3.

$P3_4$, $P3_6$ are in common with the external interrupt input pins INT1, INT2 and $P3_5$, $P3_6$ are in common with the analog input pins of A-D converter A-D1, A-D2.

In the microprocessor mode or the memory expansion mode, $P3_0$, $P3_1$ works as R/$\overline{W}$ signal output pin and SYNC signal output pin.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O1 function is selected, $P4_0$ to $P4_3$ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, $P4_4$ to $P4_7$ work as input/output pins of serial I/O2.

In the special serial I/O mode, $P4_4$, $P4_5$ work as SDA, SCL pins. $P4_6$, $P4_7$ are in common with PWM8 and 9 output pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is a 5-bit output pin for CRT display and in common with $P5_2$ to $P5_6$.

(9) Port P6

Port P6 is a 4-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

This port is in common with 8-bit PWM output pin PWM0 to PWM3.

(10) ϕ pin

The internal system clock (1/2 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

(11) MO pin

This pin outputs the mode switching signal of prescalor.

The output structure is CMOS output.

(12) P/D pin

Phase detector output pin.

(13) F_{IN} pin

The clock from prescalor is input to this pin.

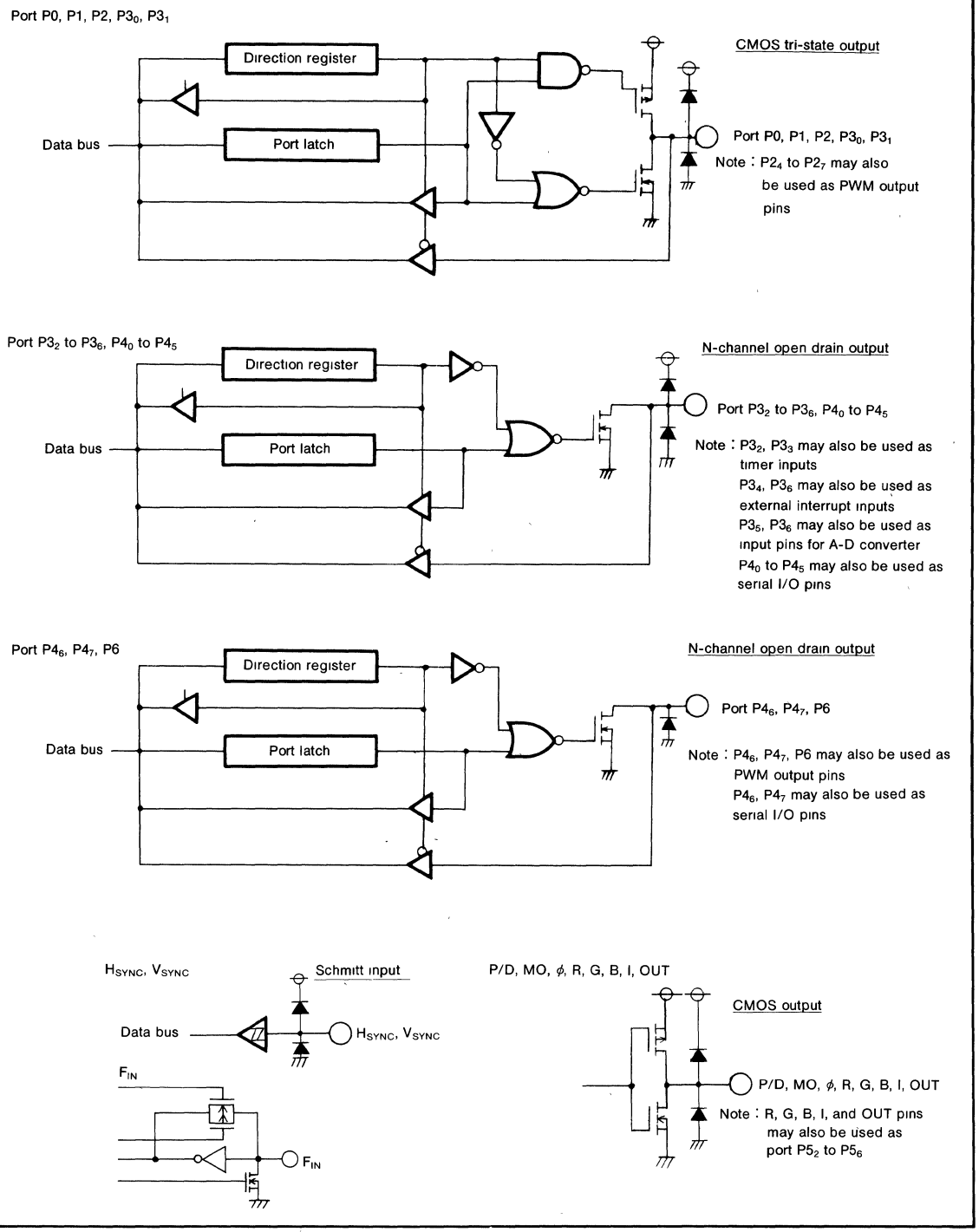


Fig. 47 Block diagram of port P0 to P6 (single-chip mode) and output format of P/D, MO, ϕ, R, G, B, I, OUT, and F_{IN}

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FB_{16}$), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode , ports P0 to P3 can be used as address, and data input/output pins.

Figure 49 shows the functions of ports P0 to P3.

The memory map for the single-chip mode is illustrated in Figure 2 and for other modes, in Figure 48.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows:

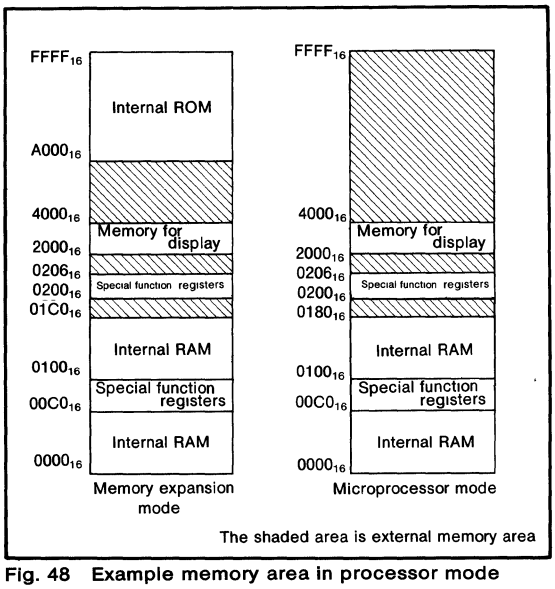


Fig. 48 Example memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 to P3 will work as original I/O ports.

(2) Memory expansion mode [01]
The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.
Port P2 becomes the data bus of D_7 to D_0 (including instruction code) and loses its normal I/O function. Port $P3_0$ and $P3_1$ works as R/$\overline{W}$ and SYNC.

(3) Microprocessor mode [10]
When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "10", or after connecting CNV_{SS} to V_{CC} and initiating a reset the microcomputer will automatically default to this mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note : Use the M37250M6-XXXSP in the microprocessor mode or the memory expansion mode only at program development.
The standards is assured only in the single-chip mode.

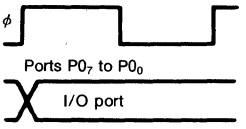
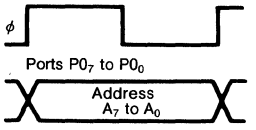
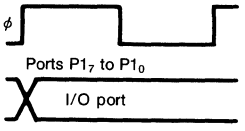
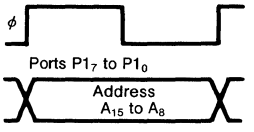
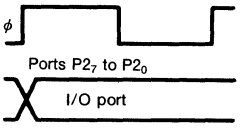
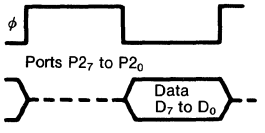
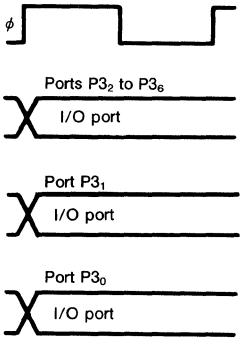
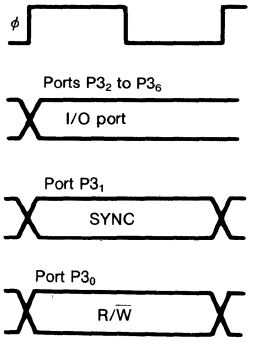
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 0, CM_0 = 1 Memory expansion mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0			Same as left
Port P1			Same as left
Port P2			Same as left
Port P3			Same as left

Fig. 49 Processor mode and function of port P0 to P3

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expansion mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 52.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 07_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 50.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 51 X_{IN} is the input, and X_{OUT} is open.

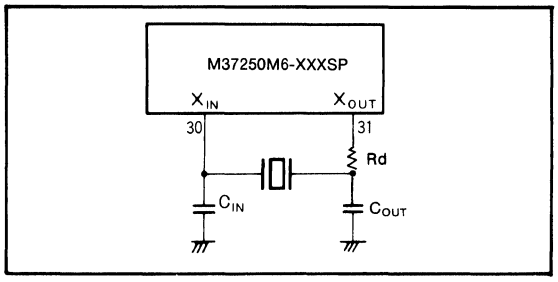


Fig. 50 External ceramic resonator circuit

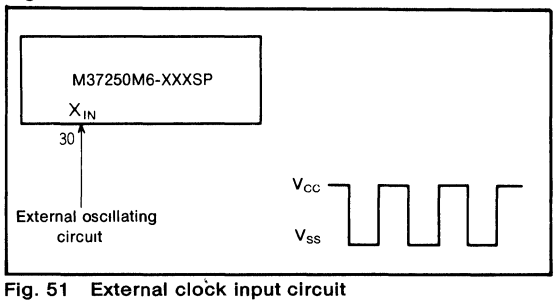


Fig. 51 External clock input circuit

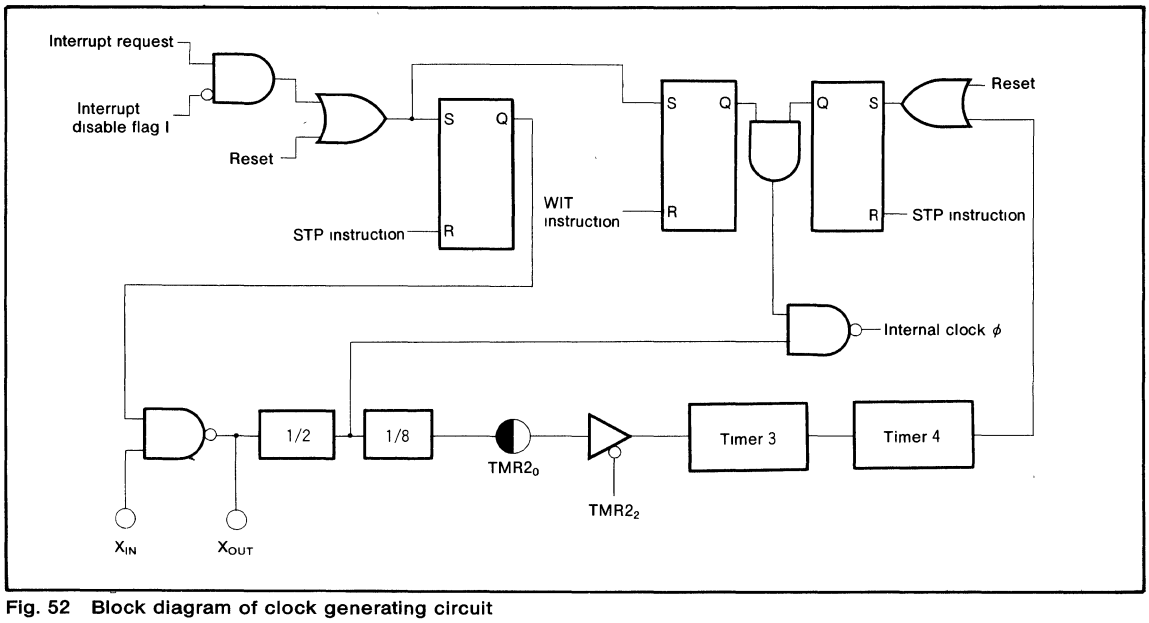


Fig. 52 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) After the ADC and SBC instructions are executed (indecimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(4) A NOP instruction must be used after the execution of a PLP insturction.

(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM order confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 6	V
V_I	Input voltage CNV_{SS}		−0.3 to 6	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_7$, $P6_0$-$P6_3$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, F_{IN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$, R, G, B, I, OUT, P/D, MO, X_{OUT}, OSC2		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P4_6$, $P4_7$, $P6_0$-$P6_3$		−0.3 to 13.0	V
I_{OH}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, P/D, MO		0 to 1(Note 1)	mA
I_{OL1}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, P/D, MO		0 to 2(Note 2)	mA
I_{OL2}	Circuit current $P6_0$-$P6_3$, $P4_6$, $P4_7$		0 to 1(Note 2)	mA
I_{OL3}	Circuit current $P2_4$-$P2_7$		0 to 10(Note 3)	mA
I_{OL4}	Circuit current $P4_4$, $P4_5$		0 to 3(Note 2)	mA
Pd	Power dissipation	T_a=25℃	550	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10 to 70℃ unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ	Max	
V_{CC}	Supply voltage(Note 4) During the PLL, CRT operation		4.5	5.0	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, $P4_6$,$P4_7$, $P6_0$-$P6_3$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_4$, $P4_5$		0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_5$, $P4_0$, $P4_3$-$P4_5$, $P4_7$, $P6_0$-$P6_3$		0		0.4V_{CC}	V
V_{IL}	"L" input voltage $P3_2$-$P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_6$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1		0		0.2V_{CC}	V
I_{OH}	"H" average output current (Note 1) R,G,B,I,OUT,$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, P/D, MO				1	mA
I_{OL1}	"L" average output current (Note 2) R,G,B,I,OUT,$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, P/D, MO				2	mA
I_{OL2}	"L" average output current (Note 2) $P6_0$-$P6_3$, $P4_6$, $P4_7$				1	mA
I_{OL3}	"L" average output current (Note 3) $P2_4$-$P2_7$				10	mA
I_{OL4}	"L" average output current (Note 2) $P4_4$, $P4_5$				3	mA
f_{CPU}	Oscillating frequency (for CPU operation)(Note 5)		3.6	4.0	4.4	MHz
f_{CRT}	Oscillating frequency (for CRT display)		6.0	7.0	8.0	MHz
fhs	Input frequency $P3_2$-$P3_4$, $P3_6$, $P4_5$				100	kHz
fhs	Input frequency $P4_1$				1	MHz
fhs	Input frequency F_{IN} V_I=0.6 V_{P-P}	Sine wave	1.0		15	MHz
		Square wave	0.1		15	MHz

Note 1 : The total current that flows out of the IC should be 20mA (max.)
2 : The total of I_{OL1}, I_{OL2}, and I_{OL4} should be 30mA (max).
3 : The total of I_{OL} of port $P2_4$-$P2_7$ should be 20mA (max).
4 : Apply 0.15μF or grater capacitance externally between the V_{CC}−V_{SS} power supply pins so as to reduce power source noise Apply 0.15μF or grater capacitance externally between the V_{CC2}−V_{SS2} as same
Also apply 0.15μF or greater capacitance externally between the V_{CC}−CNV_{SS} pins
5 : Use the quartz crystal oscillator for CPU oscillation circuit

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, f(X_{IN})=4MHz unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V, f(X_{IN})=4MHz CRT OFF		10	20	mA
		V_{CC}=5.5V, f(X_{IN})=4MHz CRT ON, PLL ON		25	35	
		At wait mode V_{CC}=5.0V		500	800	μA
		At stop mode V_{CC}=5.0V		1	10	μA
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT, P/D, MO	V_{CC}=4.5V I_{OH}=−0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, R, G, B, I, OUT, P/D, MO	V_{CC}=4.5V I_{OL}=0.5mA			0.4	V
	"L" output voltage $P6_0$-$P6_3$, $P4_6$, $P4_7$	V_{CC}=4.5V I_{OL}=0.5mA			0.4	
	"L" output voltage $P2_4$-$P2_7$	V_{CC}=4.5V I_{OL}=10mA			3.0	
	"L" output voltage $P4_4$, $P4_5$	V_{CC}=4.5V I_{OL}=3mA			0.4	
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5.0V		0.5	0.7	V
	Hysteresis (Note) H_{SYNC}, V_{SYNC}, $P3_2$-$P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_4$-$P4_6$	V_{CC}=5.0V		0.5	1.3	
I_{OZH}	"H" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$	V_{CC}=5.5V V_O=5.5V			5	μA
	"H" input leak current $P6_0$-$P6_3$, $P4_6$, $P4_7$	V_{CC}=5.5V V_O=12V			10	
	"H" input leak current P/D	V_{CC}=5.5V V_O=5.5V			1	
I_{OZL}	"L" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_7$, $P6_0$-$P6_3$	V_{CC}=5.5V V_O=0V			5	μA
	"L" input leak current P/D	V_{CC}=5.5V V_O=0V			1	

Note 1. $P3_2$-$P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P4_1$, $P4_2$, $P4_4$-$P4_6$ have the hysteresis when these pins are used as serial I/O ports