# 4556 Group SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

### DESCRIPTION

The 4556 Group is a 4-bit single-chip microcomputer designed with CMOS technology. Its CPU is that of the 4500 series using a simple, high-speed instruction set. The computer is equipped with two 8-bit timers (each timer has one or two reload registers), a 16-bit timer for clock count, interrupts, and oscillation circuit switch function.

The various microcomputers in the 4556 Group include variations of the built-in memory size as shown in the table below.

# FEATURES

<ul> <li>Minimum instruction execution time</li> </ul>	
Mask ROM version	0.5 μs
(at 6 MHz oscillation frequency, in high-speed	d through-mode)
One Time PROM version	0.68 μs
(at 4.4 MHz oscillation frequency, in high-spe	ed through-mode)
<ul> <li>Supply voltage</li> </ul>	
Mask ROM version	1.8 to 5.5 V
One Time PROM version	1.8 to 3.6 V
(It depends on operation source clock, oscilla	tion frequency and op-
eration mode)	

### Timers

Timer 1 8-bit timer with a reload registe
Timer 2 8-bit timer with two reload registers
Timer 3 16-bit timer (fixed dividing frequency
Interrupt
Key-on wakeup function pins
LCD control circuit
Segment output 23
Common output
<ul> <li>Voltage drop detection circuit (only H version)</li> </ul>
Reset occurrence Typ. 1.8 V (Ta = 25 °C
Reset release Typ. 1.9 V (Ta = 25 °C
Watchdog timer
Clock generating circuit
Built-in clock
(on-chip oscillator)
Main clock
(ceramic resonator/RC oscillation)
Sub-clock
(quartz-crystal oscillation)
LED drive directly enabled (port D)

# **APPLICATION**

Remote control transmitter

Part number		ROM (PROM) size	RAM size	Package		
	i art number	(X 10 bits)	(× 4 bits)	i dokuge	i com type	
	M34556M4-XXXFP	4096 words	288 words	42P2R-A	Mask ROM	
dnc	M34556M8-XXXFP	8192 words	288 words	42P2R-A	Mask ROM	
Ū	M34556G8FP (Note)	8192 words	288 words	42P2R-A	One Time PROM	
556	M34556M4H-XXXFP	4096 words	288 words	42P2R-A	Mask ROM	
45	M34556M8H-XXXFP	8192 words	288 words	42P2R-A	Mask ROM	
	M34556G8HFP (Note)	8192 words	288 words	42P2R-A	One Time PROM	

Note: Shipped in blank.



### **PIN CONFIGURATION**



Pin configuration (top view) (4556 Group)



Block diagram (4556 Group)

# PERFORMANCE OVERVIEW

Parameter		r	Function				
Number of basic	M345	56M	4/M8/G8	123			
instructions	M345	56M	4H/M8H/G8H	124			
Minimum	Mask ROM version		M version	0.5 $\mu$ s (at 6 MHz oscillation frequency, in through mode)			
execution time	One 7	Fime	PROM version	0.68 $\mu$ s (at 4.4 MHz oscillation frequency, in through mode)			
Memory sizes	ROM	M3	4556M4	4096 words X 10 bits			
		M34	4556M4H				
		M3	4556M8/G8	8192 words X 10 bits			
		M34	4556M8H/G8H				
	RAM	M3	4556M4/M8/G8	288 words X 4 bits (including LCD display RAM 23 words X 4 bits)			
		M34	1556M4H/M8H/G8H				
Input/Output ports	Do-D	5	I/O	Six independent I/O ports. Input is examined by skip decision. The output structure can be switched by software. Port D5 is also used as INT pin.			
	D6, D	7	Output	Two independent output ports. Ports D6 and D7 are also used as XCIN and XCOUT, respectively.			
	P00-F	<b>2</b> 03	I/O	4-bit I/O port; A pull-up function, a key-on wakeup function and output structure can be switched by software. Ports P00–P03 are also used as SEG21–SEG24, respectively.			
	P10-F	<b>2</b> 13	I/O	4-bit I/O port; A pull-up function, a key-on wakeup function and output structure can be switched by software. Ports P10–P13 are also used as SEG25–SEG28, respectively.			
	P20-F	<b>2</b> 3	I/O	4-bit I/O port; The output structure can be switched by software. Ports P20–P23 are also used as SEG17–SEG20, respectively.			
	C Output		Output	1-bit output; Port C is also used as CNTR pin.			
Timers	Timer	1		8-bit programmable timer with a reload register and has an event counter.			
	Timer	2		8-bit programmable timer with two reload registers and PWM output function.			
	Timer	3		16-bit timer, fixed dividing frequency (timer for clock count)			
	Timer	LC		4-bit timer with a reload register (for LCD clock)			
	Watch	ndog	ı timer	16-bit timer (fixed dividing frequency) (for watchdog)			
LCD control	Selec	tive	bias value	1/2, 1/3 bias			
circuit	Selec	tive	duty value	2, 3, 4 duty			
	Comn	non	output	4			
	Segm	ent	output	23			
	Intern powe	al re r sup	esistor for	2r X 3, 2r X 2, r X 3, r X 2 (r = 80 kΩ, (Ta = 25 °C, Typical value))			
Interrupt	Sourc	es		4 (one for external, three for timer)			
	Nestir	ng		1 level			
Subroutine ne	sting			8 levels			
Device structu	Device structure			CMOS silicon gate			
Package			42-pin plastic molded SSOP (42P2R-A)				
Operating temperature range		ange	–20 °C to 85 °C				
Supply	Supply Mask ROM version		M version	1.8 to 5.5 V (It depends on operation source clock, oscillation frequency and operation mode)			
voltage	One Time PROM version		PROM version	1.8 to 3.6 V (It depends on operation source clock, oscillation frequency and operation mode)			
Power dissipation	Active mode (Mask ROM version)		de M version)	2.2 mA (at room temperature, $VDD = 5 V$ , $f(XIN) = 6 MHz$ , $f(XCIN) = stop$ , $f(RING) = stop$ , $f(STCK) = f(XIN)/1$ )			
(Typ.value)	At clo (Mask	ck o k RO	perating mode M version)	6 $\mu$ A (at room temperature, VDD = 5 V, f(XCIN) = 32 kHz)			
	At RAM back-up (Mask ROM version)		ack-up 0M version)	0.1 $\mu$ A (at room temperature, VDD = 5 V, output transistor is cut-off state)			

### **PIN DESCRIPTION**

Pin	Name	Input/Output	Function
Vdd	Power supply		Connected to a plus power supply.
Vss	Ground		Connected to a 0 V power supply.
CNVss	CNVss		Connect CNVss to Vss and apply "L" (0V) to CNVss certainly.
RESET	Reset input/output	I/O	An N-channel open-drain I/O pin for a system reset. When the SRST instruction, watchdog timer, the built-in power-on reset or the voltage drop detection circuit causes the system to be reset, the RESET pin outputs "L" level.
Xin	Main clock input	Input	I/O pins of the main clock generating circuit. When using a ceramic resonator, connect it between pins XIN and XOUT. A feedback resistor is built-in between them.
Хоит	Main clock output	Output	When using the RC oscillation, connect a resistor and a capacitor to XIN, and leave XOUT pin open.
XCIN	Sub-clock input	Input	I/O pins of the sub-clock generating circuit. Connect a 32.768 kHz quartz-crystal oscilla- tor between pins XCIN and XCOUT. A feedback resistor is built-in between them. XCIN and
Хсоит	Sub-clock output	Output	XCOUT pins are also used as ports D6 and D7, respectively.
D0D5	I/O port D Input is examined by skip decision.	I/O	Each pin of port D has an independent 1-bit wide I/O function. The output structure can be switched to N-channel open-drain or CMOS by software. For input use, set the latch of the specified bit to "1" and select the N-channel open-drain. Port D5 is also used as INT pin.
D6, D7	Output port D	Output	Each pin of port D has an independent 1-bit wide output function. The output struc- ture is N-channel open-drain. Ports D6 and D7 are also used as XCIN pin and XCOUT pin, respectively.
P00–P03	I/O port P0	I/O	Port P0 serves as a 4-bit I/O port. The output structure can be switched to N-channel open-drain or CMOS by software. For input use, set the latch of the specified bit to "1" and select the N-channel open-drain. Port P0 has a key-on wakeup function and a pull-up function. Both functions can be switched by software. Ports P00–P03 are also used as SEG21–SEG24, respectively.
P10-P13	I/O port P1	I/O	Port P1 serves as a 4-bit I/O port. The output structure can be switched to N-channel open-drain or CMOS by software. For input use, set the latch of the specified bit to "1" and select the N-channel open-drain. Port P1 has a key-on wakeup function and a pull-up function. Both functions can be switched by software. Ports P10–P13 are also used as SEG25–SEG28, respectively.
P20-P23	I/O port P2	I/O	Port P2 serves as a 4-bit I/O port. The output structure can be switched to N-channel open-drain or CMOS by software. For input use, set the latch of the specified bit to "1" and select the N-channel open-drain. Ports P20–P23 are also used as SEG17–SEG20, respectively.
Port C	Output port C	Output	1-bit output port. The output structure is CMOS. Port C is also used as CNTR pin.
COM0– COM3	Common output	Output	LCD common output pins. Pins COM <sub>0</sub> and COM <sub>1</sub> are used at 1/2 duty, pins COM <sub>0</sub> – COM <sub>2</sub> are used at 1/3 duty and pins COM <sub>0</sub> –COM <sub>3</sub> are used at 1/4 duty.
SEG0-SEG10 SEG17-SEG28 (Note)	Segment output	Output	LCD segment output pins. SEG0–SEG2 pins are used as VLC3–VLC1 pins, respec- tively. SEG17–SEG28 pins are used as Ports P20–P23, Ports P00–P03 and Ports P10–P13, respectively.
CNTR	Timer input/output	I/O	CNTR pin has the function to input the clock for the timer 1 event counter and to output the PWM signal generated by timer 2.CNTR pin is also used as Port C.
INT	Interrupt input	Input	INT pin accepts external interrupts. They have the key-on wakeup function which can be switched by software. INT pin is also used as Port D5.

Note: SEG11 to SEG16 pins are not existed in the 4556 Group.

### **MULTIFUNCTION**

Pin	Multifunction	Pin	Multifunction	Pin	Multifunction	Pin	Multifunction
XCIN	D6	D6	XCIN	P20	SEG17	SEG17	P20
Хсоит	D7	D7	Хсоит	P21	SEG18	SEG18	P21
P00	SEG21	SEG21	P00	P22	SEG19	SEG19	P22
P01	SEG22	SEG22	P01	P23	SEG20	SEG20	P23
P02	SEG23	SEG23	P02	D5	INT	INT	D5
P03	SEG24	SEG24	P03	С	CNTR	CNTR	С
P10	SEG25	SEG25	P10	SEG0	VLC3	VLC3	SEG0
P11	SEG26	SEG26	P11	SEG1	VLC2	VLC2	SEG1
P12	SEG27	SEG27	P12	SEG2	VLC1	VLC1	SEG2
P13	SEG28	SEG28	P13				

Notes 1: Pins except above have just single function.

Phile except above have just single function.
 The input/output of D5 can be used even when INT is selected. The threshold value is different between port D5 and INT. Accordingly, be careful when the input of both is used.
 The port C "H" output function can be used even when CNTR (output) is selected.



# DEFINITION OF CLOCK AND CYCLE

- Operation source clock
  - The operation source clock is the source clock to operate this product. In this product, the following clocks are used.
  - Clock (f(XIN)) by the external ceramic resonator
  - Clock (f(XIN)) by the external RC oscillation
  - Clock (f(XIN)) by the external input
  - Clock (f(RING)) of the on-chip oscillator which is the internal oscillator
  - Clock (f(XCIN)) by the external quartz-crystal resonator

• System clock (STCK)

The system clock is the basic clock for controlling this product. The system clock is selected by the clock control register MR shown as the table below.

Instruction clock (INSTCK)

The instruction clock is the basic clock for controlling CPU. The instruction clock (INSTCK) is a signal derived by dividing the system clock (STCK) by 3. The one instruction clock cycle generates the one machine cycle.

### Machine cycle

The machine cycle is the standard cycle required to execute the instruction.

Table S	able Selection of system clock						
Register MR				System clock	Operation mode		
MR3	MR2	MR1	MR <sub>0</sub>				
1	1	0	0	f(STCK) = f(RING)/8	Internal frequency divided by 8 mode		
1	0	0	0	f(STCK) = f(RING)/4	Internal frequency divided by 4 mode		
0	1	0	0	f(STCK) = f(RING)/2	Internal frequency divided by 2 mode		
0	0	0	0	f(STCK) = f(RING)	Internal frequency through mode		
1	1	0	1	f(STCK) = f(XIN)/8	High-speed frequency divided by 8 mode		
1	0	0	1	f(STCK) = f(XIN)/4	High-speed frequency divided by 4 mode		
0	1	0	1	f(STCK) = f(XIN)/2	High-speed frequency divided by 2 mode		
0	0	0	1	f(STCK) = f(XIN)	High-speed through mode		
1	1	1	0	f(STCK) = f(XCIN)/8	Low-speed frequency divided by 8 mode		
1	0	1	0	f(STCK) = f(XCIN)/4	Low-speed frequency divided by 4 mode		
0	1	1	0	f(STCK) = f(XCIN)/2	Low-speed frequency divided by 2 mode		
0	0	1	0	f(STCK) = f(XCIN)	Low-speed through mode		

Note: The f(RING)/8 is selected after system is released from reset.

# PORT FUNCTION

Port Pin		Input	Output structure	I/O	Control	Control	Bomark
FUIL	F III	Output	Output structure	unit	instructions	registers	Kellialk
Port D	D0–D4, D5/INT	I/O	N-channel open-drain/	1	SD, RD	FR1, FR2	Output structure selection
		(6)	CMOS		SZD	l1, K2	function (programmable)
					CLD		
	XCIN/D6, XCOUT/D7	Output	N-channel open-drain	1		RG	
		(2)					
Port P0	P00/SEG21-P03/SEG24	I/O	N-channel open-drain/	4	OP0A	FR0, PU0	Built-in pull-up functions, key-on
		(4)	CMOS		IAP0	K0	wakeup functions and output
						C1	structure selection function
							(programmable)
Port P1	P10/SEG25-P13/SEG28	I/O	N-channel open-drain/	4	OP1A	FR0, PU1	Built-in pull-up functions, key-on
		(4)	CMOS		IAP1	K0, K1	wakeup functions and output
						C2	structure selection function
							(programmable)
Port P2	P20/SEG17-P23/SEG20	I/O	N-channel open-drain/	4	OP2A	FR2	Output structure selection func
		(4)	CMOS		IAP2	L3	tion (programmable)
Port C	C/CNTR	Output	CMOS	1	RCP	W1	
		(1)			SCP		

### **CONNECTIONS OF UNUSED PINS**

Pin	Connection	Usage condition
Xin	Connect to Vss.	RC oscillator is not selected
Хоит	Open.	
XCIN/D6	Connect to Vss.	
XCOUT/D7	Open.	
D0D4	Open.	
	Connect to Vss.	N-channel open-drain is selected for the output structure.
D5/INT	Open.	INT pin input is disabled.
	Connect to Vss.	N-channel open-drain is selected for the output structure.
C/CNTR	Open.	CNTR input is not selected for timer 1 count source.
P00/SEG21-	Open.	The key-on wakeup function is invalid.
P03/SEG24	Connect to Vss.	Segment output is not selected.
		N-channel open-drain is selected for the output structure.
		Pull-up transistor is OFF.
		The key-on wakeup function is invalid.
P10/SEG25-	Open.	The key-on wakeup function is invalid.
P13/SEG28	Connect to Vss.	Segment output is not selected.
		N-channel open-drain is selected for the output structure.
		Pull-up transistor is OFF.
		The key-on wakeup function is invalid.
P20/SEG17-	Open.	
P23/SEG20	Connect to Vss.	Segment output is not selected.
		N-channel open-drain is selected for the output structure.
COM0-COM3	Open.	
SEG0/VLC3	Open.	SEGo pin is selected.
SEG1/VLC2	Open.	SEG1 pin is selected.
SEG2/VLC1	Open.	SEG2 pin is selected.
SEG3-SEG10	Open.	
(Note)		

Note: SEG11 to SEG16 pins are not existed in the 4556 Group.

(Note when connecting to Vss and VDD) • Connect the unused pins to Vss and VDD using the thickest wire at the shortest distance against noise.



### PORT BLOCK DIAGRAMS



Port block diagram (1)











Port block diagram (5)



Port block diagram (6)





Port block diagram (7)



Block diagram of external interrupt



# FUNCTION BLOCK OPERATIONS CPU

### (1) Arithmetic logic unit (ALU)

The arithmetic logic unit ALU performs 4-bit arithmetic such as 4bit data addition, comparison, AND operation, OR operation, and bit manipulation.

### (2) Register A and carry flag

Register A is a 4-bit register used for arithmetic, transfer, exchange, and I/O operation.

Carry flag CY is a 1-bit flag that is set to "1" when there is a carry with the AMC instruction (Figure 1).

It is unchanged with both A n instruction and AM instruction. The value of A<sub>0</sub> is stored in carry flag CY with the RAR instruction (Figure 2).

Carry flag CY can be set to "1" with the SC instruction and cleared to "0" with the RC instruction.

### (3) Registers B and E

Register B is a 4-bit register used for temporary storage of 4-bit data, and for 8-bit data transfer together with register A.

Register E is an 8-bit register. It can be used for 8-bit data transfer with register B used as the high-order 4 bits and register A as the low-order 4 bits (Figure 3).

Register E is undefined after system is released from reset and returned from the power down mode. Accordingly, set the initial value.

### (4) Register D

Register D is a 3-bit register.

It is used to store a 7-bit ROM address together with register A and is used as a pointer within the specified page when the TABP p, BLA p, or BMLA p instruction is executed (Figure 4).

Also, when the TABP p instruction is executed at UPTF flag = "1", the high-order 2 bits of ROM reference data is stored to the low-order 2 bits of register D, the high-order 1 bit of register D is "0". When the TABP p instruction is executed at UPTF flag = "0", the contents of register D remains unchanged. The UPTF flag is set to "1" with the SUPT instruction and cleared to "0" with the RUPT instruction. The initial value of UPTF flag is "0".

Register D is undefined after system is released from reset and returned from the power down mode. Accordingly, set the initial value.



Fig. 1 AMC instruction execution example



Fig. 2 RAR instruction execution example



Fig. 3 Registers A, B and register E



### (5) Stack registers (SKs) and stack pointer (SP)

Stack registers (SKs) are used to temporarily store the contents of program counter (PC) just before branching until returning to the original routine when;

- branching to an interrupt service routine (referred to as an interrupt service routine),
- performing a subroutine call, or
- executing the table reference instruction (TABP p).

Stack registers (SKs) are eight identical registers, so that subroutines can be nested up to 8 levels. However, one of stack registers is used respectively when using an interrupt service routine and when executing a table reference instruction. Accordingly, be careful not to over the stack when performing these operations together. The contents of registers SKs are destroyed when 8 levels are exceeded.

The register SK nesting level is pointed automatically by 3-bit stack pointer (SP). The contents of the stack pointer (SP) can be transferred to register A with the TASP instruction.

Figure 5 shows the stack registers (SKs) structure.

Figure 6 shows the example of operation at subroutine call.

### (6) Interrupt stack register (SDP)

Interrupt stack register (SDP) is a 1-stage register. When an interrupt occurs, this register (SDP) is used to temporarily store the contents of data pointer, carry flag, skip flag, register A, and register B just before an interrupt until returning to the original routine. Unlike the stack registers (SKs), this register (SDP) is not used when executing the subroutine call instruction and the table reference instruction.

# (7) Skip flag

Skip flag controls skip decision for the conditional skip instructions and continuous described skip instructions. When an interrupt occurs, the contents of skip flag is stored automatically in the interrupt stack register (SDP) and the skip condition is retained.

Program counter	r (PC)				
Executing <b>BM</b> instruction	Executing <b>RT</b> instruction				
SK0	(SP) = 0				
SK1	(SP) = 1				
SK2	(SP) = 2				
SK3	(SP) = 3				
SK4	(SP) = 4				
SK5	(SP) = 5				
SK6	(SP) = 6				
SK7	(SP) = 7				
Stack pointer (SP) points "7" at reset or returning from power down mode. It points "0" by executing the first <b>BM</b> instruction, and the contents of program counter is stored in SKo. When the <b>BM</b> instruction is executed after eight stack registers are used ((SP) = 7), (SP) = 0 and the contents of SKo is destroyed.					





Fig. 6 Example of operation at subroutine call



# (8) Program counter (PC)

Program counter (PC) is used to specify a ROM address (page and address). It determines a sequence in which instructions stored in ROM are read. It is a binary counter that increments the number of instruction bytes each time an instruction is executed. However, the value changes to a specified address when branch instructions, subroutine call instructions, return instructions, or the table reference instruction (TABP p) is executed.

Program counter consists of PCH (most significant bit to bit 7) which specifies to a ROM page and PCL (bits 6 to 0) which specifies an address within a page. After it reaches the last address (address 127) of a page, it specifies address 0 of the next page (Figure 7).

Make sure that the  $\mathsf{PCH}$  does not specify after the last page of the built-in ROM.

# (9) Data pointer (DP)

Data pointer (DP) is used to specify a RAM address and consists of registers Z, X, and Y. Register Z specifies a RAM file group, register X specifies a file, and register Y specifies a RAM digit (Figure 8).

Register Y is also used to specify the port D bit position.

When using port D, set the port D bit position to register Y certainly and execute the SD, RD, or SZD instruction (Figure 9).

### Note

Register Z of data pointer is undefined after system is released from reset.

Also, registers Z, X and Y are undefined in the power down mode. After system is returned from the power down mode, set these registers.



Fig. 7 Program counter (PC) structure



Fig. 8 Data pointer (DP) structure



Fig. 9 SD instruction execution example

### **PROGRAM MEMORY (ROM)**

The program memory is a mask ROM. 1 word of ROM is composed of 10 bits. ROM is separated every 128 words by the unit of page (addresses 0 to 127). Table 1 shows the ROM size and pages. Figure 10 shows the ROM map of M34556ED.

Table	1	ROM	size	and	pages
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Part number	ROM (PROM) size (X 10 bits)	Pages
M34556M4	4096 words	32 (0 to 31)
M34556M4H		
M34556M8	8192 words	64 (0 to 63)
M34556M8H		
M34556G8	1	
M34556G8H		

A part of page 1 (addresses 008016 to 00FF16) is reserved for interrupt addresses (Figure 11). When an interrupt occurs, the address (interrupt address) corresponding to each interrupt is set in the program counter, and the instruction at the interrupt address is executed. When using an interrupt service routine, write the instruction generating the branch to that routine at an interrupt address.

Page 2 (addresses 010016 to 017F16) is the special page for subroutine calls. Subroutines written in this page can be called from any page with the 1-word instruction (BM). Subroutines extending from page 2 to another page can also be called with the BM instruction when it starts on page 2.

ROM pattern (bits 7 to 0) of all addresses can be used as data areas with the TABP p instruction.



Fig. 10 ROM map of M34556M8/M8H/G8/G8H



Fig. 11 Page 1 (addresses 008016 to 00FF16) structure



### DATA MEMORY (RAM)

1 word of RAM is composed of 4 bits, but 1-bit manipulation (with the SB j, RB j, and SZB j instructions) is enabled for the entire memory area. A RAM address is specified by a data pointer. The data pointer consists of registers Z, X, and Y. Set a value to the data pointer certainly when executing an instruction to access RAM (also, set a value after system returns from power down mode).

RAM includes the area for LCD.

When writing "1" to a bit corresponding to displayed segment, the segment is turned on.

Table 2 shows the RAM size. Figure 12 shows the RAM map.

### Note

Register Z of data pointer is undefined after system is released from reset.

Also, registers Z, X and Y are undefined in the RAM back-up. After system is returned from the power down mode, set these registers.

### Table 2 RAM size

Part number	RAM size
M34556M4/M4H	288 words X 4 bits (1152 bits)
M34556M8/M8H	
M34556G8/G8H	



### Fig. 12 RAM map

### **INTERRUPT FUNCTION**

The interrupt type is a vectored interrupt branching to an individual address (interrupt address) according to each interrupt source. An interrupt occurs when the following 3 conditions are satisfied.

• An interrupt activated condition is satisfied (request flag = "1")

- Interrupt enable bit is enabled ("1")
- Interrupt enable flag is enabled (INTE = "1")

Table 3 shows interrupt sources. (Refer to each interrupt request flag for details of activated conditions.)

# (1) Interrupt enable flag (INTE)

The interrupt enable flag (INTE) controls whether the every interrupt enable/disable. Interrupts are enabled when INTE flag is set to "1" with the EI instruction and disabled when INTE flag is cleared to "0" with the DI instruction. When any interrupt occurs, the INTE flag is automatically cleared to "0," so that other interrupts are disabled until the EI instruction is executed.

### (2) Interrupt enable bit

Use an interrupt enable bit of interrupt control registers V1 and V2 to select the corresponding interrupt or skip instruction.

Table 4 shows the interrupt request flag, interrupt enable bit and skip instruction.

Table 5 shows the interrupt enable bit function.

### (3) Interrupt request flag

When the activated condition for each interrupt is satisfied, the corresponding interrupt request flag is set to "1." Each interrupt request flag is cleared to "0" when either;

• an interrupt occurs, or

• the next instruction is skipped with a skip instruction.

Each interrupt request flag is set when the activated condition is satisfied even if the interrupt is disabled by the INTE flag or its interrupt enable bit. Once set, the interrupt request flag retains set until a clear condition is satisfied.

Accordingly, an interrupt occurs when the interrupt disable state is released while the interrupt request flag is set.

If more than one interrupt request flag is set when the interrupt disable state is released, the interrupt priority level is as follows shown in Table 3.

#### Table 3 Interrupt sources

Priority level	Interrupt name	Activated condition	Interrupt address
1	External 0 interrupt	Level change of INT pin	Address 0 in page 1
2	Timer 1 interrupt	Timer 1 underflow	Address 4 in page 1
3	Timer 2 interrupt	Timer 2 underflow	Address 6 in page 1
4	Timer 3 interrupt	Timer 3 underflow	Address 8 in page 1

# Table 4 Interrupt request flag, interrupt enable bit and skip in-

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Interrupt name	Request flag	uest flag Skip instruction	
External 0 interrupt	EXF0	SNZ0	V10
Timer 1 interrupt	T1F	SNZT1	V12
Timer 2 interrupt	T2F	SNZT2	V13
Timer 3 interrupt	T3F	SNZT3	V20

### Table 5 Interrupt enable bit function

Interrupt enable bit	Occurrence of interrupt	Skip instruction
1	Enabled	Invalid
0	Disabled	Valid



### (4) Internal state during an interrupt

The internal state of the microcomputer during an interrupt is as follows (Figure 14).

- Program counter (PC)
- An interrupt address is set in program counter. The address to be executed when returning to the main routine is automatically stored in the stack register (SK).
- Interrupt enable flag (INTE)
- INTE flag is cleared to "0" so that interrupts are disabled.
- Interrupt request flag
   Only the request flag for the current interrupt source is cleared to "0."
- Data pointer, carry flag, skip flag, registers A and B
- The contents of these registers and flags are stored automatically in the interrupt stack register (SDP).

# (5) Interrupt processing

When an interrupt occurs, a program at an interrupt address is executed after branching a data store sequence to stack register. Write the branch instruction to an interrupt service routine at an interrupt address.

Use the RTI instruction to return from an interrupt service routine. Interrupt enabled by executing the EI instruction is performed after executing 1 instruction (just after the next instruction is executed). Accordingly, when the EI instruction is executed just before the RTI instruction, interrupts are enabled after returning the main routine. (Refer to Figure 13)



Fig. 13 Program example of interrupt processing









### (6) Interrupt control registers

Interrupt control register V1

Interrupt enable bits of external 0, timer 1 and timer 2 are assigned to register V1. Set the contents of this register through register A with the TV1A instruction. The TAV1 instruction can be used to transfer the contents of register V1 to register A.

### Table 6 Interrupt control registers

• Interrupt control register V2

The timer 3 interrupt enable bit is assigned to register V2. Set the contents of this register through register A with the TV2A instruction. The TAV2 instruction can be used to transfer the contents of register V2 to register A.

Interrupt control register V1		at reset : 00002		at power down : 00002	R/W TAV1/TV1A
V13 Timer 2 interrupt enable bit		0	Interrupt disabled (	SNZT2 instruction is valid)	
		1	Interrupt enabled (	SNZT2 instruction is invalid)	
V/10 Timor 1 interrupt enable k	Timor 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)		
V 12		1	Interrupt enabled (	SNZT1 instruction is invalid)	
1/14	Not used	0	This hit has no function, but read/units is enabled		
		1	This bit has no lun	ction, but read/write is enabled.	
	External 0 interrupt enable bit	0	Interrupt disabled (	(SNZ0 i <mark>nstruction is va</mark> lid)	
VIU		1	Interrupt enabled (	SNZ0 instruction is invalid)	

Interrupt control register V2		at reset : 00002		at power down : 00002	R/W TAV2/TV2A
V23 Not used		0	This bit has no fun	ction, but read/write is enabled.	
		1			
Not used	Notused	0	This bit has no function, but read/write is enabled.		
VZZ	Notused	1			
1/0.	Not word		This bit has no fun	ction, but road/write is enabled	
		1		ction, but read/write is enabled.	
	Timer 2 internunt en able bit	0	Interrupt disabled (	SNZT3 instruction is valid)	
V20		1	Interrupt enabled (	SNZT3 instruction is invalid)	

Note: "R" represents read enabled, and "W" represents write enabled.



### (7) Interrupt sequence

Interrupts only occur when the respective INTE flag, interrupt enable bits (V10, V12, V13, V20), and interrupt request flag are "1." The interrupt actually occurs 2 to 3 machine cycles after the cycle in which all three conditions are satisfied. The interrupt occurs after 3 machine cycles only when the three interrupt conditions are satisfied on execution of other than one-cycle instructions (Refer to Figure 16).



Fig. 16 Interrupt sequence



### **EXTERNAL INTERRUPTS**

The 4556 Group has the external 0 interrupt.

An external interrupt request occurs when a valid waveform is input to an interrupt input pin (edge detection).

The external interrupt can be controlled with the interrupt control register I1.

### Table 7 External interrupt activated conditions

Name	Input pin	Activated condition	Valid waveform selection bit
External 0 interrupt	D5/INT	When the next waveform is input to D5/INT pin	l11
		<ul> <li>Falling waveform ("H"→"L")</li> </ul>	l12
		<ul> <li>Rising waveform ("L"→"H")</li> </ul>	
		<ul> <li>Both rising and falling waveforms</li> </ul>	



Fig. 17 External interrupt circuit structure



### (1) External 0 interrupt request flag (EXF0)

External 0 interrupt request flag (EXF0) is set to "1" when a valid waveform is input to D5/INT pin.

The valid waveforms causing the interrupt must be retained at their level for 4 clock cycles or more of the system clock (Refer to Figure 16). The state of EXF0 flag can be examined with the skip instruction (SNZ0). Use the interrupt control register V1 to select the interrupt or the skip instruction. The EXF0 flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with the skip instruction.

• External 0 interrupt activated condition

External 0 interrupt activated condition is satisfied when a valid waveform is input to D5/INT pin.

The valid waveform can be selected from rising waveform, falling waveform or both rising and falling waveforms. An example of how to use the external 0 interrupt is as follows.

- ① Set the bit 3 of register I1 to "1" for the INT pin to be in the input enabled state.
- $\ensuremath{\textcircled{O}}$  Select the valid waveform with the bits 1 and 2 of register I1.
- $\ensuremath{\textcircled{3}}$  Clear the EXF0 flag to "0" with the SNZ0 instruction.
- ④ Set the NOP instruction for the case when a skip is performed with the SNZ0 instruction.
- Set both the external 0 interrupt enable bit (V10) and the INTE flag to "1."

The external 0 interrupt is now enabled. Now when a valid waveform is input to the D5/INT pin, the EXF0 flag is set to "1" and the external 0 interrupt occurs.

### Table 8 External interrupt control register

#### R/W at reset : 00002 Interrupt control register I1 at power down : state retained TAI1/TI1A 0 INT pin input disabled I13 INT pin input control bit (Note 2) 1 INT pin input enabled Falling waveform/"L" level ("L" level is recognized with the SNZIO 0 Interrupt valid waveform for INT pin/ instruction) I12 return level selection bit (Note 2) Rising waveform/"H" level ("H" level is recognized with the SNZI0 1 instruction) 0 One-sided edge detected 111 INT pin edge detection circuit control bit 1 Both edges detected INT pin Timer 1 count start synchronous 0 Timer 1 count start synchronous circuit not selected 110 circuit selection bit 1 Timer 1 count start synchronous circuit selected

(2) External interrupt control registers

Register I1 controls the valid waveform for the external 0 inter-

rupt. Set the contents of this register through register A with the

TI1A instruction. The TAI1 instruction can be used to transfer the

• Interrupt control register I1

contents of register I1 to register A.

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: When the contents of these bits (I12, I13) are changed, the external interrupt request flag (EXF0) may be set.

### (3) Notes on External 0 interrupts

① Note [1] on bit 3 of register I1
 When the input of the INT pin is controlled with the bit 3 of register I1 in software, be careful about the following notes.

Depending on the input state of the D5/INT pin, the external 0 interrupt request flag (EXF0) may be set when the bit 3 of register I1 is changed. In order to avoid the occurrence of an unexpected interrupt, clear the bit 0 of register V1 to "0" (refer to Figure 18<sup>(1)</sup>) and then, change the bit 3 of register I1.

In addition, execute the SNZ0 instruction to clear the EXF0 flag to "0" after executing at least one instruction (refer to Figure 18<sup>(2)</sup>). Also, set the NOP instruction for the case when a skip is performed with the SNZ0 instruction (refer to Figure 18<sup>(3)</sup>).

•		
LA	4	; ( <b>XXX</b> 02)
TV1A		; The SNZ0 instruction is valid0
LA	8	; (1XXX2)
TI1A		; Control of INT pin input is changed
NOP		
SNZ0		; The SNZ0 instruction is executed
		(EXF0 flag cleared)
NOP		
:		

Fig. 18 External 0 interrupt program example-1

2 Note [2] on bit 3 of register I1

When the bit 3 of register I1 is cleared to "0", the RAM back-up mode is selected and the input of INT pin is disabled, be careful about the following notes.

• When the key-on wakeup function of INT pin is not used (register K20 = "0"), clear bits 2 and 3 of register [1 before system enters to the power down mode. (refer to Figure 19①).

:	
LA 0	; (00 <b>XX</b> 2)
TI1A	; Input of INT disabled①
DI	
EPOF	
POF2	; power down mode
:	
X : these	bits are not used here.

Fig. 19 External 0 interrupt program example-2

#### 3 Note on bit 2 of register I1

When the interrupt valid waveform of the D5/INT pin is changed with the bit 2 of register 11 in software, be careful about the following notes.

Depending on the input state of the D5/INT pin, the external 0 interrupt request flag (EXF0) may be set when the bit 2 of register I1 is changed. In order to avoid the occurrence of an unexpected interrupt, clear the bit 0 of register V1 to "0" (refer to Figure 20<sup>(1)</sup>) and then, change the bit 2 of register I1.

In addition, execute the SNZ0 instruction to clear the EXF0 flag to "0" after executing at least one instruction (refer to Figure 20<sup>(2)</sup>). Also, set the NOP instruction for the case when a skip is performed with the SNZ0 instruction (refer to Figure 20<sup>(3)</sup>).







### TIMERS

The 4556 Group has the following timers.

• Programmable timer

The programmable timer has a reload register and enables the frequency dividing ratio to be set. It is decremented from a setting value n. When it underflows (count to n + 1), a timer interrupt request flag is set to "1," new data is loaded from the reload register, and count continues (auto-reload function).

• Fixed dividing frequency timer

The fixed dividing frequency timer has the fixed frequency dividing ratio (n). An interrupt request flag is set to "1" after every n count of a count pulse.

# FF16 n : Counter initial value Count starts Reload Reload n The contents of counter 1st underflow 2nd underflow 0016 Time n+1 count n+1 count Timer interrupt "೧ request flag An interrupt occurs or a skip instruction is executed.

Fig. 21 Auto-reload function

The 4556 Group timer consists of the following circuits.

- Prescaler : 8-bit programmable timer
- Timer 1 : 8-bit programmable timer
- Timer 2 : 8-bit programmable timer
- Timer 3 : 16-bit fixed dividing frequency timer
- Timer LC : 4-bit programmable timer
- Watchdog timer : 16-bit fixed dividing frequency timer (Timers 1, 2, and 3 have the interrupt function, respectively)

Prescaler and timers 1, 2, 3 and LC can be controlled with the timer control registers PA, W1 to W4. The watchdog timer is a free counter which is not controlled with the control register. Each function is described below.



### Table 9 Function related timers

Circuit	Structure	Count source	Frequency dividing ratio	Use of output signal	Control register
Prescaler	8-bit programmable	Instruction clock (INSTCK)	1 to 256	• Timer 1, 2, and 3 count sources	PA
	binary down counter				
Timer 1	8-bit programmable	PWM output (PWMOUT)	1 to 256	CNTR output control	W1
	binary down counter	Prescaler output (ORCLK)		Timer 1 interrupt	
	(link to INT input)	Timer 3 underflow			
		(T3UDF)			
		CNTR input			
Timer 2	8-bit programmable	• XIN input	1 to 256	Timer 1 count source	W2
	binary down counter	Prescaler output (ORCLK)		CNTR output	
	(PWM output function)	divided by 2		Timer 2 interrupt	
Timer 3	16-bit fixed dividing	XCIN input	8192	Timer 1 count source	W3
	frequency	• ORCLK	16384	Timer 3 interrupt	
			32768	<ul> <li>Timer LC count source</li> </ul>	
			65536		
Timer LC	4-bit programmable	Bit 4 of timer 3	1 to 16	LCD clock	W4
	binary down counter	System clock (STCK)			
Watchdog	16-bit fixed dividing	Instruction clock (INSTCK)	65534 🬰	System reset (count twice)	
timer	frequency			WDF flag decision	







Fig. 23 Timer structure (2)

### Table 10 Timer related registers

Timer control register PA		at reset : 02		at power down : 02	W TPAA
PA <sub>0</sub>	Prescaler control bit	0	Stop (state retaine	d)	
FAU		1	Operating		

Timer control register W1			at reset : 00002		at power down : state retained	R/W TAW1/TW1A
W13	Timer 1 count auto-stop circuit selection	(	C	Timer 1 count auto	-stop circuit not selected	
	bit (Note 2)	1		Timer 1 count auto	-stop circuit selected	
W/12	W12 Timer 1 control bit		C	Stop (state retained	(b	
VV12			1	Operating		
		W11	W10		Count source	
W11		0	0	PWM signal (PWM	OUT)	
	Timer 1 count source selection bits	0	1	Prescaler output (C	DRCLK)	
W10	(Note 3)	1	0	Timer 3 underflow	signal (T3UDF)	
			1	CNTR input		

Timer control register W2		at reset : 00002		at power down : 00002	R/W TAW2/TW2A	
W23	CNTR pin output control bit	0	CNTR pin output invalid			
		1	CNTR pin o <mark>ut</mark> put valid			
W22	PWM signal interrupt valid waveform/ return level selection bit	0	PWM signal "H" interval expansion function invalid			
		1	PWM signal "H" interval expansion function valid			
W21	Timer 2 control bit	0	Stop (state retained)			
		1	Operating			
W20	Timer 2 count soruce selection bit	0	XIN input			
		1	Prescaler output (ORCLK)/2 signal output			

Timer control register W3			at reset : 00002		at power down : state retained	R/W TAW3/TW3A
W33	Timer 3 count auto-stop circuit selection bit	(	C	XCIN input		
			1 Prescaler output (ORCLK)			
W32	Timer 3 control bit	0		Stop (Initial state)		
			1	Operating		
W31 W30	Timer 3 count value selection bits	W31	W30	Count value		
		0	0	Underflow occurs every 8192 counts		
		0	1	Underflow occurs every 16384 counts		
		1	0	Underflow occurs every 32768 counts		
		1 1		Underflow occurs every 65536 counts		

Timer control register W4		at reset : 00002		at power down : state retained	R/W TAW4/TW4A	
W43	Timer LC control bit	0	Stop (state retained)			
		1	Operating			
W42	Timer LC count source selection bit	0	Bit 4 (T34) of timer 3			
		1	System clock (STCK)			
W41	CNTR output auto-control circuit	0	CNTR output auto-control circuit not selected			
	selection bit	1	CNTR output auto-control circuit selected			
W40	CNTR pin input count edge selection bit	0	Falling edge			
		1	Rising edge			

Notes 1: "R" represents read enabled, and "W" represents write enabled.

This function is valid only when the timer 1 count start synchronous circuit is selected (I10="1").
 Port C output is invalid when CNTR input is selected for the timer 1 count source.



### (1) Timer control registers

### Timer control register PA

Register PA controls the count operation of prescaler. Set the contents of this register through register A with the TPAA instruction.

Timer control register W1

Register W1 controls the selection of timer 1 count auto-stop circuit, and the count operation and count source of timer 1. Set the contents of this register through register A with the TW1A instruction. The TAW1 instruction can be used to transfer the contents of register W1 to register A.

• Timer control register W2

Register W2 controls the CNTR output, the expansion of "H" interval of PWM output, and the count operation and count source of timer 2. Set the contents of this register through register A with the TW2A instruction. The TAW2 instruction can be used to transfer the contents of register W2 to register A.

• Timer control register W3

Register W3 controls the count operation and count source of timer 3. Set the contents of this register through register A with the TW5A instruction. The TAW3 instruction can be used to transfer the contents of register W3 to register A.

• Timer control register W4

Register W4 controls the operation and count source of timer LC, the selection of CNTR output auto-control circuit and the count edge of CNTR input. Set the contents of this register through register A with the TW4A instruction. The TAW4 instruction can be used to transfer the contents of register W4 to register A...

### (2) Prescaler (interrupt function)

Prescaler is an 8-bit binary down counter with the prescaler reload register RPS. Data can be set simultaneously in prescaler and the reload register RPS with the TPSAB instruction. Data can be read from reload register RPS with the TABPS instruction.

Stop counting and then execute the TPSAB or TABPS instruction to read or set prescaler data.

Prescaler starts counting after the following process;

① set data in prescaler, and

② set the bit 0 of register PA to "1."

When a value set in reload register RPS is n, prescaler divides the count source signal by n + 1 (n = 0 to 255).

Count source for prescaler is the instruction clock (INSTCK).

Once count is started, when prescaler underflows (the next count pulse is input after the contents of prescaler becomes "0"), new data is loaded from reload register RPS, and count continues (auto-reload function).

The output signal (ORCLK) of prescaler can be used for timer 1, 2, and 3 count sources.

# (3) Timer 1 (interrupt function)

Timer 1 is an 8-bit binary down counter with the timer 1 reload register (R1). Data can be set simultaneously in timer 1 and the reload register (R1) with the T1AB instruction. Data can be written to reload register (R1) with the TR1AB instruction. Data can be read from timer 1 with the TAB1 instruction.

Stop counting and then execute the T1AB or TAB1 instruction to read or set timer 1 data.

When executing the TR1AB instruction to set data to reload register R1 while timer 1 is operating, avoid a timing when timer 1 underflows.

Timer 1 starts counting after the following process;

- ① set data in timer 1
- 2 set count source by bits 0 and 1 of register W1, and
- 3 set the bit 2 of register W1 to "1."

When a value set in reload register R1 is n, timer 1 divides the count source signal by n + 1 (n = 0 to 255).

Once count is started, when timer 1 underflows (the next count pulse is input after the contents of timer 1 becomes "0"), the timer 1 interrupt request flag (T1F) is set to "1," new data is loaded from reload register R1, and count continues (auto-reload function).

INT pin input can be used as the start trigger for timer 1 count operation by setting the bit 0 of register I1 to "1."

Also, in this time, the auto-stop function by timer 1 underflow can be performed by setting the bit 3 of register W1 to "1."



### (4) Timer 2 (interrupt function)

Timer 2 is an 8-bit binary down counter with two timer 2 reload registers (R2L, R2H). Data can be set simultaneously in timer 2 and the reload register R2L with the T2AB instruction. Data can be set in the reload register R2H with the T2HAB instruction. The contents of reload register R2L set with the T2AB instruction can be set to timer 2 again with the T2R2L instruction. Data can be read from timer 2 with the TAB2 instruction.

Stop counting and then execute the T2AB or TAB2 instruction to read or set timer 2 data.

When executing the T2HAB instruction to set data to reload register R2H while timer 2 is operating, avoid a timing when timer 2 underflows.

Timer 2 starts counting after the following process;

① set data in timer 2

2 set count source by bit 0 of register W2, and

③ set the bit 1 of register W2 to "1."

When a value set in reload register R2L is n, timer 2 divides the count source signal by n + 1 (n = 0 to 255).

Once count is started, when timer 2 underflows (the next count pulse is input after the contents of timer 2 becomes "0"), the timer 2 interrupt request flag (T2F) is set to "1," new data is loaded from reload register R2L, and count continues (auto-reload function). When bit 3 of register W2 is set to "1", timer 2 reloads data from re-

load register R2L and R2H alternately each underflow.

Timer 2 generates the PWM signal (PWMOUT) of the "L" interval set as reload register R2L, and the "H" interval set as reload register R2H. The PWM signal (PWMOUT) is output from CNTR pin.

When bit 2 of register W2 is set to "1" at this time, the interval (PWM signal "H" interval) set to reload register R2H for the counter of timer 2 is extended for a half period of count source.

In this case, when a value set in reload register R2H is n, timer 2 divides the count source signal by n + 1.5 (n = 1 to 255).

When this function is used, set "1" or more to reload register R2H. When bit 1 of register W4 is set to "1", the PWM signal output to CNTR pin is switched to valid/invalid each timer 1 underflow. However, when timer 1 is stopped (bit 2 of register W1 is cleared to "0"), this function is canceled.

Even when bit 1 of a register W2 is cleared to "0" in the "H" interval of PWM signal, timer 2 does not stop until it next timer 2 underflow. When clearing bit 1 of register W2 to "0" to stop timer 2, avoid a timing when timer 2 underflows.

### (5) Timer 3 (interrupt function)

Timer 3 is a 16-bit binary down counter.

Timer 3 starts counting after the following process;

set count value by bits 0 and 1 of register W3,

 $\ensuremath{\textcircled{@}}$  set count source by bit 3 of register W3, and

3 set the bit 2 of register W3 to "1."

Once count is started, when timer 3 underflows (the set count value is counted), the timer 3 interrupt request flag (T3F) is set to "1," and count continues.

Bit 4 of timer 3 can be used as the timer LC count source for the LCD clock generating.

When bit 2 of register W3 is cleared to "0", timer 3 is initialized to "FFFF16" and count is stopped.

Timer 3 can be used as the counter for clock because it can be operated at clock operating mode (POF instruction execution). When timer 3 underflow occurs at clock operating mode, system returns from the power down state.

When operating timer 3 during clock operating mode, set 1 cycle or more of count source to the following period; from setting bit 2 of register W3 to "1" till executing the POF instruction.

# (6) Timer LC

Timer LC is a 4-bit binary down counter with the timer LC reload register (RLC). Data can be set simultaneously in timer LC and the reload register (RLC) with the TLCA instruction. Data cannot be read from timer LC. Stop counting and then execute the TLCA instruction to set timer LC data.

Timer LC starts counting after the following process;

① set data in timer LC,

② select the count source with the bit 2 of register W4, and

 $\ensuremath{\textcircled{}}$  3 set the bit 3 of register W4 to "1."

When a value set in reload register RLC is n, timer LC divides the count source signal by n + 1 (n = 0 to 15).

Once count is started, when timer LC underflows (the next count pulse is input after the contents of timer LC becomes "0"), new data is loaded from reload register RLC, and count continues (auto-reload function).

Timer LC underflow signal divided by 2 can be used for the LCD clock.

### (7) Timer input/output pin (C/CNTR pin)

CNTR pin is used to input the timer 1 count source and output the PWM signal generated by timer 2. When the PWM signal is output from C/CNTR pin, set "0" to the output latch of port C.

The selection of CNTR output signal can be controlled by bit 3 of register W2.

When the CNTR input is selected for timer 1 count source, timer 1 counts the waveform of CNTR input selected by bit 0 of register W4. Also, when the CNTR input is selected, the output of port C is invalid (high-impedance state).

# (8) Timer interrupt request flags (T1F, T2F, T3F)

Each timer interrupt request flag is set to "1" when each timer underflows. The state of these flags can be examined with the skip instructions (SNZT1, SNZT2, SNZT3).

Use the interrupt control register V1, V2 to select an interrupt or a skip instruction.

An interrupt request flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with a skip instruction.

# (9) Count start synchronization circuit (timer 1)

Timer 1 has the count start synchronous circuit which synchronizes the input of INT pin, and can start the timer count operation.

Timer 1 count start synchronous circuit function is selected by setting the bit 0 of register I1 to "1" and the control by INT pin input can be performed.

When timer 1 count start synchronous circuit is used, the count start synchronous circuit is set, the count source is input to each timer by inputting valid waveform to INT pin.

The valid waveform of INT pin to set the count start synchronous circuit is the same as the external interrupt activated condition.

Once set, the count start synchronous circuit is cleared by clearing the bit I10 to "0" or reset.

However, when the count auto-stop circuit is selected, the count start synchronous circuit is cleared (auto-stop) at the timer 1 underflow.

### (10) Count auto-stop circuit (timer 1)

Timer 1 has the count auto-stop circuit which is used to stop timer 1 automatically by the timer 1 underflow when the count start synchronous circuit is used.

The count auto-stop cicuit is valid by setting the bit 3 of register W1 to "1". It is cleared by the timer 1 underflow and the count source to timer 1 is stopped.

This function is valid only when the timer 1 count start synchronous circuit is selected.

# (11) Precautions

Note the following for the use of timers.

• Prescaler

Stop counting and then execute the TABPS instruction to read from prescaler data.

Stop counting and then execute the TPSAB instruction to set prescaler data.

- Timer count source Stop timer 1, 2, and LC counting to change its count source.
- Reading the count value

Stop timer 1 or 2 counting and then execute the data read instruction (TAB1, TAB2) to read its data.

Writing to the timer

Stop timer 1, 2 or LC counting and then execute the data write instruction (T1AB, T2AB, TLCA) to write its data.

- Writing to reload register R1, R2H When writing data to reload register R1 or reload regiser R2H while timer 1 or timer 2 is operating, avoid a timing when timer 1 or timer 2 underflows.
- Timer 2

Avoid a timing when timer 2 underflows to stop timer 2 at PWM output function used.

When "H" interval extension function of the PWM signal is set to be "valid", set "1" or more to reload register R2H.

- Timer 3 Stop timer 3 counting to change its count source.
- Timer input/output pin Set the port C output latch to "0" to output the PWM signal from C/CNTR pin.



 Prescaler and Timer 1 count start timing and count time when operation starts

Count starts from the first rising edge of the count source (2) after Prescaler and Timer 1 operations start (1).

Time to first underflow (3) is shorter (for up to 1 period of the count source) than time among next underflow (4) by the timing to start the timer and count source operations after count starts. When selecting CNTR input as the count source of Timer 1,

Timer 1 operates synchronizing with the falling edge of CNTR input.



Fig. 24 Timer count start timing and count time when operation starts (Prescaler and Timer 1)

Timer 2 and Timer LC count start timing and count time when operation starts

Count starts from the rising edge (2) after the first falling edge of the count source, after Timer 2 and Timer LC operations start (1). Time to first underflow (3) is different from time among next underflow (4) by the timing to start the timer and count source operations after count starts.



Fig. 25 Timer count start timing and count time when operation starts (Timer 2 and Timer LC)
Timer 2 count value (Reload register)						
Timer 2 count value (Reload register)	0316 0210 0116 0016 ( (R2L)	0316021601160				
(Reload register)	(R2L)		016,0316,0216,0116	0016031602160	116,001,0316,0216	0110 0016
	I I	<b>†</b> R2L)	(R2L)	(R2L)	<b>†</b> (R2L)	
Timer 2 underflow signal						
PWM signal (output invalid)						
	t Timer 2 start				PWM si fixed	gnal "L"
<ul> <li>CNTR output: valid (W23 = " PWM signal "H" interval ext</li> </ul>	1") ension function: invalid (W2:	2 = "0")				
Timer 2 count source	ļuuų	ιιιί	uuu	uur	บบบบุ	
Timer 2 count value	0316 0216 0116 0016	0212011600160	316021601120016	0216 01 16 00 16 0	316021601160016	0216 0116
(Reload	(R2L)	<b>†</b> (R2H) (F	R2L)	(R2H) (F	R2L)	<b>†</b> (R2H)
Timer 2 underflow signal	T				1	
PWM		—3 clock —►		<a>→ 3 clock→</a>		
signal	Timer 2 start	PWM perio	od 7 clock	PWM perio	od 7 clock	
● CNTR output: valid (W23 : PWM signal "H" interval e	= "1") xtension function: valid (W2	2 = "1") (Note)				
Timer 2 count source	huui		ىىتىت	ηπι	цили	11
Timer 2 count value	0316 0216 0116 0016	0216 0116 0016	03160216011600	0216 01160	016 0316 0216 0116	0016 0216
(Reload register)	(R2L)	<b>1</b> (R2H)	<b> </b>   (R2L)	¦ <b>Î</b> ¦(R2H)	<b>f</b> (R2L)	¦ <b>1</b> ¦(R2H)
Timer 2 underflow signal			Γ	_T		
PWM			4	<ul> <li>≼3.5 clock_</li> </ul>	<b>→</b>	
signal	t Timer 2 start	PWM per	iod 7.5 clock	PWM	period 7.5 clock	→
Note: At PWM signal "H" inter	val extension function: valid	, set "0116" or mor	e to reload register F	R2H.		

Fig. 26 Timer 2 operation (reload register R2L: "0316", R2H: "0216")



Fig. 27 CNTR output auto-control function by timer 1



		ng			
Machine cycle	Mi		Mi+1		Mi+2
-	<u> </u>	TW2A instruction	execution c	/cle (W21) ← 1	
System clock <sup>–</sup> f(STCK)=f(XIN)/4					
XIN input (count source selected)				uuu	hunn
Register W21					2
Timer 2 count value		0316		X0216X 0116X 0016	x0216x0116x0016x0316x0216x0116
(Reioad register) -		(R2L)			<b>1</b> (R2H) <b>1</b> (R2L)
Timer 2 underflow signal					ΓΓ
PWM signal					
0					
				Timer 2 count st	l tart timing
—Timer 2 count si				Timer 2 count si	tart timing
—Timer 2 count st	top timing-			Timer 2 count si	tart timing
—Timer 2 count si Machine cycle	top timing—		Mi+1	Timer 2 count si	tart timing Mi+2
—Timer 2 count si Machine cycle System clock f(STCK)=f(XIN)/4	top timing— Mi	TW2A instruction	Mi+1 execution cy	Timer 2 count since $rac{1}{2}$	tart timing
—Timer 2 count si Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected)—	top timing-		Mi+1 execution cy	Timer 2 count since $C$ and	 tart timing 
—Timer 2 count si Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected)— Register W21	top timing—		Mi+1 execution cy	Timer 2 count since $(W21) \leftarrow 0$	 tart timing 
—Timer 2 count st Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected)– Register W21 Timer 2 count value	top timing— <u>Mi</u> (0216)(0116)(001		<u>Mi+1</u> execution cy	Timer 2 count since $Cle (W21) \leftarrow 0$	 tart timing 
—Timer 2 count st Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected)– Register W21 Timer 2 count value (Reload register)	top timing— Mi	TW2A instruction	<u>Mi+1</u> execution cy	Timer 2 count since $Cle (W21) \leftarrow 0$ $Cle (W21) \leftarrow 0$ 0216 (R2H)	 tart timing 
—Timer 2 count si Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected) Register W21 Timer 2 count value (Reload register) Timer 2 underflow signal	top timing-	TW2A instruction  6\0216\0116\0016\0316\ ↓ (R2H) ↓ (R2L	<u>Mi+1</u> execution cy	Timer 2 count st $cle (W21) \leftarrow 0$ $Cle (W21) \leftarrow 0$	tart timing
——Timer 2 count si Machine cycle System clock f(STCK)=f(XIN)/4 XIN input (count source selected)— Register W21 Timer 2 count value (Reload register) Timer 2 underflow signal	top timing	TW2A instruction	Mi+1 <u>execution cy</u> <u>0216(0116(0016)</u> )	Timer 2 count since $2 = 0$ $cle (W21) \leftarrow 0$ 1 = 0 0216 (R2H) (Note 1)	Image:

## WATCHDOG TIMER

Watchdog timer provides a method to reset the system when a program run-away occurs. Watchdog timer consists of timer WDT(16-bit binary counter), watchdog timer enable flag (WEF), and watchdog timer flags (WDF1, WDF2).

The timer WDT downcounts the instruction clocks as the count source from "FFFF16" after system is released from reset.

After the count is started, when the timer WDT underflow occurs (after the count value of timer WDT reaches "000016," the next count pulse is input), the WDF1 flag is set to "1."

If the WRST instruction is never executed until the timer WDT underflow occurs (until timer WDT counts 65534), WDF2 flag is set to "1," and the  $\overrightarrow{\text{RESET}}$  pin outputs "L" level to reset the microcomputer.

Execute the WRST instruction at each period of 65534 machine cycle or less by software when using watchdog timer to keep the microcomputer operating normally.

When the WEF flag is set to "1" after system is released from reset, the watchdog timer function is valid.

When the DWDT instruction and the WRST instruction are executed continuously, the WEF flag is cleared to "0" and the watchdog timer function is invalid.

The WEF flag is set to "1" at system reset or RAM back-up mode.

The WRST instruction has the skip function. When the WRST instruction is executed while the WDF1 flag is "1", the WDF1 flag is cleared to "0" and the next instruction is skipped.

When the WRST instruction is executed while the WDF1 flag is "0", the next instruction is not skipped.

The skip function of the WRST instruction can be used even when the watchdog timer function is invalid.



③ When the WRST instruction is executed, WDF1 flag is cleared to "0," the next instruction is skipped.

 When timer WDT underflow occurs while WDF1 flag is "1," WDF2 flag is set to "1" and the watchdog reset signal is output.

⑤ The output transistor of RESET pin is turned "ON" by the watchdog reset signal and system reset is executed.

Note: The number of count is equal to the number of cycle because the count source of watchdog timer is the instruction clock.

Fig. 29 Watchdog timer function

When the watchdog timer is used, clear the WDF1 flag at the period of 65534 machine cycles or less with the WRST instruction. When the watchdog timer is not used, execute the DWDT instruction and the WRST instruction continuously (refer to Figure 30).

The watchdog timer is not stopped with only the DWDT instruction. The contents of WDF1 flag and timer WDT are initialized at the power down mode.

When using the watchdog timer and the power down mode, initialize the WDF1 flag with the WRST instruction just before the microcomputer enters the power down state (refer to Figure 31).

The watchdog timer function is valid after system is returned from the power down. When not using the watchdog timer function, execute the DWDT instruction and the WRST instruction continuously every system is returned from the power down, and stop the watchdog timer function.

WRST	; WDF1 flag cleared
DI DWDT WRST	; Watchdog timer function enabled/disabled ; WEF and WDF1 flags cleared

Fig. 30 Program example to start/stop watchdog timer







## LCD FUNCTION

The 4556 Group has an LCD (Liquid Crystal Display) controller/ driver. When the proper voltage is applied to LCD power supply input pins (VLC1–VLC3) and data are set in timer control register (W4), timer LC, LCD control registers (L1, L2, L3, C1, C2), and LCD RAM, the LCD controller/driver automatically reads the display data and controls the LCD display by setting duty and bias.

4 common signal output pins and 23 segment signal output pins can be used to drive the LCD. By using these pins, up to 92 segments (when 1/4 duty and 1/3 bias are selected) can be controlled to display. The LCD power input pins (VLC1–VLC3) are also used as pins SEG0–SEG2. When SEG0–SEG2 are selected, the internal power (VDD) is used for the LCD power.

## (1) Duty and bias

There are 3 combinations of duty and bias for displaying data on the LCD. Use bits 0 and 1 of LCD control register (L1) to select the proper display method for the LCD panel being used.

- 1/2 duty, 1/2 bias
- 1/3 duty, 1/3 bias
- 1/4 duty, 1/3 bias

#### Table 11 Duty and maximum number of displayed pixels

Duty	Maximum number of displayed pixels	Used COM pins
1/2	46 segments	COM0, COM1 (Note)
1/3	69 segments	COM0-COM2 (Note)
1/4	92 segments	COM0–COM3

Note: Leave unused COM pins open.

## (2) LCD clock control

The LCD clock is determined by the timer LC count source selection bit (W42), timer LC control bit (W43), and timer LC. Accordingly, the frequency (F) of the LCD clock is obtained by the following formula. Numbers (① to ③) shown below the formula correspond to numbers in Figure 32, respectively.

 When using the prescaler output (ORCLK) as timer LC count source (W42="1")

$$F = ORCLK \times \frac{1}{||C| + 1||} \times \frac{1}{2}$$

• When using the bit 4 of timer 3 as timer LC count source (W42="0")

$$F = \begin{array}{ccc} T34 & X & \frac{1}{LC+1} & X & \frac{1}{2} \\ \hline 0 & 2 & 3 \end{array}$$

[LC: 0 to 15]

The frame frequency and frame period for each display method can be obtained by the following formula:

Frame frequency = 
$$\frac{F}{n}$$
 (Hz)  
Frame period =  $\frac{n}{F}$  (s)  
[F: LCD clock frequency]  
 $1/n:$  Duty



Fig. 32 LCD clock control circuit structure



Fig. 33 LCD controller/driver

## (3) LCD RAM

RAM contains areas corresponding to the liquid crystal display. When "1" is written to this LCD RAM, the display pixel corresponding to the bit is automatically displayed.

## (4) LCD drive waveform

When "1" is written to a bit in the LCD RAM data, the voltage difference between common pin and segment pin which correspond to the bit automatically becomes IVLC3I and the display pixel at the cross section turns on.

When returning from reset, and in the RAM back-up mode, a display pixel turns off because every segment output pin and common output pin becomes VLC3 level.

X	<u> </u>		0 1 2				1						3			
Y Bits	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	SEG0	SEG0	SEG0	SEG0	SEG8	SEG8	SEG8	SEG8					SEG24	SEG24	SEG24	SEG2
9	SEG1	SEG1	SEG1	SEG1	SEG9	SEG9	SEG9	SEG9	SEG17	SEG17	SEG17	SEG17	SEG25	SEG25	SEG25	SEG2
10	SEG2	SEG2	SEG2	SEG2	SEG10	SEG10	SEG10	SEG10	SEG18	SEG18	SEG18	SEG18	SEG26	SEG26	SEG26	SEG26
11	SEG3	SEG3	SEG3	SEG3		—		—	SEG19	SEG19	SEG19	SEG19	SEG27	SEG27	SEG27	SEG2
12	SEG4	SEG4	SEG4	SEG4					SEG20	SEG20	SEG20	SEG20	SEG28	SEG28	SEG28	SEG28
13	SEG5	SEG5	SEG5	SEG5			—		SEG21	SEG21	SEG21	SEG21				
14	SEG6	SEG6	SEG6	SEG6					SEG22	SEG22	SEG22	SEG22				
15	SEG7	SEG7	SEG7	SEG7					SEG23	SEG23	SEG23	SEG23				
COM	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM
Note: The a	Note: The area marked " — " is not the LCD display RAM.															



#### Table 12 LCD control registers (1)

LCD control register L1			at	reset : 00002	at power dov	vn : state retained	R/W TAL1/TL1A
1.12	Internal dividing resistor for LCD power	0	0 2r × 3, 2r × 2		•		
L13	supply selection bit (Note 2)	1 r X 3, r X 2					
		0	)	Stop			
	LCD control bit		1	Operating			
		L11	L10	Duty		Bias	
L11		0	0		Not av	ailable	
	LCD duty and bias selection bits	0	1	1/2		1/2	
L10		1	0	1/3		1/3	
		1	1	1/4		1/3	

	LCD control register L2	at	reset : 00002	at power down : state retained	W TL2A
L23 SEG0/VLC3 pin function switch bit (Note 3)		0	SEG0		
		1	VLC3		
		0	SEG1		
	SEGI/VEC2 pin function switch bit (Note 4)	1	VLC2		
1.07		0	SEG2		
L21	SEG2/VLC1 pin function switch bit (Note 4)	1	VLC1		
Internal dividing resistor for LCD power		0	Internal dividing res	sistor valid	
L20	supply control bit	1	Internal dividing res	sistor invalid	

LCD control register L3			at	reset : 11112	at power down : state retained	W TL3A
L33 P23/SEG20 pin function switch bit		0	/	SEG20		
		1		P23		
1.20	D22/SEC to pip function quitch hit		•	SEG19		
L32	F22/3EG19 pin function switch bit	<u> </u>		P22		
1.0.	B24/SEC40 pip function quitch hit	0		SEG18		
L31	L31 P21/SEG18 pin function switch bit			P21		
1.00		0		SEG17		
L30	F20/SEGT/ pin function switch bit	1		P20		

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: "r (resistor) multiplied by 3" is used at 1/3 bias, and "r multiplied by 2" is used at 1/2 bias.

3: VLC3 is connected to VDD internally when SEG0 pin is selected.

4: Use internal dividing resistor when SEG1 and SEG2 pins are selected.



## Table 12 LCD control registers (2)

LCD control register C1		at reset : 11112		at power down : state retained	W TC1A
C13 P03/SEG24 pin function switch bit		0	SEG24		- -
		1	P03		
C10 P02/SEC22 pin function switch bit	0	SEG23			
012	F 02/3E G23 pin runction switch bit	1	P02		
<u> </u>	B04/SEC 22 pin function awitch hit	0	SEG22		
C11	F07/3EG22 pill function switch bit	1	P01		
C10	Dos/CECor sis function quitab bit	0	SEG21		
U10		1	P00		

LCD control register C2		at reset : 11112		at power down : state retained	W TC2A
C23 P13/SEG28 pin function switch bit		0	SEG28		
		1	P13		
C20 P12/SEG27 pin function switch bit	0 SEG27				
022		1	P12		
<u> </u>	R14/SEC on pin function quitch hit	0	SEG26		
621	C21 P11/SEG26 pin function switch bit		P11		
<u> </u>	P10/SEG25 pin function switch bit	0	SEG25		
020		1	P10		

Note: "R" represents read enabled, and "W" represents write enabled.

-C





Fig. 35 LCD controller/driver structure

## (5) LCD power supply circuit

Select the LCD power supply circuit suitable for the using LCD panel.

The LCD power supply circuit is fixed by the followings;

- The internal dividing resistor is controlled by bit 0 of register L2.
- The internal dividing resistor is selected by bit 3 of register L1.
- The bias condition is selected by bits 0 and 1 of register L1.

#### Internal dividing resistor

The 4556 Group has the internal dividing resistor for LCD power supply.

When bit 0 of register L2 is set to "0", the internal dividing resistor is valid. However, when the LCD is turned off by setting bit 2 of register L1 to "0", the internal dividing resistor is turned off. The same six resistor (r) is prepared for the internal dividing resistor. According to the setting value of bit 3 of register L1 and

- using bias condition, the resistor is prepared as follows; • L13 = "0", 1/3 bias used: 2r X 3 = 6r
- L13 = "0", 1/2 bias used: 2r × 3 = 0
- L13 = "1", 1/3 bias used: r X 3 = 3r
- L13 = "1", 1/2 bias used: r X 2 = 2r

●VLC3/SEG0 pin

The selection of VLC3/SEG0 pin function is controlled with the bit 3 of register L2.

When the VLC3 pin function is selected, apply voltage of VLC3 < VDD to the pin externally.

When the SEG0 pin function is selected, VLC3 is connected to VDD internally.

#### VLC2/SEG1, VLC1/SEG2 pin

The selection of VLC2/SEG1 pin function is controlled with the bit 2 of register L2.

The selection of VLC1/SEG2 pin function is controlled with the bit 1 of register L2.

When the VLC2 pin and VLC1 pin functions are selected and the internal dividing resistor is not used, apply voltage of 0<VLC1<VLC2<VLC3 to these pins. Short the VLC2 pin and VLC1 pin at 1/2 bias.

When the VLC2 pin and VLC1 pin functions are selected and the internal dividing resistor is used, the dividing voltage value generated internally is output from the VLC1 pin and VLC2 pin. The VLC2 pin and VLC1 pin have the same electric potential at 1/2 bias. When SEG1 and SEG2 pin functions are selected, use the internal dividing resistor. In this time, VLC2 and VLC1 are connected to the generated dividing voltage.



Fig. 36 LCD power supply circuit example (1/3 bias condition selected)

## **RESET FUNCTION**

System reset is performed by applying "L" level to RESET pin for 1 machine cycle or more when the following condition is satisfied; the value of supply voltage is the minimum value or more of the recommended operating conditions.

Then when "H" level is applied to RESET pin, software starts from address 0 in page 0.









### (1) Power-on reset

Reset can be automatically performed at power on (power-on reset) by the built-in power-on reset circuit. When the built-in power-on reset circuit is used, set the time for the supply voltage to rise from 0 V to the minimum voltage of recommended operating conditions to 100  $\mu$ s or less.

If the rising time exceeds 100  $\mu$ s, connect a capacitor between the RESET pin and Vss at the shortest distance, and input "L" level to RESET pin until the value of supply voltage reaches the minimum operating voltage.



Fig. 39 Structure of reset pin and its peripherals,, and power-on reset operation

#### Table 13 Port state at reset

Name	Function	State
D0D4	D0-D4	High-impedance (Notes 1, 2)
D5/INT	D5	High-impedance (Notes 1, 2)
XCIN/D6, XCOUT/D7	XCIN, XCOUT	Sub-clock input
P00/SEG21-P03/SEG24	P00–P03	High-impedance (Notes 1, 2, 3)
P10/SEG25-P13/SEG28	P10–P13	High-impedance (Notes 1, 2, 3)
P20/SEG17-P23/SEG20	P20-P23	High-impedance (Notes 1, 2, 3)
SEG0/VLC3-SEG2/VLC1	SEG0-SEG2	VLC3 (VDD) level
SEG3-SEG10	SEG3-SEG10	VLC3 (VDD) level
COM0–COM3	COM0-COM3	VLC3 (VDD) level
C/CNTR	С	"L" (Vss) level

Notes 1: Output latch is set to "1."

2: Output structure is N-channel open-drain.

3: Pull-up transistor is turned OFF.



## (2) Internal state at reset

Figure 40 shows internal state at reset (they are the same after system is released from reset). The contents of timers, registers, flags and RAM except shown in Figure 40 are undefined, so set the initial value to them.

Program counter (PC)	
Address 0 in page 0 is set to program counter	
Interrupt enable flag (INTE)	(Interrupt disabled)
Power down flag (P)	
Evternal 0 interrunt request flag (EXE0)	
Interrupt control register V1	
Interrupt control register V1	$\frac{1}{10000000000000000000000000000000000$
Interrupt control register 12	
Timer 1 interrupt request flag (T1E)	
Timer 2 interrupt request flag (TTF)	
Timer 2 interrupt request flag (T2F)	
Watchdog timer flags (WDE1_WDE2)	
• Watchdog timer mags (WDF1, WDF2)	U
Watchoog timer enable hag (WEF)	
Timer control register PA	(Prescaler stopped)
Timer control register W1     Timer control register W0	
• Timer control register W2	
Imer control register W3	
Imer control register W4	
Clock control register MR	
Clock control register RG	
LCD control register L1	
LCD control register L2	0000
LCD control register L3	
LCD control register C1	
LCD control register C2	
Key-on wakeup control register K0	0000
Key-on wakeup control register K1	
Key-on wakeup control register K2	
Pull-up control register PU0	0000
Pull-up control register PU1	0000
Port output structure control register FR0	0000
Port output structure control register FR1	0000
Port output structure control register FR2	0000
Carry flag (CY)	0
High-order bit reference enable flag (UPTF)	0
Register A	
Register B	
Register D	
• Register E X >	
Register X	
Register Y	
Register Z	X X
Stack pointer (SP)	
Operation source clock On-chi	p oscillator (operating)
Ceramic resonator circuit	Operating
RC oscillation circuit	
Quartz-crystal oscillator	
,	

Fig. 40 Internal state at reset



## VOLTAGE DROP DETECTION CIRCUIT (only for H version)

The built-in voltage drop detection circuit is designed to detect a drop in voltage and to reset the microcomputer if the supply voltage drops below a set value.

(1) SVDE instruction

When the SVDE instruction is executed, the voltage drop detection circuit is valid even after system enters into the power down mode. The SVDE instruction can be executed only once.

In order to release the execution of the SVDE instruction, the system reset is required.





Note: Detection voltage hysteresis of voltage drop detection circuit is 0.1 V (Typ).

#### Fig. 42 Voltage drop detection circuit operation waveform

#### (2) Note on voltage drop detection circuit

The voltage drop detection circuit detection voltage of this product is set up lower than the minimum value of the supply voltage of the recommended operating conditions.

When the supply voltage of a microcomputer falls below to the minimum value of recommended operating conditions and regoes up (ex. battery exchange of an application product), depending on the capacity value of the bypass capacitor added to the power supply pin, the following case may cause program failure (Figure 43);

supply voltage does not fall below to VRST-, and

its voltage re-goes up with no reset.

In such a case, please design a system which supply voltage is once reduced below to VRST<sup>-</sup> and re-goes up after that.





## POWER DOWN FUNCTION

The 4556 Group has 2-type power down functions. System enters into each power down state by executing the following instructions.

- Clock operating mode ..... EPOF and POF instructions
- RAM back-up mode ..... EPOF and POF2 instructions

When the EPOF instruction is not executed before the POF or POF2 instruction is executed, these instructions are equivalent to the NOP instruction.

## (1) Clock operating mode

The following functions and states are retained.

- RAM
- Reset circuit
- XCIN-XCOUT oscillation
- LCD display
- Timer 3

## (2) RAM back-up mode

- The following functions and states are retained.
- RAM
- Reset circuit

## (3) Warm start condition

- The system returns from the power down state when;
- External wakeup signal is input
- Timer 3 underflow occurs
- in the power down mode.
- In either case, the CPU starts executing the software from address 0 in page 0. In this case, the P flag is "1."

## (4) Cold start condition

The CPU starts executing the software from address 0 in page 0 when;

• reset pulse is input to RESET pin,

- reset by watchdog timer is performed, or
- reset by the voltage drop detection circuit is performed.

In this case, the P flag is "0."

## (5) Identification of the start condition

Warm start or cold start can be identified by examining the state of the power down flag (P) with the SNZP instruction. The warm start condition from the clock operating mode can be identified by examining the state of T3F flag.

#### Table 15 Functions and states retained at power down mode

	Power down mode			
Function	Clock	RAM		
	operating	раск-ир		
Program counter (PC), registers A, B,	x	x		
carry flag (CY), stack pointer (SP) (Note 2)				
Contents of RAM	0	0		
Interrupt control registers V1, V2	X	X		
Interrupt control register I1	0	0		
Selected oscillation circuit	0	0		
Clock control register MR, RG	0	0		
Timer 1 to timer 2 functions	(Note 3)	(Note 3)		
Timer 3 function	0	(Note 3)		
Timer LC function	0	(Note 3)		
Watchdog timer function	X (Note 4)	X (Note 4)		
Timer control registers PA	X	X		
Timer control registers W1 to W4	0	0		
LCD display function	0	(Note 5)		
LCD control registers L1 to L3, C1, C2	0	0		
Voltage drop detection circuit	(Note 6)	(Note 6)		
Port level	(Note 7)	(Note 7)		
Pull-up control registers PU0, PU1	0	0		
Key-on wakeup control registers K0 to K2	0	0		
Port output structure control registers	0	0		
FR0 to FR2				
External interrupt request flag	×	×		
(EXF0)				
Timer interrupt request flags (T1F, T2F)	(Note 3)	(Note 3)		
Timer interrupt request flag (T3F)	0	(Note 3)		
Interrupt enable flag (INTE)	X	X		
Watchdog timer flags (WDF1, WDF2)	X (Note 4)	X (Note 4)		
Watchdog timer enable flag (WEF)	X (Note 4)	X (Note 4)		

Notes 1:"O" represents that the function can be retained, and "X" represents that the function is initialized.

- Registers and flags other than the above are undefined at RAM back-up, and set an initial value after returning.
- 2: The stack pointer (SP) points the level of the stack register and is initialized to "7" at RAM back-up.
- 3: The state of the timer is undefined.
- 4: Initialize the watchdog timer with the WRST instruction, and then go into the power down state.
- 5: LCD is turned off.
- 6: When the SVDE instruction is executed, this function is valid at power down.
- 7: In the RAM back-up mode, C/CNTR pin outputs "L" level. However, when the CNTR input is selected (W11, W10="11"), C/ CNTR pin is in an input enabled state (output = high-impedance). Other ports retain their respective output levels.

## (6) Return signal

An external wakeup signal or timer 3 interrupt request flag (T3F) is used to return from the clock operating mode.

An external wakeup signal is used to return from the RAM back-up mode because the oscillation is stopped.

Table 16 shows the return condition for each return source.

## (7) Control registers

• Key-on wakeup control register K0

Register K0 controls the ports P0 and P1 key-on wakeup function. Set the contents of this register through register A with the TK0A instruction. In addition, the TAK0 instruction can be used to transfer the contents of register K0 to register A.

Key-on wakeup control register K1

Register K1 controls the return condition and the selection of valid waveform/level of port P1. Set the contents of this register through register A with the TK1A instruction. In addition, the TAK1 instruction can be used to transfer the contents of register K0 to register A.

• Key-on wakeup control register K2

Register K2 controls the INT pin key-on wakeup function and the selection of return codition. Set the contents of this register through register A with the TK2A instruction. In addition, the TAK2 instruction can be used to transfer the contents of register K2 to register A.

• Pull-up control register PU0

Register PU0 controls the ON/OFF of the port P0 pull-up transistor. Set the contents of this register through register A with the TPU0A instruction. In addition, the TAPU0 instruction can be used to transfer the contents of register PU0 to register A.

• Pull-up control register PU1

Register PU1 controls the ON/OFF of the port P1 pull-up transistor. Set the contents of this register through register A with the TPU1A instruction. In addition, the TAPU1 instruction can be used to transfer the contents of register PU1 to register A.

• External interrupt control register I1

Register I1 controls the valid waveform of the external 0 interrupt, the input control of INT pin and the return input level. Set the contents of this register through register A with the TI1A instruction. In addition, the TAI1 instruction can be used to transfer the contents of register I1 to register A.

	Return source	Return condition	Remarks
lal	Ports P00-P03	Return by an external falling edge ("H" $\rightarrow$ "L").	The key-on wakeup function can be selected by two port unit.
akeup sigr	Ports P10–P13	Return by an external "H" level or "L" level input, or rising edge ("L" $\rightarrow$ "H") or falling edge ("H" $\rightarrow$ "L"). Return by an external "L" level input.	The key-on wakeup function can be selected by two port unit. Select the re- turn level ("L" level or "H" level) and return condition (return by level or edge) with register K1 according to the external state before going into the power down state.
ternal w	INT pin	Return by an external "H" level or "L" level input, or rising edge ("L" $\rightarrow$ "H") or falling edge ("H" $\rightarrow$ "L").	Select the return level ("L" level or "H" level) with register 11 and return con- dition (return by level or edge) with register K2 according to the external state before going into the power down state.
Ш		When the return level is input, the in- terrupt request flag (EXF0) is not set.	
Tim requ	er 3 interrupt est flag (T3F)	Return by timer 3 underflow or by setting T3F to "1".	Clear T3F with the SNZT3 instruction before system enters into the power down state.
		It can be used in the clock operating mode.	When system enters into the power down state while T3F is "1", system re- turns from the state immediately because it is recognized as return condition.

#### Table 16 Return source and return condition









Key-on wakeup control register K0		at reset : 00002		at power down : state retained	R/W TAK0/ TK0A
KOa	Port P12, P13 key-on wakeup	0	Key-on wakeup not	used	
K03	control bit (Note 3)	1 Key-on wakeup used		ed	
KOo	Port P10, P11 key-on wakeup	0 Key-on wakeup not used			
K02	control bit (Note 2)	1	Key-on wakeup use	ed	
KO	Port P02, P03 key-on wakeup	0	Key-on wakeup not	used	
K01	control bit	1	Key-on wakeup use	ed	
KOo	Port P00, P01 key-on wakeup	0	Key-on wakeup not	used	
K00	control bit	1	Key-on wakeup use	ed	

#### Table 17 Key-on wakeup control register, pull-up control register and interrupt control register

Key-on wakeup control register K1		at reset : 00002		at power down : state retained	R/W TAK1/ TK1A
K10	Ports P12, P13 return condition selection bit	0	0 Returned by edge		
(Note 3) 1 Returned by level					
K10	Ports P12, P13 valid waveform/level	0 Falling waveform/"L" level			
K12 selection bit (Note 3)			Rising waveform/"H" level		
K1.	Ports P10, P11 return condition selection bit	0	Returned by edge		
	(Note 2)	1	Returned by level		
K10	Ports P10, P11 valid waveform/level	0	Falling waveform/"L	" level	
<b>N10</b>	selection bit (Note 2)	1	Rising waveform/"H	" level	

Key-on wakeup control register K2 a		at	reset : 00002	at power down : state retained	R/W TAK2/ TK2A
K23	Not used	0	This bit has no fund	tion, but read/write is enabled.	
K22	Not used	0	This bit has no function, but read/write is enabled.		
K24	K21 INT pin return condition selection bit		Returned by level		
<b>K</b> 21			Returned by edge		
K20	INT his key on wakeup control hit	0	Key-on wakeup inv	alid	
K20	INT pin key-on wakeup control bit	1	Key-on wakeup val	id	

Notes 1: "R" represents read enabled, and "W" represents write enabled.

To be invalid (K02 = "0") key-on wakeup of ports P10 and P11, set the registers K10 and K11 to "0".
 To be invalid (K03 = "0") key-on wakeup of ports P12 and P13, set the registers K12 and K13 to "0".

	Pull-up control register PU0	ntrol register PU0 at reset : 00002		at power down : state retained	R/W TAPU0/ TPU0A
DUOs	Port P03 pull-up transistor	0	Pull-up transistor O	FF	
P003	control bit	1	Pull-up transistor O	Ν	
DUOs	Port P02 pull-up transistor	0 Pull-up transistor OFF			
P002	control bit	1	Pull-up transistor O	Ν	
DU0.	Port P01 pull-up transistor	0	Pull-up transistor O	FF	
P001	control bit	1	Pull-up transistor O	N	
DUIDo	Port P00 pull-up transistor	0	Pull-up transistor O	FF	
P000	control bit	1	Pull-up transistor O	Ν	

Pull-up control register PU1		at reset : 00002		at power down : state retained	R/W TAPU1/ TPU1A
DUIA	Port P13 pull-up transistor	0	Pull-up transistor O	FF	
P013	control bit	1	Pull-up transistor O	N	
DUIA	Port P12 pull-up transistor	0	Pull-up transistor O	FF	
P012	control bit	1	Pull-up transistor ON		
	Port P11 pull-up transistor	0	Pull-up transistor O	FF	
P011	control bit	1	Pull-up transistor O	N	
DUIA	Port P10 pull-up transistor	0	Pull-up transistor O	FF	
PU10	control bit	1	Pull-up transistor O	N	

Interrupt control register 11		at reset : 00002		at power down : state retained	R/W TAI1/TI1A
110	INT pip input control bit (Note 2)	0	INT pin input disat	bled	
		1	INT pin input enab	led	
		0	Falling waveform/"L" level ("L" level is recognized with the SNZIO		
112	Interrupt valid waveform for INT pin/ return level selection bit (Note 2)		instruction)		
112			Rising waveform/"H" level ("H" level is recognized with the SNZI0		
		1	instruction)		
111	INT pip edge detection circuit control bit	0	One-sided edge de	etected	
In pin edge detection circuit control bit		1	Both edges detected		
110	INT pin Timer 1 count start synchronous	0	Timer 1 count star	t synchronous circuit not selected	
110	circuit selection bit	1	Timer 1 count star	t synchronous circuit selected	

Notes 1: "R" represents read enabled, and "W" represents write enabled. 2: When the contents of I12 and I13 are changed, the external interrupt request flag (EXF0) may be set.



## **CLOCK CONTROL**

- The clock control circuit consists of the following circuits.
- On-chip oscillator (internal oscillator)
- Ceramic resonator
- RC oscillation circuit
- Quartz-crystal oscillation circuit
- Multi-plexer (clock selection circuit)
- Frequency divider
- Internal clock generating circuit

The system clock and the instruction clock are generated as the source clock for operation by these circuits.

Figure 47 shows the structure of the clock control circuit.

The 4556 Group operates by the on-chip oscillator clock (f(RING)) which is the internal oscillator after system is released from reset. Also, the ceramic resonator or the RC oscillation can be used for the main clock (f(XIN)) of the 4556 Group.

The quartz-crystal oscillator can be used for sub-clock (f(XCIN)).



Fig. 47 Clock control circuit structure

## (1) On-chip oscillator operation

After system is released from reset, the MCU starts operation by the clock output from the on-chip oscillator which is the internal oscillator.

The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.

Be careful that variable frequencies when designing application products.

## (2) Main clock generating circuit (f(XIN))

When the MCU operates by the ceramic resonator or the RC oscillator as the main clock (f(XIN)).

After system is released from reset, the ceramic oscillation is valid for main clock.

The ceramic oscillation is invalid and the RC oscillation circuit is valid with the CRCK instruction.

The CRCK instruction can be executed only once.

Execute the CRCK instruction in the initial setting routine (executing it in address 0 in page 0 is recommended).

When the main clock (f(XIN)) is not used, connect XIN pin to Vss and leave XOUT pin open, and do not execute the CRCK instruction (Figure 49).

## (3) Ceramic resonator

When the ceramic resonator is used as the main clock (f(XIN)), connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT (Figure 50). Do not execute the CRCK instruction in program.

## (4) RC oscillation

When the RC oscillation is used as the main clock (f(XIN)), connect the XIN pin to the external circuit of resistor R and the capacitor C at the shortest distance and leave XOUT pin open. Then, execute the CRCK instruction (Figure 51).

The frequency is affected by a capacitor, a resistor and a microcomputer. So, set the constants within the range of the frequency limits.



Fig. 48 Switch to ceramic oscillation/RC oscillation



Fig. 49 Handling of XIN and XOUT when operating on-chip oscillator







Fig. 51 External RC circuit



## (5) External clock

When the external clock signal is used as the main clock (f(XIN)), connect the XIN pin to the clock source and leave XOUT pin open. (Figure 52). Do not execute the CRCK instruction.

Be careful that the maximum value of the oscillation frequency when using the external clock differs from the value when using the ceramic resonator (refer to the recommended operating condition). Also, note that the power down mode (POF and POF2 instructions) cannot be used when using the external clock.

## (6) Sub-clock generating circuit f(XCIN)

Sub-clock signal f(XCIN) is obtained by externally connecting a quartz-crystal oscillator. Connect this external circuit and a quartzcrystal oscillator to pins XCIN and XCOUT at the shortest distance. A feedback resistor is built in between pins XCIN and XCOUT (Figure 53). XCIN pin and XCOUT pin are also used as ports D6 and D7, respectively. The sub-clock oscillation circuit is invalid and the function of ports D6 and D7 are valid by setting bit 2 of register RG to "1".

When sub-clock, ports D6 and D7 are not used, connect XCIN/D6 to Vss and leave Xcout/D7 open.

## (7) Clock control register MR

Register MR controls system clock. Set the contents of this register through register A with the TMRA instruction. In addition, the TAMR instruction can be used to transfer the contents of register MR to register A.

## (8) Clock control register RG

Register RG controls the start/stop of each oscillation circuit. Set the contents of this register through register A with the TRGA instruction.

#### **Table 18 Clock control registers**







Fig. 53 External quartz-crystal circuit

## **ROM ORDERING METHOD**

1.Mask ROM Order Confirmation Form\* 2.Mark Specification Form\* 3.Data to be written to ROM...one floppy disk.

\* For the mask ROM confirmation and the mark specifications, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).

Clock control register MR			at	reset : 11002	at power down : state retained	TAMR/ TMRA	
MR3		MR3	MR2	Operation mode			
		0	0	Through mode			
	MR2	0	1	Frequency divided b	Frequency divided by 2 mode		
MR2		1	0	Frequency divided by 4 mode			
IVII V2		1	1	Frequency divided by 8 mode			
		MR1	MR0		System clock		
MR3	System clock selection bits (Note 3)	0	0	f(RING)			
		0	1	f(XIN)			
MR2		1	0	f(XCIN)			
		1	1	Not available (Note	2)		

	Clock control register RG	at	t reset : 0002	at power down : state retained	W TRGA
RG2 Sub-clock (f(XCIN)) control bit (Note 2)		0	Sub-clock (f(XCIN)) oscillation available, ports D6 and D7 not selected		
		1	Sub-clock (f(XCIN)) oscillation stop, ports D6 and D7 selected		
RG1 Main-clock (f(XIN)) control bit (Note 2)		0	Main clock (f(XIN)) oscillation available		
		1	Main clock (f(XIN))	oscillation stop	
	On-chip oscillator (f(RING)) control bit	0	On-chip oscillator (f	(RING)) oscillation available	
RG0	(Note 2)	1	On-chip oscillator (f	(RING)) oscillation stop	

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: "11" cannot be set to the low-order 2 bits (MR1, MR0) of register MR.

## NOTES ON NOISE

Countermeasures against noise are described below.

The following countermeasures are effective against noise in theory, however, it is necessary not only to take measures as follows but to evaluate before actual use.

#### 1. Shortest wiring length

#### (1) Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring.

#### <Reason>

In order to reset a microcomputer correctly, 1 machine cycle or more of the width of a pulse input into the RESET pin is required. If noise having a shorter pulse width than this is input to the RESET input pin, the reset is released before the internal state of the microcomputer is completely initialized.

This may cause a program runaway.



Fig. 54 Wiring for the RESET pin

(2) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

#### <Reason>

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.



Fig. 55 Wiring for clock I/O pins

#### (3) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance.

The GND pattern is required to be as close as possible to the GND supplied to Vss.

In order to improve the noise reduction, to connect a 5  $k\Omega$  resistor serially to the CNVss pin - GND line may be valid.

As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

#### <Reason>

The CNVss pin of the One Time PROM is the power source input pin for the built-in One Time PROM. When programming in the built-in One Time PROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the One Time PROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in One Time PROM, which may cause a program runaway.



Fig. 56 Wiring for the CNVss pin of the One Time PROM

# 2. Connection of bypass capacitor across Vss line and Vbb line Connect an approximately 0.1 $\mu$ F bypass capacitor across the Vss line and the Vbb line as follows:

- Connect a bypass capacitor across the VSS pin and the VDD pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VDD pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and VDD line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the VDD pin.



Fig. 57 Bypass capacitor across the Vss line and the VDD line



#### 3. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

#### (1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

#### <Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

#### <Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.



Fig. 58 Wiring for a large current signal line



Fig. 59 Wiring to a signal line where potential levels change frequently

#### (3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.



Fig. 60 Vss pattern on the underside of an oscillator



#### 4. Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

• Connect a resistor of 100  $\Omega$  or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port or an I/O port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to pull-up control registers at fixed periods.

#### 5. Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing. <The main routine>

 Assigns a single word of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:

 $N+1 \ge$  (Counts of interrupt processing executed in each main routine)

As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.

- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:

If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:

If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.



Fig. 61 Watchdog timer by software

## LIST OF PRECAUTIONS

#### ① Noise and latch-up prevention

Connect a capacitor on the following condition to prevent noise and latch-up;

- connect a bypass capacitor (approx. 0.1  $\mu F)$  between pins VDD and Vss at the shortest distance,
- equalize its wiring in width and length, and

• use relatively thick wire.

In the One Time PROM version, CNVss pin is also used as VPP pin. Accordingly, when using this pin, connect this pin to Vss through a resistor about 5 k $\Omega$  (connect this resistor to CNVss/ VPP pin as close as possible).

In addition, the MCU may be replaced with mask ROM version without the need to remove the resistor from the circuit and without any adverse effect on operation.

#### ② Register initial values 1

The initial value of the following registers are undefined after system is released from reset. After system is released from reset, set initial values.

- Register Z (2 bits)
- Register D (3 bits)
- Register E (8 bits)

#### ③Register initial values 2

The initial value of the following registers are undefined at RAM backup. After system is returned from RAM back-up, set initial values.

- Register Z (2 bits)
- Register X (4 bits)
- Register Y (4 bits)
- Register D (3 bits)
- Register E (8 bits)

#### ④ Stack registers (SKs)

Stack registers (SKs) are eight identical registers, so that subroutines can be nested up to 8 levels. However, one of stack registers is used respectively when using an interrupt service routine and when executing a table reference instruction. Accordingly, be careful not to over the stack when performing these operations together.

#### 5 Prescaler

Stop counting and then execute the TABPS instruction to read from prescaler data.

Stop counting and then execute the TPSAB instruction to set prescaler data.

#### 6 Timer count source

Stop timer 1, 2 and LC counting to change its count source.

#### ⑦ Reading the count value

Stop timer 1 or 2 counting and then execute the data read instruction (TAB1, TAB2) to read its data.

#### Writing to the timer

Stop timer 1, 2 or LC counting and then execute the data write instruction (T1AB, T2AB, TLCA) to write its data.

#### 9 Writing to reload register R1, R2H

When writing data to reload register R1, reload register R2H while timer 1 or timer 2 is operating, avoid a timing when timer 1 or timer 2 underflows.

#### <sup>®</sup>Timer 2

Avoid a timing when timer 2 underflows to stop timer 2 at PWM output function used.

When "H" interval extension function of the PWM signal is set to be "valid", set "1" or more to reload register R2H.

#### 10 Timer 3

Stop timer 3 counting to change its count source.

#### <sup>12</sup>Timer input/output pin

Set the port C output latch to "0" to output the PWM signal from C/CNTR pin.



Prescaler and Timer 1 count start timing and count time when operation starts

Count starts from the first rising edge of the count source (2) after Prescaler and Timer 1 operations start (1).

Time to first underflow (3) is shorter (for up to 1 period of the count source) than time among next underflow (4) by the timing to start the timer and count source operations after count starts.

When selecting CNTR input as the count source of Timer 1, Timer 1 operates synchronizing with the falling edge of CNTR input.



#### Fig. 62 Timer count start timing and count time when operation starts (Prescaler and Timer 1)

<sup>(a)</sup> Timer 2 and Timer LC count start timing and count time when operation starts

Count starts from the rising edge (2) after the first falling edge of the count source, after Timer 2 and Timer LC operations start (1). Time to first underflow (3) is different from time among next underflow (4) by the timing to start the timer and count source operations after count starts.



Fig. 63 Timer count start timing and count time when operation starts (Timer 2 and Timer LC)

#### Watchdog timer

- The watchdog timer function is valid after system is released from reset. When not using the watchdog timer function, execute the DWDT instruction and the WRST instruction continuously, and clear the WEF flag to "0" to stop the watchdog timer function.
- The watchdog timer function is valid after system is returned from the power down state. When not using the watchdog timer function, execute the DWDT instruction and the WRST instruction continuously every system is returned from the power down state, and stop the watchdog timer function.
- When the watchdog timer function and power down function are used at the same time, execute the WRST instruction before system enters into the power down state and initialize the flag WDF1.

#### <sup>®</sup>Multifunction

• Be careful that the output of port Ds can be used even when INT pin is selected.

The threshold value is different between port D5 and INT. Accordingly, be careful when the input of both is used.

 Be careful that the "H" output of port C can be used even when output of CNTR pin are selected.

#### Program counter

Make sure that the PCH does not specify after the last page of the built-in ROM.



#### 18 D5/INT pin

• Note [1] on bit 3 of register I1

When the input of the INT pin is controlled with the bit 3 of register 11 in software, be careful about the following notes.

Depending on the input state of the D5/INT pin, the external 0 interrupt request flag (EXF0) may be set when the bit 3 of register I1 is changed. In order to avoid the occurrence of an unexpected interrupt, clear the bit 0 of register V1 to "0" (refer to Figure 64<sup>(1)</sup>) and then, change the bit 3 of register I1.

In addition, execute the SNZ0 instruction to clear the EXF0 flag to "0" after executing at least one instruction (refer to Figure 64<sup>(2)</sup>). Also, set the NOP instruction for the case when a skip is performed with the SNZ0 instruction (refer to Figure 64<sup>(3)</sup>).

1 ^	4	
LA	4	, (XXX02)
TV1A		; The SNZ0 instruction is valid
LA	8	; (1XXX2)
TI1A		; Control of INT pin input is changed
NOP		
SNZ0		; The SNZ0 instruction is executed
		(EXF0 flag cleared)
NOP		3
:		

Fig. 64 External 0 interrupt program example-1

• Note [2] on bit 3 of register I1

When the bit 3 of register I1 is cleared to "0", the RAM back-up mode is selected and the input of INT pin is disabled, be careful about the following notes.

• When the key-on wakeup function of INT pin is not used (register K20 = "0"), clear bits 2 and 3 of register 11 before system enters to the power down mode. (refer to Figure 65<sup>(1)</sup>).

; (00 <b>XX</b> 2)
; Input of INT disabled ${f I}$
; Power down mode
e bits are not used here.

Fig. 65 External 0 interrupt program example-2

Note on bit 2 of register I1

When the interrupt valid waveform of the D5/INT pin is changed with the bit 2 of register I1 in software, be careful about the following notes.

Depending on the input state of the D5/INT pin, the external 0 interrupt request flag (EXF0) may be set when the bit 2 of register I1 is changed. In order to avoid the occurrence of an unexpected interrupt, clear the bit 0 of register V1 to "0" (refer to Figure 66<sup>(1)</sup>) and then, change the bit 2 of register I1.

In addition, execute the SNZ0 instruction to clear the EXF0 flag to "0" after executing at least one instruction (refer to Figure 66<sup>(2)</sup>). Also, set the NOP instruction for the case when a skip is performed with the SNZ0 instruction (refer to Figure 66<sup>(3)</sup>).







#### <sup>(9)</sup>POF and POF2 instructions

When the POF or POF2 instruction is executed continuously after the EPOF instruction, system enters the power down state.

Note that system cannot enter the power down state when executing only the POF or POF2 instruction.

Be sure to disable interrupts by executing the DI instruction before executing the EPOF instruction and the POF or POF2 instruction continuously.

#### Power-on reset

When the built-in power-on reset circuit is used, set the time for the supply voltage to rise from 0 V to the minimum voltage of recommended operating conditions to 100  $\mu$ s or less.

If the rising time exceeds 100  $\mu$ s, connect a capacitor between the RESET pin and Vss at the shortest distance, and input "L" level to RESET pin until the value of supply voltage reaches the minimum operating voltage.

#### Voltage drop detection circuit (only in H version)

The voltage drop detection circuit detection voltage of this product is set up lower than the minimum value of the supply voltage of the recommended operating conditions.

When the supply voltage of a microcomputer falls below to the minimum value of recommended operating conditions and regoes up (ex. battery exchange of an application product), depending on the capacity value of the bypass capacitor added to the power supply pin, the following case may cause program failure (Figure 67);

supply voltage does not fall below to VRST, and

its voltage re-goes up with no reset.

In such a case, please design a system which supply voltage is once reduced below to VRST<sup>-</sup> and re-goes up after that.



Fig. 67 VDD and VRST-

#### Clock control

Execute the CRCK instruction in the initial setting routine of program (executing it in address 0 in page 0 is recommended). The oscillation circuit by the CRCK instruction can be selected only once.

#### On-chip oscillator

The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.

Be careful that variable frequencies when designing application products.

Also, the oscillation stabilize wait time after system is released from reset is generated by the on-chip oscillator clock. When considering the oscillation stabilize wait time after system is released from reset, be careful that the variable frequency of the on-chip oscillator clock.

#### @External clock

When the external signal clock is used as the source oscillation (f(XIN)), note that the power down mode (POF and POF2 instructions) cannot be used.

#### Difference between Mask ROM version and One Time PROM version Mask ROM version and One Time PROM version have some dif-

ference of the following characteristics within the limits of an electrical property by difference of a manufacture process, builtin ROM, and a layout pattern.

- a characteristic value
- a margin of operation
- the amount of noise-proof
- noise radiation, etc.,

Accordingly, be careful of them when swithcing.

#### ®Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.



## **CONTROL REGISTERS**

Interrupt control register V1		at reset : 00002		at power down : 00002	R/W TAV1/TV1A
1/12	Timer 2 interrupt enable bit	0	Interrupt disabled	(SNZT2 instruction is valid)	
V13		1	Interrupt enabled (	SNZT2 instruction is invalid)	
V12 Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)			
VIZ		1	Interrupt enabled (SNZT1 instruction is invalid)		
1/14	Netused	0	This bit has no function, but read/write is enabled.		
VII		1			
1/10	External 0 interrupt enable bit	0	Interrupt disabled (SNZ0 instruction is valid)		
VIU		1	Interrupt enabled (	SNZ0 instruction is invalid)	

Interrupt control register V2		at reset : 00002		at power down : 00002	R/W TAV2/TV2A		
V23 N	Not used	0	This bit has no fun	This hit has no function, but read/write is enabled			
		1	This bit has no function, but read/whichs chabled.				
V22 Not use	Netused	0	This hit has no function, but read/write is enabled				
	Not used	1	This bit has no function, but read/write is enabled.				
NO.	Netused	0	This bit has no function, but read/write is enabled.				
V21	Not used	1					
	Timer 3 interrupt enable bit	0	Interrupt disabled (SNZT3 instruction is valid)				
v20		1	Interrupt enabled (	SNZT3 instruction is invalid)			

Interrupt control register I1		at reset : 00002		reset : 00002	at power down : state retained	R/W TAI1/TI1A
110				INT pin input disab	led	
113	IN I pin input control bit (Note 2)	1		INT pin input enabl	ed	
	Interrupt valid waveform for INT pin/ return level selection bit (Note 3)	0		Falling waveform/"L" level ("L" level is recognized with the SNZIO		the SNZI0
112		U	instruction)			
112		Rising waveform/"		Rising waveform/"H	H" level ("H" level is recognized with	the SNZI0
				instruction)		
111	INT his edge detection circuit control bit	0		One-sided edge de	tected	
	INT pin edge detection circuit control bit	1		Both edges detected		
110	INT pin Timer 1 count start synchronous	0		Timer 1 count start	synchronous circuit not selected	
110	circuit selection bit	1	1 Timer 1 count star		synchronous circuit selected	

Clock control register MR		at reset : 11002		reset : 11002	at power down : state retained	R/W TAMR/ TMRA
		MR3	MR2		Operation mode	
MR3		0	0	Through mode		
	Operation mode selection bits	0	1	Frequency divided I	by 2 mode	
MR2		1	0	Frequency divided by 4 mode		
		1	1	Frequency divided by 8 mode		
		MR1	MR0		System clock	
MR3		0	0	f(RING)		
	System clock selection bits (Note 3)	0	1	f(XIN)	f(XIN)	
MR2		1	0	f(XCIN)		
		1	1	Not available (Note	4)	

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: When the contents of I12 and I13 are changed, the external interrupt request flag (EXF0) may be set.

3: The stopped clock cannot be selected for system clock. 4: "11" cannot be set to the low-order 2 bits (MR1, MR0) of register MR.



Clock control register RG		at reset : 0002		at power down : state retained	W TRGA	
PC2 Sub clock (f(Xc(N))) control bit (Note 2)		0	Sub-clock (f(XCIN))	oscillation available, ports D6 and [	D7 not selected	
1.02		1	Sub-clock (f(XCIN)) oscillation stop, ports D6 and D7 selected			
	Main clock (f(X))) control bit (Note 2)	0	Main clock (f(XIN)) oscillation available			
RG1		1	Main clock (f(XIN))	oscillation stop		
	On-chip oscillator (f(RING)) control bit	0	On-chip oscillator (f	(RING)) oscillation available		
RG0	(Note 2)	1	On-chip oscillator (f(RING)) oscillation stop			

	Timer control register PA		at reset : 02	at power down : 02	W TPAA
PA <sub>0</sub>	Proscelar control hit	0	Stop (state retaine	d)	
I AU		1	Operating		

Timer control register W1		at reset : 00002		reset : 00002 at power down : state retained	R/W TAW1/TW1A
W13	Timer 1 count auto-stop circuit selection	0		Timer 1 count auto-stop circuit not selected	
	bit (Note 3)	-	1 Timer 1 count auto-stop circuit selected		
W/12			)	Stop (state retained)	
VV 12			1	Operating	
		W11	W10	Count source	
VV11		0	0	PWM signa <mark>l (</mark> PWMOUT)	
	Timer 1 count source selection bits	0	1	Prescaler output (ORCLK)	
W10	(Note 4)	1	0	Time <mark>r 3</mark> underflow signal (T3UDF)	
		1	1	CNTR input	

Timer control register W2			at reset : 00002		at power down : 00002	R/W TAW2/TW2A	
W/22 CNTP nin output control hit		0	0 CNTR pin output invalid				
1125		1		CNTR pin output v	alid		
10/20	W22 PWM signal interrupt valid waveform/ return level selection bit	0		PWM signal "H" interval expansion function invalid			
VVZZ		1		PWM signal "H" interval expansion function valid			
\N/21	Timer O control bit	0		Stop (state retaine	d)		
VV21	Timer 2 control bit	1		Operating			
1//20	Times 2 count course calestics hit	0		XIN input			
VV20	Timer 2 count soruce selection bit	1		Prescaler output (ORCLK)/2 signal output			

Timer control register W3			at reset : 00002		at power down : state retained	R/W TAW3/TW3A
W33	Timer 3 count auto-stop circuit selection	(	)	XCIN input		
1103	bit		1	Prescaler output (ORCLK)		
W/32	W/20 T 0 1 1 1		)	Stop (Initial state)		
1102			1	Operating		
		W31	W30		Count value	
W31	Timer 2 count value calentian hite	0	0	Underflow occurs e	every 8192 counts	
	limer 3 count value selection bits	0	1	Underflow occurs every 16384 counts		
W30		1	0	Underflow occurs every 32768 counts		
		1	1	Underflow occurs e	every 65536 counts	

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: The oscillation circuit selected for system clock cannot be stopped.

3: This function is valid only when the timer 1 count start synchronous circuit is selected (I10="1").
4: Port C output is invalid when CNTR input is selected for the timer 1 count source.



Timer control register W4		at reset : 00002		at power down : state retained	R/W TAW4/TW4A		
W/43	Timer I C control bit	0	Stop (state retaine	d)	•		
VV <del>-</del> 3		1	Operating				
W/42	Timer LC count source selection bit	0	Bit 4 (T34) of timer 3				
VV42		1	System clock (STCK)				
W/41	CNTR output auto-control circuit	0	CNTR output auto-control circuit not selected				
VV-4 1	selection bit	1	CNTR output auto-control circuit selected				
W/40		0	Falling edge				
VV40	CNTR pin input count edge selection bit	1	Rising edge				

LCD control register L1		at reset : 00002		at power dov	vn : state retained	R/W TAL1/TL1A	
1.12	Internal dividing resistor for LCD power	(	)	2r X 3, 2r X 2			
L13	supply selection bit (Note 2)		1	r X 3, r X 2			
L12	LCD control bit	(	)	Stop			
			1	Operating			
		L11	L10	Duty		Bias	;
L11		0	0		Not av	ailable	
	LCD duty and bias selection bits	0	1	1/2		1/2	
110		1	0	1/3		1/3	
		1	1	1/4		1/3	

LCD control register L2		at reset : 00002		at power down : state retained	W TL2A
1 23	SEG $_{0}$ //( c3 pin function switch bit (Note 3)	0	SEG0		
L23	BEG0/VECS pintunction switch bit (Note 3)	1	VLC3		
$\mathbf{F} = \mathbf{F} \mathbf{C} (A/t) \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C}$	0	SEG1			
LZ2	SEG1/VLC2 pin function switch bit (Note 4)	1	VLC2		
1.24	SECo(t) of pip function switch bit (Note 4)	0	SEG2		
L21	SEG2/VLC1 pin function switch bit (Note 4)	1	VLC1		
1.00	Internal dividing resistor for LCD power	0	Internal dividing res	sistor valid	
L20	supply control bit	1	Internal dividing resistor invalid		

LCD control register L3		at reset : 11112		at power down : state retained	W TL3A
L33	P23/SEG20 pin function switch bit	0	SEG20		
		1	P23		
1.0-	P22/SEG19 pin function switch bit	0	SEG19		
L32		1	P22		
1.24	P21/SEG18 pin function switch bit	0	SEG18		
L31		1	P21		
L30	P20/SEG17 pin function switch bit	0	SEG17		
		1	P20		

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: "r (resistor) multiplied by 3" is used at 1/3 bias, and "r multiplied by 2" is used at 1/2 bias.
3: VLC3 is connected to VDD internally when SEG0 pin is selected.

4: Use internal dividing resistor when SEG1 and SEG2 pins are selected.



LCD control register C1		at reset : 11112		at power down : state retained	W TC1A	
C13	P03/SEG24 pin function switch bit	0	SEG24			
		1	P03			
04.5	P02/SEG23 pin function switch bit	0	SEG23			
012		1	P02			
C14	P01/SEG22 pin function switch bit	0	SEG22			
CII		1	P01			
C10	Boo/SECon pip function quaitab bit	0	SEG21			
		1	P00			

LCD control register C2		at reset : 11112		at power down : state retained	W TC2A
000	P13/SEG28 pin function switch bit	0	SEG28		
623		1	P13	<u> </u>	
C22	P12/SEG27 pin function switch bit	0	SEG27		
		1	P12		
<u> </u>	P11/SEG26 pin function switch bit	0	SEG26		
C21		1	P11		
000	P10/SECor pin function owitch hit	0	0 SEG25		
C20		1	P10		
	·				

Pull-up control register PU0		at	reset : 00002 at power down : state retained TAPU0/ TPU0A		
DUOs	Port P03 pull-up transistor	0	Pull-up transistor OFF		
P003	control bit	1	Pull-up transistor ON		
DUOs	Port P02 pull-up transistor	0	Pull-up transistor OFF		
P002	control bit	1	Pull-up transistor ON		
DU0.	Port P01 pull-up transistor	0	Pull-up transistor OFF		
P001	control bit	1	Pull-up transistor ON		
DUOs	Port P00 pull-up transistor	0	Pull-up transistor OFF		
P000	control bit	1	Pull-up transistor ON		

Pull-up control register PU1		at reset : 00002		at power down : state retained	R/W TAPU1/ TPU1A
DUIA	Port P13 pull-up transistor	0	Pull-up transistor O	FF	
PU13	control bit	1	Pull-up transistor ON		
5114	Port P12 pull-up transistor	0	Pull-up transistor O	FF	
PU12	control bit	1	Pull-up transistor O	N	
	Port P11 pull-up transistor	0	Pull-up transistor O	FF	
PU11	control bit	1	Pull-up transistor ON		
PU10	Port P10 pull-up transistor	0	Pull-up transistor OFF		
	control bit	1	Pull-up transistor O	N	

Note: "W" represents write enabled.



Port output structure control register FR0		at reset : 00002		at power down : state retained	W TFR0A	
Ports P12, P13 output structure selection		0	N-channel open-drain output			
FR03	bit	1	CMOS output	CMOS output		
ED 0-	Ports P10, P11 output structure selection	0	N-channel open-drain output			
FR02	bit	1	CMOS output			
	Ports P02, P03 output structure selection	0	N-channel open-drain output			
FR01	bit	1	CMOS output			
FR00	Ports P00, P01 output structure selection	0	N-channel open-drain output			
	bit	1	CMOS output			

Port output structure control register FR1		at reset : 00002		at power down : state retained	W TFR1A
ED4a Data Data data data data data data dat		0	N-channel open-dra	ain output	
FR13		1 CMOS output	CMOS output	<u> </u>	
FR12	Dort Do output atructure coloction hit	0	N-channel open-drain output		
	Port D2 output structure selection bit	1	CMOS output		
	Port D1 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
FR10	Dant Da autout atmosture calentian hit	0	N-channel open-dra	ain output	
	Port D0 output structure selection bit	1	CMOS output		

Port output structure control register FR2		at reset : 00002		at power down : state retained	W TFR2A	
		0	N-channel open-drain output			
FR23	Ports P22, P23 output structure selection bit	1	CMOS output	CMOS output		
500	Ports P20, P21 output structure selection bit	0	N-channel open-drain output			
FR22		1	CMOS output			
ED24	Port D5 output structure selection bit	0	N-channel open-drain output			
		1	CMOS output			
FR20	Part D4 output atructure calection, bit	0	N-channel open-dra	in output		
	Port D4 output structure selection bit	1	CMOS output			

Note: "W" represents write enabled.
	Key-on wakeup control register K0	at	reset : 00002	at power down : state retained	R/W TAK0/ TK0A					
KOa	Port P12, P13 key-on wakeup	0	Key-on wakeup not used							
KU3	control bit (Note 3)	1	1 Key-on wakeup used							
KOo	Port P10, P11 key-on wakeup	0	Key-on wakeup not used							
K02	control bit (Note 2)	1	Key-on wakeup used							
KOA	Port P02, P03 key-on wakeup	0	Key-on wakeup not used							
<b>K</b> 01	control bit	1	Key-on wakeup used							
KOo	Port P00, P01 key-on wakeup	0	Key-on wakeup not used							
K00	control bit	1	Key-on wakeup used							

	Key-on wakeup control register K1	at	reset : 00002	at power down : state retained R/W TAK1/ TK1A							
K12	Ports P12, P13 return condition selection bit	0	0 Returned by edge								
113	(Note 3)	1	Returned by level								
K10	Ports P12, P13 valid waveform/level	0	Falling waveform/"L" level								
K12	selection bit (Note 3)	1	Rising waveform/"H" level								
K4.	Ports P10, P11 return condition selection bit	0	Returned by edge								
<b>K</b> 11	(Note 2)	1	Returned by level								
K10	Ports P10, P11 valid waveform/level	0	Falling waveform/"L" level								
K10	selection bit (Note 2)	1	Rising waveform/"H" level								

	Key-on wakeup control register K2	at	reset : 00002 at power down : state retained R/W TAK2/ TK2A								
K23	Notused	0	This bit has no function, but read/write is enabled.								
1123		1									
KDo	Netwood	0	This bit has no function, but read/write is enabled								
NZ2		1	This bit has no function, but read/write is chabled.								
Kat	INIT his return condition coloction hit	0	Returned by level								
<b>K</b> 21	INT pin return condition selection bit	1	Returned by edge								
K20	INT pin koy on wakoup control bit	0	Key-on wakeup invalid								
r 20	INT pill key-on wakeup control bit	1	Key-on wakeup valid								

Notes 1: "R" represents read enabled, and "W" represents write enabled. 2: To be invalid (K02 = "0") key-on wakeup of ports P10 and P11, set the registers K10 and K11 to "0". 3: To be invalid (K03 = "0") key-on wakeup of ports P12 and P13, set the registers K12 and K13 to "0".



#### INSTRUCTIONS

The 4556 Group has the 124 (123) instructions. Each instruction is described as follows;

(1) Index list of instruction function

(2) Machine instructions (index by alphabet)

(3) Machine instructions (index by function)

(4) Instruction code table

#### SYMBOL

The symbols shown below are used in the following list of instruction function and the machine instructions.

Symbol	Contents	Symbol	Contents
A	Register A (4 bits)	PS	Prescaler
В	Register B (4 bits)	T1	Timer 1
DR	Register DR (3 bits)	T2	Timer 2
F	Register F (8 bits)	T3	Timer 3
 V1	Interrupt control register V1 (4 bits)	TIC	Timer I C
V2	Interrupt control register V2 (4 bits)	T1F	Timer 1 interrupt request flag
11	Interrupt control register 12 (1 site)	T2F	Timer 2 interrupt request flag
MR	Clock control register MR (4 bits)	T3F	Timer 3 interrupt request flag
RG	Clock control register RG (3 bits)	WDF1	Watchdog timer flag
PA	Timer control register PA (1 bit)	WEF	Watchdog timer enable flag
W1	Timer control register W1 (4 bits)	INTE	Interrupt enable flag
W2	Timer control register W2 (4 bits)	EXE0	External 0 interrupt request flag
W3	Timer control register W3 (4 bits)	P	Power down flag
WA	Timer control register W4 (4 bits)		l ower down hag
	I CD control register I 1 (4 bits)	D	Port D (8 bits)
12	LCD control register L2 (4 bits)	PO	Port P0 (4 bits)
13	LCD control register L3 (4 bits)	P1	Port P1 (4 bits)
C1	LCD control register C1 (4 bits)	P2	Port P2 (4 bits)
C2	LCD control register C2 (4 bits)	C	Port C (1 bit)
PUO	Pull-up control register PU0 (4 bits)	l l	
PU1	Pull-up control register PU1 (4 bits)	x	Hexadecimal variable
FRO	Port output structure control register FR0 (4 bits)	N N	Hexadecimal variable
FR1	Port output structure control register FR1 (4 bits)	7	Hexadecimal variable
FR2	Port output structure control register FR2 (4 bits)	- n	Hexadecimal variable
KO	Key-on wakeup control register K0 (4 bits)	P n	Hexadecimal constant
K1	Key-on wakeup control register K1 (4 bits)		Hexadecimal constant
K2	Key-on wakeup control register K2 (4 bits)		Hexadecimal constant
X	Register X (4 bits)	A3A2A1A0	Binary notation of hexadecimal variable A
Y	Register Y (4 bits)		(same for others)
7	Register 7 (2 bits)		
DP	Data pointer (10 bits)	<b> </b> ←	Direction of data movement
	(It consists of registers X, Y, and Z)	$\leftrightarrow$	Data exchange between a register and memory
PC	Program counter (14 bits)	2	Decision of state shown before "?"
РСн	High-order 7 bits of program counter	()	Contents of registers and memories
PCI	Low-order 7 bits of program counter	_	Negate. Flag unchanged after executing instruction
SK	Stack register (14 bits X 8)	M(DP)	RAM address pointed by the data pointer
SP	Stack pointer (3 bits)	a	Label indicating address a6 a5 a4 a3 a2 a1 a0
CY	Carry flag	n.a	Label indicating address a6 a5 a4 a3 a2 a1 a0
UPTE	High-order bit reference enable flag	p, ~	in page p6 p5 p4 p3 p2 p1 p0
RPS	Prescaler reload register (8 bits)	С	Hex. C + Hex. number x
R1	Timer 1 reload register (8 bits)	+	
R3	Timer 3 reload register (8 bits)	^	
R2L	Timer 2 reload register (8 bits)		
R2H	Timer 2 reload register (8 bits)		
RLC	Timer LC reload register (4 bits)		
	<b>3</b> ( <b>1 1 1</b>		

Note : Some instructions of the 4556 Group has the skip function to unexecute the next described instruction. The 4556 Group just invalidates the next instruction when a skip is performed. The contents of program counter is not increased by 2. Accordingly, the number of cycles does not change even if skip is not performed. However, the cycle count becomes "1" if the TABP p, RT, or RTS instruction is skipped.



Group- ing	Mnemonic	Function		Group- ing	Mnemonic	Function
	ТАВ	$(A) \leftarrow (B)$			XAMI j	$(A) \leftarrow \rightarrow (M(DP))$
	тва	$(B) \leftarrow (A)$		transfe		$ (X) \leftarrow (X) \in XOR(J) $ $ j = 0 \text{ to } 15 $ $ (Y) \leftarrow (Y) + 1 $
	TAY	$(A) \leftarrow (Y)$		register	TMA i	$((((DP))) \leftarrow (A)$
	ΤΥΑ	$(Y) \leftarrow (A)$	AM to	······,	$(X) \leftarrow (X) EXOR(j)$ j = 0  to  15	
	TEAB	(E7−E4) ← (B)		~		
ansfer		(E3−E0) ← (A)			LA n	(A) ← n n = 0 to 15
r tra	TABE	(B) ← (E7–E4)				
registe		$(A) \leftarrow (E_3-E_0)$		TABP p	$(SP) \leftarrow (SP) + 1$ $(SK(SP)) \leftarrow (PC)$	
ster to	TDA	$(DR2-DR0) \leftarrow (A2-A0)$				$(PCH) \leftarrow p (Note)$ $(PCL) \leftarrow (DR2-DR0, A3-A0)$ at (UPTF) = 0
egis	TAD	$(A_2-A_0) \leftarrow (DR_2-DR_0)$				(B) ← (RÓM(PC))7–4
n v		(A3) ← 0				(A) $\leftarrow$ (ROM(PC))3–0 at (UPTF) = 1
						$(DR_2) \leftarrow (0)$
	TAZ	$(A1, A0) \leftarrow (Z1, Z0)$				$(DR1, DR0) \leftarrow (ROM(PC))9, 8$
		(A3, A2) ← 0	_			$(A) \leftarrow (ROM(PC))^{7-4}$
						$(PC) \leftarrow (SK(SP))$
	TAX	$(A) \leftarrow (X)$			(SP) ← (SP) – 1	
	TASP	$(A_2-A_0) \leftarrow (SP_2-SP_0)$			AM	$(A) \leftarrow (A) + (M(DP))$
		(A3) ← 0		AMC	$(A) \leftarrow (A) + (M(DP)) + (CY)$	
		(1)		atio		$(CY) \leftarrow Carry$
	LXY X, Y	$(X) \leftarrow X X = 0$ to 15 $(Y) \leftarrow V X = 0$ to 15		oper		
ses		(1) ← y y = 0 to 13	etic e	A n	$(A) \gets (A) + n$	
dress	LZ z	$(Z) \leftarrow z z = 0 \text{ to } 3$		rithme		n = 0 to 15
tAM ac	INY	$(Y) \leftarrow (Y) + 1$		<	AND	$(A) \leftarrow (A) AND (M(DP))$
L.C.	DEY	$(Y) \leftarrow (Y) - 1$		OR	$(A) \leftarrow (A) \; OR \; (M(DP))$	
	TAM j	$(A) \leftarrow (M(DP))$			sc	(CY) ← 1
J.		(X) ← (X)EXOR(j) j = 0 to 15		RC	$(CY) \leftarrow 0$	
transfe	XAM j	$(A) \leftarrow \rightarrow (M(DP))$		szc	(CY) = 0 ?	
gister		$(X) \leftarrow (X)EXOR(j)$ j = 0 to 15		СМА	$(A) \leftarrow (\overline{A})$	
to re					RAR	I→CY→A3A2A1A0
MA	XAMD j	$(A) \leftarrow \rightarrow (M(DP))$				
		$(X) \leftarrow (X) E X U K(J)$				
		J = 0   0   10				
		$(1) \leftarrow (1) = 1$				

#### INDEX LIST OF INSTRUCTION FUNCTION

Note: p is 0 to 31 for M34556M4/M4H.

p is 0 to 63 for M34556M8/M8H/G8/G8H.

RENESAS

INDEX LIST OF INSTRUCTION FUNCTION	(continued)
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Group- ing	Mnemonic	Function		Group- ing	Mnemonic	Function
	SB j	(Mj(DP)) ← 1			DI	$(INTE) \leftarrow 0$
ation	RB j	j = 0 to 3 (Mj(DP)) ← 0			EI	(INTE) ← 1
oper		j = 0 to 3			SNZ0	V10 = 0: (EXF0) = 1 ?
Bit	S7B i	(Mi(DP)) = 0.2				$(EXF0) \leftarrow 0$ V10 = 1: SNZ0 = NOP
	020 )	j = 0 to 3				
	OF AM			ion	SNZI0	12 = 1: (INT) = "H"?
rison tion	SEAM	(A) = (M(DP)) ?		oerat		112 = 0 ( $1101$ ) = L ?
ompa	SEA n	(A) = n?		npt of	TAV1	$(A) \leftarrow (V1)$
ŏ°		n = 0 to 15		nterru	TV1A	$(V1) \leftarrow (A)$
_	Ва	(PCL) ← a6–a0		_		
ation	BLp,a	 (РСн) ← р			TAV2	$(A) \leftarrow (V2)$
h oper		$(PCL) \leftarrow a6-a0$			TV2A	(V2) ← (A)
Brand	BLA p	(РСн) ← р			TAI1	(A) ← (I1)
		(PCL) ← (DR2–DR0, A3–A0)		$\bigcirc$	TI1A	(I1) ← (A)
	BM a	(SP) ← (SP) + 1				
		$(SK(SP)) \leftarrow (PC)$ $(PCH) \leftarrow 2$			TPAA	$(PA) \leftarrow (A)$
		$(PCL) \leftarrow a6-a0$			TAW1	$(A) \leftarrow (W1)$
eratior	BML p, a	$(SP) \leftarrow (SP) + 1$			TW1A	(W1) ← (A)
tine op		$(SK(SP)) \leftarrow (PC)$ $(PCH) \leftarrow p$			TAW2	(A) ← (W2)
Subrou		$(PCL) \leftarrow a6-a0$			TW2A	(W2) ← (A)
	BMLA p	$(SP) \leftarrow (SP) + 1$ $(SK(SP)) \leftarrow (PC)$			TAW3	(A) ← (W3)
		$(PCH) \leftarrow p$ $(PCL) \leftarrow (DR2-DR0, A3-A0)$		ration	ТѠЗА	(W3) ← (A)
				r ope		
	RTI	$(PC) \leftarrow (SK(SP))$ $(SP) \leftarrow (SP) - 1$		Time	TAVV4	$(A) \leftarrow (W4)$
					TW4A	$(W4) \leftarrow (A)$
	RI	$(PC) \leftarrow (SK(SP))$ $(SP) \leftarrow (SP) - 1$			TABPS	$(B) \leftarrow (TPS7-TPS4)$
ation						$(A) \leftarrow (TPS_3 - TPS_0)$
opera	RIS	$(PC) \leftarrow (SK(SP))$ $(SP) \leftarrow (SP) - 1$			TPSAB	(RPS7–RPS4) ← (B)
turn						$(TPS7-TPS4) \leftarrow (B)$
Re						(RPS3–RPS0) ← (A) (TPS3–TPS0) ← (A)

Note: p is 0 to 31 for M34556M4/M4H.



Group- ing	Mnemonic	Function		Group- ing	Mnemonic	Function
	TAB1	(B) ← (T17–T14)	1		CLD	(D) ← 1
		(A) ← (T13–T10)				
					RD	$(D(Y)) \leftarrow 0$
	T1AB	$(R17-R14) \leftarrow (B)$				(Y) = 0  to  7
		$(117-114) \leftarrow (B)$			20	
		$(R13-R10) \leftarrow (A)$			50	$(D(Y)) \leftarrow 1$
		(113-110) ← (A)				
	TAB2	(B) ← (T27–T24)			SZD	(D(Y)) = 0?
		(A) ← (T23–T20)				(Y) = 0 to 5
	T2AB	$(R27-R24) \leftarrow (B)$			RCP	$(C) \leftarrow 0$
		$(127-124) \leftarrow (B)$			COD.	$(0) \leftarrow 1$
		$(R23-R20) \leftarrow (A)$ $(T23-T20) \leftarrow (A)$			307	$(C) \leftarrow T$
		$(123, 120) \leftarrow (A)$			TAPUO	$(A) \leftarrow (PU0)$
	T2HAB	(R2H7–R2H4) ← (B)		utput operation		
E		(R2H3–R2H0) ← (A)			TPU0A	(PU0) ← (A)
operatic						
	TR1AB	$(R17-R14) \leftarrow (B)$			TAPU1	$(A) \leftarrow (PU1)$
ner		(R13–R10) ← (A)				
i 🗄	T2R2I	$(T_{27}-T_{24}) \leftarrow (R_{217}-R_{214})$		ut/O	IFUIA	$(FOT) \leftarrow (A)$
		$(T23-T20) \leftarrow (R2L3-R2L0)$		lnpu	тако	(A) ← (K0)
	TLCA	$(LC) \leftarrow (A)$			ткоа	(K0) ← (A)
		$(RLC) \leftarrow (A)$				
	SN7T1	1/10 = 0; (T1E) = 1.2			IAK1	$(A) \leftarrow (K1)$
	SINZII	V12 = 0. (11F) = 1.2 (T1F) $\leftarrow 0$			тк1а	$(K1) \leftarrow (A)$
		$V_{12} = 1$ : SNZT1 = NOP				
					TAK2	(A) ← (K2)
	SNZT2	V13 = 0: (T2F) = 1 ?				
		(T2F) ← 0			TK2A	$(K2) \leftarrow (A)$
		V13 = 1: SNZT2 = NOP			TEDOA	
	SN7T3	$V_{20} = 0$ ; (T3E) = 1.2			IFRUA	(FR0) ← (A)
	011210	$(T3F) \leftarrow 0$			TFR1A	 (FR1) ← (A)
		V20 = 1: SNZT3 = NOP				
			ļ		TFR2A	$(FR2) \leftarrow (A)$
	IAP0	$(A) \leftarrow (P0)$				
	0.004				CRCK	RC oscillator selected
atior	OPUA	$(P0) \leftarrow (A)$			TAMR	$(A) \leftarrow (MR)$
pera	IAP1	$(A) \leftarrow (P1)$		io		
nt o				erat	TMRA	$(MR) \leftarrow (A)$
Dutp	OP1A	(P1) ← (A)		do >		
ut/C				loch	TRGA	$(RG) \leftarrow (A)$
dul	IAP2	(A) ← (P2)				
	0024	$(\mathbf{P}_{2})$ (A)				
	UPZA	$(\Gamma^2) \leftarrow (A)$				

#### INDEX LIST OF INSTRUCTION FUNCTION (continued)



Group- ing	Mnemonic	Function	
	TAL1	$(A) \leftarrow (L1)$	
	TL1A	(L1) ← (A)	
eration	TL2A	(L2) ← (A)	
CD ope	TL3A	(L3) ← (A)	
L C	TC1A	(C1) ← (A)	
	TC2A	(C2) ← (A)	
	NOP	$(PC) \leftarrow (PC) + 1$	
	POF	Transition to clock operating mode	
	POF2	Transition to RAM back-up mode	
	EPOF	POF, POF2 instructions valid	0
uo	SNZP	(P) = 1 ?	.0
operati	DWDT	Stop of watchdog timer function enabled	
Other o	SRST	System reset	*
	WRST	(WDF1) = 1 ?	
	RUPT	$(WDFT) \leftarrow 0$	
	SUPT	(UPTF) ← 1	
	SVDE (Note)	At power down mode, voltage drop detection circuit valid	

#### **INDEX LIST OF INSTRUCTION FUNCTION (continued)**

Note: The SVDE instruction can be used only for the H version.

## MACHINE INSTRUCTIONS (INDEX BY ALPHABET)

An (Add n	and accumulator)										
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition						
code	0 0 0 1 1 0 n n n <sub>2</sub> 0 6 n <sub>16</sub>	1	1	_	Overflow = 0						
Operation:	$(A) \leftarrow (A) + n$	Grouping: Arithmetic operation									
	n = 0 to 15	Description: Adds the value n in the immediate field to register A, and stores a result in register A. The contents of carry flag CY remains unchanged. Skips the next instruction when there is no overflow as the result of operation. Executes the next instruction when there is overflow as the result of operation.									
AM (Add a	ccumulator and Memory)										
Instruction code	D9 D0 D0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0	Number of words	Number of cycles	Flag CY	Skip condition						
		1	1	-	-						
Operation:	$(A) \leftarrow (A) + (M(DP))$	Grouping:	Arithmetic	operation							
		<b>Description:</b> Adds the contents of M(DP) to register A.									
			of carry flag CY remains unchan								
AMC (Add	accumulator, Memory and Carry)										
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition						
		1	1	0/1	-						
Operation:	$(A) \leftarrow (A) + (M(DP)) + (CY)$	Grouping: Arithmetic operation									
	(CY) ← Carry	Description	: Adds the o CY to regi ter A and c	contents of ster A. Sto carry flag C	f M(DP) and carry flag res the result in regis- Y.						
AND (logic	al AND between accumulator and memory)										
Instruction code	D9 D0 D0 0 1 1 0 0 0 1 8	Number of words	Number of cycles	Flag CY	Skip condition						
		1	1	_	_						
Operation:	$(A) \leftarrow (A) AND (M(DP))$	Grouping:	Arithmetic	operation							
		Descriptior	1: Takes the tents of r M(DP), an	AND operated as a construction of the stores the store st	ND operation between the con- gister A and the contents of stores the result in register A.						

RENESAS

B a (Branch	1 to a	add	ress	<u>; a)</u>															
Instruction	D9								Do				Number of	Number of	Flag CY	Skip condition			
code	0	1	1	a6	as a	4 a	a a	2 a1	a0	1	8	a	words	cycles					
									2		+a	16	1	1	-	-			
Operation:	(PC	L) ←	- a6 to	o a0									Groupina:	Branch op	eration				
	(	_, .											Description: Branch within a page : Branches to address						
													a in the identical page.						
													<b>Note:</b> Specify the branch address within the page						
										including this instruction.									
BL p, a (Bra	anch	n Lo	ng t	o ad	dres	s a	in p	age	p)				1						
Instruction	D9		<u> </u>					0	D0				Number of	Number of	Flag CY	Skip condition			
code	0	0	1	1	1 p	4 n	03 D	2 01	00	0	E	p	words	cycles		-			
											2	2	-	-					
	1	0	р5	a6	as a	4 a	as a	2 <b>a</b> 1	a0 2	2	+a	a <sub>16</sub>	Grouping:	Branch op	eration				
Operation:	(PC	н) ←	- p										<b>Description</b>	: Branch out	t of a page	: Branches to address			
	(PC	L) ←	- a6 t	o a0									J. J.	a in page p	<b>)</b> .				
													Note:	p is 0 to 3	1 for M345	556M4/M4H and p is 0			
														to 63 for M	134556M8/	M8H/G8/G8H.			
BLA p (Bra	nch	Lor	na to	ado	dress	(D	) + (	A) in	pag	e p)									
	 D9		.9.10			(-	<u>,</u>	)	D0	- F/	-		Number of	Number of	Flag CY	Skip condition			
code		0	0	0	0 1	0		0	0	0	1	0	words	cycles	l lag e l	emp containen			
		•		<u> </u>	•				2		·	<u> </u>	2	2	-	_			
	1	0	<b>p</b> 5	p4	0 0	p	зр	2 p1	p0 2	2	р	р <sub>16</sub>	Grouping	Branch an	oration				
Operation:			<b>n</b>					_					Grouping: Branch operation						
Operation.	(PC	-) ← 1 ) ←	- P - (DR	2-DF	R0 A3-	-A0)	-							(DR2 DR1	DR0 A3 A	2 A1 A0)2 specified by			
	(. 0	-) `	(51)	2 01	10,710	1.0)								registers D	and A in p	bage p.			
													Note:	p is 0 to 3	1 for M345	556M4/M4H and p is 0			
														to 63 for M	34556M8/	M8H/G8/G8H.			
				_					- 1										
BM a (Bran	ch a	nd	Mar	k to	addr	ess	a ir	n pag	je 2)				1	1	1				
Instruction	D9							_	D0				Number of	Number of	Flag CY	Skip condition			
code	0	1	0	<b>a</b> 6	as a	4 a	ia a	2 <b>a</b> 1	a0 2	1	a	a <sub>16</sub>	1	1					
Operation:	(SP)	$) \leftarrow ($	(SP)	+ 1									Grouping:	Subroutine	e call opera	ation			
	(SK	(SP)	) ← (	(PC)									Description	: Call the s	ubroutine	in page 2 : Calls the			
	(PC	н) ←	- 2											subroutine	at addres	s a in page 2.			
	(PC	L) ←	- a6-a	<b>a</b> 0									Note:	Note: Subroutine extending from page					
													other page can also be called with the BM						
													Instruction when it starts on page						
														maximum l	EVEL OF SUB	routine nesting is 8			
														maximum		routine neoting is o.			



							•									•	-				
BML p, a (	Bran	ch a	and	Marl	k Lo	ong	to a	add	lres	s a	in p	a	ge p	))							
Instruction	D9															Number of words	Number of cycles	Flag CY	Skip condition		
coue	0	0	1	1		p4	рз	p2	р1	p0	2	)	+p	p	_16 □	2	2	-	-		
	1	0	<b>p</b> 5	<b>a</b> 6	as	a4	аз	a2	a1	<b>a</b> 0	2	2	+a	а	16	Grouping	Subroutine		ation		
Operation:	(SP			<b>⊥</b> 1												Description	: Call the su	broutine :	Calls the subroutine at		
operation.	(SK	$(SK(SP)) \leftarrow (PC)$													address a	in page p.					
	(PCH) ← p													Note:	p is 0 to 3	1 for M34	556M4/M4H and p is 0				
	$(PCL) \leftarrow a6-a0$														to 63 for M	34556M8/	M8H/G8/G8H.				
	`														Be careful	not to ove	the stack because the				
														maximum l	evel of sub	routine nesting is 8.					
BMLA p (B	rand	:h a	nd N	/lark	Lor	na	to a	ddr	ess	s (D)	) + (	Ά	) in	na	ae i	 כו					
Instruction		n u		nan	201	9		uui	000	D0		<u>, , ,</u>	,	րս	901	Number of	Number of	Elag CY	Skip condition		
code		0		0	1	1	0	0	0		Γ	<u> </u>	2	0	٦	words	cycles	i lag e i	emp contanion		
	<u>0 0 0 0 1 1 0 0 0 0 2</u> 0 3 0 16											2	2	_	_						
	1	0	<b>D</b> 5	D4	0	0	<b>D</b> 3	p2	D1	<b>D</b> 0		>	p	n	7						
		-	1	F.	-	-	1	F -	F.	P -	2	_	F	F	16	Grouping:	Subroutine	e call opera	ation		
Operation:	(SP	) ←	(SP)	+ 1												Description	: Call the su	broutine :	Calls the subroutine at		
	$(SK(SP)) \leftarrow (PC)$															address (DR2 DR1 DR0 A3 A2 A1 A0)2 speci-					
	(РСн) ← р														fied by reg	isters D ar	nd A in page p.				
	(PC	;L) ←	(DR	2–DR	0, A	з–А	0)									Note:	p is 0 to 3	1 for M348	556M4/M4H and p is 0		
														to 63 for M	134556M8/	M8H/G8/G8H.					
																Be careful not to over the stack because the					
																	maximum I	evel of sub	routine nesting is 8.		
CLD (CLea	r po	rt D	)																		
Instruction	D9									D0						Number of	Number of	Flag CY	Skip condition		
code	0	0	0	0	0	1	0	0	0	1		)	1	1	]	words	cycles				
											2 🗆				_16	1	1	_	_		
Operation:	(D)	← 1														Grouping:	Input/Outp	ut operatio	n		
																<b>Description:</b> Sets (1) to port D.					
CMA (CoM	plen	nent	of A	Accu	mul	lato	or)											1			
Instruction code	D9	0	0	0	0	1	1	1	0	D0 0	. [	0	1	С	٦.,	Number of words	Number of cycles	Flag CY	Skip condition		
		1					1				2 L				_16	1	1	-	_		
Operation:	(A)	$\leftarrow \overline{(A)}$	۹)													Grouping:	Arithmetic	operation			
								<b>Description:</b> Stores the one's complement for registe A's contents in register A.													



CRCK (Clo	ck select: Rc oscillation ClocK)						
Instruction code	D9 D0 1 0 1 0 0 1 1 0 1 1 2 9 B	Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	-		
Operation:	RC oscillation circuit selected	Grouping:	Clock cont	rol operati	on		
		Description	: Selects the clock f(XIN	e RC osci ).	llation circuit for main		
DEY (DEc	rement register Y)						
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	(Y) = 15		
Operation:	$(Y) \leftarrow (Y) - 1$	Grouping:	RAM addr	esses			
		Description: Subtracts 1 from the contents of reg			contents of register Y.		
			As a resu	aister Y is	action, when the con- 15 the next instruction		
			is skipped	. When the	e contents of register Y		
			is not 15, t	the next in	struction is executed.		
DI (Disable	e Interrupt)	1	1	1			
Instruction code	D9 D0 0 0 0 0 0 0 0 1 0 0 2 0 0 4 16	Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	_		
Operation:	$(INTE) \leftarrow 0$	Grouping:	rouping: Interrupt control operation				
		Description	disables th	to interrup			
		Note:	Interrupt is struction a	s disabled fter execut	by executing the DI in- ing 1 machine cycle.		
	*						
DWDT (Dis	sable WatchDog Timer)						
Instruction code	D9 D0 1 0 1 0 0 1 1 0 0 2 9 C	Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	_		
Operation:	Stop of watchdog timer function enabled	Grouping:	Other oper	ration			
		Description: Stops the watchdog timer function WRST instruction after executi DWDT instruction.			timer function by the after executing the		



EI (Enable	Interrupt)				
Instruction		Number of words	Number of cycles	Flag CY	Skip condition
coue	0 0 0 0 0 0 0 1 0 1 2 0 0 5 16	1	1	-	_
Operation:	(INTE) ← 1	Grouping:	Interrupt c	ontrol oper	ation
	(	Description	: Sets (1) to	interrupt	enable flag INTE, and
			enables th	e interrupt.	
		Note:	Interrupt is	s enabled I	by executing the EI in-
			struction a	fter execut	ing 1 machine cycle.
FPOF (En	able POF instruction)				
		Number of	Number of	Flag CY	Skip condition
code		words	cycles	lug o l	
		1	1	-	_
					L
Operation:	POF instruction, POF2 instruction valid	Grouping:	Other ope	ration	o ofter POE instruction
		or POF2 instruction valid by execu			valid by executing the
			EPOF inst	ruction.	· · · · · · · · · · · · · · · · · · ·
IAP0 (Inpu	t Accumulator from port P0)				
Instruction		Number of	Number of	Flag CY	Skip condition
code	1 0 0 1 1 0 0 0 0 0 0 2 2 6 0 <sub>16</sub>	words	cycles		
		1	1	_	_
Operation:	$(A) \leftarrow (P0)$	Grouping: Input/Output operation			
•		<b>Description:</b> Transfers the input of port P0 to register A.			
	t Accumulator from port P1)				
Instruction		Number of	Number of	Flag CY	Skip condition
code		words	cycles	l'ing e i	Chip Condition
		1	1	_	_
Operation:	$(A) \leftarrow (P1)$	Grouping:	Input/Outp	out operatio	on
		Description	1: Transfers	the input o	f port P1 to register A.



IAP2 (Inpu	t Accumulator from port P2)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	1     0     0     1     1     0     0     1     0     2     2     6     2	words	cycles 1	_	
			•		
Operation:	$(A) \leftarrow (P2)$	Grouping:	Input/Outp	ut operatio	n
		Description	: Transfers t	he input o	f port P2 to register A.
INY (INcre	ment register Y)				
		Number of	Number of	Flag CY	Skip condition
code		words	cycles	Thay OT	Skip condition
coue	0 0 0 0 0 1 0 0 1 1 2 0 1 3 16	1	1	-	(Y) = 0
Operation:	$(Y) \leftarrow (Y) + 1$	Grouping:	RAM addre	esses	
		Description	: Adds 1 to t	he content	s of register Y. As a re-
			sult of ad	ldition, w	hen the contents of
			register Y	' is 0, th	e next instruction is
			skipped. W	/hen the c	ontents of register Y is
			not 0, the r	next instrue	ction is executed.
LA n (Load	n in Accumulator)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	0 0 0 1 1 1 n n n n <sub>2</sub> 0 7 n <sub>16</sub>	words	cycles		
		1	1	-	description
Operation:	(A) ← n	Grouping:	Arithmetic	operation	
	n = 0 to 15	Description	: Loads the	value n in	the immediate field to
			register A.	A	(
		when the LA instructions are continuou coded and executed, only the first LA struction is executed and other			Lons are continuously
					uted and other LA
			instructio	ns code	d continuously are
			skipped.		
LXY x, y (l	_oad register X and Y with x and y)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	1 1 x3 x2 x1 x0 y3 y2 y1 y0 3 x y	words	cycles		
		1	1	-	Continuous description
Operation:	$(X) \leftarrow x x = 0 \text{ to } 15$	Grouping:	RAM addr	esses	
	$(Y) \leftarrow y \ y = 0 \text{ to } 15$	Description	1: Loads the	value x in	the immediate field to
			register X,	and the v	alue y in the immediate
			field to re	gister Y. V	Vhen the LXY instruc-
			tions are c	ontinuous	y coded and executed,
			only the f	irst LXY ii	nstruction is executed
			and other		uctions coded continu-
			ously are s	sкippea.	



LZ z (Load	register Z with z)					
Instruction code	D9 D0 D0 1 0 71 70 0 4 8	Number of words	Number of cycles	Flag CY	Skip condition	
	0 0 0 1 0 0 1 0 21 20 2 0 4 +z 16	1	1	-	-	
Operation:	$(Z) \leftarrow z \ z = 0 \text{ to } 3$	Grouping:	RAM addr	esses		
		Description	: Loads the	value z in	the immediate field to	
			register Z.			
NOP (NOC		Number of	Number of	Flog CV	Skip condition	
code	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	words	cycles	Flag C Y	Skip condition	
		1	1	-	-	
Operation:	$(PC) \leftarrow (PC) + 1$	Grouping:	Other ope	ration		
		Description: No operation; Adds 1 to program counter				
		value, and others remain unchanged.				
OP0A (Out	tput port P0 from Accumulator)					
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code	1 0 0 0 1 0 0 0 0 0 2 2 2 0 <sub>16</sub>	1	1	-	_	
Operation:	$(P0) \leftarrow (A)$	Grouping	Input/Outr		 מנ	
operation		<b>Description:</b> Outputs the contents of register A to port				
			Ρ0.			
OP1A (Out	tput port P1 from Accumulator)		1			
Instruction		Number of words	Number of cycles	Flag CY	Skip condition	
coue		1	1	-	_	
Operation:	(P1) ← (A)	Grouping:	Input/Outp	out operation	ิท	
		Descriptior	1: Outputs th P1.	he content	s of register A to port	



OP2A (Out	put port P2 from Accumulator)						
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition		
code	1 0 0 0 1 0 0 0 1 0 <sub>2</sub> 2 2 2 <sub>16</sub>	words	cycles				
		1	1	-	_		
Operation:	$(P2) \leftarrow (A)$	Grouping:	Input/Outp	ut operatio	on		
		Description	: Outputs th	ne content	s of register A to port		
			P2.				
OR (logica	I OR between accumulator and memory)						
Instruction code	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	-		
Operation:	$(A) \leftarrow (A) \text{ OR } (M(DP))$	Grouping:	Arithmetic	operation			
•		Description	: Takes the	OR opera	tion between the con-		
		tents of register A and the conte			and the contents of		
			M(DP), and	d stores th	e result in register A.		
POF (Pow	er OFf)		1		F		
Instruction	D9 D0 0 0 0 0 0 0 0 0 1 0 2 16	Number of	Number of	Flag CY	Skip condition		
code		words	cycles				
		ļ '	I	_	_		
Operation:	Transition to clock operating mode	Grouping:	Grouping: Other operation				
		Description	: Puts the sy	stem in cl	ock operating mode by		
			executing	the POF2	2 instruction after ex-		
		Note:	If the EPOF	instruction	n is not executed before		
			executing	this instruc	ction, this instruction is		
			equivalent	to the NOF	instruction.		
POF2 (Pov	ver UFt2)	Number	Number				
Instruction		Number of words	Number of cvcles	Flag CY	Skip condition		
coue	0 0 0 0 0 0 1 0 0 0 2 0 8 16	1	1	-	_		
Operation:	Transition to RAM back-up mode	Grouping:	Other oper	ration	I		
		Description	: Puts the s	ystem in	RAM back-up state by		
			executing	the POF	2 instruction after ex-		
			ecuting the	EPOF in	struction.		
		Note:	If the EPOI	- instructio	n is not executed before		
			executing	to the NOF	cuon, this instruction is		
			oquivalont				



RAR (Rota	te Accumulator Right)					
Instruction code	D9 D0 0 0 0 1 1 0 1 0 1 D	Number of words	Number of cycles	Flag CY	Skip condition	
		1	1	0/1	-	
Operation:	→CY → A3A2A1A0	Grouping:	Arithmetic	operation		
		Description	<ul> <li>Rotates 1 cluding the right.</li> </ul>	bit of the co e contents	ontents of register A in- of carry flag CY to the	
DB i /Door			-			
RBJ (Rese						
Instruction code	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of words	Number of cycles	Flag CY	Skip condition	
<u> </u>				_		
Operation:	$(M)(DP)) \leftarrow 0$ i = 0 to 3	Grouping:	Bit operati	on		
	] = 0.003	Description	by the va	the conter	e immediate field) of	
		5	M(DP).	···· , ··· ··		
RC (Reset	Carry flag)					
Instruction code	D9 D0 0 0 0 0 0 0 0 1 1 0 0 0 6	Number of words	Number of cycles	Flag CY	Skip condition	
		1	1	0	_	
Operation:	$(CY) \leftarrow 0$	Grouping: Arithmetic operation				
		Description		to carry ha	y C 1.	
RCP (Rese	et Port C)					
Instruction code	D9 D0 1 0 1 0 0 0 1 1 0 0 2 8 C	Number of words	Number of cycles	Flag CY	Skip condition	
		1	1	0	_	
Operation:	$(C) \leftarrow 0$	Grouping: Input/Output operation Description: Clears (0) to carry flag CY.				



RD (Reset	port D specified by register Y)					
Instruction code	D9 D0 0 0 0 1 0 1 0 0 1 4	Number of words	Number of cycles	Flag CY	Skip condition	
	2 16	1	1	-	-	
Operation:	$(D(Y)) \gets 0$	Grouping:	Input/Outp	ut operatio	n	
	However,	Description	: Clears (0)	to a bit of p	port D specified by reg-	
	(Y) = 0 to 7		ISLET T.			
RT (ReTur	n from subroutine)					
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code	0 0 0 1 0 0 0 1 0 0 2 0 4 4 16	words	cycles			
			2	_	_	
Operation:	$(PC) \leftarrow (SK(SP))$		Return ope	eration		
	$(SP) \leftarrow (SP) = 1$	Descriptior	n: Returns f	from subroutine to the routine		
				Subroutine		
RTI (ReTur	n from Interrupt)					
Instruction		Number of	Number of	Flag CY	Skip condition	
code	0 0 0 1 0 0 0 1 1 0 2 0 4 6 16	1	1	-	-	
Operation:	$(PC) \leftarrow (SK(SP))$	Grouping:	Return ope	eration		
	$(SP) \leftarrow (SP) - 1$	Description	: Returns fr main routir	om interru ne.	upt service routine to	
			Returns ea	ich value o	f data pointer (X, Y, Z),	
			the continu	skip status ious descri	ption of the LA/LXY in-	
			struction,	register A	and register B to the	
			states just	before inte	errupt.	
RTS (ReTu	Irn from subroutine and Skip)	1	1			
Instruction code	D9 D0 0 0 0 1 0 0 1 0 1 0 1 0 4 5 16	Number of words	Number of cycles	Flag CY	Skip condition	
		1	2	-	Skip at uncondition	
Operation:	$(PC) \leftarrow (SK(SP))$	Grouping:	Return ope	eration		
	(SP) ← (SP) – 1	<b>Description:</b> Returns from subroutine to the rout called the subroutine, and skips the nex struction at uncondition.			outine to the routine , and skips the next in- on.	



RUPT (Re	set UPTF flag)					
Instruction		Number of	Number of	Flag CY	Skip condition	
code	0 0 0 1 0 1 1 0 0 0 0 1 0 1 1 0 0 0 0 1 1 0	1	1	_	_	
Operation		Crownings	Other and	ration		
Operation.	$(OFTF) \leftarrow O$	Descriptior	Clears (0)	to the high	gh-order bit reference	
			enable flag	g.	-	
SR i (Sot F	2;+\					
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code	0 0 0 1 0 1 1 j j 2 0 5 C ti 16	words	cycles			
		1	1	-	-	
Operation:	$(Mj(DP)) \leftarrow 1$	Grouping:	Bit operati	on		
	j = 0 to 3	Description	: Sets (1) th	e contents	of bit j (bit specified by	
			the value j	in the init		
SC (Set Ca	arry flag)	1				
Instruction		Number of	Number of	Flag CY	Skip condition	
code	0 0 0 0 0 0 0 1 1 1 2 0 0 7 16	1	1	1	-	
Operation:	(CY) ← 1	Grouping:	Arithmetic	operation		
•		<b>Description:</b> Sets (1) to carry flag CY.				
SCP (Set F	Port C)					
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code	1 0 1 0 0 0 1 1 0 1 2 2 8 D 16	1	1	_	-	
Operation		Grouping	Input/Outp		n	
Operation:	$(C) \leftarrow T$	Description	: Sets (1) to	port C.		



SD (Set po	rt D specified by register Y)				
Instruction		Number of	Number of	Flag CY	Skip condition
code	0 0 0 0 0 1 0 1 0 1 2 0 1 5 16	1	1	-	
Operation		Grouping	Input/Outp		n
Operation:	$(D(f)) \leftarrow T$ $(Y) = 0 \text{ to } 7$	Description	n: Sets (1) to	a bit of po	ort D specified by regis-
			ter Y.		
SEA n (Sk	in Equal Accumulator with immediate data n				
JEA II (SK		Number of	Number of	Elag CV	Skin condition
code	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	words	cycles	riag CT	
		2	2	-	(A) = n
	0 0 0 1 1 1 n n n <sub>2</sub> 0 7 n <sub>16</sub>	Grouping	Comparis	 on operativ	<u>n = 0 to 15</u>
Operation:	$(A) = n^{2}$	Description	1: Skips the	next inst	ruction when the con-
oporation	n = 0 to 15		tents of re	gister A is	equal to the value n in
			the immed	liate field.	
			Executes	the next in	struction when the con-
			tents of re	gister A is	not equal to the value n
			in the imm	leulate liel	u.
SEAM (Sk	ip Equal, Accumulator with Memory)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	$0 0 0 0 1 0 0 1 1 0_{2} 0 2 6_{16}$	words	cycles		
		1	1	_	(A) = (M(DP))
Operation:	(A) = (M(DP)) ?	Grouping:	Compariso	on operatio	on
		Description	1: Skips the	next inst	ruction when the con-
			M(DP).	gister A is	equal to the contents of
			Executes	the next in	struction when the con-
			tents of	register A	A is not equal to the
			contents c	of M(DP).	
CN70 (Ski	n if Non Zoro condition of outernal 0 interrupt reque	t flog)			
		Number of	Number of	Flag CV	Skin condition
code		words	cycles	riay CT	
	0 0 0 0 1 1 1 0 0 0 2 0 3 0 16	1	1	-	V10 = 0: (EXF0) = 1
Operation:	V10 = 0: (EXF0) = 1 ?	Grouping:	Interrupt o	peration	
	$(EXF0) \leftarrow 0$	Description	: When V10	= 0 : Clea	ars (0) to the EXF0 flag
	V10 = 1: SNZ0 = NOP		and skips	the next in	struction when external
	(V10 : bit 0 of the interrupt control register V1)		0 interrupt	request f	lag EXF0 is "1." When
			the EXF0	flag is "0,'	' executes the next in-
			Struction.	$1 - 1 \cdot This$	s instruction is equiva-
			lent to the	NOP instr	uction.



SNZIO (Skir	o if Non Zero condition of external 0 Interrupt input	oin)			
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code		words	cycles	0	
	0 0 0 0 1 1 1 0 1 0 2 0 0 X 16	1	1	-	I12 = 0 : (INT) = "L" I12 = 1 : (INT) = "H"
Operation:	I12 = 0 : (INT) = "L" ?	Grouping:	Interrupt of	peration	· · ·
	I12 = 1 : (INT) = "H" ?	Description	: When I12	= 0 : Skip	s the next instruction
	(I12 : bit 2 of the interrupt control register I1)		when the I	evel of IN	T pin is "L." Executes
			the next in	struction	when the level of INT
			µinis ⊓. When l12	– 1 · Skir	s the next instruction
			when the l	evel of IN	T pin is "H." Executes
			the next in	struction	when the level of INT
			pin is "L."		
SNZP (Skip	o if Non Zero condition of Power down flag)				
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition
		1	1	-	(P) = 1
Operation:	(P) = 1 ?	Grouping:	Other oper	ation	
		<b>Description</b>	: Skips the r	next instru	ction when the P flag is
			"1".		
			After skip	ping, the	P flag remains un-
			changed.	(h.a	a star set is a sub a star D
			Executes flog is "0."	the next li	nstruction when the P
			llag is 0.		
SNZT1 (Sk	ip if Non Zero condition of Timer 1 interrupt request	tlag)			
Instruction		Number of	Number of	Flag CY	Skip condition
code	1 0 1 0 0 0 0 0 0 0 0 2 2 8 0 <sub>16</sub>	1	1		1/10 - 0.7(T1E) - 1
				_	$V_{12} = 0. (11F) = 1$
Operation:	V12 = 0: (T1F) = 1 ?	Grouping:	Timer oper	ration	
	(T1F) ← 0	Description	1: When V12	e = 0 : Cle	ars (0) to the T1F flag
	V12 = 1: SNZT1 = NOP		and skips	the next ir	struction when timer 1
	(V12 = bit 2 of interrupt control register V1)		interrupt r	equest fla	g T1F is "1." When the
			I 1F flag is	s "0," exe	cutes the next instruc-
			When V/1a	— 1 · Thi	s instruction is equiva-
			lent to the	NOP instr	uction.
<b>SN7T2</b> (Sk	in if Non Zero condition of Timer 2 interrupt request	flag)			
Instruction		Number of	Number of	Flag CY	Skip condition
code		words	cycles	r lag or	Onp condition
	1 0 1 0 0 0 0 0 0 1 2 2 0 1 16	1	1	-	V13 = 0: (T2F) = 1
Operation:	V13 = 0: (T2F) = 1 ?	Grouping:	Timer oper	ration	
-	$(T2F) \leftarrow 0$	Description	: When V13	s = 0 : Cle	ars (0) to the T2F flag
	V13 = 1: SNZT2 = NOP		and skips	the next ir	struction when timer 2
	(V13 = bit 3 of interrupt control register V1)		interrupt r	equest fla	g T2F is "1." When the
			T2F flag is	s "0," exe	cutes the next instruc-
			tion.		
			When V13	s = 1 : This	s instruction is equiva-
			ient to the	NOP Instr	



SNZT3 (Sk	ip if Non Zero condition of Timer 3 interrupt request	flag)				
Instruction code	D9 D0 1 0 1 0 0 0 0 1 0 2 8 2	Number of words	Number of cycles	Flag CY	Skip condition	
		1	1	-	V20 = 0: (T3F) = 1	
Operation:	V20 = 0: (T3F) = 1 ?	Grouping:	Timer oper	ation		
	$(T3F) \leftarrow 0$	Description	: When V20	= 0 : Clea	ars (0) to the T3F flag	
	V20 = 1: SNZT3 = NOP		and skips	the next in	struction when timer 3	
	(V20 = bit 0 of interrupt control register V2)		interrupt re	equest flag	T3F is "1." When the	
			T3F flag is	s "0," exec	utes the next instruc-	
			tion.			
			When V20	= 1 : This	instruction is equiva-	
			lent to the	NOP instru	uction.	
SRST (Svs	tem ReSeT)		- *			
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code	0 0 0 0 0 0 0 0 0 1 2 0 0 1 16	words	cycles	Jung of		
		1	1	-	_	
Operation:	System reset occurrence	Grouping:	Other oper	ation		
		Description: System reset occurs.				
SUPT (Set	UPTF flag)					
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition	
code		words	cycles	- 5 -		
		1	1	-	_	
Operation:	(UPTF) ← 1	Grouping: Other operation				
		<b>Description:</b> Sets (1) to high-order bit reference enable				
			flag.			
<b>JVDE</b> (Se		Number of	Number of	Flac CV	Skip condition	
code		words	cycles	Flag C f	Skip condition	
		1	1	-	_	
Operation:	Voltage drop detection circuit valid at powerdown mode.	Grouping:	Other oper	ation		
		Description: Voltage drop detection circuit is valid at				
			powerdow	n mode (d	clock operating mode,	
			RAM back	-up mode)		
		Note: This in	nstruction car	be used o	only for H version.	



SZB j (Skip	o if Zero, Bit)				
Instruction		Number of words	Number of	Flag CY	Skip condition
code	0 0 0 0 1 0 0 j j <sub>2</sub> 0 2 j <sub>16</sub>	1	1	-	(Mj(DP)) = 0 i = 0 to 3
Operation:	(Mi(DP)) = 0 ?	Grouping:	Bit operatio	on	,
	i = 0  to  3	Description	: Skips the	next instr	uction when the con-
	,		tents of bi	t i (bit spe	cified by the value i in
			the immed	iate field)	of M(DP) is "0."
			Executes t	he next ins	struction when the con-
			tents of bit	j of M(DP)	) is "1."
SZC (Skip	if Zero, Carry flag)	1	- <b>T</b>		
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	0 0 0 0 1 0 1 1 1 1 0 2 F	words	cycles		
		1	1	-	(CY) = 0
Ornerstiers		Oneuminau	A :: the sec a time		
Operation:	(CY) = 0?	Grouping:	Arithmetic Skips the	operation	ruction when the con-
		Description	tents of ca	rry flag C)	/ is "0 "
			After skin	pina, the	CY flag remains un-
			changed.	p	
			Executes	the next in	struction when the con-
			tents of the	e CY flag i	s "1."
SZD (Skip	if Zero, port D specified by register Y)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code		words	cycles		•
		2	2	-	(D(Y)) = 0
	0 0 0 0 1 0 1 0 1 1 <sub>2</sub> 0 2 B <sub>16</sub>				(Y) = 0 to 7
Operation:	(D(Y)) = 0?	Grouping:	Input/Outp	ut operatio	ิท
•	(Y) = 0  to  7	Description	: Skips the r	next instru	ction when a bit of port
			D specified	d by registe	er Y is "0." Executes the
		Note	$(\mathbf{X}) = 0$ to $\mathbf{F}$		
		Note.	Do not exe	cute this i	nstruction if values ex-
			cept above	e are set to	register Y.
T1AB (Tra	nsfer data to timer 1 and register R1 from Accumula	tor and rec	nister B)		
Instruction		Number of	Number of	Flag CY	Skip condition
code		words	cycles	ji lag e l	emp contaition
		1	1	-	_
Operation:	$(T17-T14) \leftarrow (B)$	Grouping:	Timer ope	ration	
	$(R17-R14) \leftarrow (B)$	Description	n: Transfers	the conte	nts of register B to the
	$(T13-T10) \leftarrow (A)$		high-orde	r 4 bits of	timer 1 and timer 1 re-
	$(R13-R10) \leftarrow (A)$		load regis	ter R1. Tr	ansfers the contents of
			register A	to the low	order 4 bits of timer 1
			and timer	1 reload re	egister R1.

RENESAS

T2AB (Trai	nsfer data to timer 2 and register R2L from Accumul	ator and re	gister B)				
Instruction code	D9 D0 1 0 0 0 1 1 0 0 0 1 2 3 1	Number of words	Number of cycles	Flag CY	Skip condition		
	<u> </u>	1	1	-	_		
Operation:	$(R2L7-R2L4) \leftarrow (B)$ (T27-T24) $\leftarrow (B)$ (R2L3-R2L0) $\leftarrow (A)$ (T23-T20) $\leftarrow (A)$	Grouping:       Timer operation         Description:       Transfers the contents of register B to the high-order 4 bits of timer 2 and timer 2 reload register R2L. Transfers the contents of register A to the low-order 4 bits of timer 2 and timer 2 reload register R2L.					
<b>Τ2ΗΔΒ</b> (Tr	ansfer data to register R2H from Accumulator and r	edister B)					
Instruction code	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of words	Number of cycles	Flag CY	Skip condition		
				_	—		
Operation:	(R2H7–R2H4) ← (B) (R2H3–R2H0) ← (A)	Grouping: Description	Timer oper Transfers high-order load regist register A and timer 2	ration the conter 4 bits of t er R2H. Tr to the low- 2 reload re	nts of register B to the imer 2 and timer 2 re- ansfers the contents of order 4 bits of timer 2 gister R2H.		
T2R2L (Tra	ansfer data to timer 2 from register R2L)						
Instruction code	D9 D0 1 0 1 0 0 1 0 1 0 1 2 9 5 16	Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	_		
Operation:	(T27–T20) ← (R2L7–R2L0)	Grouping: Descriptior	Timer oper Transfers R2L to tim	ration the conte er 2.	ents of reload register		
TAB (Trans	sfer data to Accumulator from register B)						
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	-		
Operation:	(A) ← (B)	Grouping: Description	Register to Transfers to ister A.	o register tr the conten	ansfer ts of register B to reg-		



Instruction D9 Do	er 1)			
	Number of	Number of	Flag CY	Skip condition
code 1 0 0 1 1 1 0 0 0 0 2 7 0	words	cycles	_	
	16 1	1	-	_
<b>Operation:</b> (B) $\leftarrow$ (T17-T14)	Grouping	Timer oper	ration	
$(A) \leftarrow (T13-T10)$	Description:	Transfers t	the high-or	rder 4 bits (T17–T14) of
		timer 1 to i	register B.	
		Transfers	the low-or	der 4 bits (T13–T10) of
		timer 1 to 1	register A	
			egictor /	
TAD2 (Transfer data to Accumulator and register D from tim				
TAB2 (Transfer data to Accumulator and register B from tim	er Z)		-	0.1
Instruction         D9         D0           code         1         0         1         1         0         0         1         2         7         1	Number of words	Number of cycles	Flag CY	Skip condition
	<sup>16</sup> 1	1	-	-
Operation: (B) ← (T27–T24)	Grouping:	Timer oper	ration	
(A) ← (T23–T20)	Description:	Transfers t	the high-or	rder 4 bits (T27-T24) of
		timer 2 to I	register B.	
		Transfers	the low-or	der 4 bits (T23-T20) of
		timer 2 to i	register A.	
TABE (Transfer data to Accumulator and register B from rec	ister E)			
	Number of	Number of	Flag CY	Skip condition
	words	cycles		entp containen
	16 1	1	_	_
Operation: (B) $\leftarrow$ (E7–E4)	Grouping:	Register to	register tr	ansfer
Operation: $(B) \leftarrow (E7-E4)$ $(A) \leftarrow (E3-E0)$	Grouping: Description:	Register to Transfers	register tr the high-o	ransfer order 4 bits (E7-E4) of
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t	register tr the high-o o register	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A.
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A.
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A.
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer Inder 4 bits (E7–E4) of B, and low-order 4 bits er A.
Operation: (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A.
<b>Operation:</b> (B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0) <b>TABP p</b> (Transfer data to Accumulator and register B from F	Grouping: Description:	Register to Transfers register E t of register	register tr the high-o o register E to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A.
Operation:       (B) $\leftarrow$ (E7–E4)         (A) $\leftarrow$ (E3–E0)         TABP p (Transfer data to Accumulator and register B from F         Instruction       D9	Grouping: Description: Program memo	Register to Transfers register E t of register	register tr the high-o o register E to regist to regist	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition
Operation:       (B) $\leftarrow$ (E7–E4)         (A) $\leftarrow$ (E3–E0)         TABP p (Transfer data to Accumulator and register B from F         Instruction       D9         Code       0       0       1       0       ps       ps       0       8       ps	Program memo	Register to Transfers register E t of register	register tr the high-o o register E to regist E to regist P) Flag CY	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition
Operation:(B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)TABP p (Transfer data to Accumulator and register B from F Instruction codeD0 D0 D0 D0 CodeO010p5p4p3p2p1p0 p00 $\frac{8}{+p}$ p	Program memo Number of words	Register to Transfers register E t of register	register tr the high-o o register E to regist E to regist Flag CY	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition –
Operation:       (B) $\leftarrow$ (E7–E4)         (A) $\leftarrow$ (E3–E0)         TABP p (Transfer data to Accumulator and register B from F         Instruction       D9         code       0       1       0       p5       p4       p3       p2       p1       p0       2       0 $\frac{8}{+p}$ p         Operation:       Grauning: Arith	Program memo Number of words 16	Register to Transfers register E t of register	register tr the high-o o register E to regist E to regist Flag CY	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition
Operation:(B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)TABP p (Transfer data to Accumulator and register B from F InstructionD9D0 Code0010p5p4p3p2p1p0 $_2$ 0 $\frac{8}{+p}$ pOperation: (SP) $\leftarrow$ (SP) + 1Grouping: Arith Description:	Grouping:         Description:         Program memory         Number of words         16         1         metic operation	Register to Transfers register E t of register	register tr the high-o o register E to regist E to regist Flag CY	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition
Operation:(B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)TABP p (Transfer data to Accumulator and register B from F Instruction D9D0 codeD0010p5p4p3Operation: (SP() $\leftarrow$ p (Note)Grouping: Arith Description: UPTF = 0: Transfers	Program memo Number of words 16 1 metic operation	Register to Transfers a register E t of register of register vry in page Number of cycles 3 ster B and b	register tr the high-o o register E to regist E to regist P) Flag CY 	ransfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition – o register A. These bits
$\begin{array}{c} \textbf{Operation:} & (B) \leftarrow (E7-E4) \\ & (A) \leftarrow (E3-E0) \end{array} \\ \hline \textbf{TABP p (Transfer data to Accumulator and register B from Finstruction D9 D0 \\ \hline \textbf{code} & 0 & 1 & 0 & p5 & p4 & p3 & p2 & p1 & p0 \\ \hline \textbf{Operation:} \\ & (SP) \leftarrow (SP) + 1 \\ & (SK(SP)) \leftarrow (PC) \\ & (PCL) \leftarrow (DR2-DR0, A3-A0) \end{array} \\ \hline \textbf{Grouping: Arith Description:} \\ & UPTF = 0: Transfers 9 to 0 are the ROM 9 to 0 are 0 to 0 $	Program memo Number of words Number of words 16 1 metic operation	Register to Transfers register E t of register of register number of cycles 3 ster B and b ss (DR2 DR	register tr the high-o o register E to regist E to regist Plag CY - its 3 to 0 t 1 DR0 A3 d	ansfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition – o register A. These bits A2 A1 A0)2 specified by
Operation:(B) $\leftarrow$ (E7–E4) (A) $\leftarrow$ (E3–E0)TABP p (Transfer data to Accumulator and register B from F Instruction D9 codeD0 D0 D0Operation: (SP) $\leftarrow$ (SP) + 1 (SK(SP)) $\leftarrow$ (PC) (PCL) $\leftarrow$ p (Note) (PCL) $\leftarrow$ (DR2–DR0, A3–A0) at (UPTF) = 1 (B) $\leftarrow$ (BOM(PC))7–4 (UPTF) = 1 (C)Grouping: Arith Description: UPTF = 1: Transfers 9 to 0 are the ROM UPTF = 1: Transfers	Grouping:         Description:         Description:         Program memory         Number of words         16         1         metic operation         bits 7 to 4 to regipattern in ad-drep page p. bits 9, 8 to registry	Register to Transfers register E t of register of register number of cycles 3 ster B and b ss (DR2 DR er D, bits 7 to	register tr the high-o o register E to regist E to regist P) Flag CY - its 3 to 0 t 1 DR0 A3 / o 4 to regist	ansfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition – o register A. These bits A2 A1 A0)2 specified by ster B and bits 3 to 0 to
$\begin{array}{llllllllllllllllllllllllllllllllllll$	Grouping:         Description:         Description:         Program memory         Number of words         16         1         metic operation         bits 7 to 4 to regipatern in ad-drepage p.         bits 9, 8 to regists         s 7 to 0 are the F	Register to Transfers register E t of register Pry in page Number of cycles 3 ister B and b ss (DR2 DR er D, bits 7 to ROM pattern	register tr the high-o o register E to regist E to regist Flag CY - its 3 to 0 t 1 DR0 A3 / o 4 to regis in address	ansfer order 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition – o register A. These bits A2 A1 A0)2 specified by ster B and bits 3 to 0 to s (DR2 DR1 DR0 A3 A2
$\begin{array}{llllllllllllllllllllllllllllllllllll$	Grouping:         Description:         Description:         Program memory         Number of words         16         1         metic operation         bits 7 to 4 to registers n and dreg p.         bits 9, 8 to registers A and D registers A and D registers A and D	Register to Transfers f register E t of register Number of cycles 3 ster B and b ss (DR2 DR er D, bits 7 to OM pattern in page p. and b is 0 f	register tr the high-o o register E to regist Flag CY - its 3 to 0 t 1 DR0 A3 / o 4 to regis in address	ansfer and low-order 4 bits and low-order 4 bits er A. Skip condition - o register A. These bits A2 A1 A0)2 specified by ster B and bits 3 to 0 to s (DR2 DR1 DR0 A3 A2 34556M8/M8H/C2/C21
$\begin{array}{llllllllllllllllllllllllllllllllllll$	Grouping:         Description:         Description:         Program memory         Number of words         16         1         metic operation         bits 7 to 4 to reging pattern in ad-dree page p.         bits 9, 8 to registers A and D registers A and D registers A and D r M34556M4/M4H	Register to Transfers register E t of register wry in page Number of cycles 3 ster B and b ss (DR2 DR er D, bits 7 to ROM pattern in page p. , and p is 0 tr ed, be carefu	register tr the high-o o register E to regist Flag CY - its 3 to 0 t 1 DR0 A3 / o 4 to regis in address	ansfer rder 4 bits (E7–E4) of B, and low-order 4 bits er A. Skip condition - o register A. These bits A2 A1 A0)2 specified by ster B and bits 3 to 0 to s (DR2 DR1 DR0 A3 A2 34556M8/M8H/G8/G8H. ver the stack because 1

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TABPS (Tr	ansfer data to Accumulator and register B from Pres	Scaler)			
Instruction code	D9 D0 1 1 1 0 1 0 1 2 7 5	Number of words	Number of cycles	Flag CY	Skip condition
		1	1	-	_
Operation:	$(B) \leftarrow (TPS7\text{-}TPS4)$	Grouping:	Timer oper	ation	
	(A) ← (TPS3–TPS0)	Description	: Transfers TPS4) of transfers th of prescale	the high- prescale he low-ord er to registe	order 4 bits (TPS7– r to register B, and er 4 bits (TPS3–TPS0) er A.
TAD (Trans	sfer data to Accumulator from register D)		- <b>N</b>		
Instruction code	D9 D0 D0 1 0 1 0 0 1 0 5 1	Number of words	Number of cycles	Flag CY	Skip condition
		1	1	-	-
Operation:	$(A_2 - A_0) \leftarrow (DR_2 - DR_0)$	Grouping:	Register to	register tr	ansfer
	(A3) ← 0	Description	: Transfers	the conter	nts of register D to the
		Note:	When this	instructio	on is executed, "0" is
			stored to the	ne bit 3 (As	B) of register A.
TAI1 (Trans	sfer data to Accumulator from register 11)				
Instruction code	D9 D0 1 0 0 1 0 1 0 0 1 1 2 5 3 16	Number of words	Number of cycles	Flag CY	Skip condition
		1	1	-	-
Operation:	$(A) \leftarrow (I1)$	Grouping:	Interrupt of	peration	
		Description	register I1	to register	A.
TAK0 (Trar	nsfer data to Accumulator from register K0)				
Instruction code	D9 D0 1 0 1 0 1 0 2 5 6	Number of words	Number of cycles	Flag CY	Skip condition
		1	1	-	_
Operation:	(A) ← (K0)	Grouping:	Input/Outp	ut operatio	n
		Description	: Transfers control reg	the conter ister K0 to	nts of key-on wakeup register A.



TAK1 (Tra	nsfer data to Accumulator from register K1)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code		words	cycles		
		1	1	-	-
Operation:	$(A) \leftarrow (K1)$	Grouping:	Input/Outp	ut operatio	on
•		Description	: Transfers	the conte	nts of key-on wakeup
			control reg	jister K1 to	register A.
TAK2 (Tran	efer data to Accumulator from register K2)				
Instruction		Number of	Number of	Flag CV	Skip condition
code		words	cycles	Tiay CT	Skip condition
coue	1 0 0 1 0 1 1 0 1 0 2 2 5 A <sub>16</sub>	1	1	-	-
Operation:	$(A) \leftarrow (K2)$	Grouping	Input/Outpu	It operatio	n
oporation		Description:	Transfers t	the conter	its of key-on wakeup
			control regi	ster K2 to	register A.
TAL1 (Trar	nsfer data to Accumulator from register L1)	1			
Instruction		Number of words	Number of cvcles	Flag CY	Skip condition
code		1	1	_	
Operation:	$(A) \leftarrow (L1)$	Grouping:	LCD contr	ol operatio	n
		Description	1: Transfers	the conten	ts of LCD control regis-
			ter L1 to re	egister A.	
TAM j (Trar	nsfer data to Accumulator from Memory)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	1 0 1 1 0 0 j j j j <sub>2</sub> 2 C j <sub>16</sub>	words	cycles		
		1	1	-	-
Operation.	$(A) \leftarrow (M(DP))$	Groupina:	RAM to rea	ister trans	fer
	$(X) \leftarrow (X) EXOR(j)$	Description:	After transf	erring the	contents of M(DP) to
	j = 0 to 15		register A,	an exclu	sive OR operation is
			performed l	petween re	gister X and the value
			j in the imn	nediate fie	ld, and stores the re-
			suit in regis	ster X.	



TAMR (Tra	nsfer data to Accumulator from register MR)				
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition
	<u>1 0 0 1 0 1 0 0 1 0 2 2 5 2 16</u>	1	1	-	_
Operation:	$(A) \leftarrow (MR)$	Grouping:	Clock oper	ation	
•		Description	: Transfers t	the conten	ts of clock control reg-
			ister MR to	o register A	
TAPU0 (Tr	ansfer data to Accumulator from register PLIO				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	1 0 0 1 0 1 0 1 1 1 2 2 5 7 16	words	cycles		
		1	1	-	_
Operation:	$(A) \leftarrow (PU0)$	Grouping:	Input/Outp	ut operatio	n
		Description	: Transfers	the conte	nts of pull-up control
			regiotor r c		
		2			
TAPU1 (Tr	ansfer data to Accumulator from register PU1)	i			
Instruction		Number of words	Number of cvcles	Flag CY	Skip condition
code	1 0 0 1 0 1 1 1 1 0 2 2 5 E 16	1	1	-	_
Operation:	(A) ← (PU1)	Grouping:	Input/Outp	ut operatio	n
-		Description	: Transfers	the conte	nts of pull-up control
			register PC	J1 to regist	ter A.
TASP (Tran	nsfer data to Accumulator from Stack Pointer)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	0 0 0 1 0 1 0 0 0 0 0 0 0 0 1	words 1	cycles 1	_	
			I		
Operation:	$(A_2-A_0) \leftarrow (SP_2-SP_0)$	Grouping:	Register to	register tr	ansfer
	$(A3) \leftarrow 0$	Description	to the low-	order 3 bits	s (A2–A0) of register A.
		Note:	After this	instructio	n is executed, "0" is
			stored to th	ne bit 3 (Aa	e) of register A.



TAV1 (Tran	nsfer data to Accumulator from register V1)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	0 0 0 1 0 1 0 1 0 0 0 5 4	words	cycles		
		1	1	-	-
Operation:	$(A) \leftarrow (V1)$	Groupina:	Interrupt o	peration	
		Description	: Transfers	the conter	nts of interrupt control
			register V1	I to registe	r A.
			-	-	
TAV2 (Trai	nsfer data to Accumulator from register V2)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code		words	cycles	Ū	·
		1	1	-	_
Operation:	$(A) \leftarrow (V2)$	Grouping:	Interrupt o	peration	
		Description	1: Transfers	the conter	nts of interrupt control
			register va	2 to registe	rA.
<b>TANA/4</b> /Tro	refer date to A coursulator from register (M/4)				
	nsier data to Accumulator from register w ()	Number	Number		
Instruction		words	cvcles	Flag CY	Skip condition
code		1	1	_	_
			•		
Operation:	$(A) \leftarrow (W1)$	Grouping:	Timer ope	ration	
		Description	1: Transfers	the conten	ts of timer control reg-
			ister W1 to	o register A	
TAW2 (Tra	nsfer data to Accumulator from register W2)	1		1 1	
Instruction		Number of	Number of	Flag CY	Skip condition
code	1 0 0 1 0 0 1 1 0 0 <sub>2</sub> 2 4 C <sub>16</sub>	words	cycles		
		1	1	-	-
Operation:	$(A) \leftarrow (W2)$	Grouping:	Timer ope	ration	
••••••		Description	1: Transfers	the conter	ts of timer control reg-
			ister W2 to	o register A	
				-	



TAW3 (Tra	nsfer data to Accumulator from register W3)							
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code		words	cycles		-			
		1	1	-	_			
Operation:	$(A) \leftarrow (W3)$	Grouping:	Timer oper	ration				
		<b>Description:</b> Transfers the contents of timer control rea-						
			ister W3 to	o register A				
TAW4 (Tra	nsfer data to Accumulator from register W4)							
Instruction code	D9 D0 1 0 0 1 1 0 2 4 F	Number of words	Number of cycles	Flag CY	Skip condition			
		1	1	-	-			
Operation:	$(A) \leftarrow (W4)$	Grouping:	Timer ope	ration				
		<b>Description:</b> Transfers the contents of timer control reg-						
			ister W4 to	o register A				
TAX (Trans	sfer data to Accumulator from register X)	1						
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code		words	cycles	_				
		1	1	-	-			
Operation:	$(A) \leftarrow (X)$	Grouping:	Register to	o register tr	ansfer			
		Description	: Transfers	the conten	ts of register X to reg-			
			ister A.					
TAY (Trans	fer data to Accumulator from register Y)							
Instruction code	D9 D0 D0 1 1 1 1 1 0 1 E	Number of words	Number of cycles	Flag CY	Skip condition			
	<b>6 6 6 6 1 1 1 1 1 1 2 6 1 1 1 1 1 1 1 1 1 1</b>	1	1	-	_			
Operation:	$(A) \leftarrow (Y)$	Grouping:	Register to	o register tr	ansfer			
		<b>Description:</b> Transfers the contents of register Y to register A.						



TAZ (Trans	fer data to Accumulator from register Z)									
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition					
code	0 0 0 1 0 1 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 1 1 0	words 1	cycles 1	_	_					
Operation:	$(A1, A0) \leftarrow (Z1, Z0)$	Grouping:	Register to	register tr	ansfer					
oporation	$(A3, A2) \leftarrow 0$	<b>Description:</b> Transfers the contents of register Z to the								
		low-order 2 bits (A1, A0) of register A.								
		<b>Note:</b> After this instruction is executed, "0" is								
			stored to t	the high-o	rder 2 bits (A3, A2) of					
			register A.							
TBA (Trans	sfer data to register B from Accumulator)		- *							
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition					
code	0 0 0 0 0 0 1 1 1 0 0 0 E 16	words	cycles	_						
		1	1	-	-					
Operation:	$(B) \leftarrow (A)$	Grouping	Register to	register tr	ansfer					
oporation		Description	: Transfers t	the content	s of register A to regis-					
			ter B.							
TC1A (Trai	nsfer data to register C1 from Accumulator)									
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition					
code	1 0 1 0 1 0 1 0 0 0 2 2 A 8 16	words	cycles							
		1	1	-	-					
Operation:	(C1) ← (A)	Grouping:	LCD contr	ol operatio	n					
		Description	1: Transfers	the conter	nts of register A to the					
			LCD contr	ol register	C1.					
TC2A (Trai	nsfer data to register C2 from Accumulator)									
Instruction		Number of	Number of	Flag CY	Skip condition					
code	1 0 1 0 1 0 1 0 1 <u>0</u> 1 <u>0</u> 1 <u>1</u> <u>0</u> <u>1</u> <u>2</u> <u>1</u> <u>9</u> <u>16</u>	words	cycles 1							
					-					
Operation:	$(C2) \leftarrow (A)$	Grouping:	LCD contr	ol operatio	n					
		Description	1: Transfers	the conter	nts of register A to the					
			LCD contr	orregister	02.					



TDA (Trans	sfer data to register D from Accumulator and registe	r B)						
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code	$\begin{vmatrix} 0 & 0 & 0 & 0 \end{vmatrix} 1 \begin{vmatrix} 0 & 1 & 0 & 0 \end{vmatrix} 1 \begin{vmatrix} 0 & 0 & 1 \end{vmatrix}_{2} \begin{vmatrix} 0 & 2 & 9 \end{vmatrix}_{16}$	words	cycles					
		1	1	-	-			
Operation:	$(DR2-DR0) \leftarrow (A2-A0)$	Grouping:	Register to	o register t	ransfer			
		Description	n: Transfers	the low-o	rder 3 bits (A2-A0) of			
			register A	to register	D.			
TEAB (Tra	nsfer data to register E from Accumulator and register	ter B)						
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code	0 0 0 0 0 1 1 0 1 0 0 1 A 16	words	cycles					
		1	1	-	-			
Operation:	(E7–E4) ← (B)	Grouping:	Register to	o register t	ransfer			
	$(E_3-E_0) \leftarrow (A)$	<b>Description:</b> Transfers the contents of register B to the						
		high-order 4 bits (E7–E4) of register E, and the contents of register A to the low-order 4						
		bits (E3–E0) of register E.						
				,				
TFR0A (Tr	ansfer data to register FR0 from Accumulator)							
Instruction		Number of	Number of	Flag CY	Skip condition			
code	1 0 0 0 1 0 1 0 0 0 2 2 2 8 <sub>16</sub>	words	cycles					
		1	1	-	_			
Operation:	$(FR0) \leftarrow (A)$	Grouping:	Input/Outp	out operation	วท			
		<b>Description:</b> Transfers the contents of register A to the						
			port outpu	t structure	control register FR0.			
TFR1A (Tr	ansfer data to register FR1 from Accumulator)							
Instruction		Number of	Number of	Flag CY	Skip condition			
code	<u>1 0 0 0 1 0 1 0 1 2 2 2 9 16</u>	1	1	_				
Operation:	$(FR1) \leftarrow (A)$	Grouping:	Input/Outp	out operatio	on			
		Description	<ol> <li>Transfers</li> </ol>	the conte	nts of register A to the			
			ροπ οπρυ	i siruciure	CONTROL TEGISTER FR1.			



TFR2A (Tra	ansf	er c	lata	a to	o re	egi	ste	er l	FR	21	frc	m	A	CC	un	nul	at	or)								
Instruction	Ds	)												D0							Number of		Number of	Flag	CY	Skip condition
code	1	0	0		0	1	0		1	0	)	1		0	_	2		2	А		words		cycles			
															2					10	1		1	_		-
Operation:	(FF	82) ←	– (A	)																	Grouping:		Input/Output	ut ope	ratic	ิท
																					Description	n:	Transfers t port output	he co struct	nter ure	nts of register A to the control register FR2.
TI1A (Tran	sfer	da	ta t	o r	eg	iste	er I	11	fro	m	A	СС	ur	nu	lat	or)										
Instruction	Ds	)											-	D0	1					_	Number of		Number of	Flag	CY	Skip condition
code	1	0	0		0	0	1		0	1	1	1		1	2	2		1	7	, 16	1		1			_
Operation:	(11	) (	(A)																		Grouping			nerati	n	
operation	(11	,`	(/ ()																		Descriptio	n:	Transfers	the co	nter	nts of register A to inter-
																							rupt contro	l regis	ster	I1.
														<	6											
TK0A (Tra	nsfe	r da	ata	to	re	gis	ter	K	0 f	roi	m	Ac	с	um	ul	ato	or)							-		
Instruction	Ds	)											_	D0	1	_				_	Number of	:	Number of	Flag	CY	Skip condition
code	1	0	0		0	0	1		1	C	)	1		1	2	2		1	В	16	1		1			-
Operation:	(K(	)) ←	(A)			_	1														Grouping:	_	Input/Outp	ut ope	ratio	on
•••••	(	-) (	(, ,)																		Description: Transfers the contents of register A to kev-					
																							on wakeup	contr	ol re	יgister K0.
TK1A (Tra	nsfe	r da	ata	to	reę	gis	ter	Κ	1 fi	ror	m	Ac	С	um	ul	atc	or)					_				
Instruction	Ds	)								_			_	D0	1		_			_	Number of		Number of	Flag	CY	Skip condition
code	1	0	0		0	0	1		0	1		0		0	2	2		1	4	16	1		1	_		
Operation:	(K	1) ←	(A)																		Grouping:		Input/Outp	ut ope	ratio	 วท
	,		( )																		Descriptio	n:	Transfers to on wakeup	he co	nter ol re	its of register A to key- gister K1.



TK2A (Trar	nsfer data to register K2 from Accumulator)							
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code	1     0     0     0     1     0     1     0     1     2     2     1     5     16	1	1	-	_			
Operation:	(K2) ← (A)	Grouping:	Input/Outp	ut operatio	n			
		<b>Description:</b> Transfers the contents of register A to k on wakeup control register K2.						
IL1A (Iran	Ister data to register L1 from Accumulator)	Number of	Number of	Flog CV	Chip condition			
code	$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ \end{bmatrix}_{2} \begin{bmatrix} 2 & 0 & A \end{bmatrix}_{16}$	words	cycles	Flag C f	Skip condition			
		1	1	-	-			
Operation:	$(L1) \leftarrow (A)$	Grouping:	LCD contro	ol operation	า			
		Description	: Transfers t control reg	he conten ister L1.	ts of register A to LCD			
TL2A (Tran	sfer data to register L2 from Accumulator)							
Instruction		Number of	Number of	Flag CY	Skip condition			
code	1 0 0 0 0 0 1 0 1 1 <sub>2</sub> 2 0 B <sub>16</sub>	1	1	-	_			
Operation:	$(L2) \leftarrow (A)$	Grouping:	LCD contro	l operatio	 າ			
		Description	: Transfers t control reg	he conten ister L2.	ts of register A to LCD			
TL3A (Trar	sfer data to register L3 from Accumulator)							
Instruction code	D9 D0 1 1 0 0 C	Number of words	Number of cycles	Flag CY	Skip condition			
		1	1	-	-			
Operation:	$(L3) \leftarrow (A)$	Grouping:	LCD contro	ol operation	า			
		Description	: Transfers t control reg	he conten ister L3.	ts of register A to LCD			



TLCA (Tra	nsfer data to register LC from Accumulator)							
Instruction code	D9 D0 1 1 0 1 2 0 D	Number of words	Number of cycles	Flag CY	Skip condition			
	1 0 0 0 0 0 1 1 0 1 2 2 0 D 16	1	1	-	-			
Operation:	$(LC) \leftarrow (A)$ $(RLC) \leftarrow (A)$	Grouping: Description	Timer oper Transfers t LC and rel	ration the conten oad registe	ts of register A to timer er RLC.			
IMA J (Ira	nster data to Memory from Accumulator)							
Instruction code	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of words	Number of cycles	Flag CY	Skip condition			
		1	1	-	_			
Operation:	$(M(DP)) \gets (A)$	Grouping: RAM to register transfer						
	$(X) \leftarrow (X) EXOR(j)$	<b>Description:</b> After transferring the contents of register A						
	j = 0 to 15		to M(DP),	an exclusiv	ve OR operation is per-			
			formed be	tween reg	ister X and the value j			
			in the initiation		a, and stores the result			
			III legister	Λ.				
TMRA (Tra	nsfer data to register MR from Accumulator)							
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition			
code	1 0 0 0 0 1 0 1 1 0 2 2 1 6 <sub>16</sub>	words 1	cycles 1	-	- -			
Operation:	$(MR) \leftarrow (A)$	Grouping	Other oper	ration				
operation		<b>Description:</b> Transfers the contents of register A to clock						
			control reg	ister MR.				
TPAA (Trai	nsfer data to register PA from Accumulator)							
Instruction code	D9 D0 1 0 1 0 1 0 1 0 1 0 2 A A	Number of words	Number of cycles	Flag CY	Skip condition			
	2 16	1	1	-	-			
Operation:	$(PA_0) \leftarrow (A_0)$	Grouping: Timer operation						
		<b>Description:</b> Transfers the contents of lowermost bit (A0) register A to timer control register PA.						



TPSAB (Tra	ansfer data to Pre-Scaler from Accumulator and reg	ister B)						
Instruction		Number of words	Number of cycles	Flag CY	Skip condition			
code		1	1	-	_			
Operation:	$(RPS7-RPS4) \leftarrow (B)$	Grouping:	Timer oper	ation				
	$(TPS7-TPS4) \leftarrow (B)$ $(RPS3-RPS0) \leftarrow (A)$ $(TPS3-TPS0) \leftarrow (A)$	Description: Transfers the contents of register B to the high-order 4 bits of prescaler and prescaler reload register RPS, and transfers the con- tents of register A to the low-order 4 bits of prescaler and prescaler reload register RPS.						
TPU0A (Tra	ansfer data to register PU0 from Accumulator)	<u> </u>						
Instruction		Number of words	Number of cycles	Flag CY	Skip condition			
code		1	1	-	-			
Operation:	$(PU0) \leftarrow (A)$	Grouping: Input/Output operation						
		Description: Transfers the contents of register A to pull-						
		up control register PU0.						
TPU1A (Tra	ansfer data to register PU1 from Accumulator)							
Instruction		Number of words	Number of cycles	Flag CY	Skip condition			
code		1	1	-	-			
Operation:	(PU1) ← (A)	Grouping: Input/Output operation						
		<b>Description:</b> Transfers the contents of register A to pull-						
			up control	register Pt	J1.			
TR1AB (Tra	ansfer data to register R1 from Accumulator and rec	gister B)						
Instruction code	D9 D0 1 0 0 0 1 1 1 1 1 2 3 F	Number of words	Number of cycles	Flag CY	Skip condition			
		1	1	-	-			
Operation:	(R17–R14) ← (B)	Grouping: Timer operation						
	(R13–R10) ← (A)	<b>Description:</b> Transfers the contents of register B to the high-order 4 bits (R17–R14) of reload register R1, and the contents of register A to the low-order 4 bits (R13–R10) of reload register R1.						



TRGA (Tra	nsfe	r da	ita to	o re	gist	er F	۲G f	ron	n A	ссι	Jmu	ulate	or)							
Instruction	D9									D	0					Number of	Number of	Flag CY	Skip condition	
code	1	0	0	0	0	0	1	0	0	1	٦.	2	0	9		words	cycles			
											2				16	1	1	-	-	
Operation:	$(RG) \leftarrow (A)$												Grouping: Clock control operation							
													Description: Transfers the contents of register A to regis-							
																	ter RG.			
TV1A (Trar	nsfei	dat	ta to	reç	giste	er V	1 frc	sm	Ac	cur	mul	ato	r)							
Instruction code	D9	0	0	0	1	1	1	1	1	D 1	0	0	3	F		Number of words	Number of cycles	Flag CY	Skip condition	
											2		1	1	-	_				
Operation:	$(V1) \leftarrow (A)$													Grouping: Interrupt operation						
-															Description: Transfers the contents of register A to inter-					
															rupt control register V1.					
TV2A (Trar	nsfer	dat	a to	reg	jiste	er V	2 frc	m	Aco	cur	nul	ator	-)							
Instruction	D9									D	0					Number of	Number of	Flag CY	Skip condition	
code	0	0	0	0	1	1	1	1	1	0	2	0	3	E	16	words	cycles			
						_										1	1	-	_	
Operation:	(V2	) ←	(A)													Grouping: Interrupt operation				
															<b>Description:</b> Transfers the contents of register A to inter-					
														Tupi control register v2.						
IWIA (Ira	nste	r da	ta to	) re	gist	er v	V1 fi	ron	n A		ιmι	late	or)			Next	Neurole		01 10 101	
Instruction	D9			_						D	0			1-		Number of words	Number of cycles	Flag CY	Skip condition	
code	<u>1 0 0 0 0 0 1 1 1 0 2 2 0 E <sub>16</sub></u>								2	1	1	-	_							
Operation:	$(W(1) \leftarrow (A)$													Grouping: Timer operation						
•••••	$(W1) \leftarrow (A)$													<b>Description:</b> Transfers the contents of register A to timer						
														control register W1.						



TW2A (Trai	nsfer data to register W2 from Accumulator)						
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition		
	1 0 0 0 0 0 1 1 1 2 2 0 1 16	1	1	-	_		
Operation:	$(W2) \leftarrow (A)$	Grouping: Timer operation					
		Description	: Transfers t control reg	he content ister W2.	s of register A to timer		
	notor data ta raziatar 10/2 from Accumulator)	<u> </u>					
	hster data to register VV3 from Accumulator)	Number of	Number of	Flag CV	Skip condition		
code	$\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}_2 \begin{bmatrix} 2 & 1 & 0 \end{bmatrix}_{16}$	words	cycles	riay C f			
		1	1	-	-		
Operation:	$(W3) \leftarrow (A)$	Grouping: Timer operation					
		<b>Description:</b> Transfers the contents of register A to timer					
		control register W3.					
TW4A (Tra	nsfer data to register W4 from Accumulator)	1					
Instruction		Number of	Number of	Flag CY	Skip condition		
code	1 0 0 0 0 1 0 0 0 1 <sub>2</sub> 2 1 1 <sub>16</sub>	words 1	cycles 1	_			
Operation:	$(W4) \leftarrow (A)$	Grouping	Timer one	ration			
oporation		<b>Description:</b> Transfers the contents of register A to timer					
			control reg	jister W4.			
TYA (Trans	fer data to register Y from Accumulator)						
Instruction code		Number of words	Number of cycles	Flag CY	Skip condition		
		1	1	-	-		
Operation:	(Y) ← (A)	Grouping: Description	Register to Transfers t ter Y.	b register tr	ansfer ts of register A to regis-		


WRST (Wa	tchdog timer ReSeT)				
Instruction	D9 D0	Number of	Number of	Flag CY	Skip condition
code	1     0     1     0     0     0     0     0     0       2     A     0     16	words 1	cycles 1	_	(WDF1) = 1
Operation:	(WDF1) = 1 ?	Grouping:	Other oper	ation	
	$(WDF1) \leftarrow 0$	Description	: Clears (0)	to the WI	OF1 flag and skips the
			next instru	iction whe	n watchdog timer flag
			WDF1 is "	I." When the	ne WDF1 flag is "0," ex-
			ecutes the	next insti	uction. Also, stops the
				amer funct	mediately after the
			DWDT inst	truction	inneulately alter the
XAM J (exc	hange Accumulator and Memory data)	Number	Number of		Olvin andition
Instruction		words	cvcles	Flag CY	Skip condition
code	1 0 1 1 0 1 j j j <sub>2</sub> 2 D j <sub>16</sub>	1	1	_	
Operation:	$(A) \leftarrow \rightarrow (M(DP))$	Grouping:	RAM to reg	gister trans	sfer
	$(X) \leftarrow (X) EXOR(j)$	Description	: After exch	nanging th	e contents of M(DP)
	j = 0 to 15		with the co	ntents of r	egister A, an exclusive
	C		OR operat	ion is perf	ormed between regis-
			ter X and t	he value j	in the immediate field,
			and stores	the result	in register X.
XAMD J (e)	Change Accumulator and Memory data and Decren	nent regist	er Y and sk	ip)	
Instruction		Number of words	Number of cycles	Flag CY	Skip condition
code	1 0 1 1 1 1 j j j j <sub>2</sub> 2 F j <sub>16</sub>	1	1		(V) – 15
		•			(1) = 10
Operation:	$(A) \leftarrow \rightarrow (M(DP))$	Grouping:	RAM to reg	gister trans	fer
-	$(X) \leftarrow (X) EXOR(j)$	Description	with the co	ntents of r	egister A, an exclusive
	j = 0 to 15		OR operat	ion is perf	ormed between regis-
	$(Y) \leftarrow (Y) - 1$		ter X and t and stores	he value j	in the immediate field,
			Subtracts 7	1 from the	contents of register Y.
			As a resul	t of subtra	action, when the con-
			is skipped.	When the	contents of register Y
			is not 15, tl	<u>he next ins</u>	truction is executed.
XAMI J (eX	change Accumulator and Memory data and Increme	ent register	Y and skip		
Instruction		Number of words	Number of	Flag CY	Skip condition
code	1 0 1 1 1 0 j j j j 2 2 E j <sub>16</sub>	1	1	_	(X) = 0
		· ·	I		(1) = 0
Operation:	$(A) \leftarrow \rightarrow (M(DP))$	Grouping:	RAM to reg	gister trans	sfer
	$(X) \leftarrow (X) EXOR(j)$	Description	with the co	intents of i	egister A, an exclusive
	j = 0 to 15		OR operat	ion is perf	ormed between regis-
	$(Y) \leftarrow (Y) + 1$		ter X and t	he value j	in the immediate field,
			Adds 1 to t	the conten	s of register Y. As a re-
			sult of ac	dition, w	hen the contents of
			skinned w	'is 0, th when the co	e next instruction is
			not 0, the r	next instru	ction is executed.



Parameter	r	Instruction code													er of s	er of is	Function
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	Do	Hexa	ade otati	cimal on	Numbe word	Numbe cycle	Function
	ТАВ	0	0	0	0	0	1	1	1	1	0	0	1	Е	1	1	$(A) \leftarrow (B)$
	тва	0	0	0	0	0	0	1	1	1	0	0	0	Е	1	1	$(B) \leftarrow (A)$
	TAY	0	0	0	0	0	1	1	1	1	1	0	1	F	1	1	$(A) \leftarrow (Y)$
	ТҮА	0	0	0	0	0	0	1	1	0	0	0	0	С	1	1	$(Y) \leftarrow (A)$
transfei	ТЕАВ	0	0	0	0	0	1	1	0	1	0	0	1	A	1	1	$\begin{array}{l} (E7-E4) \leftarrow (B) \\ (E3-E0) \leftarrow (A) \end{array}$
egister	TABE	0	0	0	0	1	0	1	0	1	0	0	2	A	1	1	
er to i	TDA	0	0	0	0	1	0	1	0	0	1	0	2	9	1	1	$(DR2-DR0) \leftarrow (A2-A0)$
Registe	TAD	0	0	0	1	0	1	0	0	0	1	0	5	1	1	1	$\begin{array}{l} (A2-A0) \leftarrow (DR2-DR0) \\ (A3) \leftarrow 0 \end{array}$
	TAZ	0	0	0	1	0	1	0	0	1	1	0	5	3	1	1	$(A_1, A_0) \leftarrow (Z_1, Z_0) (A_3, A_2) \leftarrow 0$
	ТАХ	0	0	0	1	0	1	0	0	1	0	0	5	2	1	1	$(A) \leftarrow (X)$
	TASP	0	0	0	1	0	1	0	0	0	0	0	5	0	1	1	$\begin{array}{l} (A_2-A_0) \leftarrow (SP_2-SP_0) \\ (A_3) \leftarrow 0 \end{array}$
	LXY x, y	1	1	<b>X</b> 3	<b>X</b> 2	<b>X</b> 1	<b>X</b> 0	уз	y2	y1	y0	3	x	у	1	1	$ \begin{array}{l} (X) \leftarrow x \ x = 0 \ \text{to} \ 15 \\ (Y) \leftarrow y \ y = 0 \ \text{to} \ 15 \end{array} $
resses	LZ z	0	0	0	1	0	0	1	0	Z1	Z0	0	4	8 +z	1	1	$(Z) \leftarrow z \ z = 0 \text{ to } 3$
AM add	INY	0	0	0	0	0	1	0	0	1	1	0	1	3	1	1	$(Y) \leftarrow (Y) + 1$
	DEY	0	0	0	0	0	1	0	1	1	1	0	1	7	1	1	$(Y) \leftarrow (Y) - 1$
	TAM j	1	0	1	1	0	0	j	j	j	j	2	С	j	1	1	$\begin{array}{l} (A) \leftarrow (M(DP)) \\ (X) \leftarrow (X)EXOR(j) \\ j = 0 \text{ to } 15 \end{array}$
	XAM j	1	0	1	1	0	1	j	j	j	j	2	D	j	1	1	$\begin{array}{l} (A) \leftarrow \rightarrow (M(DP)) \\ (X) \leftarrow (X)EXOR(j) \\ j = 0 \text{ to } 15 \end{array}$
ister transfe	XAMD j	1	0	1	1	1	1	j	j	j	j	2	F	j	1	1	$(A) \leftarrow \rightarrow (M(DP))$ $(X) \leftarrow (X)EXOR(j)$ j = 0  to  15 $(Y) \leftarrow (Y) - 1$
RAM to reg	XAMI j	1	0	1	1	1	0	j	j	j	j	2	E	j	1	1	$\begin{array}{l} (A) \leftarrow \rightarrow (M(DP)) \\ (X) \leftarrow (X)EXOR(j) \\ j = 0 \text{ to } 15 \\ (Y) \leftarrow (Y) + 1 \end{array}$
	TMA j	1	0	1	0	1	1	j	j	j	j	2	В	j	1	1	$(M(DP)) \leftarrow (A)$ $(X) \leftarrow (X)EXOR(j)$ j = 0  to  15

# MACHINE INSTRUCTIONS (INDEX BY TYPES)



Skip condition	Carry flag CY	Datailed description
-	-	Transfers the contents of register B to register A.
-	-	Transfers the contents of register A to register B.
-	-	Transfers the contents of register Y to register A.
-	-	Transfers the contents of register A to register Y.
-	-	Transfers the contents of register B to the high-order 4 bits (E7–E4) of register E, and the contents of register A to the low-order 4 bits (E3–E0) of register E.
-	-	Transfers the high-order 4 bits (E7–E4) of register E to register B, and low-order 4 bits (E3–E0) of register E to register A.
-	-	Transfers the contents of the low-order 3 bits (A2–A0) of register A to register D.
-	-	Transfers the contents of register D to the low-order 3 bits (A2–A0) of register A.
-	-	Transfers the contents of register Z to the low-order 2 bits (A1, A0) of register A.
-	_	Transfers the contents of register X to register A.
-	-	Transfers the contents of stack pointer (SP) to the low-order 3 bits (A2–A0) of register A.
Continuous description	_	Loads the value x in the immediate field to register X, and the value y in the immediate field to register Y. When the LXY instructions are continuously coded and executed, only the first LXY instruction is executed and other LXY instructions coded continuously are skipped.
_	-	Loads the value z in the immediate field to register Z.
(Y) = 0	-	Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next in- struction is skipped. When the contents of register Y is not 0, the next instruction is executed.
(Y) = 15	-	Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped. When the contents of register Y is not 15, the next instruction is executed.
_	-	After transferring the contents of M(DP) to register A, an exclusive OR operation is performed between reg- ister X and the value j in the immediate field, and stores the result in register X.
-	-	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is per- formed between register X and the value j in the immediate field, and stores the result in register X.
(Y) = 15	-	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is per- formed between register X and the value j in the immediate field, and stores the result in register X. Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped. When the contents of register Y is not 15, the next instruction is executed.
(Y) = 0	-	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is per- formed between register X and the value j in the immediate field, and stores the result in register X. Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next in- struction is skipped. When the contents of register Y is not 0, the next instruction is executed.
_	_	After transferring the contents of register A to M(DP), an exclusive OR operation is performed between reg- ister X and the value j in the immediate field, and stores the result in register X.



Parameter	r					Ir	nstru	ctior	n coc	le					r of s	r of s	Eurotion	
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	ade otat	cimal ion	Numbe word	Numbe cycle	Function	
	LA n	0	0	0	1	1	1	n	n	n	n	0	7	n	1	1	$(A) \leftarrow n$ n = 0  to  15	
	TABP p	0	0	1	0	p5	p4	рз	p2	p1	po	0	8 +r	p	1	3	$(SP) \leftarrow (SP) + 1$ $(SK(SP)) \leftarrow (PC)$ $(PCH) \leftarrow p (Note)$ $(PCL) \leftarrow (DR2-DR0, A3-A0)$ at (UPTF) = 0 $(B) \leftarrow (ROM(PC))7-4$ $(A) \leftarrow (ROM(PC))3-0$ at (UPTF) = 1 $(DR2) \leftarrow (0)$ $(DR1, DR0) \leftarrow (ROM(PC))9, 8$ $(B) \leftarrow (ROM(PC))7-4$	
ration	АМ	0	0	0	0	0	0	1	0	1	0	0	0	A	1	1	$(A) \leftarrow (A) + (M(DP))$	
etic ope	AMC	0	0	0	0	0	0	1	0	1	1	0	0	в	1	1	$(A) \leftarrow (A) + (M(DP)) + (CY)$ $(CY) \leftarrow Carry$	
Arithm	A n	0	0	0	1	1	0	n	n	n	n	0	6	n	1	1	(A) ← (A) + n n = 0 to 15	
	AND	0	0	0	0	0	1	1	0	0	0	0	1	8	1	1	(A) ← (A) AND (M(DP))	
	OR	0	0	0	0	0	1	1	0	0	1	0	1	9	1	1	(A) ← (A) OR (M(DP))	
	sc	0	0	0	0	0	0	0	1	1	1	0	0	7	1	1	(CY) ← 1	
	RC	0	0	0	0	0	0	0	1	1	0		0	, 6	1	1	$(CY) \leftarrow 0$	
	870		0	0	0	1	0	1	1	1	1		2	F	1	1	(CX) = 0.2	
	CMA		0	0	0	0	1	1	1	0	0		4	, C	1	1	(0,1) = 0	
			0	0	0	0	1	י א	, ,	0	0		1	0				
	RAR		0	0	0	0	1	1	1	0	1	0	1	D	1	1		
ç	SB j	0	0	0	1	0	1	1	1	j	j	0	5	C +j	1	1	$(Mj(DP)) \leftarrow 1$ j = 0  to  3	
operatic	RB j	0	0	0	1	0	0	1	1	j	j	0	4	C +j	1	1	$\begin{array}{l} (Mj(DP)) \leftarrow 0\\ j = 0 \text{ to } 3 \end{array}$	
Bit	SZB j	0	0	0	0	1	0	0	0	j	j	0	2	j	1	1	(Mj(DP)) = 0 ? j = 0 to 3	
son	SEAM	0	0	0	0	1	0	0	1	1	0	0	2	6	1	1	(A) = (M(DP)) ?	
npari	SEA n	0	0	0	0	1	0	0	1	0	1	0	2	5	2	2	(A) = n ?	
Co Co		0	0	0	1	1	1	n	n	n	n	0	7	n		-	n = 0 to 15	
Note: p is	0 to 31 for M34	4556l	0 M4/M	4H. p	is 0	to 63	· 3 for	M345	556M	8/M8	 H/G8/	1 U G8H.			I	1	1	



Skip condition	Carry flag CY	Datailed description
Continuous description	-	Loads the value n in the immediate field to register A. When the LA instructions are continuously coded and executed, only the first LA instruction is executed and other LA instructions coded continuously are skipped.
_	-	UPTF = 0: Transfers bits 7 to 4 to register B and bits 3 to 0 to register A. These bits 9 to 0 are the ROM pattern in ad- dress (DR2 DR1 DR0 A3 A2 A1 A0)2 specified by registers A and D in page p. When this instruction is executed, be careful not to over the stack because 1 stage of stack register is used. UPTF = 1: Transfers bits 9, 8 to register D, bits 7 to 4 to register B and bits 3 to 0 to register A. These bits 7 to 0 are the ROM pattern in address (DR2 DR1 DR0 A3 A2 A1 A0)2 specified by registers A and D in page p. When this instruction is executed, be careful not to over the stack because 1 stage of stack register is used.
-	-	Adds the contents of M(DP) to register A. Stores the result in register A. The contents of carry flag CY re- mains unchanged.
-	0/1	Adds the contents of M(DP) and carry flag CY to register A. Stores the result in register A and carry flag CY.
Overflow = 0	-	Adds the value n in the immediate field to register A, and stores a result in register A. The contents of carry flag CY remains unchanged. Skips the next instruction when there is no overflow as the result of operation. Executes the next instruction when there is overflow as the result of operation.
-	-	Takes the AND operation between the contents of register A and the contents of M(DP), and stores the re- sult in register A.
_	-	Takes the OR operation between the contents of register A and the contents of M(DP), and stores the result in register A.
-	1	Sets (1) to carry flag CY.
-	0	Clears (0) to carry flag CY.
(CY) = 0	-	Skips the next instruction when the contents of carry flag CY is "0."
-	-	Stores the one's complement for register A's contents in register A.
-	0/1	Rotates 1 bit of the contents of register A including the contents of carry flag CY to the right.
_	-	Sets (1) the contents of bit j (bit specified by the value j in the immediate field) of M(DP).
-	-	Clears (0) the contents of bit j (bit specified by the value j in the immediate field) of M(DP).
(Mj(DP)) = 0 j = 0 to 3	-	Skips the next instruction when the contents of bit j (bit specified by the value j in the immediate field) of M(DP) is "0." Executes the next instruction when the contents of bit j of M(DP) is "1."
(A) = (M(DP))	-	Skips the next instruction when the contents of register A is equal to the contents of $M(DP)$ . Executes the next instruction when the contents of register A is not equal to the contents of $M(DP)$ .
(A) = n	-	Skips the next instruction when the contents of register A is equal to the value n in the immediate field. Executes the next instruction when the contents of register A is not equal to the value n in the immediate field.



Parameter	arameter					Ir	nstru	ctior	n cod	le			er of Is	er of es	Function	
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	Do	Hexadecimal notation	Numbe word	Numbe cycle	Function	
	Ва	0	1	1	<b>a</b> 6	<b>a</b> 5	a4	a3	a2	<b>a</b> 1	<b>a</b> 0	1 8 a +a	1	1	(PCL) ← a6–a0	
ation	BL p, a	0	0	1	1	1	p4	рз	p2	p1	p0	0 E p +p	2	2	(PCH) ← p (Note) (PCL) ← a6–a0	
ch oper		1	p6	p5	a6	<b>a</b> 5	a4	аз	a2	aı	a0	2 p a +p+a				
Bran	BLA p	0	0	0	0	0	1	0	0	0	0	0 1 0	2	2	$(PCH) \leftarrow p (Note)$	
		1	p6	p5	p4	0	0	рз	p2	p1	p0	2 p p +p				
	BM a	0	1	0	a6	a5	<b>a</b> 4	аз	a2	<b>a</b> 1	a0	1 a a	1	1	(SP) ← (SP) + 1 (SK(SP)) ← (PC)	
															$\begin{array}{l} (PCH) \leftarrow 2 \\ (PCL) \leftarrow a_{6-a_{0}} \end{array}$	
operatio	BML p, a	0	0	1	1	0	p4	рз	p2	p1	p0	0 C p +p	2	2	$(SP) \leftarrow (SP) + 1$ $(SK(SP)) \leftarrow (PC)$ $(PCH) \leftarrow p (Note)$	
outine (		1	p6	p5	a6	<b>a</b> 5	a4	аз	a2	<b>a</b> 1	<b>a</b> 0	2 p a +p +a			$(PCL) \leftarrow a6-a0$	
Subre	BMLA p	0	0	0	0	1	1	0	0	0	0	030	2	2	 (SP) ← (SP) + 1 (SK(SP)) ← (PC)	
		1	p6	p5	p4	0	0	рз	p2	p1	p0	2 p p +p			$(PCH) \leftarrow p (Note) (PCL) \leftarrow (DR2-DR0,A3-A0)$	
	RTI	0	0	0	1	0	0	0	1	1	0	046	1	1	(PC) ← (SK(SP)) (SP) ← (SP) – 1	
n operation	RT	0	0	0	1	0	0	0	1	0	0	044	1	2	(PC) ← (SK(SP)) (SP) ← (SP) − 1	
Retur	RTS	0	0	0	1	0	0	0	1	0	1	045	1	2	(PC) ← (SK(SP)) (SP) ← (SP) − 1	

Note: p is 0 to 31 for M34556M4/M4H.

p is 0 to 63 for M34556M8/M8H/G8/G8H.

Skip condition	Carry flag CY	Datailed description
-	-	Branch within a page : Branches to address a in the identical page.
-	-	Branch out of a page : Branches to address a in page p.
_	-	Branch out of a page : Branches to address (DR2 DR1 DR0 A3 A2 A1 A0)2 specified by registers D and A in page p.
_	-	Call the subroutine in page 2 : Calls the subroutine at address a in page 2.
_	-	Call the subroutine : Calls the subroutine at address a in page p.
_	_	Call the subroutine : Calls the subroutine at address (DR2 DR1 DR0 A3 A2 A1 A0)2 specified by registers D and A in page p.
_	-	Returns from inte <mark>rrup</mark> t service routine to main routine. Returns each value of data pointer (X, Y, Z), carry flag, skip status, NOP mode status by the continuous de- scription of the LA/LXY instruction, register A and register B to the states just before interrupt.
_	-	Returns from subroutine to the routine called the subroutine.
Skip at uncondition	-	Returns from subroutine to the routine called the subroutine, and skips the next instruction at uncondition.



Parameter						Ir	nstru	ctior		le					er of Is	er of es	E se d'an	
Type of instructions	Mnemonic	D9	D8	D7	D6	D5 D4 D3 D2 D1 D0 Hexadecimal notation		Function										
	DI	0	0	0	0	0	0	0	1	0	0	0	0	4	1	1	$(INTE) \leftarrow 0$	
	EI	0	0	0	0	0	0	0	1	0	1	0	0	5	1	1	(INTE) ← 1	
	SNZ0	0	0	0	0	1	1	1	0	0	0	0	3	8	1	1	V10 = 0: (EXF0) = 1 ? (EXF0) ← 0 V10 = 1: SNZ0 = NOP	
	SNZI0	0	0	0	0	1	1	1	0	1	0	0	3	А	1	1	l12 = 1 : (INT) = "H" ?	
t operation																	l12 = 0 : (INT) = "L" ?	
errup	TAV1	0	0	0	1	0	1	0	1	0	0	0	5	4	1	1	$(A) \leftarrow (V1)$	
<u></u>	TV1A	0	0	0	0	1	1	1	1	1	1	0	3	F	1	1	$(\vee 1) \leftarrow (A)$	
	TAV2	0	0	0	1	0	1	0	1	0	1	0	5	5	1	1	$(A) \leftarrow (V2)$	
	TV2A	0	0	0	0	1	1	1	1	1	0	0	3	E	1	1	$(\vee 2) \leftarrow (A)$	
	TAI1	1	0	0	1	0	1	0	0	1	1	2	5	3	1	1	(A) ← (I1)	
	TI1A	1	0	0	0	0	1	0	1	1	1	2	1	7	1	1	(I1) ← (A)	

Note: p is 0 to 31 for M34556M4/M4H.

p is 0 to 63 for M34556M8/M8H/G8/G8H.

Skip condition	Carry flag CY	Datailed description
-	-	Clears (0) to interrupt enable flag INTE, and disables the interrupt.
_	-	Sets (1) to interrupt enable flag INTE, and enables the interrupt.
V10 = 0: (EXF0) = 1	-	When $V10 = 0$ : Clears (0) to the EXF0 flag and skips the next instruction when external 0 interrupt request flag EXF0 is "1." When the EXF0 flag is "0," executes the next instruction. When $V10 = 1$ : This instruction is equivalent to the NOP instruction. (V10: bit 0 of interrupt control register V1)
(INT) = "H" However, I12 = 1	-	When I12 = 1 : Skips the next instruction when the level of INT pin is "H." (I12: bit 2 of interrupt control reg- ister I1)
(INT) = "L" However, I12 = 0	-	When $I12 = 0$ : Skips the next instruction when the level of INT pin is "L."
_	_	Transfers the contents of interrupt control register V1 to register A.
-	-	Transfers the contents of register A to interrupt control register V1.
-	-	Transfers the contents of interrupt control register V2 to register A.
-	-	Transfers the contents of register A to interrupt control register V2.
_	-	Transfers the contents of interrupt control register 11 to register A.
-	-	Transfers the contents of register A to interrupt control register I1.
	1	



Parameter	Parameter					Ir	nstru	ctior		le		er of Is er of			
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hexadecimal notation	Numbe word	Numbe cycle	Function
	ТРАА	1	0	1	0	1	0	1	0	1	0	2 A A	1	1	(PA) ← (A)
	TAW1	1	0	0	1	0	0	1	0	1	1	24 B	1	1	$(A) \leftarrow (W1)$
	TW1A	1	0	0	0	0	0	1	1	1	0	2 0 E	1	1	$(W1) \leftarrow (A)$
	TAW2	1	0	0	1	0	0	1	1	0	0	2 4 C	1	1	$(A) \leftarrow (W2)$
	TW2A	1	0	0	0	0	0	1	1	1	1	2 0 F	1	1	(W2) ← (A)
	TAW3	1	0	0	1	0	0	1	1	0	1	24D	1	1	$(A) \leftarrow (W3)$
	тwза	1	0	0	0	0	1	0	0	0	0	2 1 0	1	1	$(W3) \leftarrow (A)$
	TAW4	1	0	0	1	0	0	1	1	1	0	24 E	1	1	$(A) \leftarrow (W4)$
	TW4A	1	0	0	0	0	1	0	0	0	1	2 1 1	1	1	(W4) ← (A)
	TABPS	1	0	0	1	1	1	0	1	0	1	275	1	1	(B) ← (TPS7–TPS4) (A) ← (TPS3–TPS0)
	TPSAB	1	0	0	0	1	1	0	1	0	1	235	1	1	$\begin{array}{l} (RPS7\text{-}RPS4) \leftarrow (B) \\ (TPS7\text{-}TPS4) \leftarrow (B) \\ (RPS3\text{-}RPS0) \leftarrow (A) \\ (TPS3\text{-}TPS0) \leftarrow (A) \end{array}$
	TAB1	1	0	0	1	1	1	0	0	0	0	270	1	1	(B) ← (T17–T14) (A) ← (T13–T10)
er operation	T1AB	1	0	0	0	1	1	0	0	0	0	230	1	1	$\begin{array}{l} (R17-R14) \leftarrow (B) \\ (T17-T14) \leftarrow (B) \\ (R13-R10) \leftarrow (A) \\ (T13-T10) \leftarrow (A) \end{array}$
Time	TAB2	1	0	0	1	1	1	0	0	0	1	271	1	1	(B) ← (T27–T24) (A) ← (T23–T20)
	T2AB	1	0	0	0	1	1	0	0	0	1	231	1	1	$(R2L7-R2L4) \leftarrow (B)$ $(T27-T24) \leftarrow (B)$ $(R2L3-R2L0) \leftarrow (A)$ $(T23-T20) \leftarrow (A)$
	T2HAB	1	0	1	0	0	1	0	1	0	0	294	1	1	(R2H7–R2H4) ← (B) (R2H3–R2H0) ← (A)
	TR1AB	1	0	0	0	1	1	1	1	1	1	23F	1	1	(R17–R14) ← (B) (R13–R10) ← (A)
	T2R2L	1	0	1	0	0	1	0	1	0	1	295	1	1	(T27–T20) ← (R2L7–R2L0)
	TLCA	1	0	0	0	0	0	1	1	0	1	2 0 D	1	1	$(LC) \leftarrow (A)$ $(RLC) \leftarrow (A)$
	SNZT1	1	0	1	0	0	0	0	0	0	0	280	1	1	V12 = 0: (T1F) = 1 ? (T1F) ← 0 V12 = 1: SNZT1 = NOP
	SNZT2	1	0	1	0	0	0	0	0	0	1	281	1	1	V13 = 0: (T2F) = 1 ? (T2F) ← 0 V13 = 1: SNZT2 = NOP
	SNZT3	1	0	1	0	0	0	0	0	1	0	282	1	1	V20 = 0: (T3F) = 1 ? (T3F) ← 0 V20 = 1: SNZT3 = NOP



Skip condition	Carry flag CY	Datailed description
-	-	Transfers the contents of register A to timer control register PA.
-	-	Transfers the contents of timer control register W1 to register A.
-	-	Transfers the contents of register A to timer control register W1.
-	-	Transfers the contents of timer control register W2 to register A.
-	-	Transfers the contents of register A to timer control register W2.
-	-	Transfers the contents of timer control register W3 to register A.
-	-	Transfers the contents of register A to timer control register W3.
-	-	Transfers the contents of timer control register W4 to register A.
-	-	Transfers the contents of register A to timer control register W4.
-	-	Transfers the high-order 4 bits of prescaler to register B, and transfers the low-order 4 bits of prescaler to register A.
-	-	Transfers the contents of register B to the high-order 4 bits of prescaler and prescaler reload register RPS, and transfers the contents of register A to the low-order 4 bits of prescaler and prescaler reload register RPS.
-	-	Transfers the high-order 4 bits of timer 1 to register B, and transfers the low-order 4 bits of timer 1 to register A.
-	-	Transfers the contents of register B to the high-order 4 bits of timer 1 and timer 1 reload register R1, and transfers the contents of register A to the low-order 4 bits of timer 1 and timer 1 reload register R1.
-	-	Transfers the high-order 4 bits of timer 2 to register B, and transfers the low-order 4 bits of timer 2 to regis- ter A.
-	-	Transfers the contents of register B to the high-order 4 bits of timer 2 and timer 2 reload register R2L, and transfers the contents of register A to the low-order 4 bits of timer 2 and timer 2 reload register R2L.
_	-	Transfers the contents of register B to the high-order 4 bits of timer 2 reload register R2H, and transfers the contents of register A to the low-order 4 bits of timer 2 reload register R2H.
-	-	Transfers the contents of register B to the high-order 4 bits of timer 1 reload register R1, and transfers the contents of register A to the low-order 4 bits of timer 1 reload register R1.
-	-	Transfers the contents of timer 2 reload register R2L to timer 2.
-	-	Transfers the contents of register A to timer LC and timer LC reload register RLC.
V12 = 0: (T1F) = 1	_	When $V12 = 0$ : Clears (0) to the T1F flag and skips the next instruction when timer 1 interrupt request flag T1F is "1". When the T1F flag is "0", executes the next instruction. When $V12 = 1$ : This instruction is equivalent to the NOP instruction. (V12: bit 2 of interrupt control register V1)
V13 = 0: (T2F) =1	_	When V13 = 0 : Clears (0) to the T2F flag and skips the next instruction when timer 2 interrupt request flag T2F is "1". When the T2F flag is "0", executes the next instruction. When V13 = 1 : This instruction is equivalent to the NOP instruction. (V13: bit 3 of interrupt control register V1)
V20 = 0: (T3F) = 1	_	When V20 = 0 : Clears (0) to the T3F flag and skips the next instruction when timer 3 interrupt request flag T3F is "1". When the T3F flag is "0", executes the next instruction. When V20 = 1 : This instruction is equivalent to the NOP instruction. (V20: bit 0 of interrupt control register V2)



Parameter						Ir	nstru	ction	cod	le					er of ds er of		<b>–</b> "	
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	Do	Hex	ade otati	cimal on	Numbe worc	Numbe cycle	Function	
	IAP0	1	0	0	1	1	0	0	0	0	0	2	6	0	1	1	(A) ← (P0)	
	OP0A	1	0	0	0	1	0	0	0	0	0	2	2	0	1	1	(P0) ← (A)	
	IAP1	1	0	0	1	1	0	0	0	0	1	2	6	1	1	1	(A) ← (P1)	
	OP1A	1	0	0	0	1	0	0	0	0	1	2	2	1	1	1	(P1) ← (A)	
	IAP2	1	0	0	1	1	0	0	0	1	0	2	6	2	1	1	(A) ← (P2)	
	OP2A	1	0	0	0	1	0	0	0	1	0	2	2	2	1	1	(P2) ← (A)	
	CLD	0	0	0	0	0	1	0	0	0	1	0	1	1	1	1	(D) ← 1	
	RD	0	0	0	0	0	1	0	1	0	0	0	1	4	1	1	$(D(Y)) \leftarrow 0$ (Y) = 0  to  7	
	SD	0	0	0	0	0	1	0	1	0	1	0	1	5	1	1	(D(Y)) ← 1 (Y) = 0 to 7	
	SZD	0	0	0	0	1	0	0	1	0	0	0	2	4	1	1	(D(Y)) = 0?	
L L C		0	0	0	0	1	0	1	0	1	1	0	2	в	1	1	(Y) = 0  to  5	
eratio	RCP	1	0	1	0	0	0	1	1	0	0	2	8	с	1	1	$(C) \leftarrow 0$	
ut op	SCP	1	0	1	0	0	0	1	1	0	1	2	8	D	1	1	(C) ← 1	
/Outp	TAPU0	1	0	0	1	0	1	0	1	1	1	2	5	7	1	1	(A) ← (PU0)	
Input	TPU0A	1	0	0	0	1	0	1	1	0	1	2	2	D	1	1	$(PU0) \leftarrow (A)$	
	TAPU1	1	0	0	1	0	1	1	1	1	0	2	5	Е	1	1	$(A) \leftarrow (PU1)$	
	TPU1A	1	0	0	0	1	0	1	1	1	0	2	2	Е	1	1	$(PU1) \leftarrow (A)$	
	тако	1	0	0	1	0	1	0	1	1	0	2	5	6	1	1	(A) ← (K0)	
	ткоа	1	0	0	0	0	1	1	0	1	1	2	1	В	1	1	(K0) ← (A)	
	TAK1	1	0	0	1	0	1	1	0	0	1	2	5	9	1	1	(A) ← (K1)	
	ΤΚ1Α	1	0	0	0	0	1	0	1	0	0	2	1	4	1	1	(K1) ← (A)	
	TAK2	1	0	0	1	0	1	1	0	1	0	2	5	А	1	1	(A) ← (K2)	
	TK2A	1	0	0	0	0	1	0	1	0	1	2	1	5	1	1	(K2) ← (A)	
	TFR0A	1	0	0	0	1	0	1	0	0	0	2	2	8	1	1	$(FR0) \leftarrow (A)$	
	TFR1A	1	0	0	0	1	0	1	0	0	1	2	2	9	1	1	$(FR1) \leftarrow (A)$	
	TFR2A	1	0	0	0	1	0	1	0	1	0	2	2	А	1	1	$(FR2) \leftarrow (A)$	



Skip condition	Carry flag CY	Datailed description
-	-	Transfers the input of port P0 to register A.
-	-	Outputs the contents of register A to port P0.
-	-	Transfers the input of port P1 to register A.
-	-	Outputs the contents of register A to port P1.
_	-	Transfers the input of port P2 to register A.
_	-	Outputs the contents of register A to port P2.
_	-	Sets (1) to all port D.
_	-	Clears (0) to a bit of port D specified by register Y.
_	_	Sets (1) to a bit of port D specified by register Y.
(D(Y)) = 0 However, (Y)=0 to 5	-	Skips the next instruction when a bit of port D specified by register Y is "0." Executes the next instruction when a bit of port D specified by register Y is "1."
_	_	Clears (0) to port C.
-	_	Sets (1) to port C.
-	_	Transfers the contents of pull-up control register PU0 to register A.
_	-	Transfers the contents of register A to pull-up control register PU0.
_	-	Transfers the contents of pull-up control register PU1 to register A.
_	-	Transfers the contents of register A to pull-up control register PU1.
-	-	Transfers the contents of key-on wakeup control register K0 to register A.
-	_	Transfers the contents of register A to key-on wakeup control register K0.
-	-	Transfers the contents of key-on wakeup control register K1 to register A.
-	-	Transfers the contents of register A to key-on wakeup control register K1.
-	-	Transfers the contents of key-on wakeup control register K2 to register A.
-	-	Transfers the contents of register A to key-on wakeup control register K2.
-	-	Transferts the contents of register A to port output structure control register FR0.
-	-	Transferts the contents of register A to port output structure control register FR1.
-	-	Transferts the contents of register A to port output structure control register FR2.

Parameter						Ir	nstru	ctior	1 COC	le					er of Is	er of	
Type of instructions	Mnemonic	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	ade ota	ecima tion	Numbe	Numbe cycle	Function
	TAL1	1	0	0	1	0	0	1	0	1	0	2	4	A	1	1	$(A) \leftarrow (L1)$
	TL1A	1	0	0	0	0	0	1	0	1	0	2	0	А	1	1	(L1) ← (A)
eratio	TL2A	1	0	0	0	0	0	1	0	1	1	2	0	В	1	1	(L2) ← (A)
D op(	TL3A	1	0	0	0	0	0	1	1	0	0	2	0	С	1	1	$(L3) \leftarrow (A)$
LCI	TC1A	1	0	1	0	1	0	1	0	0	0	2	A	. 8	1	1	(C1) ← (A)
	TC2A	1	0	1	0	1	0	1	0	0	1	2	A	. 9	1	1	(C2) ← (A)
u	CRCK	1	0	1	0	0	1	1	0	1	1	2	9	В	1	1	RC oscillator selected
perati	TAMR	1	0	0	1	0	1	0	0	1	0	2	5	2	1	1	$(A) \leftarrow (MR)$
ck of	TMRA	1	0	0	0	0	1	0	1	1	0	2	1	6	1	1	(MR) ← (A)
Clo	TRGA	1	0	0	0	0	0	1	0	0	1	2	0	9	1	1	(RG) ← (A)
	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	$(PC) \leftarrow (PC) + 1$
	POF	0	0	0	0	0	0	0	0	1	0	0	0	2	1	1	Transition to clock operating mode
	POF2	0	0	0	0	0	0	1	0	0	0	0	0	8	1	1	Transition to RAM back-up mode
	EDOE	0	0	0	4	0	4	4	0	_			F	Б			
	EPOF	U	U	U	1	U	1	1	0				5	в			POF, POF2 instructions valid
	SNZP	0	0	0	0	0	0	0	0	1	1	0	0	3	1	1	(P) = 1 ?
eration	WRST	1	0	1	0	1	0	0	0	0	0	2	A	. 0	1	1	(WDF1) = 1 ? (WDF1) ← 0
ner op	DWDT	1	0	1	0	0	1	1	1	0	0	2	9	С	1	1	Stop of watchdog timer function enabled
đ	SRST	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	System reset
	RUPT	0	0	0	1	0	1	1	0	0	0	0	5	8	1	1	$(UPTF) \leftarrow 0$
	SUPT	0	0	0	1	0	1	1	0	0	1	0	5	9	1	1	(UPTF) ← 1
	SVDE	1	0	1	0	0	1	0	0	1	1	2	9	3	1	1	At power down mode, voltage drop detection circuit valid

Note: SVDE instruction can be used only in H version.

Skip condition	Carry flag CY	Datailed description
_	-	Transfers the contents of LCD control register L1 to register A.
-	-	Transfers the contents of register A to LCD control register L1.
-	-	Transfers the contents of register A to LCD control register L2.
-	-	Transfers the contents of register A to LCD control register L3.
-	-	Transfers the contents of register A to LCD control register C1.
-	-	Transfers the contents of register A to LCD control register C2.
-	-	Selects the RC oscillation circuit for main clock, stops the on-chip oscillator (internal oscillator).
-	-	Transfers the contents of clock control regiser MR to register A.
-	-	Transfers the contents of register A to clock control register MR.
-	-	Transfers the contents of register A to clock control register RG.
-	-	No operation; Adds 1 to program counter value, and others remain unchanged.
-	-	Puts the system in clock operating mode by executing the POF instruction after executing the EPOF instruction.
-	-	Puts the system in RAM back-up mode by executing the POF2 instruction after executing the EPOF instruction.
_	_	Makes the immediate after POF or POF2 instruction valid by executing the EPOF instruction.
(P) = 1	-	Skips the next instruction when the P flag is "1". After skipping, the P flag remains unchanged.
(WDF1) = 1	-	Clears (0) to the WDF1 flag and skips the next instruction when watchdog timer flag WDF1 is "1." When the WDF1 flag is "0", executes the next instruction. Also, stops the watchdog timer function when executing the WRST instruction immediately after the DWDT instruction.
-	-	Stops the watchdog timer function by the WRST instruction.
-	- 1	System reset occurs.
-	-	Clears (0) to the high-order bit reference enable flag UPTF.
-	-	Sets (1) to the high-order bit reference enable flag UPTF.
-	-	Validates the voltage drop detection circuit at power down (clock operating mode and RAM back-up mode).



#### **INSTRUCTION CODE TABLE**

																		-	
	D9–D4	000000	000001	000010	000011	000100	000101	000110	000111	001000	001001	001010	001011	001100	001101	001110	001111	010000 010111	011000 011111
D3–D0	Hex. notation	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10–17	18–1F
0000	0	NOP	BLA	SZB 0	BMLA	_	TASP	A 0	LA 0	TABP 0	TABP 16	TABP 32*	TABP 48*	BML	BML	BL	BL	BM	В
0001	1	SRST	CLD	SZB 1	-	_	TAD	A 1	LA 1	TABP 1	TABP 17	TABP 33*	TABP 49*	BML	BML	BL	BL	BM	в
0010	2	POF	_	SZB 2	_	_	ТАХ	A 2	LA 2	TABP 2	TABP 18	TABP 34*	TABP 50*	BML	BML	BL	BL	BM	в
0011	3	SNZP	INY	SZB 3	-	_	TAZ	A 3	LA 3	TABP 3	TABP 19	TABP 35*	TABP 51*	BML	BML	BL	BL	BM	в
0100	4	DI	RD	SZD	-	RT	TAV1	A 4	LA 4	TABP 4	TABP 20	TABP 36*	TABP 52*	BML	BML	BL	BL	BM	в
0101	5	EI	SD	SEAn	-	RTS	TAV2	A 5	LA 5	TABP 5	TABP 21	TABP 37*	TABP 53*	BML	BML	BL	BL	BM	в
0110	6	RC	_	SEAM	-	RTI	-	A 6	LA 6	TABP 6	TABP 22	TABP 38*	TABP 54*	BML	BML	BL	BL	BM	в
0111	7	sc	DEY	_	_	_	_	A 7	LA 7	TABP 7	TABP 23	TABP 39*	TABP 55*	BML	BML	BL	BL	BM	в
1000	8	POF2	AND	_	SNZ0	LZ 0	RUPT	A 8	LA 8	TABP 8	TABP 24	TABP 40*	TABP 56*	BML	BML	BL	BL	BM	в
1001	9	_	OR	TDA	_	LZ 1	SUPT	A 9	LA 9	TABP 9	TABP 25	TABP 41*	TABP 57*	BML	BML	BL	BL	BM	в
1010	А	AM	ТЕАВ	TABE	SNZI0	LZ 2	-	A 10	LA 10	TABP 10	TABP 26	TABP 42*	TABP 58*	BML	BML	BL	BL	BM	В
1011	В	AMC	-	_	-	LZ 3	EPOF	A 11	LA 11	TABP 11	TABP 27	TABP 43*	TABP 59*	BML	BML	BL	BL	BM	в
1100	с	TYA	СМА	_	_	RB 0	SB 0	A 12	LA 12	TABP 12	TABP 28	TABP 44*	TABP 60*	BML	BML	BL	BL	BM	в
1101	D	_	RAR	_	-	RB 1	SB 1	A 13	LA 13	TABP 13	TABP 29	TABP 45*	TABP 61*	BML	BML	BL	BL	BM	В
1110	E	тва	ТАВ	-	TV2A	RB 2	SB 2	A 14	LA 14	TABP 14	TABP 30	TABP 46*	TABP 62*	BML	BML	BL	BL	BM	В
1111	F	_	TAY	SZC	TV1A	RB 3	SB 3	A 15	LA 15	TABP 15	TABP 31	TABP 47*	TABP 63*	BML	BML	BL	BL	BM	в

The above table shows the relationship between machine language codes and machine language instructions. D<sub>3</sub>–D<sub>0</sub> show the low-order 4 bits of the machine language code, and D<sub>9</sub>–D<sub>4</sub> show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked "–."

The codes for the second word of a two-word instruction are described below.

	The	The second word								
BL	1р	paaa	aaaa							
BML	1р	paaa	aaaa							
BLA	1p	pp00	рррр							
BMLA	1p	pp00	рррр							
SEA	00	0111	nnnn							
SZD	00	0010	1011							

• \* cannot be used in the M3455xM4/M4H.

	D9-D4	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111	110000 <u>111111</u>
D3-D0	Hex. notation	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30–3F
0000	0	_	тwза	OP0A	T1AB	_	_	IAP0	TAB1	SNZT1	_	WRST	TMA 0	TAM 0	XAM 0	XAMI 0	XAMD 0	LXY
0001	1	_	TW4A	OP1A	T2AB	_	_	IAP1	TAB2	SNZT2	-	_	TMA 1	TAM 1	XAM 1	XAMI 1	XAMD 1	LXY
0010	2	_	_	OP2A	_	_	TAMR	IAP2	_	SNZT3		_	TMA 2	TAM 2	XAM 2	XAMI 2	XAMD 2	LXY
0011	3	_	_	_	_	_	TAI1	_	_	_	SVDE**	_	TMA 3	TAM 3	XAM 3	XAMI 3	XAMD 3	LXY
0100	4	_	TK1A	_	_	_	_	_	_	_	Т2НАВ	_	TMA 4	TAM 4	XAM 4	XAMI 4	XAMD 4	LXY
0101	5	_	TK2A	_	TPSAB	_	_	_	TABPS	_	T2R2L	_	TMA 5	TAM 5	XAM 5	XAMI 5	XAMD 5	LXY
0110	6	_	TMRA	_	-	_	ТАКО	-	_	-	_	_	TMA 6	TAM 6	XAM 6	XAMI 6	XAMD 6	LXY
0111	7	-	TI1A	_	-	_	TAPU0	_	_	_	-<	-	TMA 7	TAM 7	XAM 7	XAMI 7	XAMD 7	LXY
1000	8	_	-	TFR0A	-	_	-	_	_	-	-(	TC1A	TMA 8	TAM 8	XAM 8	XAMI 8	XAMD 8	LXY
1001	9	TRGA	_	TFR1A	_	_	TAK1	-	_	(	-	TC2A	TMA 9	TAM 9	XAM 9	XAMI 9	XAMD 9	LXY
1010	А	TL1A	_	TFR2A	_	TAL1	TAK2	-	_	-	2	TPAA	TMA 10	TAM 10	XAM 10	XAMI 10	XAMD 10	LXY
1011	В	TL2A	ткоа	_	-	TAW1	-	$\leq$	2	-	CRCK	_	TMA 11	TAM 11	XAM 11	XAMI 11	XAMD 11	LXY
1100	С	TL3A	_	_	-	TAW2	-	-		RCP	DWDT	_	TMA 12	TAM 12	XAM 12	XAMI 12	XAMD 12	LXY
1101	D	TLCA	_	TPU0A	-	TAW3	-	-	_	SCP	_	-	TMA 13	TAM 13	XAM 13	XAMI 13	XAMD 13	LXY
1110	Е	TW1A	_	TPU1A	(	TAW4	TAPU1	-	_	_	_	_	TMA 14	TAM 14	XAM 14	XAMI 14	XAMD 14	LXY
1111	F	TW2A	_		TR1AB	-	-	_	_	_	_	-	TMA 15	TAM 15	XAM 15	XAMI 15	XAMD 15	LXY

### **INSTRUCTION CODE TABLE (continued)**

The above table shows the relationship between machine language codes and machine language instructions. D<sub>3</sub>–D<sub>0</sub> show the loworder 4 bits of the machine language code, and D<sub>9</sub>–D<sub>4</sub> show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked "–."

The codes for the second word of a two-word instruction are described below.

	The	The second word									
BL	1p	paaa	aaaa								
BML	1p	paaa	aaaa								
BLA	1p	pp00	рррр								
BMLA	1p	pp00	pppp								
SEA	00	0111	nnnn								
SZD	00	0010	1011								

• \*\* can be used only in the M3455xM4H/M8H/G8H.

## **ELECTRICAL CHARACTERISTICS**

### (1) Mask ROM version

## ABSOLUTE MAXIMUM RATINGS (Mask ROM version)

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply voltage		-0.3 to 6.5	V
VI	Input voltage P0, P1, P2, D0–D5, RESET, INT, XIN, XCIN		-0.3 to VDD+0.3	V
VI	Input voltage CNTR		-0.3 to VDD+0.3	V
Vo	Output voltage P0, P1, P2, D0–D7, RESET, CNTR	Output transistors in cut-off state	-0.3 to VDD+0.3	V
Vo	Output voltage C, XOUT, XCOUT		-0.3 to VDD+0.3	V
Vo	Output voltage SEG0–SEG28, COM0–COM3		-0.3 to VDD+0.3	V
Pd	Power dissipation	Ta = 25 °C	300	mW
Topr	Operating temperature range		-20 to 85	°C
Tstg	Storage temperature range		-40 to 125	°C

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### **RECOMMENDED OPERATING CONDITIONS 1**

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 5.5 V, unless otherwise noted)

Syllindi         Final metter         Conduction         Min.         Typ.         Max.         Offit           Vibo         Supply voltage (when ceramic resonator is used)         I(STCK) 5 4.4 MHz         2.7         5.5         V           Vibo         Supply voltage (when quart_crystal/on-chip oscillation is used)         I(STCK) 5 2.2 MHz         2.7         5.5         V           Vibo         Supply voltage (when quart_crystal/on-chip oscillation is used)         IfSTCK) 5 4.4 MHz         1.8         5.5         V           Vibo         Supply voltage (when RC oscillation is used)         IfSTCK) 5 4.4 MHz         2.7         5.5         V           Vibo         Supply voltage (when RC oscillation is used)         IfSTCK) 5 4.4 MHz         2.7         5.5         V           Vibo         Supply voltage         at RAM back-up mode         1.6         V         V           Viba         Mack-up voltage         at RAM back-up mode         1.8         VDD         V           Viba         LCD power supply (Note 1)         Viba         0         VDD         VDD         VDD           Vibit         "H" level input voltage         P0, P1, P2, Do-D5         0.8VDO         VDD         VDD           INT         0.8VDO         VDD         0         <	Currente e l	Devenueter	Candi	Conditions			Limits			
	Symbol	Parameter	Condi	tions	Min.	Тур.	Max.	Unit		
(when ceramic resonator is used)         If(STCK) \$ 4.4 MHz         2.7         5.5           If(STCK) \$ 2.2 MHz         2         5.5           VDD         Supply voltage (when quartz-crystal/on-chip oscillation is used)         1.8         5.5         V           VDD         Supply voltage (when RC oscillation is used)         1.8         5.5         V           VDD         Supply voltage (when RC oscillation is used)         1.8         5.5         V           VRAM         RAM back-up voltage         at RAM back-up mode         1.6         V         V           VC3         LCD power supply (Note 1)         -         0         VDD         V         V           VI:         "H" level input voltage         P0, P1, P2, Do-Ds         0.8VDD         VDD         V           VII.         "L" level input voltage         P0, P1, P2, Do-Ds         0         0.2VDD         VDD           VII.         "L" level input voltage         P0, P1, P2, Do-Ds         0         0.3VDD         VDD           VII.         "L" level input voltage         P0, P1, P2, Do-Ds         0         0.3VDD         VDD           VII.         "L" level average output current (Note 2)         P0, P1, P2, Do-Ds         VDD = 5 V        10         0         0.15VDD <td>Vdd</td> <td>Supply voltage</td> <td>f(STCK) ≤ 6 MHz</td> <td></td> <td>4</td> <td></td> <td>5.5</td> <td>V</td>	Vdd	Supply voltage	f(STCK) ≤ 6 MHz		4		5.5	V		
		(when ceramic resonator is used)	f(STCK) ≤ 4.4 MHz		2.7		5.5	1		
			f(STCK) ≤ 2.2 MHz		2		5.5			
VDD         Supply voltage (when quart2-crystal/on-chip oscillation is used)         1.8         5.5         V           VDD         Supply voltage (when RC oscillation is used)         f(STCK) ≤ 4.4 MHz         2.7         5.5         V           VMM         RAM back-up coscillation is used)         at RAM back-up mode         1.6         V         V           VSS         Supply voltage         at RAM back-up mode         1.6         V         V           VLC3         LCD power supply (Note 1)         1.8         VDD         V           VL         LCD power supply (Note 1)         1.8         VDD         V           VIL         "H" level input voltage         P0, P1, P2, D0-D5         0.8VDD         VDD           INT         0.85VDD         VDD         Xin, XCIN         0         0.3VDD           VIL         "L" level input voltage         P0, P1, P2, D0-D5         0         0         0.3VDD           INT         0         0.3VDD         Xin, XCIN         0         0.3VDD         VDD           IOH(peak)         "H" level peak output current (Note 2)         P0, P1, P2, D0-D5         VDD = 5 V        10         mA           IOH(avg)         "H" level average output current (Note 2)         F0, P1, P2, D0-D7, C			f(STCK) ≤ 1.1 MHz		1.8		5.5	1		
(when quartz-crystal/on-chip oscillation is used)         (STCK) ≤ 4.4 MHz         2.7         5.5         V           VDD         Supply voltage (when RC oscillation is used)         1.6         V         V           VRAM         RAM back-up voltage         at RAM back-up mode         1.6         V         V           VSS         Supply voltage         0         V	Vdd	Supply voltage			1.8		5.5	V		
		(when quartz-crystal/on-chip								
		oscillation is used)								
(when RC oscillation is used)         RAM         RAM back-up voltage         at RAM back-up mode         1.6         V           VSS         Supply voltage         0         V         V         V         1.6         V         V           VLC3         LCD power supply (Note 1)         1.8         VDD         V         V           VIH         "H" level input voltage         P0, P1, P2, D0-D5         0.8VDD         VDD         VDD           Xin, XCIN         0.85VDD         VDD         VDD         VDD         VDD         VDD           Nin, XCIN         0.85VDD         VDD         VDD         VDD         VDD         VDD           RESET         0.85VDD         VDD         VDD         VDD         VDD         VDD           VIL         "L" level input voltage         P0, P1, P2, D0-D5         0         0.30VDD         VDD           INT         0         0.30VDD         VDD         NIN         0         0.15VDD           INT         0         0.15VDD         VDD = 3 V         -100         0.15VDD           INT         VDD = 3 V         -100         VDD = 3 V         -100         0.15VDD           INT         VDD = 3 V         -100         0.0	Vdd	Supply voltage	f(STCK) ≤ 4.4 MHz		2.7		5.5	V		
VRAM         RAM back-up voltage         at RAM back-up mode         1.6         V         V           VIC3         LCD power supply (Note 1)		(when RC oscillation is used)								
VSS         Supply voltage         0         V           VLC3         LCD power supply (Note 1)         P. P1, P2, Do-D5         0.8 Vop         Vop         V           VIH         "H" level input voltage         P0, P1, P2, Do-D5         0.8 Vop         Vop         Vop         V           RESET         0.85 Vop	Vram	RAM back-up voltage	at RAM back-up mode		1.6			V		
VLC3         LCD power supply (Note 1)         1.8         VDD         V           VIH         "H" level input voltage         P0, P1, P2, Do-D5         0.8VbD         VDD         VDD           XIN, XCIN         0.7V0D         VDD         VDD         VDD         VDD         VDD           INT         0.85VbD         VDD         VDD         VDD         VDD         VDD           VIL         "L" level input voltage         P0, P1, P2, Do-D5         0         0.85VbD         VDD           VIL         "L" level input voltage         P0, P1, P2, Do-D6         0         0.33VbD         VDD           INT         0         0.15VbD         0         0.33VbD         VDD         Stoto         P0, P1, P2, Do-D5         VDD = 5 V         -20         mA           IOH(peak)         "H" level peak output current (Note 2)         P0, P1, P2, Do-D5         VDD = 5 V         -30         CNTR         -10         D         Stoto -5         C         VDD = 3 V         -10         MA           IOH(avg)         "H" level peak output current (Note 2)         P0, P1, P2, Do-D7, C         VDD = 3 V         -5         C         CNTR         VD = 5 V         -10         MA           IOL(peak)         "L" level peak output current (No	Vss	Supply voltage				0		V		
$ \begin{array}{ c c c c c c } & \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	VLC3	LCD power supply (Note 1)			1.8	•	Vdd	V		
$   \begin{tabular}{ c c c c c c } \hline $ $ $ $ $ $ $ $ $ $ $ $ $ $ $ $ $ $ $	Viн	"H" level input voltage	P0, P1, P2, D0–D5	P0, P1, P2, D0–D5			Vdd	V		
$   \begin{tabular}{ c c c c c c c } \hline RESET & 0.85VbD & VbD \\ \hline  NT & 0 & 0.3VbD \\ \hline  RESET & 0 & 0.3VbD \\ \hline  NT & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0.15VbD \\ \hline  NT & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & $			XIN, XCIN		0.7VDD		Vdd			
$   NT & 0.85 VDD & VDD \\ \hline CNTR & 0.8VDD & VDD \\ \hline CNTR & 0.8VDD & 0.2VDD \\ \hline NT & 0 & 0.3VDD \\ \hline NT & 0 & 0.3VDD \\ \hline NT & 0 & 0.15VDD \\ \hline NT & 0 & 0.15VDD \\ \hline CNTR & 0 & 0.15VD \\ \hline CNTR & 0 & 0$			RESET		0.85Vdd		Vdd			
$ \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			INT		0.85Vdd		Vdd			
$ \begin{tabular}{ c c c c c } & $\end{tabular}{ $\end{tabular} $\end{tabular} $$ $\end{tabular} $$$ $\end{tabuar} $$$ $\end{tabuar} $$$ $tabua$			CNTR		0.8Vdd		Vdd			
$ \frac{\text{Xin, Xcin}}{\text{RESET}} 0 0 0.3 \text{Vod}}{0.3 \text{Vod}} \\ \hline \text{RESET} 0 0 0.3 \text{Vod}}{0.3 \text{Vod}} \\ \hline \text{INT} 0 0 0.15 \text{Vod}} \\ \hline \text{ONTR} 0 0 0.15 \text{Vod}} \\ \hline \text{ONTR} 0 0 0.15 \text{Vod}} \\ \hline \text{ONTR} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 5 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 5 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 5 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 5 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 5 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod}} \\ \hline \text{ODD} = 3 \text{V} 0 0 0.15 \text{Vod} 0.1$	VIL	"L" level input voltage	P0, P1, P2, D0–D5		0		0.2VDD	V		
$ \frac{ \mbox{RESET} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$			XIN, XCIN		0		0.3Vdd			
$   INT \\ CNTR \\ CNTR \\ 0 \\ 0.15VbD \\ OD = 5 \\ VDD = 5 \\ VDD = 3 \\ VDD = 5 \\ VDD = 3 \\ VDD = 3 \\ VDD = 5 \\ VD = 5 \\ V = 5 \\ VD = 5 \\ V = 5 \\ VD = 5 \\$			RESET		0		0.3Vdd	]		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			INT		0		0.15Vdd			
$ \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			CNTR		0		0.15Vdd	_		
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	loн(peak)	"H" level peak output current	P0, P1, P2, D0-D5	VDD = 5 V			-20	mA		
$ \begin{array}{ c c c c c } \hline \mbox{C} & \mbox{VD} \mbox{D} D$				VDD = 3 V			-10			
$ \begin{array}{ c c c c c } \hline \mbox{CNTR} & \mbox{Vdd} = 3 \ V & \mbox{obs} & \mbox{-15} \\ \hline \mbox{IOH(avg)} & \mbox{"H" level average output current} & \mbox{P0, P1, P2, D0-D5} & \mbox{Vdd} = 5 \ V & \mbox{IDd} = 5 \ V & \mbox{IDd} = 3 \ V & \mbox{IDd} = 5 \ V & \mbox{IDd} = 3 \ V & I$			С	VDD = 5 V			-30			
$ \begin{array}{ c c c c c c c c c } \hline \mbox{IOH}(avg) & \mbox{``H" level average output current} (Note 2) & \mbox{``De 5, V} & \\mbox{``De 5, V} & \\\mbox{``De 5, V} & \\\mbox{``De 5, V} & \\\\mbox{``De 5, V} & \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\$		4	CNTR	VDD = 3 V			-15			
$ \left( \begin{array}{c c c c c c c c c c c c } & VDD = 3 V & -5 \\ \hline C & VDD = 5 V & -20 \\ \hline CNTR & VDD = 3 V & -10 \\ \hline VDD = -10 \\ \hline VD $	IOH(avg)	"H" level average output current	P0, P1, P2, D0-D5	VDD = 5 V			-10	mA		
$ \begin{array}{ c c c c c c } \hline C & VDD = 5 V & -20 \\ \hline VDD = 3 V & -10 \\ \hline VDD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VDD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C, CNTR & -10 \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C \\ \hline VD = 1 \ PO, P1, P2, D0 - D5, C \\ \hline VD = 1 \ PO, P$		(Note 2)		VDD = 3 V			-5	]		
$ \begin{array}{ c c c c c c } \hline CNTR & VDD = 3 V & -10 \\ \hline OL(peak) & "L" level peak output current \\ \hline PO, P1, P2, Do-D7, C \\ \hline CNTR & VDD = 3 V & 24 \\ \hline RESET & VDD = 3 V & 12 \\ \hline RESET & VDD = 5 V & 10 \\ \hline VDD = 3 V & 4 \\ \hline VDD = 3 V & 4 \\ \hline OL(avg) & "L" level average output current \\ (Note 2) & \hline PO, P1, P2, Do-D7, C \\ \hline CNTR & VDD = 5 V & 15 \\ \hline CNTR & VDD = 3 V & 7 \\ \hline RESET & VDD = 5 V & 77 \\ \hline RESET & VDD = 5 V & 77 \\ \hline VDD = 3 V & 77 \\ \hline DD = 5 V & 77 \\ \hline VDD = 3 V & 77 \\ \hline DD = 5 V & 77 \\ \hline DD $			С	VDD = 5 V			-20	-		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			CNTR	VDD = 3 V			-10			
$ \begin{array}{ c c c c c c } \hline & & & & & & & & & & & & & & & & & & $	IOL(peak)	"L" level peak output current	P0, P1, P2, D0–D7, C	VDD = 5 V			24	mA		
$ \begin{array}{ c c c c c c } \hline RESET & VDD = 5 V & & & 10 \\ \hline VDD = 3 V & & & 4 \\ \hline VDD = 3 V & & & 4 \\ \hline VDD = 3 V & & & & 15 \\ \hline VDD = 3 V & & & & & 15 \\ \hline VDD = 3 V & & & & & & 7 \\ \hline \hline RESET & VDD = 5 V & & & & & & 7 \\ \hline \hline RESET & VDD = 5 V & & & & & & 5 \\ \hline VDD = 3 V & & & & & & & 7 \\ \hline \hline DD = 3 V & & & & & & & & & & & & & & & & & &$			CNTR	VDD = 3 V			12			
$ \begin{array}{ c c c c c c c } \hline & VDD = 3 V & & & & & & & & & & & & & & & & & &$			RESET	VDD = 5 V			10	1		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		÷		VDD = 3 V			4			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	loL(avg)	"L" level average output current	P0, P1, P2, D0–D7, C	VDD = 5 V			15	mA		
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	(avg)	(Note 2)	CNTR	VDD = 3 V			7			
VDD = 3 V         2           ΣΙΟΗ(avg)         "H" level total average current         P0, P1, P2, D0–D5, C, CNTR         -40         mA           ΣΙΟL(avg)         "L" level total average current         P0, P1, P2, D0–D5, C, CNTR         60         mA           Δο, D7, RESET         60         mA			RESET	VDD = 5 V			5	1		
ΣΙΟΗ(avg)         "H" level total average current         P0, P1, P2, D0–D5, C, CNTR         -40         mA           ΣΙΟL(avg)         "L" level total average current         P0, P1, P2, D0–D5, C, CNTR         60         mA           Δ0, D7, RESET         60				VDD = 3 V			2	1		
Stoll(avg)         "L" level total average current         P0, P1, P2, D0–D5, C, CNTR         60         mA           D6, D7, RESET         60	ΣIOH(avg)	"H" level total average current	P0, P1, P2, D0–D5, C, CNTR				-40	mA		
D6, D7, RESET 60	ΣIOL(avg)	"L" level total average current	P0, P1, P2, D0–D5, C, CNTR				60	mA		
			D6, D7, RESET			60	1			

Notes 1: At 1/2 bias: VLC1 = VLC2 = (1/2)•VLC3

At 1/3 bias: VLC1 = (1/3)•VLC3, VLC2 = (2/3)•VLC3

2: The average output current is the average value during 100 ms.

### **RECOMMENDED OPERATING CONDITIONS 2**

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 5.5 V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	
f(XIN)	Oscillation frequency	Through mode	VDD = 4 to 5.5 V			6	MHz
	(with a ceramic resonator)		VDD = 2.7 to 5.5 V			4.4	
			VDD = 2 to 5.5 V			2.2	
			VDD = 1.8 to 5.5 V			1.1	
		Frequency/2 mode	VDD = 2.7 to 5.5 V			6	
			VDD = 2 to 5.5 V			4.4	]
			VDD = 1.8 to 5.5 V			2.2	
		Frequency/4 mode	VDD = 2 to 5.5 V			6	
			VDD = 1.8 to 5.5 V			4.4	
		Frequency/8 mode	VDD = 1.8 to 5.5 V			6	
f(XIN)	Oscillation frequency	VDD = 2.7 to 5.5 V				4.4	MHz
	(at RC oscillation) (Note)						
f(XIN)	Oscillation frequency	Through mode	VDD = 4  to  5.5  V			4.8	MHz
	(with a ceramic oscillation selected		VDD = 2.7  to  5.5  V			3.2	
	external clock input)		VDD = 2  to  5.5  V			1.6	
			VDD = 1.8 to 5.5 V			0.8	
		Frequency/2 mode	VDD = 2.7 to 5.5 V			4.8	
			VDD = 2 to 5.5 V			3.2	
			VDD = 1.8 to 5.5 V			1.6	
		Frequency/4 mode	VDD = 2 to 5.5 V			4.8	
			VDD = 1.8 to 5.5 V			3.2	
		Frequency/8 mode	VDD = 1.8 to 5.5 V			4.8	1
f(XCIN)	Oscillation frequency (sub-clock)	Quartz-crystal oscillator	+			50	kHz
f(CNTR)	Timer external input frequency	CNTR				f(STCK)/6	Hz
tw(CNTR)	Timer external input period	CNTR		3/f(STCK)			s
	("H" and "L" pulse width)						
TPON	Power-on reset circuit	$VDD = 0 \rightarrow 1.8 V$				100	μs
	valid supply voltage rising time						

Note: The frequency is affected by a capacitor, a resistor and a microcomputer. So, set the constants within the range of the frequency limits.





System clock (STCK) operating condition map (Mask ROM version)

#### **ELECTRICAL CHARACTERISTICS 1**

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 5.5 V, unless otherwise noted)

Symbol	Parameter	conditions		Limits			
Symbol	i alametei	Test	Conditions	Min.	Тур.	Max.	Unit
Voн	"H" level output voltage	VDD = 5 V	Iон = -10 mA	3			V
	P0, P1, P2, D0–D5		Iон = -3 mA	4.1			
		VDD = 3 V	Iон = -5 mA	2.1			
			Iон = -1 mA	2.4			
Vон	"H" level output voltage	VDD = 5 V	Iон = -20 mA	3			V
	C, CNTR		Iон = -6 mA	4.1			
		VDD = 3 V	Iон = -10 mA	2.1			
			Iон = -3 mA	2.4			
Vol	"L" level output voltage	VDD = 5 V	IOL = 15 mA			2	V
	P0, P1, P2, D0–D7, C, CNTR		IOL = 5 mA			0.9	
		VDD = 3 V	IOL = 9 mA			1.4	1
			IOL = 3 mA			0.9	
Vol	"L" level output voltage	VDD = 5 V	IOL = 5 mA			2	V
	RESET		IOL = 1 mA			0.6	
		VDD = 3 V	IOL = 2 mA			0.9	
Іін	"H" level input current	VI = VDD				2	μA
	P0, P1, P2, D0–D5, XIN, XCIN, RESET						
	CNTR, INT						
lı∟	"L" level input current	VI = 0 V P0, P1 No pu			-2	μA	
	P0, P1, P2, D0–D5, XIN, XCIN, RESET						
	CNTR, INT						
Rpu	Pull-up resistor value	VI = 0 V	VDD = 5 V	30	60	125	kΩ
	P0, P1, RESET		VDD = 3 V	50	120	250	
VT+ – VT–	Hysteresis RESET	VDD = 5 V			1		V
	<u> </u>	VDD = 3 V			0.4		
Vt+ – Vt–	Hysteresis INT	VDD = 5 V			0.6		V
		VDD = 3 V			0.3		
Vt+ – Vt–	Hysteresis CNTR	VDD = 5 V			0.2		V
		VDD = 3 V			0.2		
f(RING)	On-chip oscillator clock frequency	VDD = 5 V		200	500	700	kHz
		VDD = 3 V		100	250	400	
$\Delta f(XIN)$	Frequency error	VDD = 5 V ± 10 %, Ta	= 25 °C			±17	%
	(with RC oscillation,						
	error of external R, C not included)	VDD = 3 V ± 10 %, Ta	= 25 °C			±17	
	(Note 1)						
RCOM	COM output impedance	VDD = 5 V			1.5	7.5	kΩ
	(Note 2)	VDD = 3 V			2	10	
RSEG	SEG output impedance	VDD = 5 V			1.5	7.5	kΩ
	(Note 2)	VDD = 3 V			2	10	
RVLC	Internal resistor for LCD power supply	When dividing resistor 2r X 3 selected			480	960	kΩ
		When dividing resistor	200	320	640		
		When dividing resistor	150	240	480		
		When dividing resistor	100	160	320		

Notes 1: When RC oscillation is used, use the external 33 pF capacitor (C).

2: The impedance state is the resistor value of the output voltage.

at VLC3 level output: VO = 0.8 VLC3

at VLC2 level output: VO = 0.8 VLC2 at VLC1 level output: VO = 0.2 VLC2 + VLC1

at Vss level output: VO = 0.2 Vss

### **ELECTRICAL CHARACTERISTICS 2**

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 5.5 V, unless otherwise noted)

Symbol		Parameter	Test con	ditions		Linit		
Symbol		Talameter		unions	Min.	Тур.	Max.	Unit
IDD	Supply current	at active mode	VDD = 5 V	f(STCK) = f(XIN)/8		1.2	2.4	mA
		(with a ceramic resonator)	f(XIN) = 6 MHz	f(STCK) = f(XIN)/4		1.3	2.6	
			f(RING) = stop	f(STCK) = f(XIN)/2		1.6	3.2	
			f(XCIN) = stop	f(STCK) = f(XIN)		2.2	4.4	
			VDD = 5 V	f(STCK) = f(XIN)/8		0.9	1.8	mA
			f(XIN) = 4 MHz	f(STCK) = f(XIN)/4		1	2	
			f(RING) = stop	f(STCK) = f(XIN)/2		1.2	2.4	
			f(XCIN) = stop	f(STCK) = f(XIN)		1.6	3.2	
			VDD = 3 V	f(STCK) = f(XIN)/8		0.3	0.6	mA
			f(XIN) = 4 MHz	f(STCK) = f(XIN)/4		0.4	0.8	
			f(RING) = stop	f(STCK) = f(XIN)/2		0.5	1.0	
			f(XCIN) = stop	f(STCK) = f(XIN)	9	0.7	1.4	
		at active mode	VDD = 5 V	f(STCK) = f <mark>(R</mark> ING)/8		50	100	μA
		(with an on-chip oscillator)	f(XIN) = stop	f(STCK) = f(RING)/4		60	120	
			f(RING) = active	f(STCK) = f(RING)/2		80	160	
			f(XCIN) = stop	f(STCK) = f(RING)		120	240	
			VDD = 3 V	f(STCK) = f(RING)/8		10	20	μΑ
			f(XIN) = stop	f(STCK) = f(RING)/4		13	26	
			f(RING) = active	f(STCK) = f(RING)/2		19	38	
			f(XCIN) = stop	f(STCK) = f(RING)		31	62	
		at active mode	VDD = 5 V	f(STCK) = f(XCIN)/8		7	14	μΑ
		(with a quartz-crystal	f(XIN) = stop	f(STCK) = f(XCIN)/4		8	16	
		oscillator)	f(RING) = stop	f(STCK) = f(XCIN)/2		10	20	
			f(XCIN) = 32 kHz	f(STCK) = f(XCIN)		14	28	
			VDD = 3 V	f(STCK) = f(XCIN)/8		5	10	μA
			f(XIN) = stop	f(STCK) = f(XCIN)/4		6	12	
			f(RING) = stop	f(STCK) = f(XCIN)/2		7	14	
			f(XCIN) = 32 kHz	f(STCK) = f(XCIN)		8	16	
		at clock operation mode	f(XCIN) = 32 kHz	Vdd = 5 V		6	12	μA
		(POF instruction execution)		VDD = 3 V		5	10	
		at RAM back-up mode	Ta = 25 °C			0.1	2	μA
		(POF2 instruction execution)	VDD = 5 V				10	
			VDD = 3 V				6	

### **VOLTAGE DROP DETECTION CIRCUIT CHARACTERISTICS**

(Mask ROM version: Ta = -20 °C to 85 °C, unless otherwise noted)

Symbol	Parameter	Tost conditions		Linit			
Symbol	Falameter		Min.	Тур.	Max.	Unit	
Vrst-	Detection voltage	Ta = 25 °C	1.6	1.8	2	V	
	(reset occurs) (Note 2)	-20 °C ≤ Ta < 0 °C	1.7		2.3		
		0 °C ≤ Ta < 50 °C	1.4		2.2		
		50 °C ≤ Ta ≤ 85 °C	1.2		1.9		
Vrst+	Detection voltage	Ta = 25 °C	1.7	1.9	2.1	V	
	(reset release) (Note 3)	-20 °C ≤ Ta < 0 °C	1.8		2.4		
		0 °C ≤ Ta < 50 °C	1.5		2.3		
		50 °C ≤ Ta ≤ 85 °C	1.3		2		
Vrst+-	Detection voltage hysteresis			0.1		V	
Vrst-							
IRST	Operation current (Note 4)	VDD = 5 V		50	100	μA	
		VDD = 3 V		30	60	1	
TRST	Detection time (Note 5)	$VDD \rightarrow (VRST^ 0.1 V)$		0.2	1.2	ms	

Notes 1: The voltage drop detection circuit is equipped with only the H version.

2: The detection voltage (VRST) is defined as the voltage when reset occurs when the supply voltage (VDD) is falling.

3: The detection voltage (VRST<sup>+</sup>) is defined as the voltage when reset is released when the supply voltage (VDD) is rising from reset occurs.

4: In the H version, IRST is added to IDD (power current).

5: The detection time (TRST) is defined as the time until reset occurs when the supply voltage (VDD) is falling to [VRST - 0.1 V].

6: The detection voltages (VRST<sup>+</sup>, VRST<sup>-</sup>) are set up lower than the minimum value of the supply voltage of the recommended operating conditions. As for details, refer to the LIST OF PRECAUTIONS.



## (2) One Time PROM version

## ABSOLUTE MAXIMUM RATINGS (One Time PROM version)

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply voltage		-0.3 to 4.0	V
VI	Input voltage P0, P1, P2, D0–D5, RESET, INT, XIN, XCIN		-0.3 to VDD+0.3	V
VI	Input voltage CNTR		-0.3 to VDD+0.3	V
Vo	Output voltage P0, P1, P2, D0-D7, RESET, CNTR	Output transistors in cut-off state	-0.3 to VDD+0.3	V
Vo	Output voltage C, XOUT, XCOUT		-0.3 to VDD+0.3	V
Vo	Output voltage SEG0–SEG28, COM0–COM3		-0.3 to VDD+0.3	V
Pd	Power dissipation	Ta = 25 °C	300	mW
Topr	Operating temperature range		-20 to 85	°C
Tstg	Storage temperature range		-40 to 125	°C

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### **RECOMMENDED OPERATING CONDITIONS 1**

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 3.6 V, unless otherwise noted)

Quarter	Demonster	0		1.1.4.14			
Symbol	Parameter	Conditions		Min.	Тур.	Max.	Unit
Vdd	Supply voltage	f(STCK) ≤ 4.4 MHz		2.7		3.6	V
	(when ceramic resonator is used)	f(STCK) ≤ 2.2 MHz		2		3.6	1
		f(STCK) ≤ 1.1 MHz		1.8		3.6	1
Vdd	Supply voltage			1.8		3.6	V
	(when quartz-crystal/on-chip						
	oscillator is used)						
Vdd	Supply voltage	f(STCK) ≤ 4.4 MHz		2.7		3.6	V
	(when RC oscillation is used)						
Vram	RAM back-up voltage	at RAM back-up mode		1.6			V
Vss	Supply voltage				0		V
VLC3	LCD power supply (Note 1)			1.8		Vdd	V
Viн	"H" level input voltage	P0, P1, P2, D0-D5		0.8VDD		Vdd	V
		XIN, XCIN		0.7VDD		Vdd	]
		RESET		0.85VDD		Vdd	]
		INT		0.85Vdd		Vdd	1
		CNTR		0.8Vdd		Vdd	
VIL	"L" level input voltage	P0, P1, P2, D0–D5		0		0.2Vdd	V
		XIN, XCIN		0		0.3Vdd	
		RESET		0		0.3Vdd	
		INT 🦲		0		0.15Vdd	
		CNTR		0		0.15Vdd	
IOн(peak)	"H" level peak output current	P0, P1, P2, D0–D5	VDD = 3 V			-10	mA
		C, CNTR	VDD = 3 V			-15	
Iон(avg)	"H" level average output current	P0, P1, P2, D0–D5	VDD = 3 V			-5	mA
	(Note 2)	C, CNTR	VDD = 3 V			-10	
IOL(peak)	"L" level peak output current	P0, P1, P2, D0–D7,	VDD = 3 V			12	mA
		C, CNTR					
		RESET	VDD = 3 V			4	]
IOL(avg)	"L" level average output current	P0, P1, P2, D0–D7,	VDD = 3 V			7	mA
	(Note 2)	C, CNTR					
		RESET	VDD = 3 V			2	
Σloн(avg)	"H" level total average current	P0, P1, P2, D0-D5, C,	CNTR			-40	mA
ΣIOL(avg)	"L" level total average current	P0, P1, P2, D0-D5, C,	CNTR			60	mA
		D6, D7, RESET				60	1

Notes 1: At 1/2 bias: VLC1 = VLC2 = (1/2)•VLC3 At 1/3 bias: VLC1 = (1/3)•VLC3, VLC2 = (2/3)•VLC3

2: The average output current is the average value during 100 ms.

### **RECOMMENDED OPERATING CONDITIONS 2**

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 3.6 V, unless otherwise noted)

Symbol	Parameter	Conc	Conditiona				Unit
Cymbol	T arameter		Conditions			Max.	
f(XIN)	Oscillation frequency	Through mode	VDD = 2.7 to 3.6 V			4.4	MHz
	(with a ceramic resonator)		VDD = 2 to 3.6 V			2.2	
			VDD = 1.8 to 3.6 V			1.1	
		Frequency/2 mode	VDD = 2.7 to 3.6 V			6	
			VDD = 2 to 3.6 V			4.4	
			VDD = 1.8 to 3.6 V			2.2	
		Frequency/4 mode	VDD = 2 to 3.6 V			6	
			VDD = 1.8 to 3.6 V			4.4	
		Frequency/8 mode	VDD = 1.8 to 3.6 V			6	
f(Xin)	Oscillation frequency (at RC oscillation) (Note)	VDD = 2.7 to 3.6 V	×			4.4	MHz
f(XIN)	Oscillation frequency	Through mode	VDD = 2.7 to 3.6 V			3.2	MHz
	(with a ceramic oscillation circuit		VDD = 2  to  3.6  V			1.6	
	selected, external clock input)		VDD = 1.8 to 3.6 V			0.8	
		Frequency/2 mode	VDD = 2.7 to 3.6 V			4.8	
			VDD = 2 to 3.6 V			3.2	
			VDD = 1.8 to 3.6 V			1.6	ĺ
		Frequency/4 mode	VDD = 2 to 3.6 V			4.8	
			VDD = 1.8 to 3.6 V			3.2	1
		Frequency/8 mode	VDD = 1.8 to 3.6 V			4.8	
f(XCIN)	Oscillation frequency	Quartz-crystal oscillator				50	kHz
	(with a quartz-crystal oscillator)						
f(CNTR)	Timer external input frequency	CNTR				f(STCK)/6	Hz
tw(CNTR)	Timer external input period	CNTR		3/f(STCK)			s
	("H" and "L" pulse width)						
TPON	Power-on reset circuit	$VDD = 0 \rightarrow 1.8 V$				100	μs
	valid supply voltage rising time						1

Note: The frequency is affected by a capacitor, a resistor and a microcomputer. So, set the constants within the range of the frequency limits.





System clock (STCK) operating condition map (One Time PROM version)

#### ELECTRICAL CHARACTERISTICS

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 1.8 to 3.6 V, unless otherwise noted)

Symbol		Deremeter				Limits		
Symbol	i alameter		Test conditions			Тур.	Max.	Unit
Voн	"H" level output voltage		VDD = 3 V	IOH = -5 mA	2.1			V
	P0, P1, P2, D0–D5			IOH = −1 mA	2.4			
Voн	"H" level output	voltage	VDD = 3 V	Iон = -10 mA	2.1			V
	C, CNTR			Iон = -3 mA	2.4			
Vol	"L" level output	voltage	VDD = 3 V	IOL = 9 mA			1.4	V
	P0, P1, P2, D0-	-D7, C, CNTR		IOL = 3 mA			0.9	
Vol	"L" level output	voltage	VDD = 3 V	IOL = 2 mA			0.9	V
	RESET							
Іін	"H" level input o	current	VI = VDD	·			2	μA
	P0, P1, P2, D0-	-D5, XIN, XCIN, RESET						
	CNTR, INT							
lı∟	"L" level input c	urrent	VI = 0 V P0, P1 No pull-up	)			-2	μA
	P0, P1, P2, D0-	-D5, XIN, XCIN, RESET						
	CNTR, INT							
Rpu	Pull-up resistor	value	VI = 0 V		50	120	250	kΩ
	P0, P1, RESET		VDD = 3 V					
VT+ – VT–	Hysteresis RES	ET	VDD = 3 V			0.4		V
Vt+ – Vt–	Hysteresis INT		VDD = 3 V			0.3		V
Vt+ – Vt–	Hysteresis CNT	steresis CNTR VDD = 3 V				0.2		V
f(RING)	On-chip oscillat	tor clock frequency	VDD = 3 V		100	250	400	kHz
$\Delta f(XIN)$	Frequency error		$VDD = 3 V \pm 10 \%$ , Ta = 25	5 °C			±17	%
· · /	(with RC oscillation.							
	error of external R. C not included )							
	(Note 1)	, ,						
RCOM	COM output im	pedance (Note 2)	VDD = 3 V			2	10	kΩ
RSEG	SEG output imr	pedance (Note 2)	VDD = 3 V			2	10	kΩ
RVLC	Internal resistor	r for LCD power supply	When dividing resistor 2r X 3 selected			480	960	kΩ
			When dividing resistor 2r X 2 selected			320	640	
			When dividing resistor r X	3 selected	150	240	480	
			When dividing resistor r X 2 selected			160	320	-
IDD	Supply current	at active mode	VDD = 3 V	f(STCK) = f(XIN)/8		0.3	0.6	mA
		(with a ceramic resonator)	f(XIN) = 4 MHz	f(STCK) = f(XIN)/4		0.4	0.8	-
		,	f(RING) = stop	f(STCK) = f(XIN)/2		0.6	1.2	-
			f(XCIN) = stop	f(STCK) = f(XIN)		0.9	1.8	-
		at active mode	VDD = 3 V	f(STCK) = f(RING)/8		12	24	μA
		(with an on-chip oscillator)	f(XIN) = stop	f(STCK) = f(RING)/4		17	34	,
		, , ,	f(RING) = active	f(STCK) = f(RING)/2		27	54	
			f(XCIN) = stop	f(STCK) = f(RING)		48	96	
		at active mode	VDD = 3 V	f(STCK) = f(XCIN)/8		5	10	μA
		(with a quartz-crystal	f(XIN) = stop	f(STCK) = f(XCIN)/4		6	12	
		oscillator)	f(RING) = stop	f(STCK) = f(XCIN)/2		7	14	
		,	f(Xcin) = 32 kHz	f(STCK) = f(XCIN)		9	18	
		at clock operation mode	VDD = 3 V			5	10	μA
		(POF instruction execution)	f(Xcin) = 32 kHz				-	
		at RAM back-up mode	Ta = 25 °C			0.1	2	μA
		(POF2 instruction execution)	VDD = 3 V				6	
1	1	1 ' '			1	1	1	

Notes 1: When RC oscillation is used, use the external 33 pF capacitor (C).

2: The impedance state is the resistor value of the output voltage.

at VLC3 level output: VO = 0.8 VLC3

at VLC2 level output: VO = 0.8 VLC2

at VLC1 level output: VO = 0.2 VLC2 + VLC1

at Vss level output: Vo = 0.2 Vss



## **VOLTAGE DROP DETECTION CIRCUIT CHARACTERISTICS**

(One Time PROM version: Ta = -20 °C to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Linit			
Symbol	Falalletei		Min.	Тур.	Max.	Unit	
Vrst-	Detection voltage	Ta = 25 °C	1.6	1.8	2	V	
	(reset occurs) (Note 2)	-20 °C ≤ Ta < 0 °C	1.7		2.3		
		0 °C ≤ Ta < 50 °C	1.4		2.2		
		50 °C ≤ Ta ≤ 85 °C	1.2		1.9		
Vrst <sup>+</sup>	Detection voltage	Ta = 25 °C	1.7	1.9	2.1	V	
	(reset release) (Note 3)	-20 °C ≤ Ta < 0 °C	1.8		2.4		
		0 °C ≤ Ta < 50 °C	1.5		2.3		
		50 °C ≤ Ta ≤ 85 °C	1.3		2		
Vrst+-	Detection voltage hysteresis			0.1		V	
Vrst <sup></sup>							
IRST	Operation current (Note 4)	VDD = 3 V		30	60	μA	
Trst	Detection time (Note 5)	$VDD \rightarrow (VRST^ 0.1 V)$		0.2	1.2	ms	

Notes 1: The voltage drop detection circuit is equipped with only the H version.

2: The detection voltage (VRST) is defined as the voltage when reset occurs when the supply voltage (VDD) is falling.

3: The detection voltage (VRST+) is defined as the voltage when reset is released when the supply voltage (VDD) is rising from reset occurs.

4: In the H version, IRST is added to IDD (supply current).

5: The detection time (TRST) is defined as the time until reset occurs when the supply voltage (VDD) is falling to [VRST – 0.1 V].

6: The detection voltages (VRST<sup>+</sup>, VRST<sup>-</sup>) are set up lower than the minimum value of the supply voltage of the recommended operating conditions. As for details, refer to the LIST OF PRECAUTIONS.



## **BASIC TIMING DIAGRAM**

Parameter P	Machine cycle Parameter Pin (signal) name			Mi Mi+1		
System clock	STCK					
Port D output	D0-D7		X			X
Port D input	D0D5			X		X
Ports P0, P1, P2 output	P00–P03 P10–P13 P20–P23		X		Ċ	×
Ports P0, P1, P2 input	P00–P03 P10–P13 P20–P23					×
Interrupt input	INT	6				×

#### **BUILT-IN PROM VERSION**

In addition to the mask ROM versions, the 4556 Group has the One Time PROM versions whose PROMs can only be written to and not be erased.

The built-in PROM version has functions similar to those of the mask ROM versions, but it has PROM mode that enables writing to built-in PROM.

#### Table 19 Product of built-in PROM version

Table 19 shows the product of built-in PROM version. Figure 61 shows the pin configurations of built-in PROM versions. The One Time PROM version has pin-compatibility with the mask ROM version.

able 19 Froduct of built-in FROM version							
Part number	PROM size	RAM size	Package	POM type			
Fait number	(X 10 bits)	(X 4 bits)	I ackage	Rolli type			
M34556G8FP	8192 words	288 words	42P2R-A	One Time PROM [shipped in blank]			
M34556G8HFP							

#### (1) PROM mode

The 4556 Group has a PROM mode in addition to a normal operation mode. It has a function to serially input/output the command codes, addresses, and data required for operation (e.g., read and program) on the built-in PROM using only a few pins. This mode can be selected by muddog entry after powering on the VDD pin. In the PROM mode, three types of software commands (read, program, and program verify) can be used. Clock-synchronous serial I/O is used, beginning from the LSB (LSB first).

#### (2) Notes on handling

③For the One Time PROM version shipped in blank, Renesas corp. does not perform PROM writing test and screening in the assembly process and following processes. In order to improve reliability after writing, performing writing and test according to the flow shown in Figure 60 before using is recommended (Products shipped in blank: PROM contents is not written in factory when shipped).

#### (3) Difference between Mask ROM version and One Time PROM version

Mask ROM version and One Time PROM version have some difference of the following characteristics within the limits of an electrical property by difference of a manufacture process, builtin ROM, and a layout pattern.

- a characteristic value
- a margin of operation
- the amount of noise-proof
- noise radiation, etc.,

Accordingly, be careful of them when swithcing.



Fig. 68 Flow of writing and test of the product shipped in blank



Fig. 69 Pin configuration of built-in PROM version

#### **ROM CODE ACCESS PROTECTION**

We would like to support a simple ROM code protection function that prevents a party other than the ROM-code owner to read and reprogram the built-in PROM code of the MCU.

First, Programmers must check the ID-code of the MCU.

If the ID-code is not blank, Programmer verifies it with the input IDcode. When the ID-codes do not match, Programmer will reject all further operations.

The MCU has each 10 bits of dedicated ROM spaces in address 009016 to 009616, as an ID-code (referred to as "the ID-code") enabling a Programmer to verify with the input ID-code and validate further operations.

Address 🧮		-
009016	ID1	
009116	ID2	
009216	ID3	
009316	ID4	
009416	ID5	
009516	ID6	
009616	ID7	
009716		

Fig. 70 ROM-Code Protection ID Location



#### PACKAGE OUTLINE



# **REVISION HISTORY**

# 4556 Group Data Sheet

Rev.	Date		Description
		Page	Summary
1.00	Jul. 23, 2003	_	First edition issued
1.01	Sep. 17, 2003	50	Voltage drop detection circuit (only in H version) revised.
		51	Table 15 revised.
			Timer functions, Timer control registers, Port level, and Notes 6 and 7)
		61	19 Voltage drop detection circuit (only in H version) revised.
		128	Fig.57 revised.
2.00	Feb. 24, 2004	1	FEATURES:
			• Minimum instruction execution time: time for One Time PROM version added.
			<ul> <li>Supply voltage of One Time PROM version revised.</li> </ul>
		4	PERFORMANCE OVERVIEW:
			Minimum instruction execution time: time for One Time PROM version added.
			Supply voltage of One Time PROM version revised.
			Power dissipation: Values only for Mask ROM version are listed.
		13	Port block diagram (6): SEG17–SEG28 eliminated.
		29	Table 9: Timer 3; Count source and Use of output signal revised.
		48	(1) Power-on reset : "(only for H version)" eliminated.
			Description revised.
			Fig.37: "(only for H version)" added to Voltage drop detection circuit.
		50	Fig.40: Note revised.
		58	ROM ORDERING METHOD revised.
		61	Note on 18 Power-on reset : revised.
		120 to 132	ELECTRICAL CHARACTERISTICS revised.
			The table is separated to Mask ROM version and One Time PROM version.
			Supply voltage and supply current revised mainly.
			Note 6 is added to VOLTAGE DTOP DETECTION CIRCUIT CHARACTERISTICS.
3.00	Jul. 09, 2004	All pages	Words standardized: On-chip oscillator
		5	Description of RESET pin revised.
		31	Fig.23: Note added.
		39	Some description revised.
		40	Fig.28: "DI" instruction added.
		46	(5) LCD power supply circuit
			<ul> <li>Internal dividing resistor revised.</li> </ul>
			Fig.34 d): "VLC3, VLC2, VLC1" added.
		47	Fig.35, Fig.36: Count revised.
		49	Fig.38: State of quartz-crystal oscillator added.
		61	Note on Power Source Voltage added.
		128	RECOMMENDED OPERATING CONDITIONS 1
			VDD (RC oscillation)
			Max.: 3.6

# **REVISION HISTORY**

# 4556 Group Data Sheet

Rev.	Date		Description
		Page	Summary
3.01	Jun.15, 2005	All pages 36 61	<ul> <li>Delete the following: "PRELIMINARY".</li> <li>Prescaler and Timer 1 count start timing and count time when operation starts,</li> <li>Timer 2 and Timer LC count start timing and count time when operation starts added.</li> <li>(13) Prescaler and Timer 1 count start timing and count time when operation starts,</li> <li>(14) Timer and Timer LC count start timing and count time when operation starts added.</li> </ul>
3.02	Dec. 22, 2006	$\begin{array}{c} 29, 33\\ 30, 31\\ 31\\ 32, 69\\ \end{array}$ $\begin{array}{c} 33\\ 34\\ 48\\ 52\\ \end{array}$ $\begin{array}{c} 54\\ 55, 73\\ 60\ to\ 63\\ 64\\ 77, 120,\\ 121\\ 93\\ 132\\ 132, 138\\ \end{array}$	Use of output signal of prescaler: LC eliminated. Fig.22, Fig.23: Note added. Fig.23: INSTCK (wrong) → INTSNC (correct) PAo: Stop (state <u>initialized</u> ) → (state <u>retained</u> ) W31 W30: Timer 3 count <u>source</u> selection bits → Timer 3 count <u>value</u> selection bits (2) Prescaler (interrupt function): PRS (wrong) → RPS (correct) (5) Timer 3 (interrupt function): Description added. Fig.37: Clock (wrong) → f(RING) (correct) Table 15 Timer 3 function (RAM back-up): O → (Note 3) Timer interrupt request flag (RAM back-up): O → (Note 3) Fig.44: Note 1 added. Table 17: Notes 2 and 3 added. NOTES ON NOISE added. © Noise and latch-up prevention: Description added. SZD: (Y) = 0 to <u>Z</u> → 0 to <u>5</u> SZD: Detailed description revised. Note 4: ( <u>power</u> current) → ( <u>supply</u> current) Pages 16 to 18, 20, 27, 54, 66: RAM back-up mode → power down mode Pages 77, 90 to 92, 116 to 119: SNZ0, SNZT1, SNZT2, SNZT3 revised. Pages 78, 109, 122, 123: WRST revised.
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