MITSUBISHI MICROCOMPUTERS

M34225M1-XXXSP/FP
M34225M2-XXXSP/FP

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M34225M1-XXXSP/FP and M34225M2-XXXSP/FP are single-chip 4-bit microcomputers which utilize CMOS technology. All are housed in a 30-pin shrink plastic molded DIP or 36-pin shrink plastic molded SOP, and contain a 9-bit timer, two 8-bit timers/event counters, an 8-bit timer, an A-D converter, and a serial I/O. The differences between the M34225M1-XXXSP and M34225M2-XXXSP are noted below.

Type name	ROM Size	RAM Size
M34225M1-XXXSP	1024words×9bits	64words×4bits
M34225M2-XXXSP	2048words×9bits	128words×4bits

The differences between M34225M1-XXXSP and M34225M1-XXXFP are the package outline and power dissipation (absolute maximum ratings).
The following explanations apply to the M34225M1-XXXSP. Specification variations for other chips are noted accordingly.

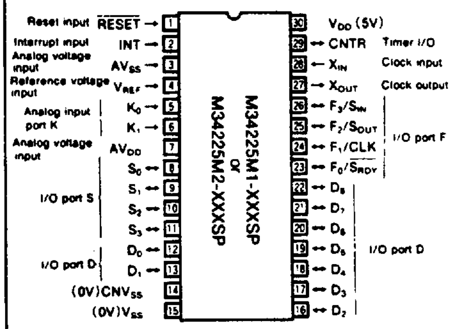
FEATURES

- Number of basic instructions 77
- Memory size
  - ROM .... 1024 words×9 bits (M34225M1-XXXSP)
  - 2048 words×9 bits (M34225M2-XXXSP)
  - RAM .... 64 words×4 bits (M34225M1-XXXSP)
  - 128 words×4 bits (M34225M2-XXXSP)
- Instruction execution time
  .... 1μs (one word instructions, at 4MHz frequency)
- Timers .... Timer 1 : 9-bit timer
  - Timer 2 : 8-bit timer/event counter (with a reload register)
  - Timer 3 : 8-bit timer/event counter (with a pulse period measurement register)
  - Timer 4 : 8-bit timer (with a reload register)
- Interrupt .... 4 types(external timer 1 or serial I/O, and timer 2), 1 level
- Subroutine nesting .... 4 levels
- Analog inputs (Port K) 2
- I/O ports (Ports D, F, S) 17
- Timer I/O port (CNTR) 1
- A-D converter .... 8-bit successive approximation
- Serial I/O .... 8-bit×1
- Built-in feed back resistance for clock

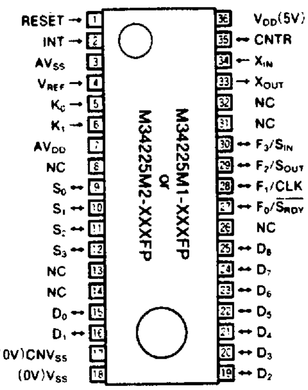
APPLICATION

Washing machine, Rice cooker, Camera, Office automation equipment, Copying machine, Medical instruments, Learning equipment, Toys

PIN CONFIGURATION (TOP VIEW)



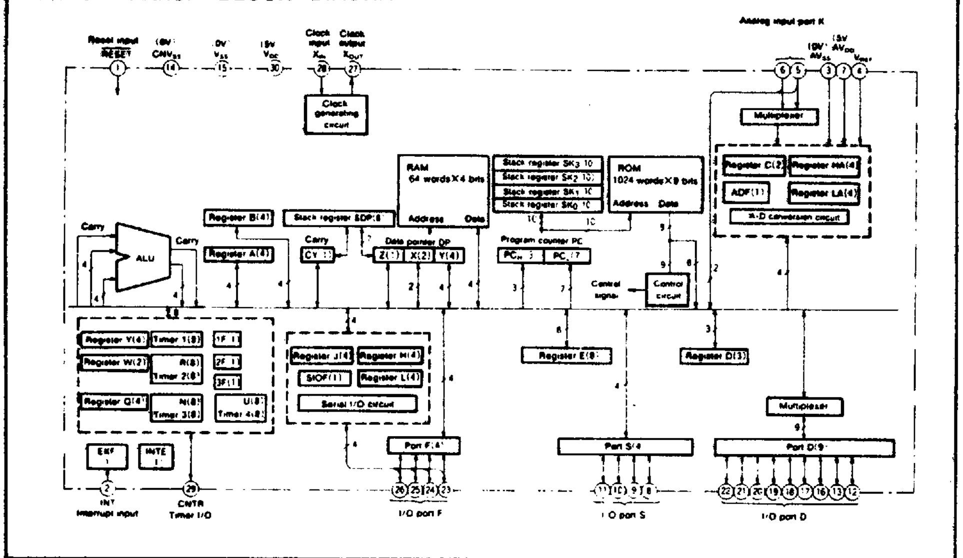
Outline 30P4B



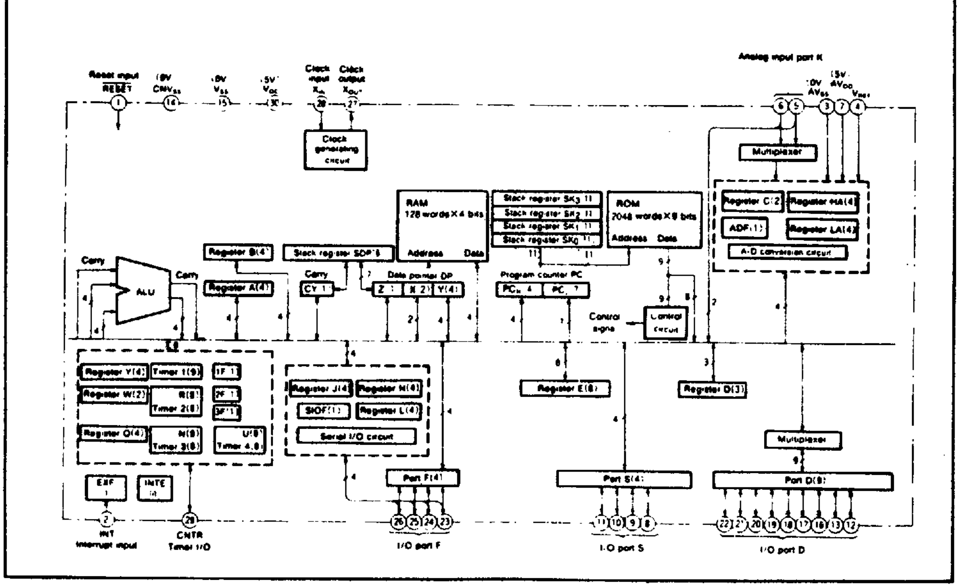
Outline 36P2R

NC : No connection

M34225M1-XXXSP BLOCK DIAGRAM



M34225M2-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M34225M1-XXXSP/FP and M34225M2-XXXSP/FP

Parameter			Functions
Number of basic instructions			77
Instruction execution time			1μs (one word instructions, at 4MHz frequency)
Clock	Clock frequency		400kHz~4MHz
	Clock generating circuit		Built-in (externally connected ceramic resonator, built-in feed back resistor)
Memory size	ROM	M34225M1-XXXSP/FP	1024words×9bits
		M34225M2-XXXSP/FP	2048words×9bits
	RAM	M34225M1-XXXSP/FP	64words×4bits
		M34225M2-XXXSP/FP	128words×4bits
Input/Output ports	D	I/O	1-bit×9
	F	I/O	4-bit×1
	S	I/O	4-bit×1
	K	Input	2 (analog input), 2-bits×1 (digital input)
	CNTR	I/O	1-bit×1
	INT	Input	1-bit×1
Input/Output characteristics	Input/Output voltage	D, S	12V (max.)
		F	10V (max.)
	Input voltage	K	5V (max.)
	Output current	D, S	12mA (avg.)
		F	5mA (avg.)
A-D converter			Built-in (absolute accuracy ±3LSB, 8-bit successive approximation)
Serial I/O			8-bit×1
Timers	Timer 1		9-bit timer, fixed division
	Timer 2		8-bit timer/event counter with an 8-bit reload register
	Timer 3		8-bit timer/event counter with a pulse period measurement register
	Timer 4		8-bit timer with an 8-bit reload register
Interrupts	Types		4types (external, timer 1 or serial I/O, and timer 2)
	Nesting		1level
Subroutine nesting			4levels (3levels, when an interrupt is used or TABPp instruction is executed)
Package	M34225M1-XXXSP, M34225M2-XXXSP		30-pin shrink plastic molded DIP
	M34225M1-XXXFP, M34225M2-XXXFP		36-pin shrink plastic molded SOP
Supply voltage			5V (typ.)
Power dissipation			17.5mW (typ.) (X_{IN} =4MHz at normal operation)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{DD}	Supply voltage		Connected to +5V power supply.
V_{SS}	Ground		Connected to 0V power supply.
$D_0 \sim D_8$	I/O port D	I/O	Each pin functions as an 1-bit unit output or input. This port is turned to an input enabled state when the output latch is set to "1". The output structure is N-channel open drain.
$F_0 \sim F_3$	I/O port F	I/O	This port functions as a 4-bit I/O. This port is turned to an input enabled state when the output latch is set to "1". When serial I/O is used, F_0, F_1, F_2, and F_3 work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. The output structure is N-channel open drain.
$K_0 \sim K_1$	Analog input port K	Input	This port functions as an input for A-D converter, and can use as a 2-bit normal input port.
$S_0 \sim S_3$	I/O port S	I/O	This port functions as a 4-bit input. This port is turned to an input enabled state when the output latch is set to "1". The output structure is N-channel open drain.
CNTR	Timer I/O	I/O	This port has an input function for the event count of timer 2 and timer 3, or an output function for the overflow signal of timer 2. Both of these functions are selected by software. The output structure is N-channel open drain.
INT	Interrupt input	Input	This is an interrupt input pin.
$\overline{RESET}$	Reset input	Input	To enter the reset state, this input pin must be kept at a "L" for more than one machine cycle.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect either a ceramic resonator (400kHz~4MHz) to these pins.
X_{OUT}	Clock output	Output	
CNV_{SS}	CNV_{SS}	Input	This is usually connected to V_{SS}, and supply "L" (0V).
AV_{DD}	Analog voltage input		This is the power supply input pin for the A-D converter.
AV_{SS}	Analog voltage input		This is the power supply input pin for the A-D converter.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.

FUNCTION BLOCK OPERATIONS

PROGRAM MEMORY (ROM)

The memory is a mask ROM of 1024 words × 9 bits, and stores user-created instruction codes. The ROM is composed of 8 pages, each page consisting of addresses from 0~127. A ROM address map is shown in Figure 1. Page 2 is a special page used for subroutine calls. A page 2 subroutine can be called from an arbitrary page by using a one-word BM instruction.

Also, by executing a $TABP_p$ instruction (p=4~7), pages 4 ~7 can be used as data area. When executing this instruction, one of the stacks is used.

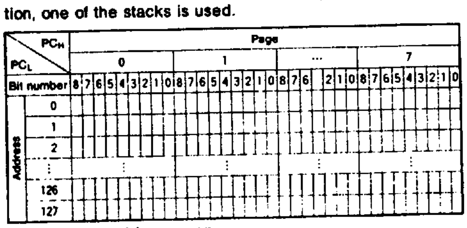


Fig.1 ROM address map

Note : The ROM of M34225M2-XXXSP is composed of 16 pages. By executing a $TABP_p$ instruction (p=12~15), pages 12~15 can be used as data area.

PROGRAM COUNTER (PC)

This counter is used to specify a ROM address, and determines the sequence in which instructions are read from the ROM. This program counter (PC) consists of 10 bits: the upper 3 bits (PC_H) stand for a ROM page, and the lower 7 bits (PC_L) stand for an address. The PC is a pure binary counter and is incremented each time an instruction is executed. However, when executing a branch instruction, subroutine call instruction or return instruction, its value takes that specified by that instruction.

The PC takes the zero address of the next page, after address 127 of that page is reached.

Note : The program counter (PC) of M34225M2-XXXSP consists of 11 bits ((PC_H)=4 bits, (PC_L) =7 bits).

STACK REGISTERS (SK_0, SK_1, SK_2, SK_3)

When a branch to a subroutine or to an interrupt handling routine is executed, these registers are used to temporarily save the contents of the PC before the branch, and until control is returned to the routine.

Since there are four 10-bit registers (SK), up to four subroutine levels can be called. If one of the levels has been used for execution of an interrupt routine or TABP p instruction, however, only 3 levels can be used for subroutines.

The address of the stack register is specified by a stack pointer.

Note : The stack register (SK) of M34225M2-XXXSP consists of four 11-bit registers.

DATA MEMORY (RAM)

This is the memory in which various processing data and control data are stored. Its size is 64 words × 4 bits (256 bits). One word of RAM is composed of 4 bits. However, bit processing can be accomplished for the entire memory area. Figure 2 shows an address map of the RAM. An address in RAM can be selected by the registers Z, X, and Y of the data pointer (DP).

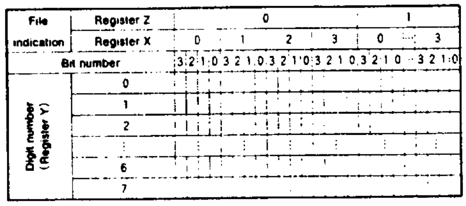


Fig.2 RAM address map

Note : The digit number in RAM of M34225M2-XXXSP is composed of 16 digits ((Y)=0~15).

DATA POINTER (DP)

This is a register to specify a RAM address and the bit location for I/O port D. The data pointer (DP) is composed of 7 bits.

Register Z, the most significant bit of the DP, specifies the RAM file group, the middle 2-bit register (X) specifies the RAM file, and the lower 4-bit register (Y) specifies the RAM digit. Register Y also specifies the bit location for I/O port D.

4-BIT ARITHMETIC AND LOGIC UNIT (ALU)

This is a 4-bit arithmetic unit, and consists of a 4-bit addition unit and its associated logical circuits. This unit performs addition, comparison, bit manipulation, and so on.

REGISTER A (ACCUMULATOR) AND CARRY FLAG (CY)

Register A is an accumulator exclusively used for computation. It is composed of 4 bits. The processing of data such as computation, transfer, exchange, transformation and I/O is executed using mainly this register. The carry flag (CY) stores the carry from the most significant bit of the ALU after executing an AMC instruction. It can also be used as an 1-bit flag.

REGISTER B AND REGISTER E

Register B is composed of 4 bits, and can be used for storage of 4-bit data or transfer of 8-bit data in conjunction with register A. Register E is composed of 8 bits, and can be used for 8-bit data transfer to or from register A and B.

REGISTER D

Register D is composed of 3 bits and in conjunction with register A, can be used to store a 7-bit ROM address. This register is used with TABP p instruction execution.

INTERRUPT

The M34225M1-XXXSP has 4 types, 1 level interrupt function. It is a vector interrupt. Table 1 shows the interrupt sources and corresponding vector interrupt addresses.

Table 1. Interrupt types and vector interrupt addresses

Interrupt types		Interrupt address
Interrupt name	Interrupting condition	
External interrupt	When a rising pulse ("L"→"H") or a falling pulse ("H"→"L") is input to the INT pin (can be selected either of those waveforms by the register Q)	Page 1, address 0
Timer 1 interrupt or Serial I/O interrupt	When the timer 1 is overflow, or receive or transmit of serial I/O is completed (can be selected either of those interrupt types by the register J)	Page 1, address 2
Timer 2 interrupt	When the timer 2 is overflow	Page 1, address 4

An interrupt is executed when one of the interrupting conditions shown in Table 1 above is satisfied, and the interrupt enable flag INTE is set to "1" (INTE = "1" when an EI instruction is executed, enables the interrupt, and INTE = "0" when a DI instruction is executed, disables the interrupt.) While INTE = "0", the interrupting condition is not changed, and an interrupt is executed only when INTE = "1". Then the priority of the interrupt is the external interrupt, timer 1 or serial I/O interrupt and timer 2 interrupt, respectively.
Either interrupting from timer 1 or serial I/O is determined by the bit 1 of the serial I/O mode register (register J).
The cause of each interrupt can be controlled by the software. If the interrupt is not executed, interrupting conditions are tested by skip instruction. Either to execute an interrupt or execute a skip instruction can be determined by bit 0~2 of the timer control register (register V).
When an interrupt handling program is executed, only one of the 4 sets of stack registers is needed to allowing the remaining 3 sets of stack registers to used for subroutine calls. After an interrupt handling program execution is started, the values of registers (such as register A or B) used in the interrupt handling program need to be saved by the program, and restored with an RTI instruction before returning to the main program. The data pointer (Z, X and Y) and carry flag however, are automatically saved and restored.
When an interrupt is executed, the internal state of the microcomputer enters the state described below:

(1) Program counter
The vector interrupt address, shown in Table 1, is set after the next (main program) instruction address is saved in one of the stack registers.

(2) Interrupt enable flag (INTE)
The INTE flag is reset to the interrupt disable state.

(3) Skip flag
The skip flag enables the determination of whether to skip when a skip instruction (or a subsequent skip instruction) is encountered. This skip flag can access the stack so when an interrupt occurs the flag is automatically saved into the stack and its skip decision condition is retained.

TIMER/EVENT COUNTER

The timer/event counter can function as four counters (timers). As shown in Figure 4, it is composed of timer 1, timer 1 interrupt request flag (1F), timer 2, timer 2 reload register (register R), timer 2 interrupt request flag (2F), timer 3, timer 3 overflow flag (3F), pulse period measurement register (register N), timer 4, timer 4 reload register (register U), timer I/O port, and timer control registers (registers V, W and Q).
The two timers (timers 1, 2, 3 and 4) are controlled by the timer control register.

(1) Timer 1
This is a 9-bit counter, and sets the timer 1 interrupt request flag (1F) every time the machine cycle count (500kHz for 2MHz clock frequency) reaches 500 or 20.
The reset and/or operation start and/or counting of the timer is controlled by the timer control register.

(2) Timer 2
Timer 2 is an 8-bit binary down counter, which has the timer 2 reload register (register R). The values of timer 2 and register R can be set by executing a T2AB instruction.
Also, the value of timer 2 can be read using a TAB2 instruction.
The start/stop of the counter and the selection of the count sources (the clock oscillating frequency divided by 4, the overflow signal from timer 1, and an external signal from the CNTR pin) can be controlled by the timer control register (W). Should it overflow, the timer 2 interrupt request flag (2F) is set and timer 2 obtains a value from the reload register (R) (auto-reload function) in order to continue counting.

(3) Timer 3
Timer 3 is an 8-bit binary down counter, which has the pulse period measurements register (register N). Timer 3 is set to FF_{16} when data is set to timer 4, and it counts the overflow signal from timer 4 or the external signal. The count source is determined by the timer control register (Q). Should it overflow, the timer 3 overflow flag (3F) is set and timer 3 is set to FF_{16} in order to continue counting.
The pulse period measurement register (register N)

latches the contents of timer 3 when the external interrupt request flag is set ("0" to "1"). The contents of register N can be read by using a TAB3 instruction.

(4) Timer 4
Timer 4 is an 8-bit binary down counter, which has a reload register (register U). The values of timer 4 and register U can be set by executing a T4AB instruction, and counts the oscillating frequency divided by four. When it overflows, timer 4 is automatically reloaded from register U and continues counting.

(5) Timer I/O (CNTR pin)
This is normally an input pin which is selected as the count source of timer 2 and timer 3 by the timer control register, otherwise this becomes an output pin for a 1/2 cycle of the timer 2 overflows.
Levels of these ports ("H" or "L") can be tested by execution of SNZC instruction.

(6) Timer 1 interrupt request flag (1F)
Timer 2 interrupt request flag (2F)
The timer 1 interrupt request flag (1F) is set every time timer 1 count reaches 500 or 20, and the timer 2 interrupt request flag (2F) is set every time timer 2 overflows. These flags can be tested by an interrupt or execution of skip instruction (SNZ1 or SNZ2). Whether to execute an interrupt or execute a skip instruction can be determined by the timer control register. Each of these tiemrs interrupt request flags (1F and 2F) can be reset by an interrupt or execution of a skip instrucrtion.

(7) Timer 3 overflow flag (3F)
This flag sets every overflow of timer 3. The testing 3F flag can be determined by the execution of skip instruction (SNZ3).
The 3F flag can be reset after skip instruction is executed and the next instruction is skipped.

(8) External interrupt request flag (EXF)
External interrupt request flag is set when the interrupting conditions are satisfied. This flag is tested by the execution of interrupt or skip instruction (SNZ0). Either interrupt or skip instruction is determined by the timer control register V. This flag is reset by the execution of interrupt or skip instruction.
INT pin (interrupt input) level can also be tested by executing the skip instruction (SNZ0). Either testing INT pin levels or EXF flag is determined by the timer control register V and Q.
EXF flag cannot be reset if the skip instruction is selected for the testing of INT pin levels and is executed.

(9) Timer control registers (V, W and Q)
The timer control registers perform the above functions, and the data is transfered to these registers from register A by the TVA, TWA or TQA instruction. Figure 3 shows the structure of these registers.

(bit 3) (bit 0)

V_3 | V_2 | V_1 | V_0 Timer control register (Register V)

External interrupt enable bit (V_0)	
0	disable (SNZ0 instruction is available)
1	enable (SNZ0 instruction is unavailable)

Timer 1 interrupt enable bit (V_1)	
0	disable (SNZ1 instruction is available)
1	enable (SNZ1 instruction is unavailable)

Timer 2 interrupt enable bit (V_2)	
0	disable (SNZ2 instruction is available)
1	enable (SNZ2 instruction is unavailable)

Timer 1 count start bit (V_3)	
0	count stop (reset state)
1	count start

(bit 1) (bit 0)

W_1 | W_0 Timer control register (Register W)

Timer 2 count source selection bit		
W_1	W_0	Count source
0	0	timer 2 count stop
0	1	external clock from CNTR pin
1	0	clock oscillating frequency divided by 4
1	1	overflow signal from timer 1

(bit 3) (bit 0)

Q_3 | Q_2 | Q_1 | Q_0 Timer control register (Register Q)

External interrupt input wavefrom selection bit		
Q_1	Q_0	Input wavefrom
0	0	falling edge (SNZ0 instruction is available for "L" level of INT pin)
0	1	rising edge (SNZ0 instruction is available for "H" level of INT pin)
1	0	falling edge (SNZ0 instruction is available for condition of EXF flag)
1	1	rising edge (SNZ0 instruction is available for condition of EXF flag)

Timer 1 count step selection bit (Q_2)	
0	20 steps (count the clock oscillating frequency divided by 4)
1	500 steps (count the clock oscillating frequency divided by 4)

Timer 3 count source selection bit (Q_3)	
0	external clock from CNTR pin
1	overflow signal from timer 4

Fig.3 Structure of timer control registers (registers V, W, and Q)

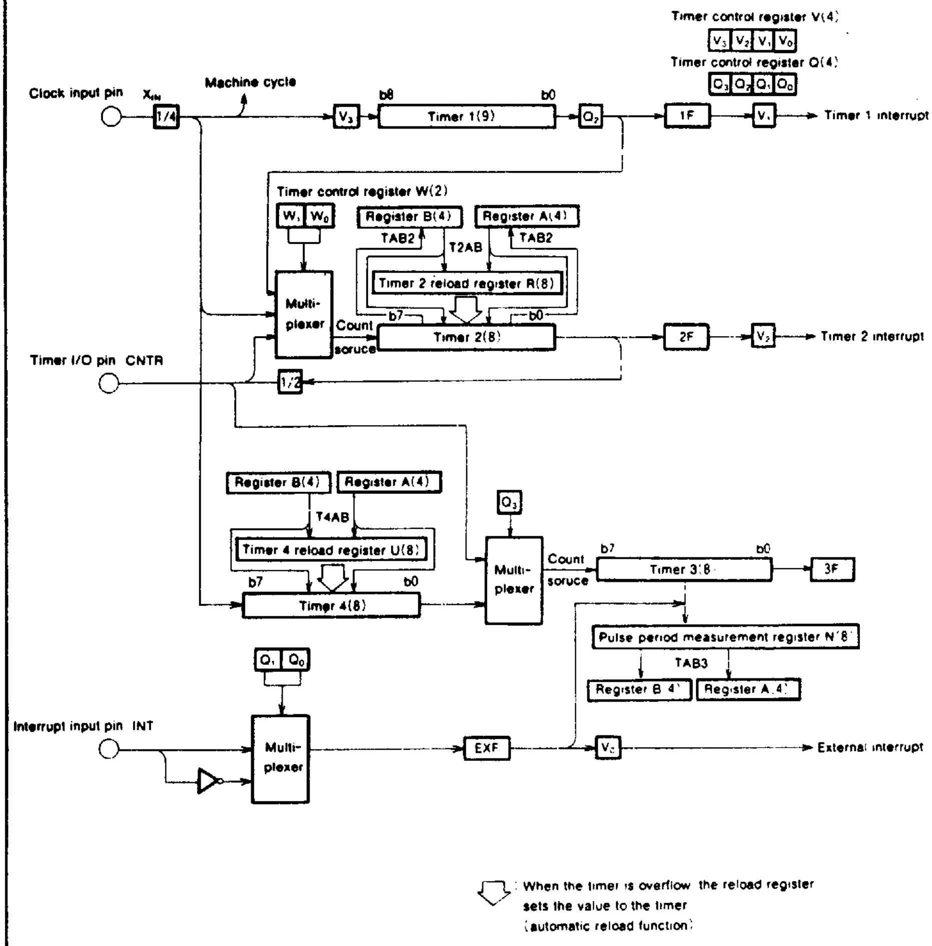


Fig.4 Block diagram of timers

SERIAL I/O

The M34225M1-XXXSP houses a clock-synchronous serial I/O which can serially receive or send 8-bit data. This serial I/O is composed of serial I/O register (H and L), serial I/O mode register (J) and a serial I/O counter. Each of the serial I/O register (H and L) are used to transmit 4-bit data. The serial I/O mode register (J) is used to select the functions denoted by its 4 bits. This serial I/O performs data transfer with the internal CPU by using the data bus, and with the external CPU by using ports $F_0 \sim F_3$. Ports $F_0 \sim F_3$ are not only I/O ports, but F_0 is also a serial I/O receive ready pin ($\overline{S_{RDY}}$), F_1 is a synchronous clock input pin (CLK), and F_2 and F_3 are serial data input/output pins (S_{OUT}, and S_{IN}). The functions of these ports can be selected by the serial I/O mode register.

(1) Serial I/O regiser (H and L)
The serial I/O register is for transforming serial data to parallel data. Each of these registers H and L consists of 4 bits The upper 4 bits of the transmitted data uses register H and the lower 4 bits, register L. The received data is stored but by bit starting from the highest bit (bit 3) of register H, and the transmitted data is transmitted bit by bit starting from the lowest bit (bit 0) of register L.

(2) Serial I/O mode register (J)
This is a 4-bit register used to select the clock source, or port function, and interrupt sources (interrupt from timer 1 or from serial I/O) with respect to the serial I/O.

(3) Serial I/O transmit/receive completion flag (SIOF)
This flag is set when the serial data transmit/receive is completed. This flag can be tested by an interrupt and the execution of a skip instruction (SZS1). Whether to enable or disable an interrupt can be decided by the serial I/O mode register.
The SIOF flag is reset, either when an interrupt is accepted or after the next instruction is skipped by the execution of the skip instruction.

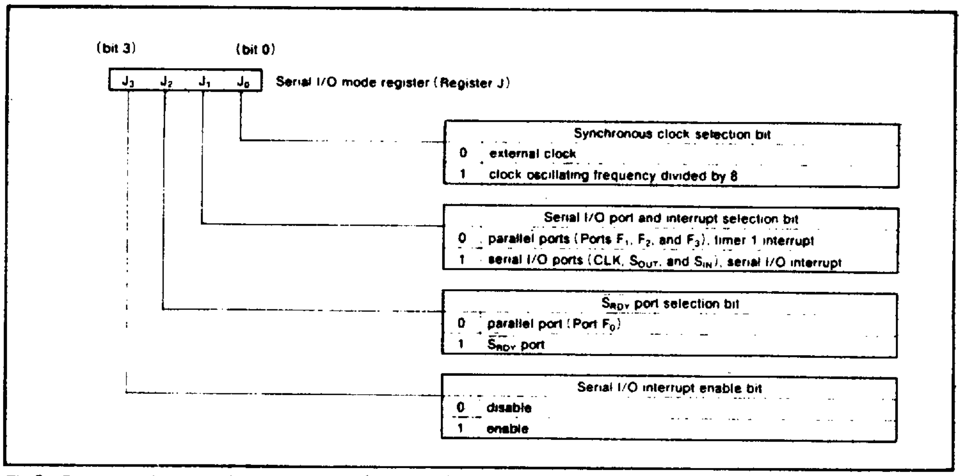


Fig.5 Structure of serial I/O mode register (register J)

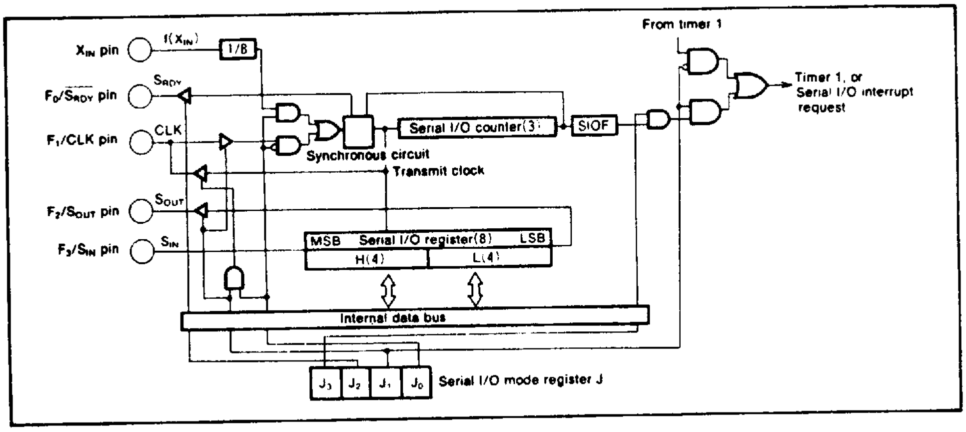


Fig.6 Block diagram of serial I/O

A-D CONVERSION

A-D conversion can be controlled such that the A-D control circuit controls those registers, etc., described below. The start and end of A-D conversion can be recognized by software. Figure 8 shows the A-D conversion circuit. The resolution of the A-D conversion is 8 bits, its analog input pins are $K_0 \sim K_1$ and its conversion speed is 36μs (when $f(X_{IN})$ =4MHz).

(1) A-D control register (C)
The A-D control register (C) is a 2-bit register. One of the two analog inputs is selected according to the combination of bits 0 and 1 of this register. Figure 7 shows the correspondence between the selected analog input pin and bit 0 or 1.

(2) The A-D conversion start instruction (ADST)
When the ADST instruction is executed, the A-D conversion begins.

(3) A-D conversion termination flag (ADF)
The A-D conversion termination flag is a 1-bit flag. When the A-D conversion is finished, this flag is set to "1".
This flag value can be tested by a skip instruction (SZAD). By executing a skip instruction, the ADF flag is set to "0".

(4) Successive approximation register (registers HA and LA)
The result of A-D conversion is stored in the succesive approximation registers, HA and LA. Registers HA and LA are each composed of 4 bits, and can send their data to register A. The upper 4 bits of the 8-bit digital data (resulting from A-D conversion) are stored in register HA, and the lower 4 bits in register LA.

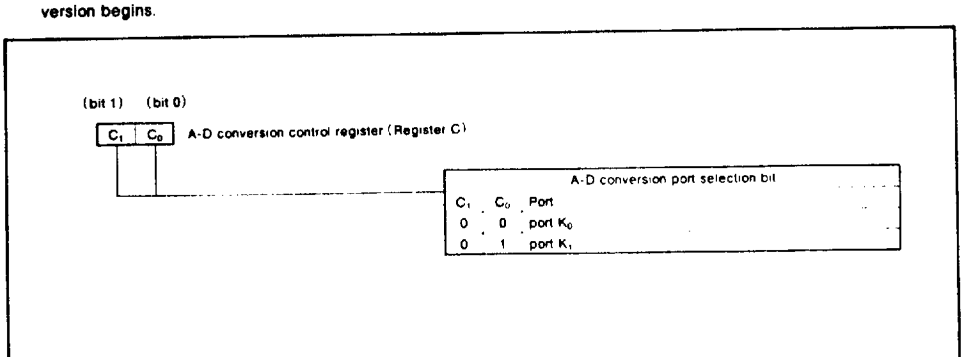


Fig.7 Structure of A-D conversion control register (register C)

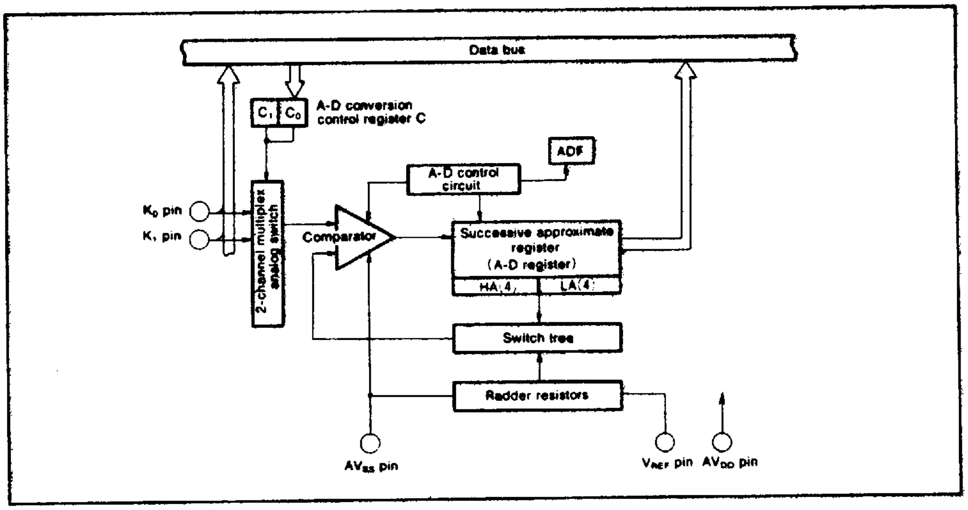


Fig.8 Block diagram of A-D conversion circuit

I/O PORT

(1) Port D (D_0~D_8)
This port performs 9-bit I/O's (SZD, SD, and RD). Its output has a latch which is capable of manipulating 1-bit, and the I/O can be carried out such that register Y of the data pointer specifies one of the D ports.
For input, the output latch of the corresponding bits must be set to "1". The instruction CLD, can set all of the port D latches to "1".
The output structure of this port is N-channel open drain.

(2) Port F (F_0~F_3)
This port has a 4-bit output (OFA) and input (IAF) function. For input, the output latch for the corresponding bits must be set to "1".
The output structure of this port is N-channel open drain.

(3) Port S (S_0~S_7)
This port has one 8-bit output (OSAB) and two 4-bit inputs (IAS).
For input, the output latch for the corresponding bits must be set to "1". The instruction CLS, can set all of the port S latches to "1".
The output structure of this port is N-channel open drain.

RESET FUNCTION

If an "L" input is supplied to the $\overline{RESET}$ pin for longer than one machine cycle, the processor is reset. After that, if the $\overline{RESET}$ pin is supplied with an "H" input, the program execution starts at address 0 of page 0.

When the processor is reset, its status is as follows:

(1) Address 0 of page 0 is input into the program counter. (PC)←0
(2) Interrupt is disabled. (INTE)←0
(the same as when a DI instruction is executed)
(3) Registers V and W are set to "0". (V)←0, and (W)←0
(4) Register Q is set to "F_{16}". (Q)←F_{16}
(5) External interrupt request flag (EXF), timer 1 interrupt request flag (1F), timer 2 interrupt request flag (2F), and timer 3 overflow flag (3F) are all reset. (EXF)=(1F)=(2F)=(3F)←0
(6) Output latches of ports D, F, S and CNTR, are all set to "1". (D)=(F)=(S)=(CNTR)←1
(7) A-D conversion termination flag (ADF) is set to "0". (ADF)←0
(8) Serial I/O send/receive completion flag (SIOF) is set to "0". (SIOF)←0
(9) Serial I/O mode register (register J) and A-D control register (register C) is set to "0". (J)←0, (C)←0

CLOCK GENERATING CIRCUIT

A clock generating circuit is built into the processor, so if a ceramic resonator is connected to the clock I/O pins a clock signals can be obtained. If the clock signals are input from an external circuit, connect the clock generating source to the X_{IN} pin and leave the X_{OUT} pin open.
Figures 9~10 show examples of the circuits.

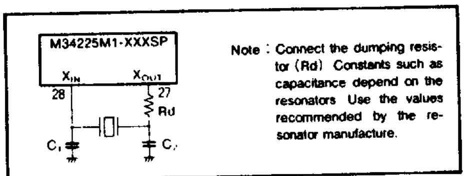


Fig.9 External ceramic resonator circuit

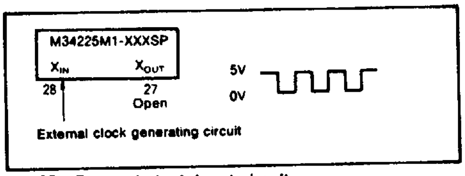


Fig.10 External clock input circuit

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) M34225M1-XXXSP/FP or M34225M2-XXXSP/FP mask confirmation sheet

(2) ROM data ·· EPROM 3 sets
(Submit three sets of EPROM's with the same data)

(3) Mark specification form for 30P4B

PRECAUTION FOR USE

① Notes on noise and latch-up

In order to avoid noise and latch-up, connect the following external circuit.

1. Connect a bypass capacitor (≈ 0.1μF) directly between the V_{DD} pin and V_{SS} pin using a heavy wire, and connect the V_{DD} pin to the AV_{DD} pin and V_{SS} pin to the AV_{SS} pin.

② Notes on INT pin

If the input polarity of the INT pin is changed by the bit 0 of the register Q (in the software program) care for the following notes:

1. Set the bit 0 of the register V to "0" (①) and the bit 1 of the register Q to "1" (②) before the input polarity of the INT pin is changed (see Figure 11).

```
    :
    LA      4      ;(0100₂) ················ ①
    TVA
    LA      3      ;(0011₂) ··········· ··· ②
    TQA
    :
```

Fig.11 Example program-1

2. Depending on the input state of the INT pin, the external interrupt request flag EXF is set when the input polarity is changed. Therefore, execute SNZ0 instruction to reset the EXF flag after the setting of the register Q.
Also, more than one instruction is need before SNZ0 instruction (③)(see Figure 12).

```
    :
    TQA          ;Set the value to register Q
    NOP          ·········································· ③
    SNZ0
    NOP
    □
    :
```

Fig.12 Example program-2

③ Notes on timer 1

When the count value of timer 1 is changed while it is counting, the first timing of timer 1 overflow just after the changing is unsettled. Therefore, change the count value while timer 1 is stopped (④)(see Figure 13).

```
    :
    LA      7
    TVA          ; Timer 1 count stop ············ ④
    LA      6
    TQA          ; Set the new value
    LA      15
    TVA          ; Timer 1 count start
    :
```

Fig.13 Example program-3

④ Notes on serial I/O

So this microcomputer continues a serial transmission as long as an external clock inputs, when selected an external clock as synchronous clock, it must be controlled externally.
(When the SST instruction is executed and the serial I/O counter counts eight clocks, the SIOF flag is set to "1".)

⑤ Note on register Y

On M34225M1-XXXSP, when the contents of register Y are 8~15, this microcomputer has no correlative memory area. At this time, do not use the reading memory instructions (AM, AMC, SEAM, SZB, TAM, XAM, XAMI, and XAMD).

INSTRUCTION CODE TABLE

D3~D0 \ D8~D4	Hexadecimal notation	0 0000 00	0 0001 01	0 0010 02	0 0011 03	0 0100 04	0 0101 05	0 0110 06	0 0111 07	0 1000 08	0 1001 09	0 1010 0A	0 1011 0B	0 1100 0C	0 1101 0D	0 1110 0E	0 1111 0F	1 0000 ~ 1 0111 10~17	1 1000 ~ 1 1111 18~1F
0000	0	NOP	BLA	SZB 0	BL	TAH	BMLA	XAM 0	BML	—	—	A 0	LA 0	LXY 0, 0	LXY 1, 0	LXY 2, 0	LXY 3, 0	BM	B
0001	1	BA	CLD	SZB 1	BL	TAL	—	XAM 1	BML	ADST	—	A 1	LA 1	LXY 0, 1	LXY 1, 1	LXY 2, 1	LXY 3, 1	BM	B
0010	2	—	CLS	SZB 2	BL	SZSI	—	XAM 2	BML	TCA	—	A 2	LA 2	LXY 0, 2	LXY 1, 2	LXY 2, 2	LXY 3, 2	BM	B
0011	3	—	INY	SZB 3	BL	SZAD	—	XAM 3	BML	TQA	—	A 3	LA 3	LXY 0, 3	LXY 1, 3	LXY 2, 3	LXY 3, 3	BM	B
0100	4	DI	RD	SZD	BL	RT	—	TAM 0	BML	OFA	** TABP 4	A 4	LA 4	LXY 0, 4	LXY 1, 4	LXY 2, 4	LXY 3, 4	BM	B
0101	5	EI	SD	SEAn	BL	RTS	IAS	TAM 1	BML	T2AB	** TABP 5	A 5	LA 5	LXY 0, 5	LXY 1, 5	LXY 2, 5	LXY 3, 5	BM	B
0110	6	RC	—	SEAM	BL	RTI	IAF	TAM 2	BML	TVA	** TABP 6	A 6	LA 6	LXY 0, 6	LXY 1, 6	LXY 2, 6	LXY 3, 6	BM	B
0111	7	SC	DEY	—	BL	—	IAK	TAM 3	BML	TWA	** TABP 7	A 7	LA 7	LXY 0, 7	LXY 1, 7	LXY 2, 7	LXY 3, 7	BM	B
1000	8	—	—	—	*BL	LZ 0	TJA	XAMI 0	*BML	TAHA	—	A 8	LA 8	LXY 0, 8	LXY 1, 8	LXY 2, 8	LXY 3, 8	BM	B
1001	9	—	T4AB	TDA	*BL	LZ 1	SST	XAMI 1	*BML	TALA	—	A 9	LA 9	LXY 0, 9	LXY 1, 9	LXY 2, 9	LXY 3, 9	BM	B
1010	A	AM	TEAB	TABE	*BL	—	THA	XAMI 2	*BML	TAB2	—	A 10	LA 10	LXY 0, 10	LXY 1, 10	LXY 2, 10	LXY 3, 10	BM	B
1011	B	AMC	OSA	—	*BL	—	TLA	XAMI 3	*BML	TAB3	—	A 11	LA 11	LXY 0, 11	LXY 1, 11	LXY 2, 11	LXY 3, 11	BM	B
1100	C	TYA	CMA	—	*BL	RB 0	SB 0	XAMD 0	*BML	SNZ1	*TABP 12	A 12	LA 12	LXY 0, 12	LXY 1, 12	LXY 2, 12	LXY 3, 12	BM	B
1101	D	—	RAR	—	*BL	RB 1	SB 1	XAMD 1	*BML	SNZ2	*TABP 13	A 13	LA 13	LXY 0, 13	LXY 1, 13	LXY 2, 13	LXY 3, 13	BM	B
1110	E	TBA	TAB	SNZ 3	*BL	RB 2	SB 2	XAMD 2	*BML	SNZC	*TABP 14	A 14	LA 14	LXY 0, 14	LXY 1, 14	LXY 2, 14	LXY 3, 14	BM	B
1111	F	—	TAY	SZC	*BL	RB 3	SB 3	XAMD 3	*BML	SNZ0	*TABP 15	A 15	LA 15	LXY 0, 15	LXY 1, 15	LXY 2, 15	LXY 3, 15	BM	B

Note 1 : The above table shows the correspondence between machine codes and machine instructions
$D_3 \sim D_0$ stands for the lower 4 bits of the machine codes, and $D_8 \sim D_4$ for the upper 5 bits of the machine codes.
Also, the hexadecimal values of those codes are listed There are two instruction types; 1-word and 2-word instructions, but in this table only the codes of the first word of each instruction is shown.
"—" : Do not use this code

2 : The second word of 2-word instructions are listed below

	The second word		
BL	1	1 a a a	a a a a
BML	1	0 a a a	a a a a
BA	1	1 a a a	a a a a
BLA	1	1 a a a	0 p p p
BMLA	1	0 a a a	0 p p p
SEA	0	1 0 1 1	n n n n
SZD	0	0 0 1 0	1 0 1 1

3 : The BL, BML, and TABP codes marked with a asterisk are not available with the M34225M1-XXXSP.
4 : The TABP codes marked with two asterisks are not available with the M34225M2-XXXSP.

SYMBOLS

The following notations are used for the following descriptions.

Symbol	Contents	Symbol	Contents
A	Register A (4-bit)	x	Hexadecimal variable
B	Register B (4-bit)	y	Hexadecimal variable
C	A-D conversion control register C (2-bit)	z	Hexadecimal variable
D	Register D (3-bit)	p	Hexadecimal variable
E	Register E (8-bit)	n	Hexadecimal constant
H	The upper 4 bits of the serial I/O register H (4-bit)	i	Hexadecimal constant
HA	The upper 4 bits of the successive approximation register HA (4-bit)	j	Hexadecimal constant
J	Serial I/O mode register J (4-bit)	$A_3\ A_2\ A_1\ A_0$	Binary representation of the register A (the same as for other registers)
L	The lower 4 bits of the serial I/O register L (4-bit)	←	Direction in which data is transferred
LA	The lower 4 bits of the successive approximation register LA (4-bit)	( )	The contents of register, memory, etc.
N	Pulse period measurement register N (8-bit)	⊻	Exclusive logical OR
Q	Timer control register Q (4-bit)	—	Negation or condition of the flag is not change after the instruction is executed
R	Timer 2 reload register (8-bit)	M(DP)	RAM address which is specified by data pointer DP
U	Timer 4 reload register U (8-bit)	a	Label to show the address of $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$
V	Timer control register V (4-bit)	p, a	Label to show the address of $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$ in the page $p_2\ p_1\ p_0$
W	Timer control register W (2-bit)	C + x	Hexadecimal value C+hexadecimal value x (the same as for other value)
X	Register X (2-bit)		
Y	Register Y (4-bit)		
Z	Register Z (1-bit)		
DP	Data pointer (7-bit) (consisting of the registers X, Y, and Z)		
PC	Program counter (10-bit)		
PC_H	The upper 3 bits of the program counter		
PC_L	The lower 7 bits of the program counter		
SK	Stack register (10-bit×4)		
SP	Stack pointer (2-bit)		
CY	Carry flag		
T1	Timer 1		
T2	Timer 2		
T3	Timer 3		
T4	Timer 4		
1F	Timer 1 interrupt request flag		
2F	Timer 2 interrupt request flag		
3F	Timer 3 overflow flag		
ADF	A-D conversion completion flag		
EXF	External interrupt request flag		
INTE	Interrupt enable flag		
INT	External interrupt signal		
SIOF	Serial I/O transmit/receive completion flag		
CNTR	Timer I/O		
D	Port D (9-bit)		
F	Port F (4-bit)		
K	Port K (2-bit)		
S	Port S (4-bit)		

Note 1 : The M34225M1-XXXSP performs a skip by ignoring the next instruction, and by not executing the instruction at the address pointed to by the contents of the program counter+2.
Therefore, the cycle number does not change, regardless of whether a skip is generated or not.
However, if TABP, RT, or RTS instruction is skipped, the cycle number becomes "1".

MACHINE INSTRUCTIONS

Type of instructions	Mnemonic	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Register to register transfers	TAB	0	0	0	0	1	1	1	1	0	0 1 E	1	1	(A)←(B)
	TBA	0	0	0	0	0	1	1	1	0	0 0 E	1	1	(B)←(A)
	TAY	0	0	0	0	1	1	1	1	1	0 1 F	1	1	(A)←(Y)
	TYA	0	0	0	0	0	1	1	0	0	0 0 C	1	1	(Y)←(A)
	TEAB	0	0	0	0	1	1	0	1	0	0 1 A	1	1	$(E_7 \sim E_4)$←(B) $(E_3 \sim E_0)$←(A)
	TDA	0	0	0	1	0	1	0	0	1	0 2 9	1	1	(D)←(A)
	TABE	0	0	0	1	0	1	0	1	0	0 2 A	1	1	(B)←$(E_7 \sim E_4)$ (A)←$(E_3 \sim E_0)$
RAM addresses	LXY x, y	0	1	1	x_1	x_0	y_3	y_2	y_1	y_0	0 C+x y	1	1	(X)← x, where x = 0 ~ 3 (Y)← y, where y = 0 ~ 15
	LZ z	0	0	1	0	0	1	0	0	z_0	0 4 8+z	1	1	(Z)← z, where z = 0, 1
	INY	0	0	0	0	1	0	0	1	1	0 1 3	1	1	(Y)←(Y)+1
	DEY	0	0	0	0	1	0	1	1	1	0 1 7	1	1	(Y)←(Y)−1
RAM to register transfers	TAM j	0	0	1	1	0	0	1	j_1	j_0	0 6 4+j	1	1	(A)←(M(DP)) (X)←(X)∀ j, where j = 0 ~ 3
	XAM j	0	0	1	1	0	0	0	j_1	j_0	0 6 j	1	1	(A)↔(M(DP)) (X)←(X)∀ j, where j = 0 ~ 3
	XAMD j	0	0	1	1	0	1	1	j_1	j_0	0 6 C+j	1	1	(A)↔(M(DP)) (X)←(X)∀ j (Y)←(Y)− 1, where j = 0 ~ 3
	XAMI j	0	0	1	1	0	1	0	j_1	j_0	0 6 8+j	1	1	(A)↔(M(DP)) (X)←(X)∀ j (Y)←(Y)+ 1, where j = 0 ~ 3
Arithmetic operations	LA n	0	1	0	1	1	n_3	n_2	n_1	n_0	0 B n	1	1	(A)← n, where n = 0 ~ 15

Skip conditions	Carry flag	Detailed description
—	—	The contents of register B are transferred to register A
—	—	The contents of register A are transferred to register B
—	—	The contents of register Y are transferred to register A
—	—	The contents of register A are transferred to register Y
—	—	The contents of register A and register B are transferred to register E
—	—	The contents of register A are transferred to register D
—	—	The contents of register E are transferred to register A and register B
continuous description	—	The immediate field value x is loaded into register X, and the immediate field value y is loaded into register Y If a continuous description of LXY instructions are written and being executed, only the first LXY instruction is executed, the following LXY instructions are all skipped
—	—	The immediate field value z is loaded to register Z
(Y) = 0	—	The contents of register Y are incremented by 1. As a result, if the contents of register Y are "0", the next instruction is skipped.
(Y) = 15	—	The contents of register Y are decremented by 1. As a result, if the contents of register Y are "15", the next instruction is skipped
—	—	After transferring the contents of M(DP) to register A, an exclusive logical OR is performed between register X and the immediate field value j, and the result is stored into register X.
—	—	After exchanging the contents of M(DP) to register A, an exclusive logical OR is performed between register X and the immediate field value j, and the result is stored into register X
(Y) = 15	—	After exchanging the contents of M(DP) to register A, an exclusive logical OR is performed between register X and the immediate field value j, and the result is stored into register X. Also, if the contents of register Y is decremented by 1 and the result is "15", then the next instruction is skipped
(Y) = 0	—	After exchanging the contents of M(DP) to register A, an exclusive logical OR is performed between register X and the immediate field value j, and the result is stored into register X Also, if the contents of register Y is incremented by 1 and the result is "0", then the next instruction is skipped
continuous description	—	The immediate field value n is loaded to register A If a continuous description of LA instructions are written and are being executed, only the first LA instruction is executed, the following LA instructions are all skipped

Type of instruction	Mnemonic	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Arithmetic operations	TABP p *Note	0	1	0	0	1	0	p_2	p_1	p_0	0 9 P	1	3	$(SK(SP)) \leftarrow (PC)$, $(SP) \leftarrow (SP)+1$ $(PC_H) \leftarrow p$ $(PC_L) \leftarrow D_2 \sim D_0\ A_3 \sim A_0$ $(B) \leftarrow (ROM(PC))_{7\sim4}$ $(A) \leftarrow (ROM(PC))_{3\sim0}$ $(SP) \leftarrow (SP)-1$, $(PC) \leftarrow (SK(SP))$ where $p=4\sim7$
	AM	0	0	0	0	0	1	0	1	0	0 0 A	1	1	$(A) \leftarrow (A)+(M(DP))$
	AMC	0	0	0	0	0	1	0	1	1	0 0 B	1	1	$(A) \leftarrow (A)+(M(DP))+(CY)$ $(CY) \leftarrow$ carry
	A n	0	1	0	1	0	n_3	n_2	n_1	n_0	0 A n	1	1	$(A) \leftarrow (A)+n$, where $n=0\sim15$
	SC	0	0	0	0	0	0	1	1	1	0 0 7	1	1	$(CY) \leftarrow 1$
	RC	0	0	0	0	0	0	1	1	0	0 0 6	1	1	$(CY) \leftarrow 0$
	SZC	0	0	0	1	0	1	1	1	1	0 2 F	1	1	$(CY)=0$?
	CMA	0	0	0	0	1	1	1	0	0	0 1 C	1	1	$(A) \leftarrow (\overline{A})$
	RAR	0	0	0	0	1	1	1	0	1	0 1 D	1	1	$\rightarrow CY \rightarrow A_3A_2A_1A_0 \rightarrow$
Bit operations	SB j	0	0	1	0	1	1	1	j_1	j_0	0 5 C+j	1	1	$(Mj(DP)) \leftarrow 1$, where $j=0\sim3$
	RB j	0	0	1	0	0	1	1	j_1	j_0	0 4 C+j	1	1	$(Mj(DP)) \leftarrow 0$, where $j=0\sim3$
	SZB j	0	0	0	1	0	0	0	j_1	j_0	0 2 j	1	1	$(Mj(DP))=0$?, where $j=0\sim3$
Comparisons	SEAM	0	0	0	1	0	0	1	1	0	0 2 6	1	1	$(A)=(M(DP))$?
	SEA n	0	0	0	1	0	0	1	0	1	0 2 5	2	2	$(A)=n$?, where $n=0\sim15$
		0	1	0	1	1	n_3	n_2	n_1	n_0	0 B n			
Timer operations	T2AB	0	1	0	0	0	0	1	0	1	0 8 5	1	1	$(R_7 \sim R_4) \leftarrow (B)$, $(T2_7 \sim T2_4) \leftarrow (B)$ $(R_3 \sim R_0) \leftarrow (A)$, $(T2_3 \sim T2_0) \leftarrow (A)$
	TAB2	0	1	0	0	0	1	0	1	0	0 8 A	1	1	$(B) \leftarrow (T2_7 \sim T2_4)$, $(A) \leftarrow (T2_3 \sim T2_0)$
	TAB3	0	1	0	0	0	1	0	1	1	0 8 B	1	1	$(B) \leftarrow (N2_7 \sim T2_4)$, $(A) \leftarrow (N2_3 \sim N2_0)$
	T4AB	0	0	0	0	1	1	0	0	1	0 1 9	1	1	$(U_7 \sim U_4) \leftarrow (B)$, $(T4_7 \sim T4_4) \leftarrow (B)$ $(U_3 \sim U_0) \leftarrow (A)$, $(T4_3 \sim T4_0) \leftarrow (A)$ $(T3_7 \sim T3_0) \leftarrow FF_{16}$
	TVA	0	1	0	0	0	0	1	1	0	0 8 6	1	1	$(V) \leftarrow (A)$

Skip conditions	Carry flag	Detailed description
—	—	Bits 7~4 of the residing at the address indicated by register A and register D (D_2 D_1 D_0 A_3 A_2 A_1 A_0), of a given page p are transferred to register B, and bits 3~0 the ROM addresses are transferred to register A. When this instruction is executed, one of stack register is used.
—	—	The contents of M(DP) are added to register A and the result is stored into register A
—	0/1	The contents of M(DP) and carry flag CY are added to register A and the result is stored into register A and into carry flag CY
overflow = 0	—	The immediate field value n is added to register A and the contents of carry flag CY are not changed as a result of this calculation. After the calculation, if the result does not overflow, the next instruction is skipped
—	1	Carry flag CY is set to 1
—	0	Carry flag CY is reset to 0.
(CY) = 0	—	If the contents of carry flag CY are "0", the next instruction is skipped
—	—	The one's complement for register A's contents are stored in register A
—	0/1	Register A, including the carry flag CY is rotated 1 bit to the right
—	—	The j-th bit of the contents of M(DP), which is the bit specified by the immediate field value j, is set to 1
—	—	The j-th bit of the contents of M(DP), which is the bit specified by the immediate field value j, is reset to 0
(Mj (DP)) = 0 where j = 0 ~ 3	—	If the j-th bit of the contents of M(DP), which is the bit specified by the immediate field value j, is "0" the next instruction is skipped
((A) = M (DP))	—	If the contents of register A are equal to the contents of M(DP), the next instruction is skipped
(A) = n where n = 0 ~ 15	—	If the contents of register A are equal to the immediate field value n the next instruction is skipped
—	—	The contents of register A and register B are transferred to timer 2 and the reload register R
—	—	The contents of timer 2 are transferred to register A and register B
—	—	The contents of the pulse period measurement register N are transferred to register A and register B
—	—	The contents of register A and register B are transferred to timer 4 and the reload register U. And then, the contents of timer 3 are reset to "FF_{16}"
—	—	The contents of register A are transferred to the timer control register V

Parameter / Type of instructions	Mnemonic	Instruction code										Number of words	Number of cycles	Functions
		D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation			
Timer operations	TWA	0	1	0	0	0	0	1	1	1	0 8 7	1	1	$(W) \leftarrow (A)$
	TOA	0	1	0	0	0	0	0	1	1	0 8 3	1	1	$(Q) \leftarrow (A)$
	SNZ 1	0	1	0	0	0	1	1	0	0	0 8 C	1	1	$(1F) = 1$?, After skip, $(1F) \leftarrow 0$
	SNZ 2	0	1	0	0	0	1	1	0	1	0 8 D	1	1	$(2F) = 1$?, After skip, $(2F) \leftarrow 0$
	SNZ 3	0	0	0	1	0	1	1	1	0	0 2 E	1	1	$(3F) = 1$?, After skip, $(3F) \leftarrow 0$
Branch operations	B a	1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 8+a a	1	1	$(PC_L) \leftarrow a_6 \sim a_0$
	BL p, a *Note	0	0	0	1	1	0	p_2	p_1	p_0	0 3 p	2	2	$(PC_H) \leftarrow p$
		1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 8+a a			$(PC_L) \leftarrow a_6 \sim a_0$
	BA a	0	0	0	0	0	0	0	0	1	0 0 1	2	2	$(PC_L) \leftarrow a_6 \sim a_4\ A_3 \sim A_0$
		1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 8+a a			
	BLA p, a *Note	0	0	0	0	1	0	0	0	0	0 1 0	2	2	$(PC_H) \leftarrow p$
		1	1	a_6	a_5	a_4	0	p_2	p_1	p_0	1 8+a p			$(PC_L) \leftarrow a_6 \sim a_4\ A_3 \sim A_0$
Subroutine call operations	BM a	1	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 a a	1	1	$(SK(SP)) \leftarrow (PC)$, $(SP) \leftarrow (SP)+1$ $(PC_H) \leftarrow 2$, $(PC_L) \leftarrow a_6 \sim a_0$
	BML p, a *Note	0	0	1	1	1	0	p_2	p_1	p_0	0 7 p	2	2	$(SK(SP)) \leftarrow (PC)$, $(SP) \leftarrow (SP)+1$
		1	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 a a			$(PC_H) \leftarrow p$, $(PC_L) \leftarrow a_6 \sim a_0$
	BMLA p, a *Note	0	0	1	0	1	0	0	0	0	0 5 0	2	2	$(SK(SP)) \leftarrow (PC)$, $(SP) \leftarrow (SP)+1$
		1	0	a_6	a_5	a_4	0	p_2	p_1	p_0	1 a p			$(PC_H) \leftarrow p$, $(PC_L) \leftarrow a_6 \sim a_4\ A_3 \sim A_0$
Return operations	RTI	0	0	1	0	0	0	1	1	0	0 4 6	1	1	$(SP) \leftarrow (SP)-1$, $(PC) \leftarrow (SK(SP))$
	RT	0	0	1	0	0	0	1	0	0	0 4 4	1	2	$(SP) \leftarrow (SP)-1$, $(PC) \leftarrow (SK(SP))$
	RTS	0	0	1	0	0	0	1	0	1	0 4 5	1	2	$(SP) \leftarrow (SP)-1$, $(PC) \leftarrow (SK(SP))$

Skip conditions	Carry flag	Detailed description
–	–	The contents of register A are transferred to the timer control register W.
–	–	The contents of register A are transferred to the timer control register Q.
(1F)=1	–	If 1F flag is "1", the next instruction is skipped. After skip, 1F flag is reset (0).
(2F)=1	–	If 2F flag is "1", the next instruction is skipped. After skip, 2F flag is reset (0).
(3F)=1	–	If 3F flag is "1", the next instruction is skipped. After skip, 3F flag is reset (0).
–	–	Branch within a page: a branch is made to the address a of the current page.
–	–	Branch out of a page: a branch is made to the address a of page p.
–	–	Branch within a page: a branch is made to the address, a_6 a_5 a_4 A_3 A_2 A_1 A_0, which is generated by replacing the lower 4 bits of address a of the current page with the corresponding bits of register A.
–	–	Branch within a page: a branch is made to the address, a_6 a_5 a_4 A_3 A_2 A_1 A_0, which is generated by replacing the lower 4 bits of address a of page p by the corresponding bits of register A.
–	–	Subroutine call in page 2: the subroutine at address a of page 2 is called.
–	–	Subroutine call: the subroutine at address a of page p is called.
–	–	Subroutine call: the subroutine at address, a_6 a_5 a_4 A_3 A_2 A_1 A_0, which is generated by replacing the lower 4 bits of address a of page p with the corresponding bits of register A.
–	–	Control is then returned from the interrupt handling routine to the main routine. Those values of data pointer (X, Y, Z), carry flag CY, skip status, and the continuous description of LA/LXY instruction NOP mode status resume their status immediately before the interrupt.
–	–	Control is then returned from the subroutine to the routine which is called the subroutine.
unconditional skip	–	Control is then returned from the subroutine to the routine which is called the subroutine, and the next instruction is unconditionally skipped.

Type of instructions \ Parameter	Mnemonic	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Input/Output operations	CLD	0	0	0	0	1	0	0	0	1	0 1 1	1	1	(D)← 1
	CLS	0	0	0	0	1	0	0	1	0	0 1 2	1	1	(S)← 1
	SD	0	0	0	0	1	0	1	0	1	0 1 5	1	1	(D(Y))← 1, where (Y)= 0 ~ 8
	RD	0	0	0	0	1	0	1	0	0	0 1 4	1	1	(D(Y))← 0, where (Y)= 0 ~ 8
	SZD	0	0	0	1	0	0	1	0	0	0 2 4	2	2	(D(Y))= 0 ?, where (Y)= 0 ~ 8
		0	0	0	1	0	1	0	1	1	0 2 B			
	OSA	0	0	0	0	1	1	0	1	1	0 1 B	1	1	(S_3~S_0)←(A)
	IAS	0	0	1	0	1	0	1	0	1	0 5 5	1	1	(A)←(S_3~S_0)
	OFA	0	1	0	0	0	0	1	0	0	0 8 4	1	1	(F)←(A)
	IAF	0	0	1	0	1	0	1	1	0	0 5 6	1	1	(A)←(F)
	IAK	0	0	1	0	1	0	1	1	1	0 5 7	1	1	(A)←(K)
	SNZC	0	1	0	0	0	1	1	1	0	0 8 E	1	1	(CNTR)= 1 ?
Interrupt operations	EI	0	0	0	0	0	0	1	0	1	0 0 5	1	1	(INTE)← 1
	DI	0	0	0	0	0	0	1	0	0	0 0 4	1	1	(INTE)← 0
	SNZ0	0	1	0	0	0	1	1	1	1	0 8 F	1	1	Q_1= 1 : (EXF)= 1 ?, After skip, (EXF)← 0
														Q_1= 0, Q_0= 1 : (INT)=H ?
														Q_1= 0, Q_0= 0 : (INT)=L ?
Serial I/O control operations	TAH	0	0	1	0	0	0	0	0	0	0 4 0	1	1	(A)←(H)
	TAL	0	0	1	0	0	0	0	0	1	0 4 1	1	1	(A)←(L)
	THA	0	0	1	0	1	1	0	1	0	0 5 A	1	1	(H)←(A)
	TLA	0	0	1	0	1	1	0	1	1	0 5 B	1	1	(L)←(A)
	TJA	0	0	1	0	1	1	0	0	0	0 5 8	1	1	(J)←(A)
	SST	0	0	1	0	1	1	0	0	1	0 5 9	1	1	(SIOF)← 0, Serial I/O start
	SNZI	0	0	1	0	0	0	0	1	0	0 4 2	1	1	(SIOF)= 1 ?, After skip, (SIOF)← 0

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Skip conditions	Carry flag	Detailed description
—	—	Port D is cleared (1)(high impedance).
—	—	Port S is cleared (1)(high impedance).
—	—	One of the ports of port D which is specified by register Y is set (1)(high impedance).
—	—	One of the ports of port D which is specified by register Y is reset (0)
(D (Y)) = 0 where (Y) = 0 ~ 8	—	If one of the ports of port D which is specified by register Y is "0", the next instruction is skipped.
—	—	The contents of register A and register B are output to the port S.
—	—	The input to the port S is transferred to register A.
—	—	The contents of register A are output to the port F
—	—	The input from the port F are transferred to register A
—		
—	—	The input from the port K are transferred to register A
(CNTR) = 1	—	If the level of the CNTR pin is "H", the next instruction is skipped
—	—	The interrupt enable flag INTE is set (1) to change the state in which an interrupt is enabled
—	—	The interrupt enable flag INTE is reset (0) to change the state in which an interrupt is disabled
(EXF) = 1 where Q_1 = 1	—	When bit 1 of register Q (Q_1) is "1" : If the EXF flag is "1", the next instruction is skipped. After the skip, the EXF flag is reset (0).
(INT) = H where Q_1 = 0, Q_0 = 1	—	When Q_1 is "0" and bit 0 of register Q (Q_0) is "1" : If the level of the INT pin is "H", the next instruction is skipped
(INT) = L where Q_1 = 0, Q_0 = 0	—	When Q_1 is "0" and Q_0 is "0" : If the level of the INT pin is "L", the next instruction is skipped
—	—	The contents of register H are transferred to register A
—	—	The contents of register L are transferred to register A
—	—	The contents of register A are transferred to register H
—	—	The contents of register A are transferred to register L.
—	—	The contents of register A are transferred to register J.
—	—	The SIOF flag is reset (0), and serial I/O is started
(SIOF) = 1	—	If the SIOF flag is "1", the next instruction is skipped. After the skip, the SIOF flag is reset (0).

Type of instructions \ Parameter	Mnemonic	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
A-D convert operations	TCA	0	1	0	0	0	0	0	1	0	0 8 2	1	1	(C)←(A)
	SZAD	0	0	1	0	0	0	0	1	1	0 4 3	1	1	(ADF)=1 ?, After skip, (ADF)←0
	TAHA	0	1	0	0	0	1	0	0	0	0 8 8	1	1	(A)←(HA)
	TALA	0	1	0	0	0	1	0	0	1	0 8 9	1	1	(A)←(LA)
	ADST	0	1	0	0	0	0	0	0	1	0 8 1	1	1	(ADF)←0, A-D conversion start
Other operations	NOP	0	0	0	0	0	0	0	0	0	0 0 0	1	1	(PC)←(PC)+1

* Note : For the M34225M2-XXXSP, the following three instructions differ from the M34225M1-XXXSP.

Type of instructions \ Parameter	Mnemonic	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Arithmetic operations	TABP p	0	1	0	0	1	p_3	p_2	p_1	p_0	0 9 p	1	3	(SK(SP))←(PC), (SP)←(SP)+1 (PC_H)←P (PC_L)← $D_2 \sim D_0$ $A_3 \sim A_0$ (B)←$(ROM(PC))_{7\sim4}$ (A)←$(ROM(PC))_{3\sim0}$ (SP)←(SP)−1, (PC)←(SK(SP)) where p=12~15
Branch operations	BL p, a	0	0	0	1	1	p_3	p_2	p_1	p_0	0 3 p	2	2	(PC_H)← p
		1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 8+a a			(PC_L)← $a_6 \sim a_0$
	BLA p, a	0	0	0	0	1	0	0	0	0	0 1 0	2	2	(PC_H)← p
		1	1	a_6	a_5	a_4	p_3	p_2	p_1	p_0	1 8+a p			(PC_L)← $a_6 \sim a_4$ $A_3 \sim A_0$
Subroutine call operations	BML p, a	0	0	1	1	1	p_3	p_2	p_1	p_0	0 7 p	2	2	(SK(SP))←(PC), (SP)←(SP)+1
		1	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 a a			(PC_H)← p, (PC_L)← $a_6 \sim a_0$
	BMLA p, a	0	0	1	0	1	0	0	0	0	0 5 0	2	2	(SK(SP))←(PC), (SP)←(SP)+1
		1	0	a_6	a_5	a_4	p_3	p_2	p_1	p_0	1 a p			(PC_H)← p, (PC_L)←$a_6 \sim a_4$ $A_3 \sim A_0$

Skip conditions	Carry flag	Detailed description
—	—	The contents of register A are transferred to register C.
(ADF) = 1	—	If the ADF flag is "1", the next instruction is skipped. After the skip, the ADF flag is reset (0).
—	—	The contents of register HA are transferred to register A.
—	—	The contents of register LA are transferred to register A.
—	—	The ADF flag is reset (0), and A-D conversion is started
—	—	No operation.

Skip conditions	Carry flag	Detailed description
—	—	Bits 7~4 of the residing at the address indicated by register A and register D, (D_2 D_1 D_0 A_3 A_2 A_1 A_0), of a given page p are transferred to register B, and bits 3~0 the ROM addresses are transferred to register A. When this instruction is executed, one of stack register is used.
—	—	Branch out of a page: a branch is made to the address a of page p.
—	—	Branch out of a page: a branch is made to the address $a_6a_5a_4A_3A_2A_1A_0$ which is generated by replacing the lower 4 bits of address a of page p by the corresponding bits of register A
—	—	Subroutine call: the subroutine at address a of page p is called.
—	—	Subroutine call: the subroutine at address, $a_6a_5a_4A_3A_2A_1A_0$, which is generated by replacing the lower 4 bits of address a of page p with the corresponding bits of register A.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{DD}	Supply voltage			−0.3〜7	V
AV_{DD}	Supply voltage for A-D			−0.3〜7	V
V_I	Input voltage X_{IN}			−0.3〜V_{DD}+0.3	V
V_I	Input voltage Ports F, INT, CNTR, RESET			−0.3〜11	V
V_I	Input voltage Ports S, D			−0.3〜13	V
V_I	Input voltage Ports K, V_{REF}			−0.3〜AV_{DD}+0.3	V
V_O	Output voltage X_{OUT}			−0.3〜V_{DD}+0.3	V
V_O	Output voltage Port F		Output transistors cut-off	−0.3〜11	V
V_O	Output voltage Ports S, D		Output transistors cut-off	−0.3〜13	V
P_d	Power dissipation	M34225M1/M2-XXXSP	T_a=25℃	1100	mW
		M34225M1/M2-XXXFP	T_a=25℃	300	mW
T_{opr}	Operating temperature			−20〜85	℃
T_{stg}	Storage temperature			−40〜125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20〜85℃)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
AV_{DD}	Supply voltage for A-D			V_{DD}		V
AV_{SS}	Supply voltage for A-D			0		V
V_{IH}	"H" input voltage Port F		0.7V_{DD}		10	V
V_{IH}	"H" input voltage Ports S, D		0.7V_{DD}		12	V
V_{IH}	"H" input voltage X_{IN}		0.7V_{DD}		V_{DD}	V
V_{IH}	"H" input voltage Port K		0.7V_{DD}		AV_{DD}	V
V_{IH}	"H" input voltage INT, CNTR		0.8V_{DD}		10	V
V_{IH}	"H" input voltage RESET		0.85V_{DD}		10	V
V_{IL}	"L" input voltage INT, CNTR		0		0.2V_{DD}	V
V_{IL}	"L" input voltage Ports F, S, K, D, X_{IN}		0		0.3V_{DD}	V
V_{IL}	"L" input voltage RESET		0		0.15V_{DD}	V
I_{OL}(peak)	"L" peak output current Ports D, S				24	mA
I_{OL}(peak)	"L" peak output current Ports F, CNTR				10	mA
I_{OL}(avg)	"L" average output current Ports D, S				12	mA
I_{OL}(avg)	"L" average output current Ports F, CNTR				5	mA
$f(X_{IN})$	Clock oscillating frequency		0.4		4	MHz

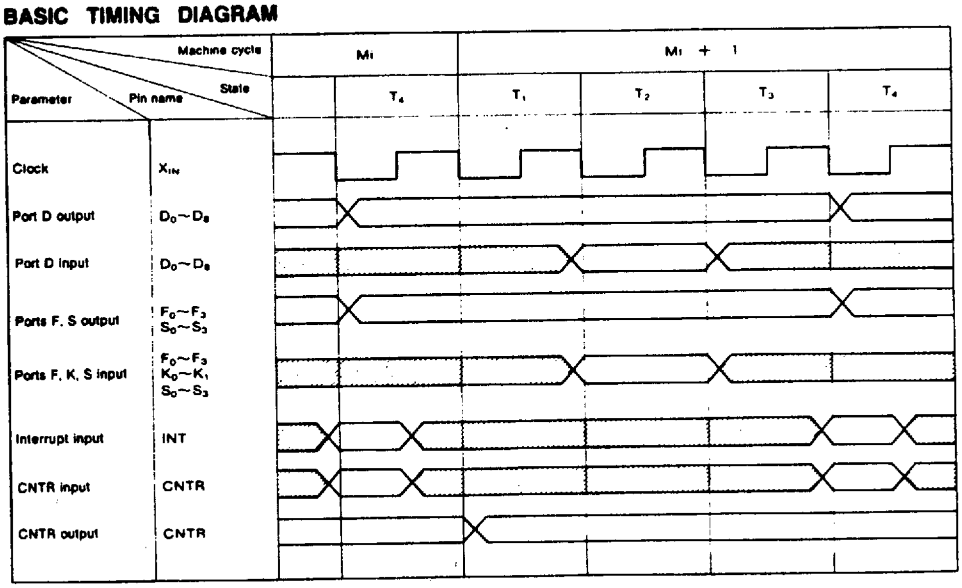
ELECTRICAL CHARACTERISTICS (T_a = −20〜85℃, V_{DD}=4.5〜5.5V)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OL}	"L" output voltage Ports F, CNTR	I_{OL}= 5 mA			2	V
V_{OL}	"L" output voltage Ports S, D	I_{OL}=12mA			2	V
I_{IH}	"H" input current Ports S, D	V_I=12V			12	μA
I_{IH}	"H" input current Port K	V_I=AV_{DD} at unselect			5	μA
I_{IL}	"L" input current Port K	V_I=0V at unselect			−5	μA
I_{IH}	"H" input current Ports F, INT, CNTR, RESET	V_I=10V			10	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{DD}			10	μA
I_{IL}	"L" input current Ports F, D, S, INT, CNTR, X_{IN}, RESET	V_I=0V			−10	μA
I_{OZH}	Output current at off Port F	V_O=10V			10	μA
I_{OZH}	Output current at off Ports D, S	V_O=12V			12	μA
C_i	Input capacitance	f = 1 MHz		7	10	pF
I_{DD}	Supply current	$f(X_{IN})$=4MHz at normal operation		3.5	7.5	mA
I_{IH}	"H" input voltage V_{REF}	V_I= 5 V			1	mA
I_{ADD}	Supply current for A-D	at A-D conversion			5	mA

A-D COVERTER CHARACTERISTICS ($V_{DD}=AV_{DD}=4.5\sim5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=-20\sim85$℃, unless otherwise noted)

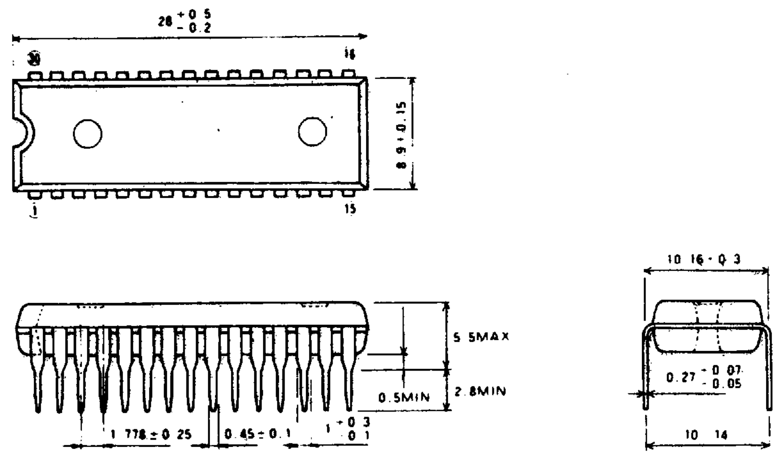
Symbol	Parameter	Test conditions	Limits Min	Limits Typ.	Limits Max	Unit
—	Resolution				8	bits
—	Absolute accuracy	$V_{DD}=AV_{DD}=V_{REF}=5.12V$			±3	LSB
R_{LADDER}	Ladder resistance value		5			kΩ
t_{CONV}	Conversion time	$f(X_{IN})=4MHz$			36	μA
V_{REF}	Reference input voltage				AV_{DD}	V
V_{IA}	Analog input voltage				V_{REF}	V

BASIC TIMING DIAGRAM



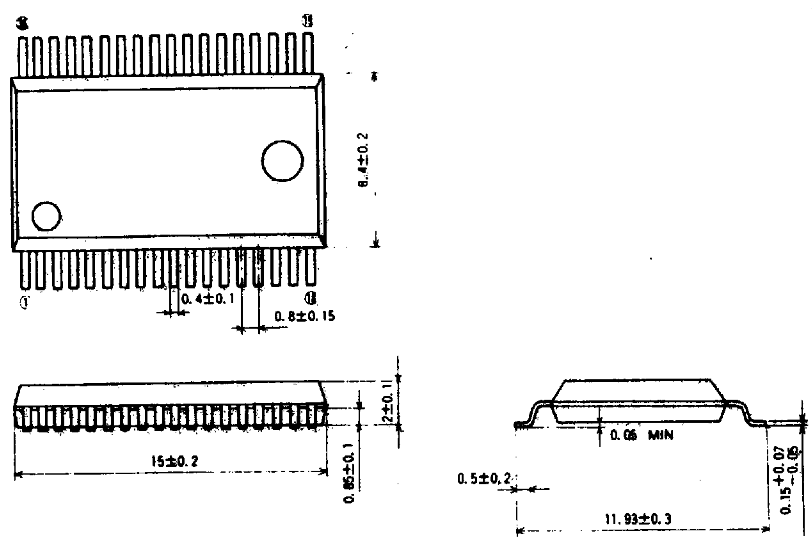
30P4B Plastic 30pin 400mil SDIP

Dimension in mm



36P2R Plastic 36pin 450mil SSOP

Dimension in mm



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