M31x Series Multiple Frequency VCXO

5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/HCMOS Output

Features:

- Multiple Output Frequencies (2, 3, or 4) - Selectable
- *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz - 1.4 GHz (LVDS/LVPECL/CML) and 10 - 150 MHz (CMOS)

Phase Lock Loop Applications:

- Where more than one selectable frequency is required for different global regions, FEC (Forward Error Correction) or selectable funcionality are required.
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

Product Definition

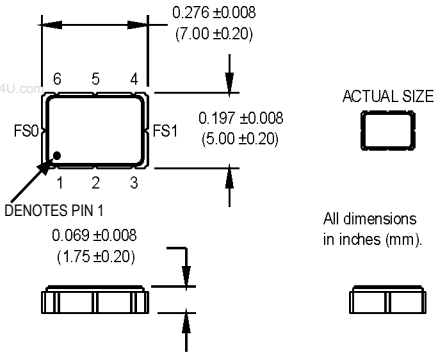
M31	**x**	**x**	**-SXXX**

Product Series

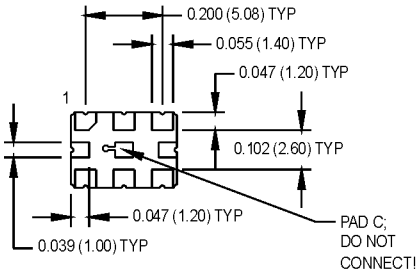
Number of Frequencies
- **2:** Two Output
- **3:** Three Output
- **4:** Four Output

Supply Voltage
- **0:** 3.3 V
- **1:** 2.5 V
- **2:** 1.8 V

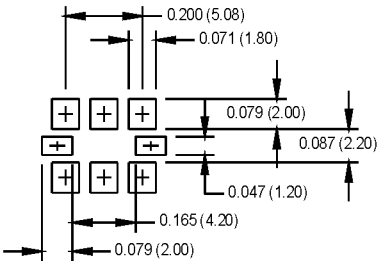
Factory Assigned to Accommodate Customer Specified Frequencies



Pad1: Voltage Control
Pad2: Enable/Disable (or N/C)
Pad3: Ground
Pad4: Output Q (LVPECL, LVDS, CML)
Pad5: Output $\overline{Q}$ (LVPECL, LVDS, CML)
Pad6: Vcc
PadA: FS0
PadB: FS1
PadC: Do not connect!



SUGGESTED SOLDER PAD LAYOUT



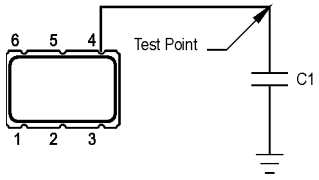
Frequency Select Truth Table		
	FS1	**FS0**
Frequency 1	High	High
Frequency 2	High	Low
Frequency 3	Low	High
Frequency 4	Low	Low

NOTE: Logic Low = 20% Vcc max.
Logic High = 80% Vcc min.

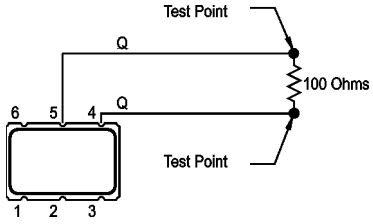
M31x Series Multiple Frequency VCXO

5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/HCMOS Output

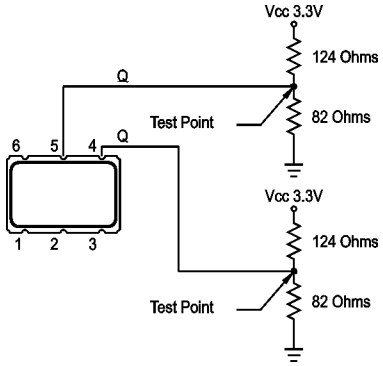
	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Electrical Specifications	Frequency Range	F	150 10		1400 125	MHz MHz	See Note 1 LVPECL/LVDS/CML HCMOS
	Operating Temperature	TA	(See ordering information)				
	Storage Temperature	Ts	-55		+125	°C	
	Frequency Stability	ΔF/F		±25		ppm	
	Aging 1st Year Thereafter (per year)		 -3 -1		 +3 +1	 ppm ppm	
	Pullability/APR		(See ordering information)				See Note 2
	Gain Transfer Function				90 135	ppm/V ppm/V	For ± 50 ppm APR For ± 100 ppm APR
	Control Voltage	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.0	V V V	@ 1.8V Vcc @ 2.5V Vcc @ 3.3V Vcc
	Linearity			1	5	%	Positive Monotonic
	Modulation Bandwidth	fm	20			KHz	-3 dB bandwidth
	Input Impedance	Zin	500k	1M		Ohms	@ DC
	Supply Voltage	Vcc	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V V V	
	Input Current	Icc			125 80	mA mA	LVPECL/LVDS/CML HCMOS
	Load						See Note 3
			50 Ohms to (Vcc –2) Vdc 100 Ohm differential load				LVPECL Waveform LVDS/CML Waveform
					15	pF	CMOS Waveform
	Symmetry (Duty Cycle)		45		55	%	@ 50% of waveform
	Output Skew				80	ps	LVPECL
					20	ps	LVDS, CML
	Differential Voltage		350	425 TBD	500	mVppd	LVDS CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc -1.02			V	LVPECL
			90% Vdd				HCMOS
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
					10% Vdd		HCMOS
	Rise/Fall Time	Tr/Tf		0.23	0.35	ns	@ 20/80% LVPECL
					6.0	ns	Ref. 10%-90% Vdd HCMOS
	Enable Function		80% Vcc min. or N/C: output active 20% Vcc max: output disables to high-Z				Output Option B
			20% Vcc max: output active 80% Vcc min: output disables to high-Z				Output Option S
	Frequency Selection		See Truth Table				
	Settling Time				10	ms	To within ± 1 ppm of frequency
	Start up Time			10		ms	
	Phase Jitter @ 622.08 MHz @ 125 MHz	 ϕJ ϕJ		0.50	 1.0	 ps RMS ps RMS	 Integrated 12 kHz – 20 MHz HCMOS (12kHz – 20 MHz)



HCMOS Load Circuit

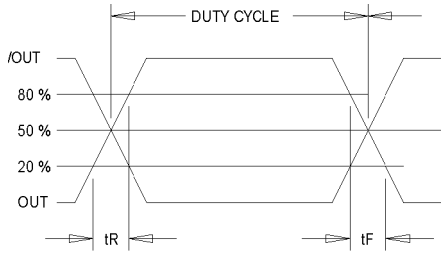


LVDS Load Circuit



3.3 V LVPECL Load Circuit

Note 1: Contact factory for exact frequency availability over 945 MHz.
Note 2: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



Output Waveform: LVDS / CML / LVPECL

MtronPTI Lead Free Solder Profile