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M30W0R6500T0

96 Mbit (64 + 32Mb, x16, Multiple Bank, Burst, Flash Memories) 1.8V Supply, Multi-Chip Package

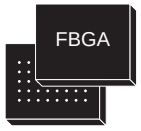
FEATURES SUMMARY

- MULTI-CHIP PACKAGE
  - 1 die of 64 Mbit (4Mb x 16) Flash Memory
  - 1 die of 32 Mbit (2Mb x 16) Flash Memory
- SUPPLY VOLTAGE
  - V_{DDF1} = V_{DDF2} = V_{DDQ} = 1.7 to 2.2V
  - V_{PP} = 12V for fast Program (optional)
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - 64Mb Device Code (Top Configuration): 8810h
  - 32Mb Device Code (Top Configuration): 8814h
- PACKAGE
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Versions

FLASH MEMORY

- SYNCHRONOUS / ASYNCHRONOUS READ
  - Synchronous Burst Read mode: 54MHz
  - Asynchronous/ Synchronous Page Read mode
  - Random Access: 70ns
- PROGRAMMING TIME
  - 8µs by Word typical for Fast Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- ARCHITECTURE
  - 64Mbit and 32Mbit Flash memories
  - Multiple Bank Memory Array: 4 Mbit Banks
  - Parameter Blocks (Top location)
- DUAL OPERATIONS
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations

Figure 1. Packages



Stacked LFBGA88 (ZA)
8 x 10mm

- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- SECURITY
  - 128 bit user programmable OTP cells
  - 64 bit unique device number
  - One parameter block permanently lockable
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

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SUMMARY DESCRIPTION

The M30W0R6500T0 is a 96 Mbit device that is composed of two separate 64-Mbit and 32-Mbit Flash memories, both with Top Boot Block architecture.

Each Flash memory can be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.7 to 2.2V V_{DD} supply for the circuitry and a 1.7 to 2.2V V_{DDQ} supply for the Input/Output pins. An optional 12V V_{PP} power supply is provided to speed up customer programming.

Two Chip Enable signals are provided to select and enable each memory. Only one memory can be selected at a time. Once selected the memory operates in the same way as the single memory devices M58WR064E and M58WR032E (refer to the respective datasheets).

The 64 Mbit Flash memory features an asymmetrical block architecture with an array of 135 blocks divided into 4 Mbit banks. It has 15 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords.

The 32 Mbit Flash memory features an asymmetrical block architecture with an array of 71 blocks divided into 4 Mbit banks. It has 7 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords.

The Multiple Bank Architecture allows Dual Operations, while programming or erasing in one bank, Read operations are possible in other banks. Only one bank at a time is allowed to be in Program or Erase mode. It is possible to perform burst reads that cross bank boundaries.

Each block can be erased separately. Erase can be suspended, in order to perform program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage V_{DD}. There are two Enhanced Factory programming commands available to speed up programming.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The M30W0R6500T0 supports synchronous burst read and asynchronous read from all blocks of each memory array; at power-up each device is configured for asynchronous read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 54MHz.

Each device features an Automatic Standby mode. When the bus is inactive during asynchronous read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value I_{DD4} and the outputs are still driven.

The M30W0R6500T0 features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power-Up.

Each memory includes a Protection Register and a Security Block to increase the protection of a system's design. Each Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by ST, and a 128 bit segment One Time Programmable (OTP) by the user. The user programmable segments can be permanently protected. The Security Blocks, parameter blocks 0, can be permanently protected by the user.

The memory is offered in a Stacked LFBGA88 (8 x 10mm, 8x10 ball array, 0.8mm pitch) package.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

The memory is supplied with all the bits erased (set to '1').

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Figure 2. Logic Diagram

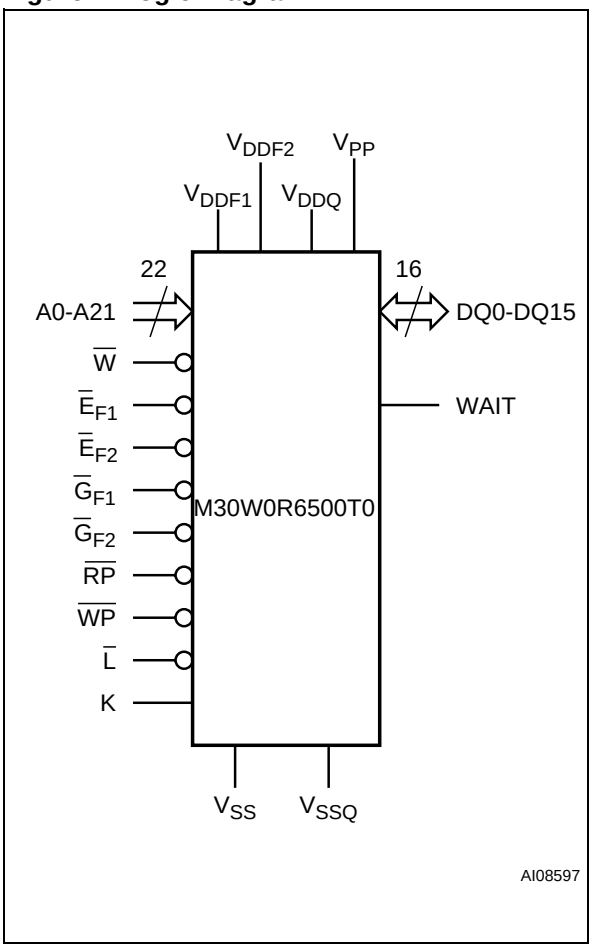

Table 1. Signal Names

A0-A21[1]	Address Inputs
DQ0-DQ15	Data Input/Outputs, Command Inputs
$\overline{E}_{F1}$	Chip Enable of 64Mb Flash Device
$\overline{E}_{F2}$	Chip Enable of 32Mb Flash Device
$\overline{G}_{F1}$	Output Enable of 64Mb Flash Device
$\overline{G}_{F2}$	Output Enable of 32Mb Flash Device
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$\overline{WP}$	Write Protect
K	Clock
$\overline{L}$	Latch Enable
WAIT	Wait
V_{DDF1}	Supply Voltage of 64Mb Flash device
V_{DDF2}	Supply Voltage of 32Mb Flash device
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
V_{SSQ}	Ground Input/Output Supply
NC	Not Connected Internally
DU	Do Not Use

Note: 1. A21 is not connected to the 32Mbit Flash Memory component.

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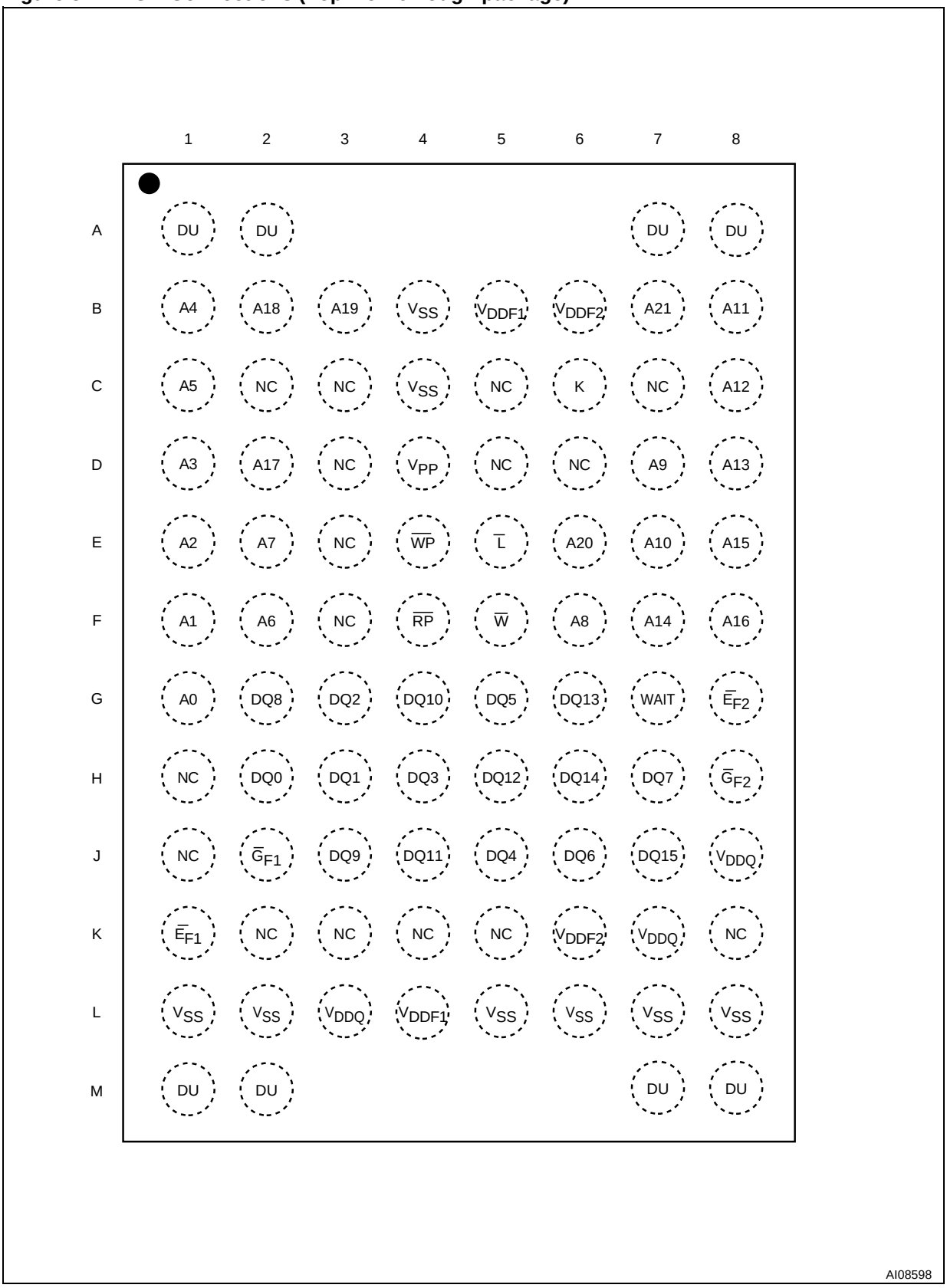
Figure 3. LFBGA Connections (Top view through package)



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SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device. Certain signals are common to both internal Flash memories, however the Chip Enable, Output Enable and V_{DD} Voltages are separate for each internal memory.

Address Inputs (A0-A21). Addresses A0-A20 are common inputs for both Flash Memory components. A21 is an input for the 64Mbit Flash Memory component only.

The Address Inputs select the cells in the selected memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Bus Write operation.

Chip Enable ($\overline{E}_{(F1/F2)}$). Each Flash memory has its own Chip Enable input that activates the memory control logic, input buffers, decoders and sense amplifiers. When a Chip Enable is at V_{IL} and Reset is at V_{IH} the corresponding Flash memory is in active mode. When a Chip Enable is at V_{IH} the corresponding Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

Only one Flash memory should be enabled at a time, which means that $\overline{E}_{F1}$ should be High whenever $\overline{E}_{F2}$ is Low and that $\overline{E}_{F2}$ should be High whenever $\overline{E}_{F1}$ is Low.

Output Enable ($\overline{G}_{(F1/F2)}$). Each Flash memory has its own Output Enable that controls data outputs during the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

Write Protect ($\overline{WP}$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked.

Reset ($\overline{RP}$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to Table 2, DC Characteristics - Currents for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to Table 7., DC Characteristics - Voltages).

Latch Enable (L). Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

Clock (K). The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is don't care during asynchronous read and in write operations.

Wait (WAIT). Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH} or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT signal is not gated by Output Enable.

$V_{DD(F1/F2)}$ Supply Voltages. V_{DDF1} and V_{DDF2} provide the power supply to the internal cores of the Flash memories. They are the main power supplies for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

V_{PP} Program Supply Voltage. V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PP} is kept in a low voltage range (0V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see Tables 6 and 7, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

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If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed.

V_{SS} Ground. V_{SS} ground is the reference for the core supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 6., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

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FUNCTIONAL DESCRIPTION

The two Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_{F1}$ and $\overline{E}_{F2}$.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on both of the Flash memories which would result in a data bus contention. Therefore it is recommended to put the one device in the high impedance state when reading the other.

Figure 4. Functional Block Diagram

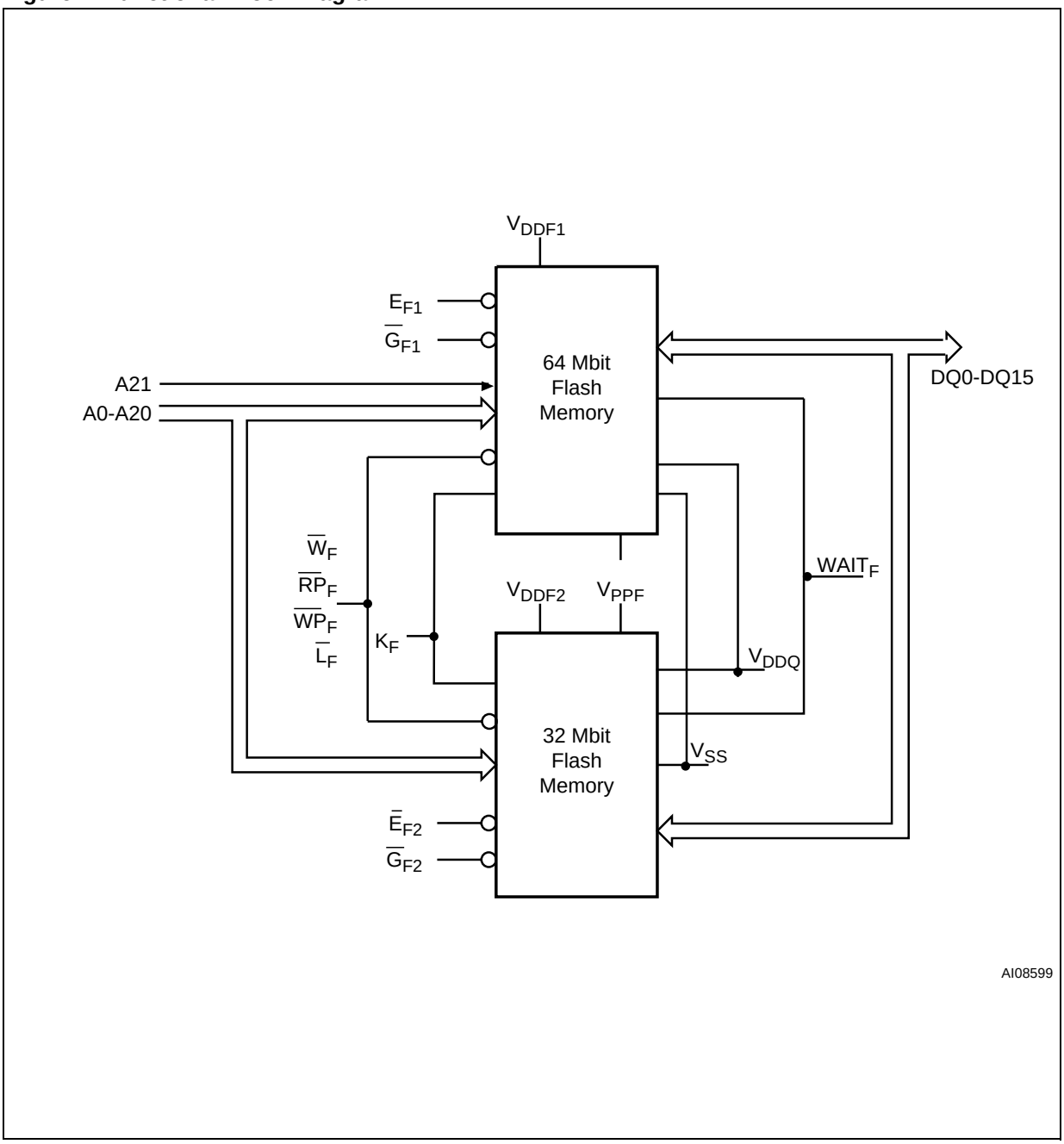

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Table 2. Main Operating modes

Operation	$\overline{E}_{F1}$	$\overline{G}_{F1}$	$\overline{E}_{F2}$	$\overline{G}_{F2}$	$\overline{W}_F$	$\overline{RP}_F$	$WAIT_F$ (3)	DQ15-DQ0
Flash1 Read	V_{IL}	V_{IL}	Flash2 must be disabled		V_{IH}	V_{IH}		Flash1 Data Out
Flash1 Write	V_{IL}	V_{IH}			V_{IL}	V_{IH}		Flash1 Data In
Flash1 Address Latch	V_{IL}	X			V_{IH}	V_{IH}		Flash1 Data Out or Hi-Z (2)
Flash1 Output Disable	V_{IL}	V_{IH}	Any mode in Flash2 is allowed.		V_{IH}	V_{IH}		Flash1 Hi-Z
Flash1 Standby	V_{IH}	X			X	V_{IH}	Hi-Z	Flash1 Hi-Z
Flash1 Reset	X	X			X	V_{IL}	Hi-Z	Flash1 Hi-Z
Flash2 Read	Flash1 must be disabled		V_{IL}	V_{IL}	V_{IH}	V_{IH}		Flash2 Data Out
Flash2 Write			V_{IL}	V_{IH}	V_{IL}	V_{IH}		Flash2 Data In
Flash2 Address Latch			V_{IL}	X	V_{IH}	V_{IH}		Flash2 Data Out or Hi-Z (2)
Flash2 Output Disable	Any mode in Flash1 is allowed.		V_{IL}	V_{IH}	V_{IH}	V_{IH}		Flash2 Hi-Z
Flash2 Standby			V_{IH}	X	X	V_{IH}	Hi-Z	Flash2 Hi-Z
Flash2 Reset			X	X	X	V_{IL}	Hi-Z	Flash2 Hi-Z

Note: 1. X = Don't care.
2. Depends on $\overline{G}_F$.
3. WAIT signal polarity is configured using the Set Configuration Register command. See M58WR064E and M58WR032E datasheets for details.

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64MBIT FLASH MEMORY COMPONENT

The M30W0R6500T0 contains a 64Mbit Flash memory. Only one Flash memory can be enabled at a time. For detailed information on how to use the device, refer to the M58WR064E datasheet which is available from the internet site *http://www.st.com* or from your local STMicroelectronics distributor.

32MBIT FLASH MEMORY COMPONENT

The M30W0R6500T0 contains a 32Mbit Flash memory. Only one Flash memory can be enabled at a time. For detailed information on how to use the device, refer to the M58WR032E datasheet which is available from the internet site *http://www.st.com* or from your local STMicroelectronics distributor.

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MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Value			Unit
	Parameter	Min	Max	
T_A	Ambient Operating Temperature	–40	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–65	155	°C
T_{LEAD}	Lead Temperature during Soldering		(1)	°C
V_{IO}	Input or Output Voltage	–0.5	V_{DDQ}+0.6	V
V_{DD}	Supply Voltage	–0.2	2.45	V
V_{DDQ}	Input/Output Supply Voltage	–0.2	3.6	V
V_{PP}	Program Voltage	–0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

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DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	Min	Max	Units
V_{DD} Supply Voltage	1.7	2.2	V
V_{DDQ} Supply Voltage	1.7	2.2	V
V_{PP} Supply Voltage (Factory environment)	11.4	12.6	V
V_{PP} Supply Voltage (Application environment)	-0.4	V_{DDQ}+0.4	V
Ambient Operating Temperature	–40	85	°C
Load Capacitance (C_L)	30		pF
Input Rise and Fall Times		5	ns
Input Pulse Voltages	0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		V

Figure 5. AC Measurement I/O Waveform

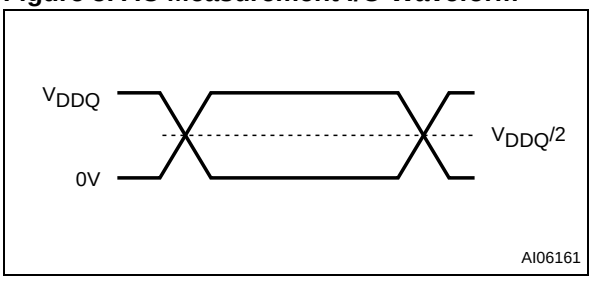

Figure 6. AC Measurement Load Circuit

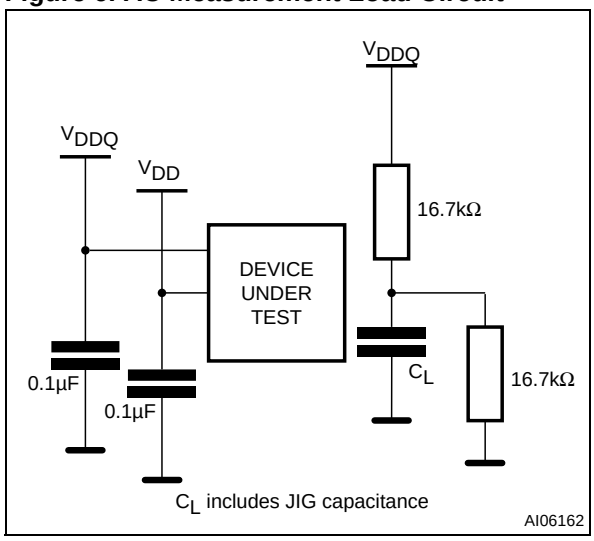

Table 5. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		15	pF

Note: Sampled only, not 100% tested.

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Table 6. DC Characteristics - Currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		3	6	mA
	Supply Current Synchronous Read (f=40MHz)	4 Word		6	13	mA
		8 Word		8	14	mA
		Continuous		6	10	mA
	Supply Current Synchronous Read (f=54MHz)	4 Word		7	16	mA
		8 Word		10	18	mA
		Continuous		13	25	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		10	50	µA
I_{DD3}	Supply Current (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		10	50	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		10	50	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
	Supply Current (Erase)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
I_{DD6} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		13	26	mA
		Program/Erase in one Bank, Synchronous Read in another Bank		16	30	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		10	50	µA
I_{PP1}(1)	V_{PP} Supply Current (Program)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	µA
	V_{PP} Supply Current (Erase)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	µA
I_{PP2}	V_{PP} Supply Current (Read)	$V_{PP} \le V_{DD}$		0.2	5	µA
I_{PP3}(1)	V_{PP} Supply Current (Standby)	$V_{PP} \le V_{DD}$		0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DD} Dual Operation current is the sum of read and program or erase currents.
3. Chip Enable, $\overline{E}$, is either $\overline{E}_{F1}$ or $\overline{E}_{F2}$ and Output Enable, $\overline{G}$, is either $\overline{G}_{F1}$ or $\overline{G}_{F2}$ depending on the memory selected.

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Table 7. DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PP} Program Voltage-Logic	Program, Erase	1	1.8	1.95	V
V_{PPH}	V_{PP} Program Voltage Factory	Program, Erase	11.4	12	12.6	V
V_{PPLK}	Program or Erase Lockout				0.9	V
V_{LKO}	V_{DD} Lock Voltage		1			V
V_{RPH}	$\overline{RP}$ pin Extended High Voltage				3.3	V

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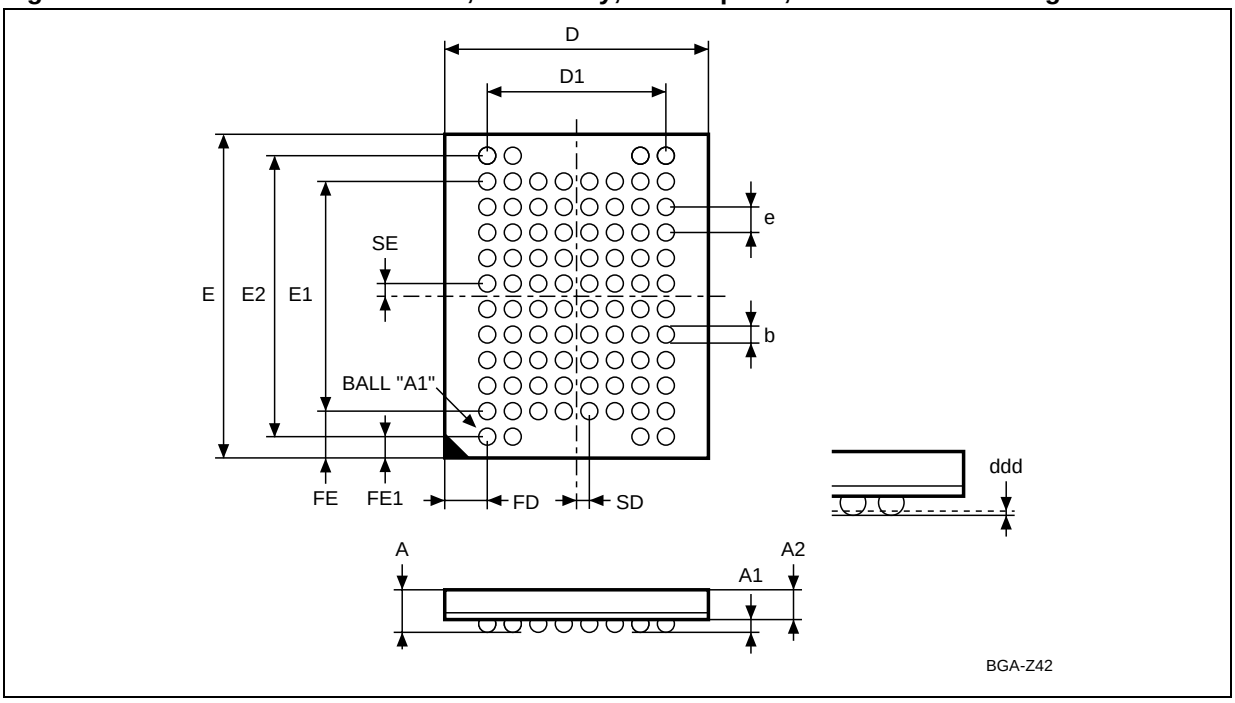
PACKAGE MECHANICAL

Figure 7. Stacked LFBGA88 8x10mm, 8x10 array, 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 8. Stacked LFBGA88 8x10mm - 8x10 ball array, 0.8mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.250			0.0098	
A2	1.000			0.0394		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600	–	–	0.2205	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200	–	–	0.2835	–	–
E2	8.800	–	–	0.3465	–	–
e	0.800	–	–	0.0315	–	–
FD	1.200	–	–	0.0472	–	–
FE	1.400	–	–	0.0551	–	–
FE1	0.600	–	–	0.0236	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

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PART NUMBERING

Table 9. Ordering Information Scheme

Example: M30 W0 R 6 5 0 0 T 0 ZAQ T

Device Type
M30 = Multi-Chip Package (Multiple Flash)

Flash 1 / Flash 2 Architecture
W = Multiple Bank, Burst mode

Flash 3 / Flash 4 Architecture
0 = No Die

Operating Voltage
R = V_{DDF1} = V_{DDF2} = V_{DDQ} = 1.7 to 2.2V

Flash 1 Density
6 = 64 Mbit

Flash 2 Density
5 = 32 Mbit

Flash 3 Density
0 = No Die

Flash 4 Density
0 = No Die

Parameter Blocks Location
T = Top Boot Block Flash Memory

Product Version
0 = 0.15µm Flash technology, 70ns speeds (both Flash memories)

Package
ZAQ = Stacked LFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-free and RoHS Package, Standard Packing
F = Lead-free and RoHS Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

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REVISION HISTORY

Table 10. Document Revision History

Date	Version	Revision Details
23-Jun-2003	1.0	First Issue
03-Dec-2004	2.0	LFBGA88 package specification updated. Table 6., DC Characteristics - Currents updated. E and F lead-free options added to Table 9., Ordering Information Scheme. LFBGA88 package fully compatible with the ST ECOPACK specification. Document status promoted from Product Preview to full Datasheet.

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