( ) Preliminary Specification
(V) Final Specification

Module	27" Color TFT-LCD
Model Name	M270DAN07.0

Customer	Date	Approved by	Date
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Record of Revision

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1 Handling Precautions

1) Since polarizer is easily damaged, do not touch or press the surface of polorizer with hand.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
14) Do not apply the same pattern for a long time, it will enhance relevant defect.
15) When this reverse-type model(PCBA on bottom side) is used as forward-type model(PCBA on top side) , AUO can not guarantee any defects of LCM .

2 General Description

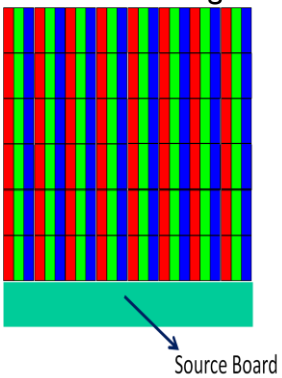
This specification applies to the 27 inch wide Color a-Si TFT-LCD Module M270DAN07.0. The display supports the QHD – 2560 (H) x 1440 (V) screen format and 16.7M colors (RGB 8-bits). The input interface is 4 port LVDS and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	684.7 (27")
Active Area	[mm]	596.736 (H) x 335.664 (V)
Pixels H x V	-	2560(x3) x 1440
Pixel Pitch	[um]	233.1 (per one triad) ×233.1
Pixel Arrangement	-	R.G.B. Vertical Stripe. Source board at bottom ***Note 2-1***
Display Mode	-	AHVA Mode (Advanced Hyper-Viewing Angle) , Normally Black
White Luminance (Center)	[cd/m^2]	350 (Typ.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	14 (Typ., GTG)
Power Consumption (LCD Module + Backligh unit)	[Watt]	15W LCD module : 3.1 (Typ.)= @ White pattern,Fv=60Hz Backlight unit : P_{BLU} (Typ.) = 11.9 @Is=60mA
Weight	[Grams]	3,250 (typ.) / 3,415(max.)
Outline Dimension	[mm]	608.8(H) × 355.3(V) × 12.8(D) Typ.
Electrical Interface	-	4 port LVDS
Support Color	-	16.7M colors (RGB 8-bits)
Surface Treatment	-	AG25% , 3H
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 8.0 Compliance

Note 2-1: The following shows the figure of pixel arrangement



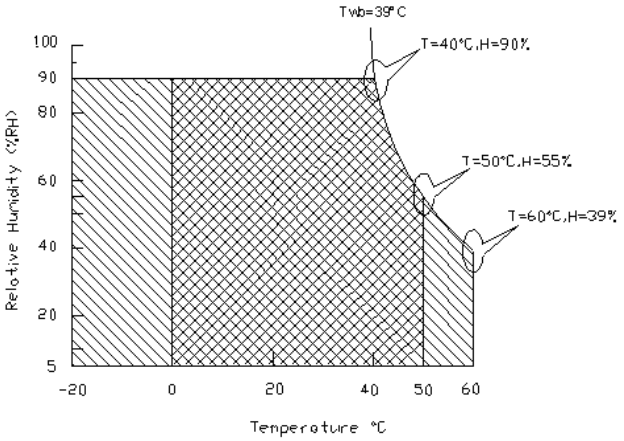
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	*Note 2-2*
TGS	Glass surface temperature (operation)	0	+65	[°C]	*Note 2-2* *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	*Note 2-2*
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-2: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation



Operating Range Storage Range +

2.3 Optical Characteristics

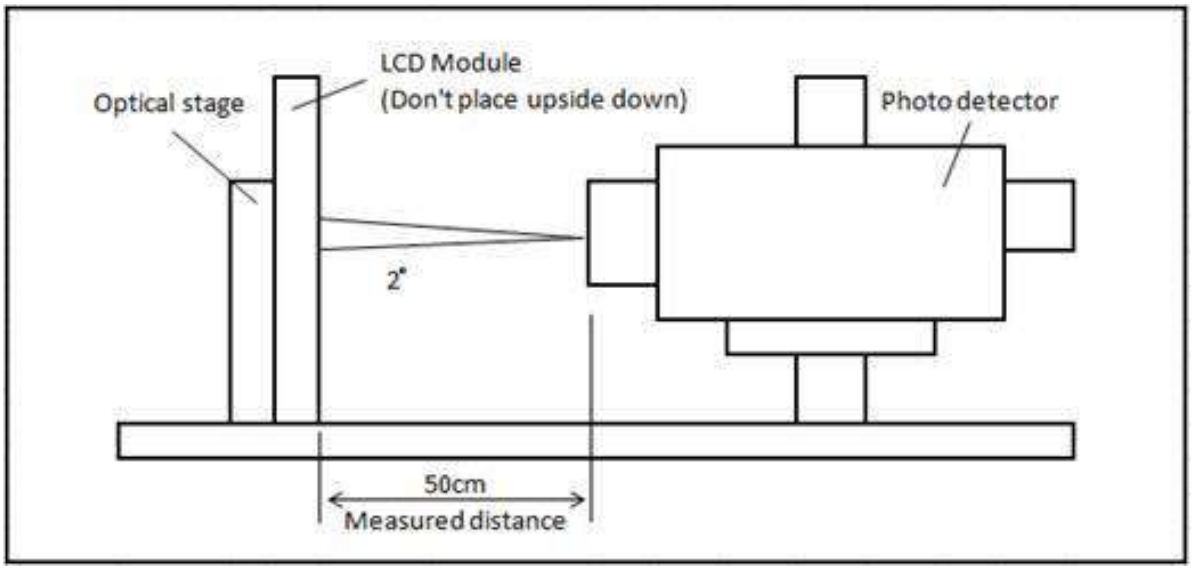
The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to ***Note 2-3***.
2. Panel Lighting time: 30 minutes
3. VDD=10.0V, Fv=60Hz,Is= 60mA,Ta=25℃

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		280	350		[cd/m2]	***Note 2-3*** *By SR-3* **Max=Peak** ***Note 2-12***
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note 2-4*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note 2-5*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	***Note 2-6*** *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	70	89	-		
Φ_L		Down	70	89	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	89	-		
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	70	89	-		
Φ_L		Down	70	89	-		
T_{GTG}	Response Time	Gray To Gray	-	14	-	[msec]	***Note 2-7*** *By TRD-100*
R_x	Color Coordinates (CIE 1931 / 1976)	Red x	0.622	0.652	0.682	-	*By SR-3*
R_y		Red y	0.308	0.338	0.368		
G_x		Green x	0.281	0.311	0.341		
G_y		Green y	0.589	0.619	0.649		
B_x		Blue x	0.115	0.145	0.175		
B_y		Blue y	0.026	0.056	0.086		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
sRGB				99		[%]	*By SR-3*

Note 2-3: Equipment setup :

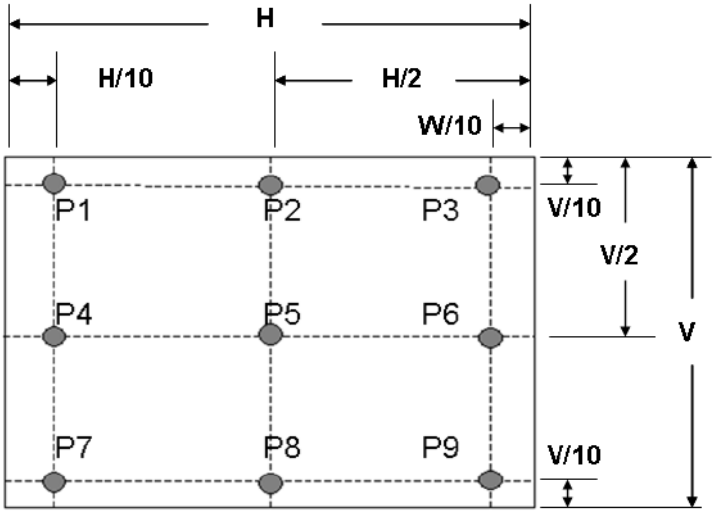


Note 2-4: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern



Note 2-5: Contrast Ratio Measurement

Definition:

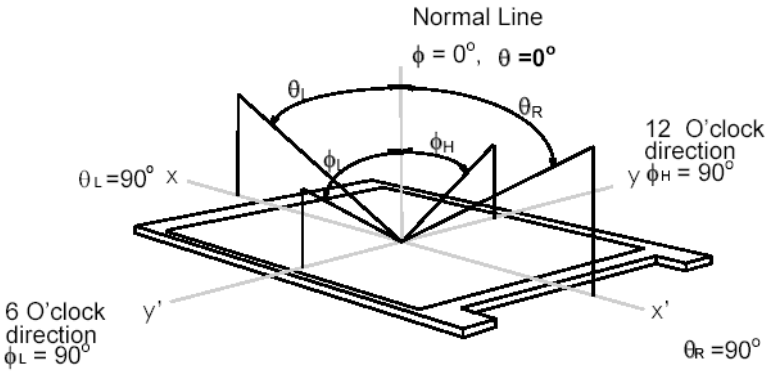
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

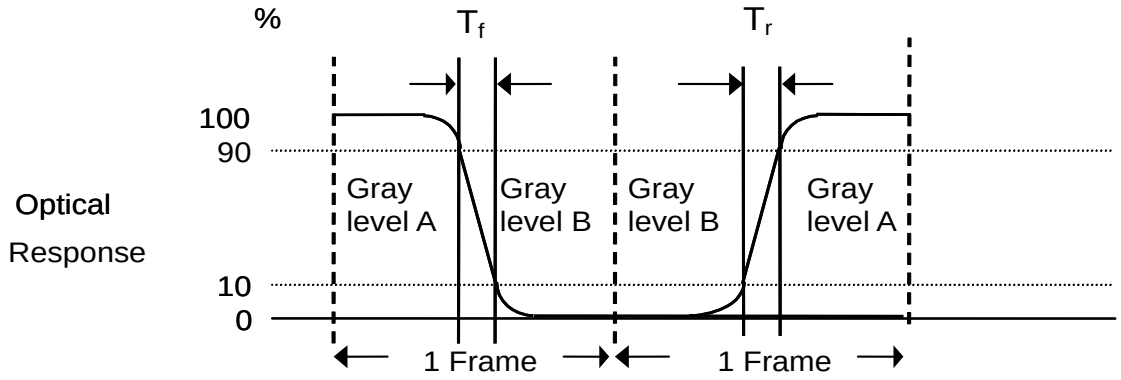
Note 2-6: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-7: Response time measurement



The output signals of photo detector are measured when the input signals are changed from “Gray level A” to “Gray level B” (falling time, TF), and from “Gray level B” to “Gray level A” (rising time, TR), respectively. The response time is interval between the 10% and 90% of optical response.
The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

2.4 Mechanical Characteristics

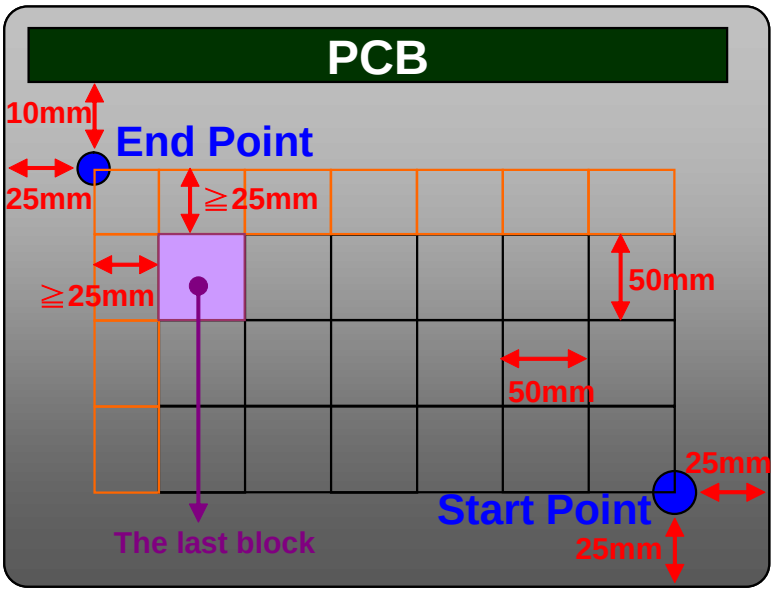
Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	*Note 2-10*

Note 2-10: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.

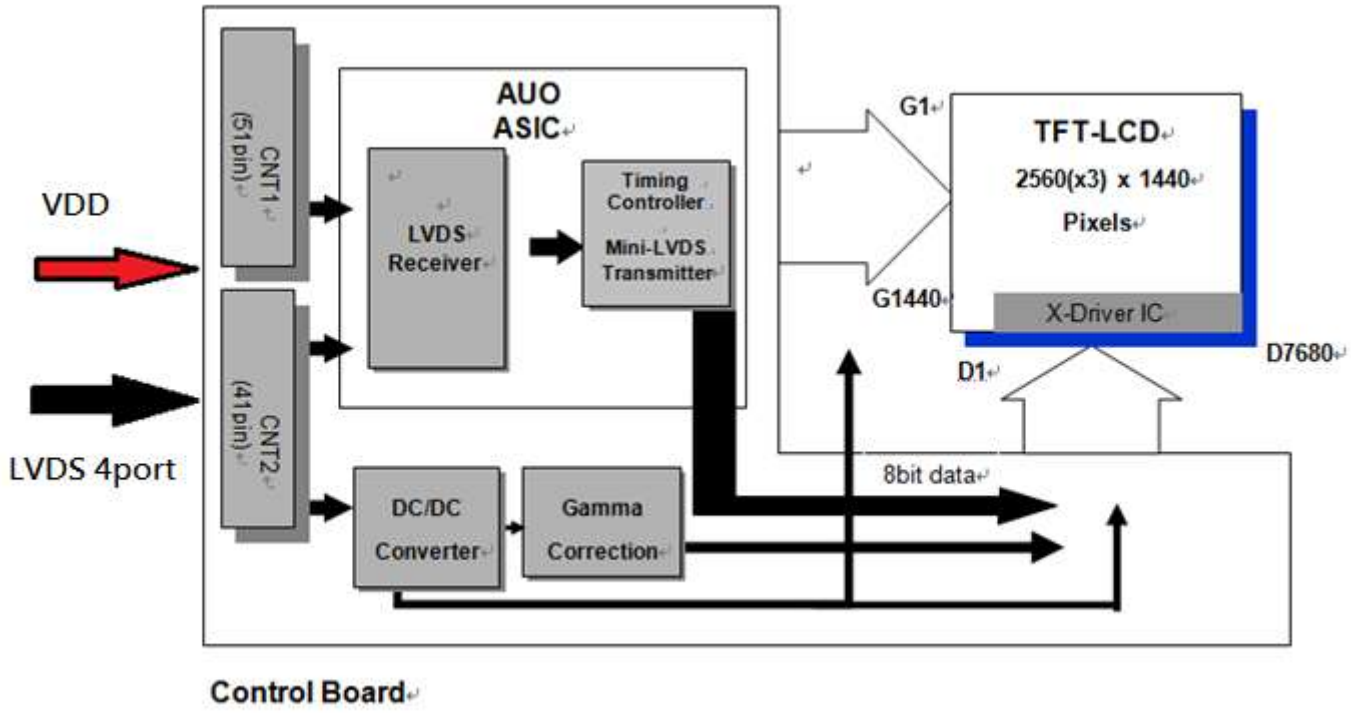


Note 2-12 : Evaluation test and mass production inspection shall be applied with LED current Is @ HDR off condition if there is not specified condition.

3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 27 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector (CNT 1)	Manufacturer	P-TWO	CHIEF LAND
	Part Number	187059-5122	115E51-0000RA-M3-R
TFT-LCD Connector (CNT 1)	Manufacturer	JAE	
	Part Number	FI-RTE51SZ-HF	
TFT-LCD Connector (CNT 2)	Manufacturer	P-TWO	CHIEF LAND
	Part Number	187060-4122	115E41-0000RA-M3-R
TFT-LCD Connector (CNT 2)	Manufacturer	JAE	
	Part Number	FI-RTE41SZ-HF	
Mating Connector (CNT 1)	Manufacturer	JAE or Compatible	
	Part Number	FI-RE51CL (Locked Type)	
Mating Connector (CNT 2)	Manufacturer	JAE or Compatible	
	Part Number	FI-RE41CL (Locked Type)	

LVDS CN1

PIN #	Symbol	Description	Remark
1	NC	No Connection (for AUO test only. Do not connect)	
2	NC	No Connection (for AUO test only. Do not connect)	
3	NC	No Connection (for AUO test only. Do not connect)	
4	NC	No Connection (for AUO test only. Do not connect)	
5	NC	No Connection (for AUO test only. Do not connect)	
6	NC	No Connection (for AUO test only. Do not connect)	
7	NC	No Connection (for AUO test only. Do not connect)	
8	NC	No Connection (for AUO test only. Do not connect)	
9	NC	No Connection (for AUO test only. Do not connect)	
10	NC	No Connection (for AUO test only. Do not connect)	
11	GND	Power Ground	
12	R1_0N	FIRST_ Negative LVDS differential data input	
13	R1_0P	FIRST_ Positive LVDS differential data input	
14	R1_1N	FIRST_ Negative LVDS differential data input	
15	R1_1P	FIRST_ Positive LVDS differential data input	
16	R1_2N	FIRST_ Negative LVDS differential data input	
17	R1_2P	FIRST_ Positive LVDS differential data input	
18	GND	Power Ground	

19	R1_CLKN	FIRST_ Negative LVDS differential clock input	
20	R1_CLKP	FIRST_ Positive LVDS differential clock input	
21	GND	Power Ground	
22	R1_3N	FIRST_ Negative LVDS differential data input	
23	R1_3P	FIRST_ Positive LVDS differential data input	
24	NC	No Connection (for AUO test only. Do not connect)	
25	NC	No Connection (for AUO test only. Do not connect)	
26	GND	Power Ground	
27	GND	Power Ground	
28	R2_0N	SECOND_ Negative LVDS differential data input	
29	R2_0P	SECOND_ Positive LVDS differential data input	
30	R2_1N	SECOND_ Negative LVDS differential data input	
31	R2_1P	SECOND_ Positive LVDS differential data input	
32	R2_2N	SECOND_ Negative LVDS differential data input	
33	R2_2P	SECOND_ Positive LVDS differential data input	
34	GND	Power Ground	
35	R2_CLKN	SECOND_ Negative LVDS differential clock input	
36	R2_CLKP	SECOND_ Positive LVDS differential clock input	
37	GND	Power Ground	
38	R2_3N	SECOND_ Negative LVDS differential data input	
39	R2_3P	SECOND_ Positive LVDS differential data input	
40	NC	No Connection (for AUO test only. Do not connect)	
41	NC	No Connection (for AUO test only. Do not connect)	
42	GND	Power Ground	
43	GND	Power Ground	
44	GND	Power Ground	
45	GND	Power Ground	
46	NC	No Connection (for AUO test only. Do not connect)	
47	NC	No Connection (for AUO test only. Do not connect)	
48	VDD	Power +10V	
49	VDD	Power +10V	
50	VDD	Power +10V	
51	VDD	Power +10V	

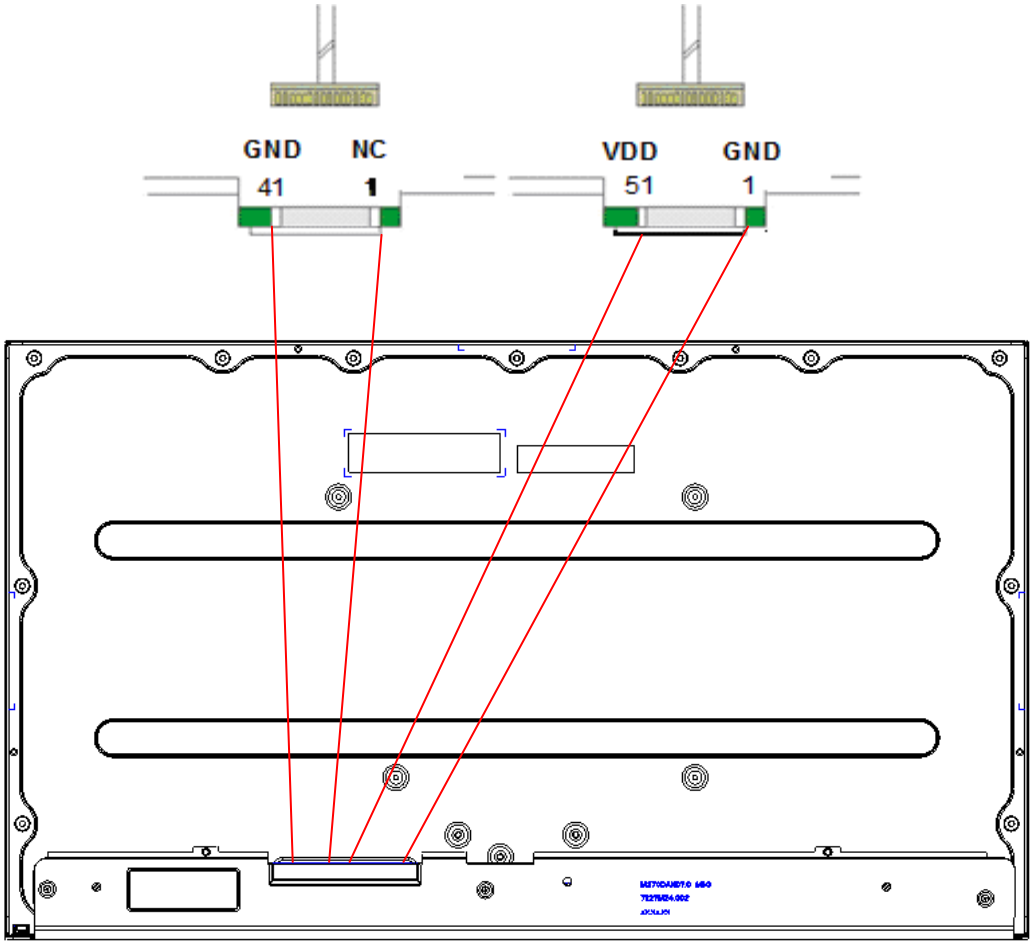
LVDS CN2

PIN #	Symbol	Description	Remark

1	NC	No Connection (for AUO test only. Do not connect)	
2	NC	No Connection (for AUO test only. Do not connect)	
3	NC	No Connection (for AUO test only. Do not connect)	
4	NC	No Connection (for AUO test only. Do not connect)	
5	NC	No Connection (for AUO test only. Do not connect)	
6	NC	No Connection (for AUO test only. Do not connect)	
7	NC	No Connection (for AUO test only. Do not connect)	
8	NC	No Connection (for AUO test only. Do not connect)	
9	GND	Power Ground	
10	R3_0N	THIRD_ Negative LVDS differential data input	
11	R3_0P	THIRD_ Positive LVDS differential data input	
12	R3_1N	THIRD_ Negative LVDS differential data input	
13	R3_1P	THIRD_ Positive LVDS differential data input	
14	R3_2N	THIRD_ Negative LVDS differential data input	
15	R3_2P	THIRD_ Positive LVDS differential data input	
16	GND	Power Ground	
17	R3_CLKN	THIRD_ Negative LVDS differential clock input	
18	R3_CLKP	THIRD_ Positive LVDS differential clock input	
19	GND	Power Ground	
20	R3_3N	THIRD_ Negative LVDS differential data input	
21	R3_3P	THIRD_ Positive LVDS differential data input	
22	NC	No Connection (for AUO test only. Do not connect)	
23	NC	No Connection (for AUO test only. Do not connect)	
24	GND	Power Ground	
25	GND	Power Ground	
26	R4_0N	FOURTH_ Negative LVDS differential data input	
27	R4_0P	FOURTH_ Positive LVDS differential data input	
28	R4_1N	FOURTH_ Negative LVDS differential data input	
29	R4_1P	FOURTH_ Positive LVDS differential data input	

30	R4_2N	FOURTH_ Negative LVDS differential data input	
31	R4_2P	FOURTH_ Positive LVDS differential data input	
32	GND	Power Ground	
33	R4_CLKN	FOURTH_ Negative LVDS differential clock input	
34	R4_CLKP	FOURTH_ Positive LVDS differential clock input	
35	GND	Power Ground	
36	R4_3N	FOURTH_ Negative LVDS differential data input	
37	R4_3P	FOURTH_ Positive LVDS differential data input	
38	NC	No Connection (for AUO test only. Do not connect)	
39	NC	No Connection (for AUO test only. Do not connect)	
40	GND	Power Ground	
41	GND	Power Ground	

3.2.2 Connector Pin Assignment



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

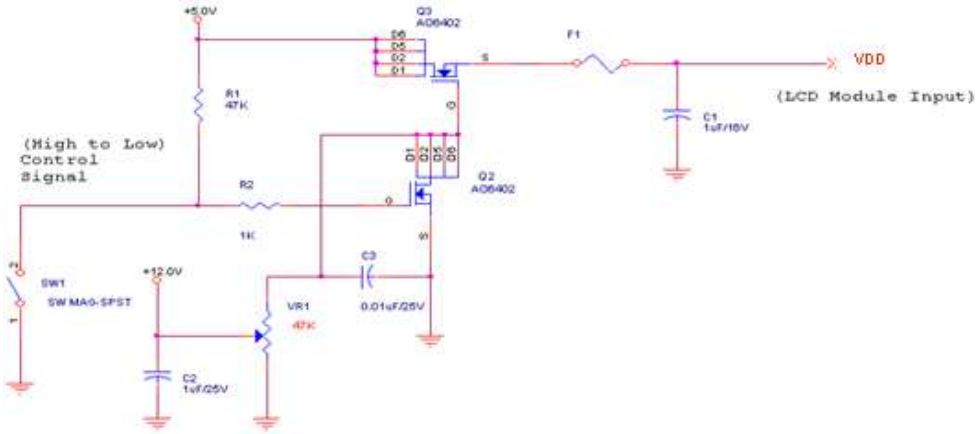
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	6.0	[Volt]	Ta=25℃

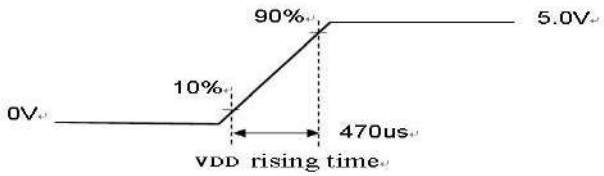
3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	9.5	10	10.5	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.31	0.73	[A]	VDD= 10.0V, White Pattern, Fv=60Hz
			0.33	0.87	[A]	VDD= 10.0V, White Pattern, Fv=75Hz
PDD	VDD Power Consumption	-	3.1	7.3	[Watt]	VDD= 10.0V, White Pattern, Fv=60Hz
			3.3	8.7	[Watt]	VDD= 10.0V, White Pattern, Fv=75Hz
IRush	Inrush Current	-		3.0	[A]	*Note 3-1*
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mV]	VDD= 10.0V, Black Pattern, Fv=75Hz

Note 3-1: Inrush Current measurement:

Test circuit:



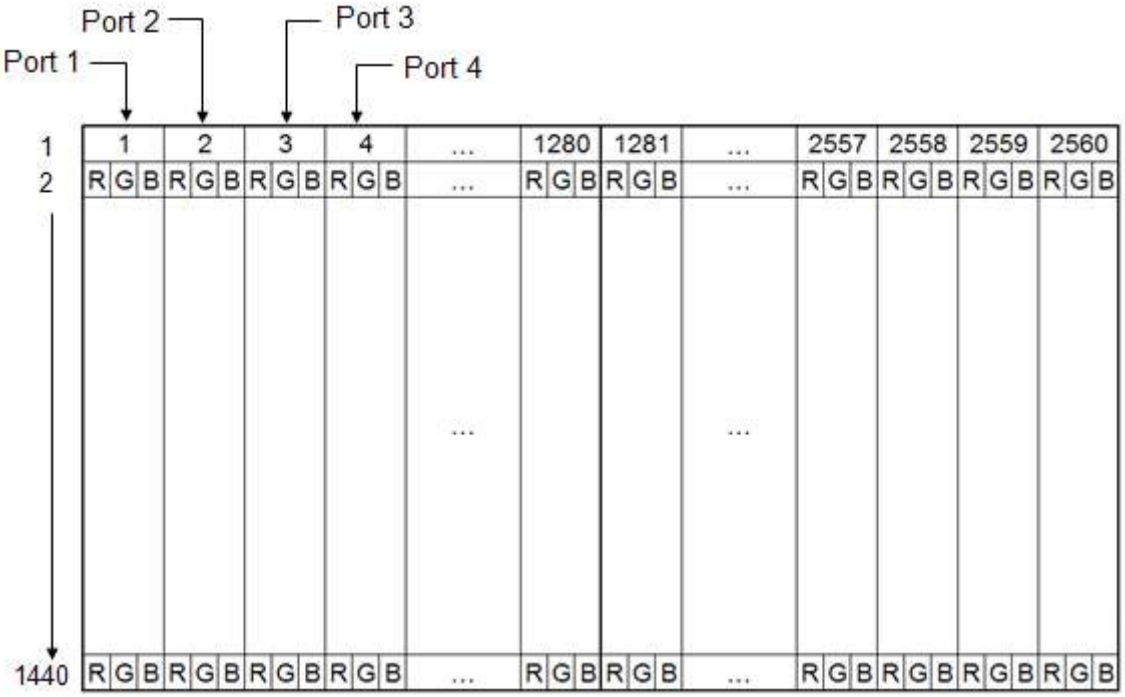


The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 1: The module use 4port-LVDS interface.

Port 1： 4N+1 (1, 5.. 2557 pixel)

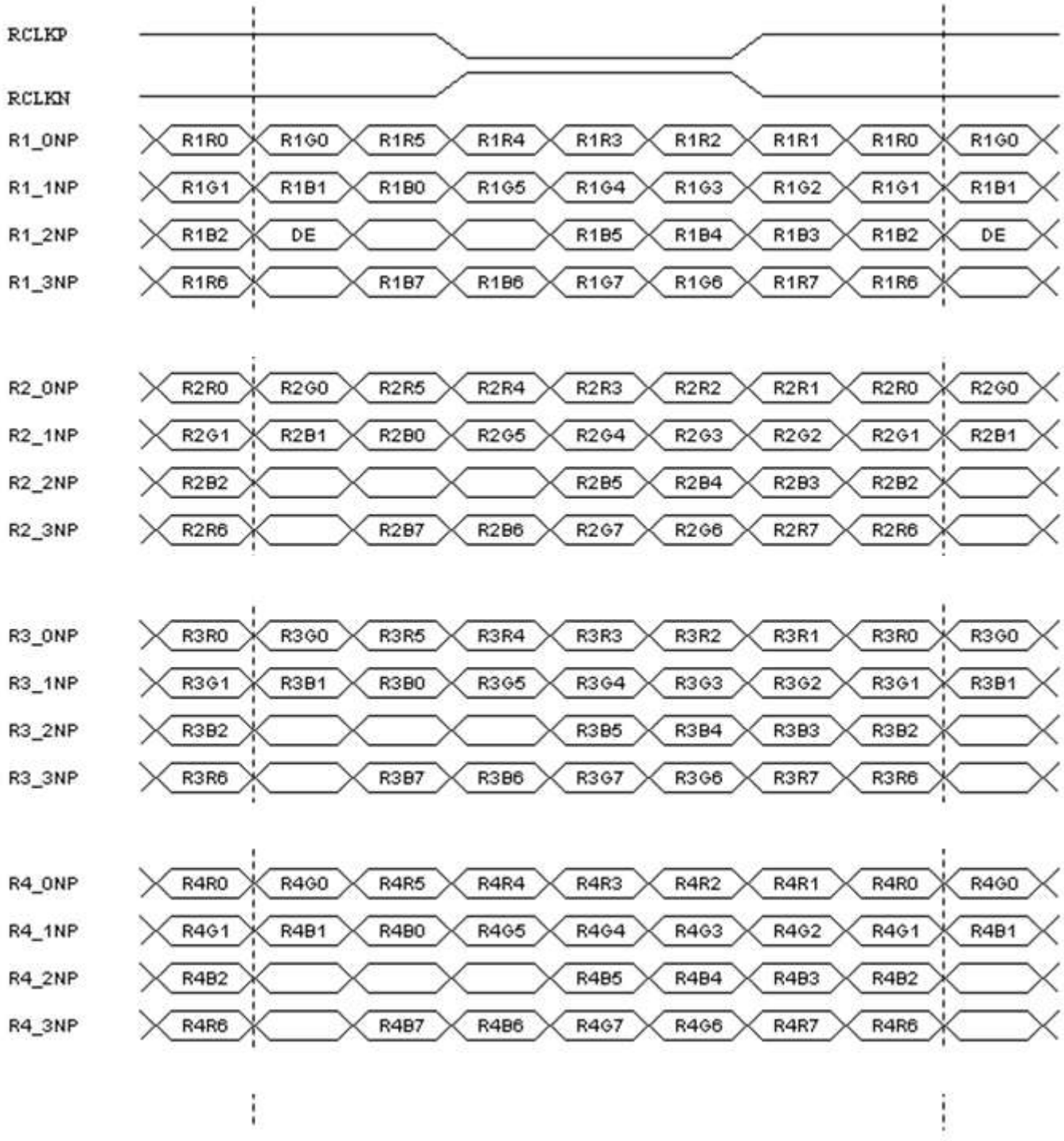
Port 2： 4N+2 (2, 6.. 2558 pixel)

Port 3： 4N+3 (3, 7.. 2559 pixel)

Port 4： 4N+4 (4, 8.. 2560 pixel)

N = 0, 1 ~639

3.4.2 LVDS Data Format



3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

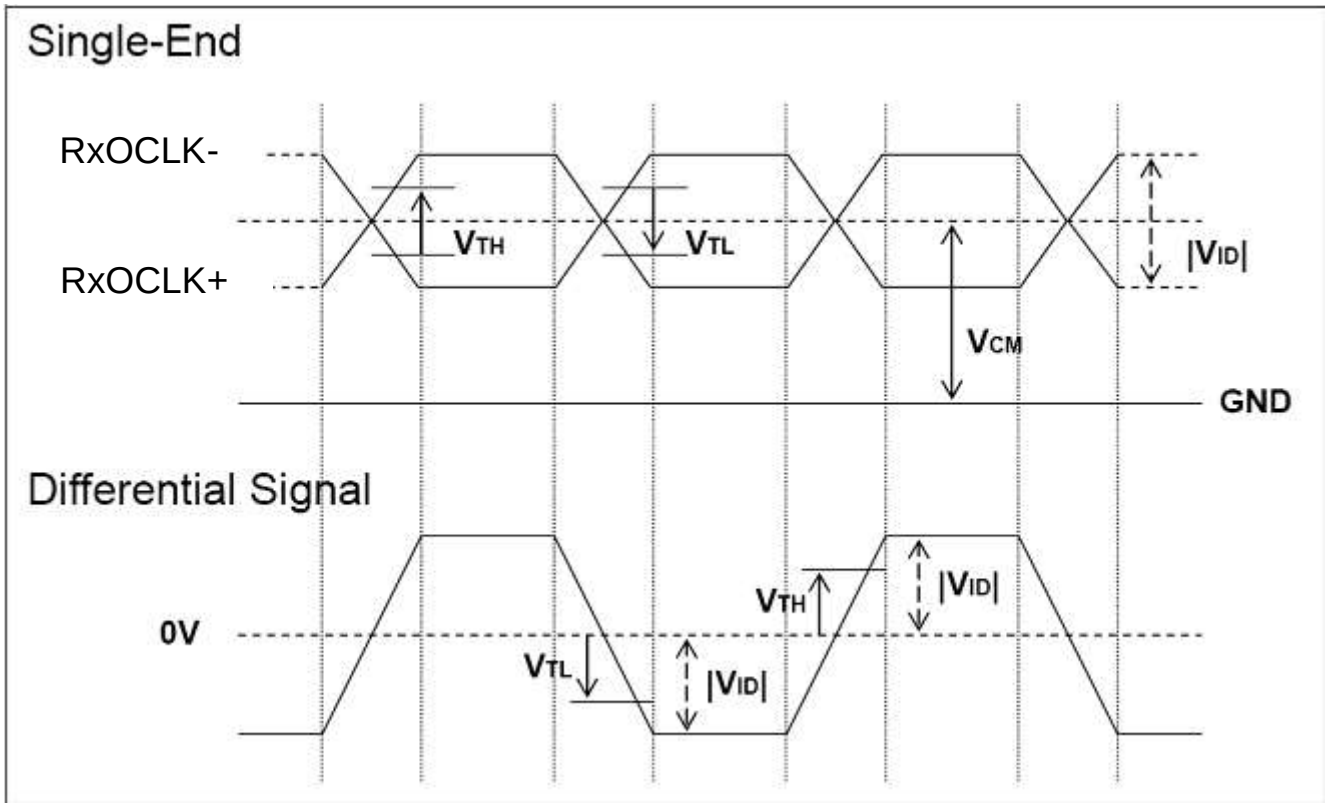
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	V_{CM} = 1.2V
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	V_{CM} = 1.2V
$\lvert V_{ID} \rvert$	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	1.0	1.2	1.5	[V]	V_{TH}-V_{TL} = 200mV

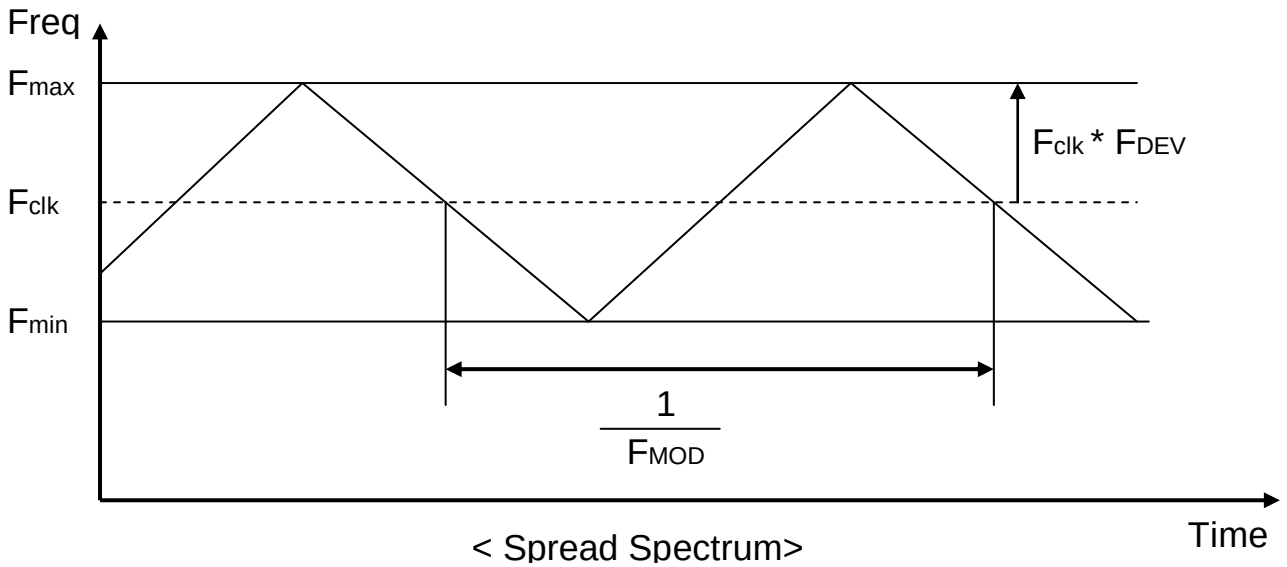
LVDS Signal Waveform:

Use RxOCLK- & RxOCLK+ as example.



b. AC Characteristics:

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



< Spread Spectrum>

Fclk: LVDS Clock Frequency

3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1452	1481	2553	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	12	41	1113	Th	
Fv		Frequency	48	60	76	Hz	
Th	Horizontal Section	Period	679	680	1023	Tclk	
Tdisp (h)		Active	640	640	640	Tclk	
Tblk (h)		Blanking	39	40	383	Tclk	
Fh		Frequency	69.7	88.8	112.7	KHz	*Note 3-4*
Tclk	LVDS Clock	Period	13.1	16.6	21.1	ns	1/Fclk
Fclk		Frequency	47.3	60.4	76.5	MHz	*Note 3-5*

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.);
Fh (Typ.) = Fclk (Typ.) / Th (Typ.);
Fh (Max.)= Fclk (Max.) / Th (Min.);

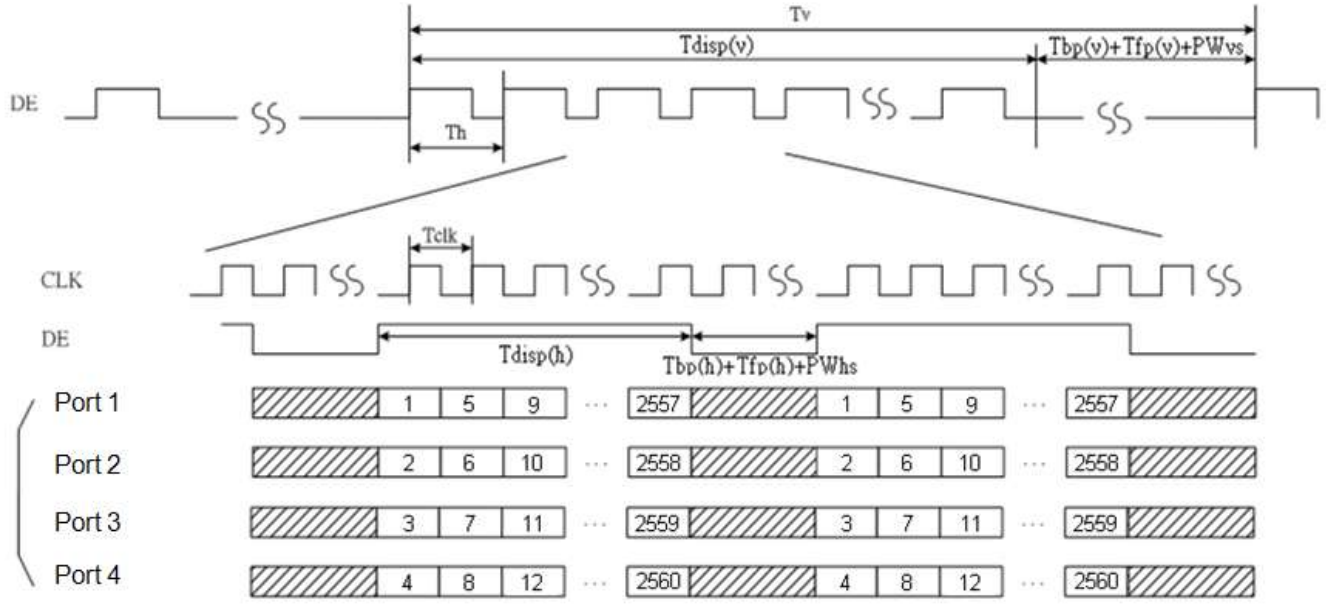
*Note 3-5: T*he equation is listed as following. Please don't exceed the above recommended value.

Fclk (Min.) = Fv (Min.) x Th (Min.) x Tv (Min.);

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.);

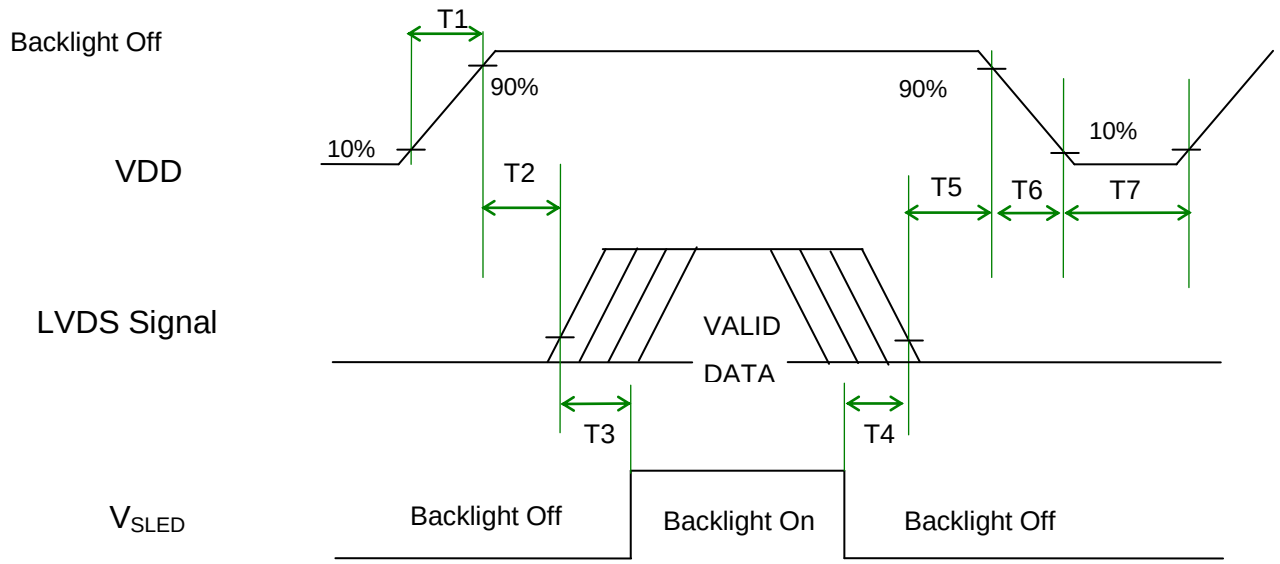
Fclk (Max.) = Fv (Max.) x Th (Typ.) x Tv (Typ.);

3.4.6 Input Timing Diagram



3.5 Power ON/OFF Sequence

VDD power,LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

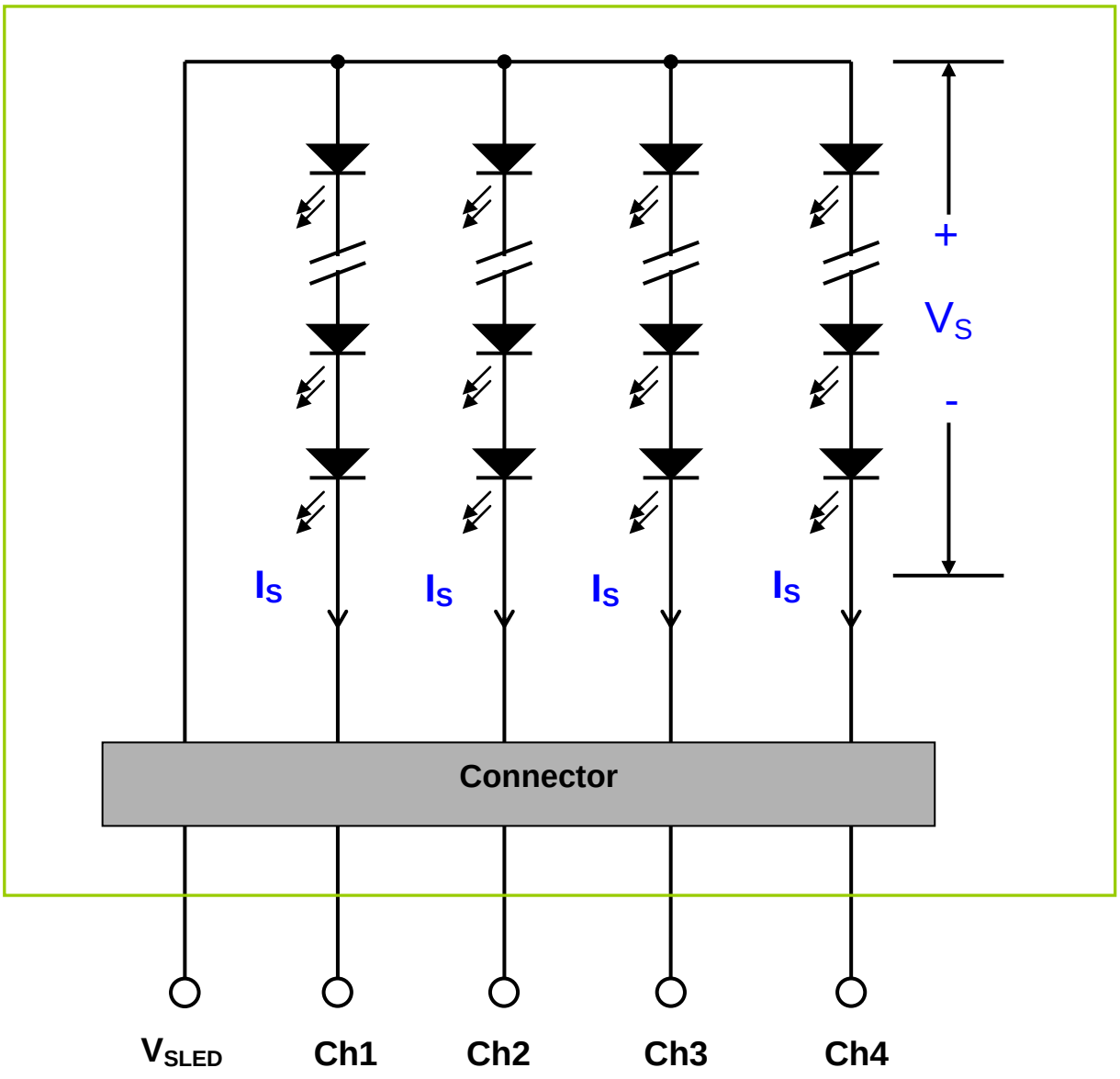
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	*Note 3-8*
T5	0		50	[ms]	*Note 3-6* *Note 3-7*
T6	0		200		*Note 3-9*
T7	1000	-	-	[ms]	

Note 3-6 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.
Note 3-7 : During T5 period , please keep the level of input LVDS signals with Hi-Z state.
Note 3-8 : If T4 < 100ms, there will be no reliability concern, but the display may momentarily show abnormal screen.
Note 3-9 : Voltage of VDD must decay smoothly after Power-off (customer system decide this value)

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 27 inch Backlight Unit. And it includes 72 pcs LED in the LED light bar. (4 strings and 18 pcs LED of one string).



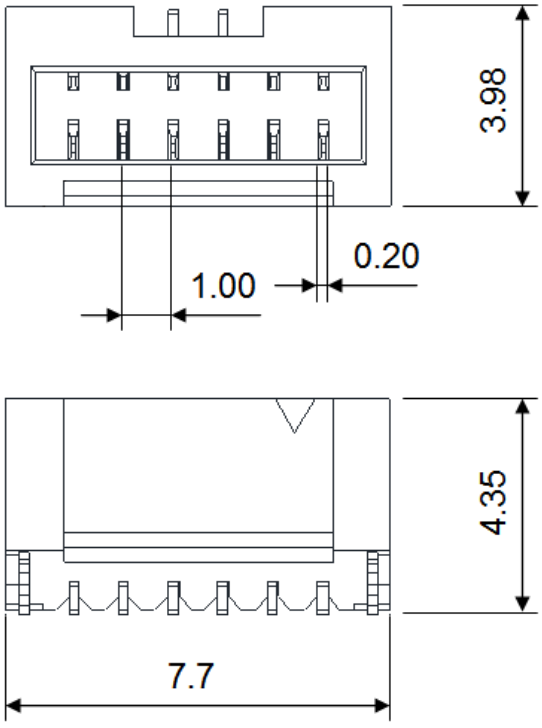
4.2 Interface Connection

4.2.1 Connector Type

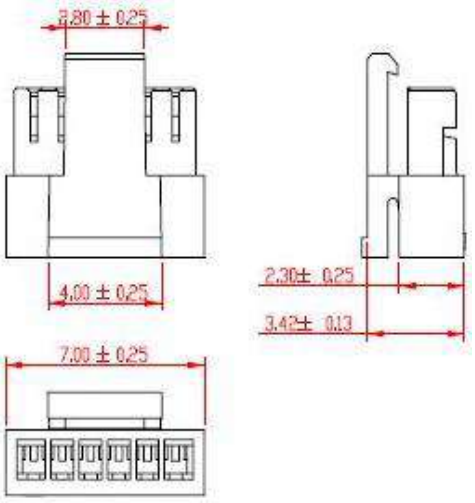
Backlight Connector	Manufacturer	Cvilux
	Part Number	CI1406M1VLD-NH
Mating Connector	Manufacturer	ENTERY
	Part Number	H112K-P06N-00B (Non-Locking type) H112K-P06N-11B(White) (Locking type) H112K-P06N-13B(Black) (Locking type)

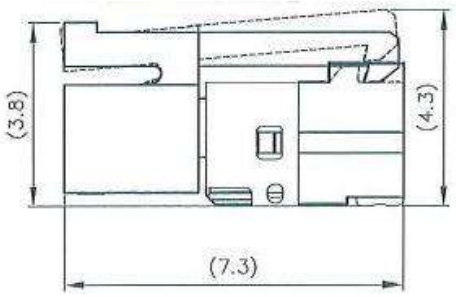
Backlight Connector dimension:

$H \times V \times D = 7.7 \times 3.98 \times 4.35, Pitch = 1.0(unit = mm)$



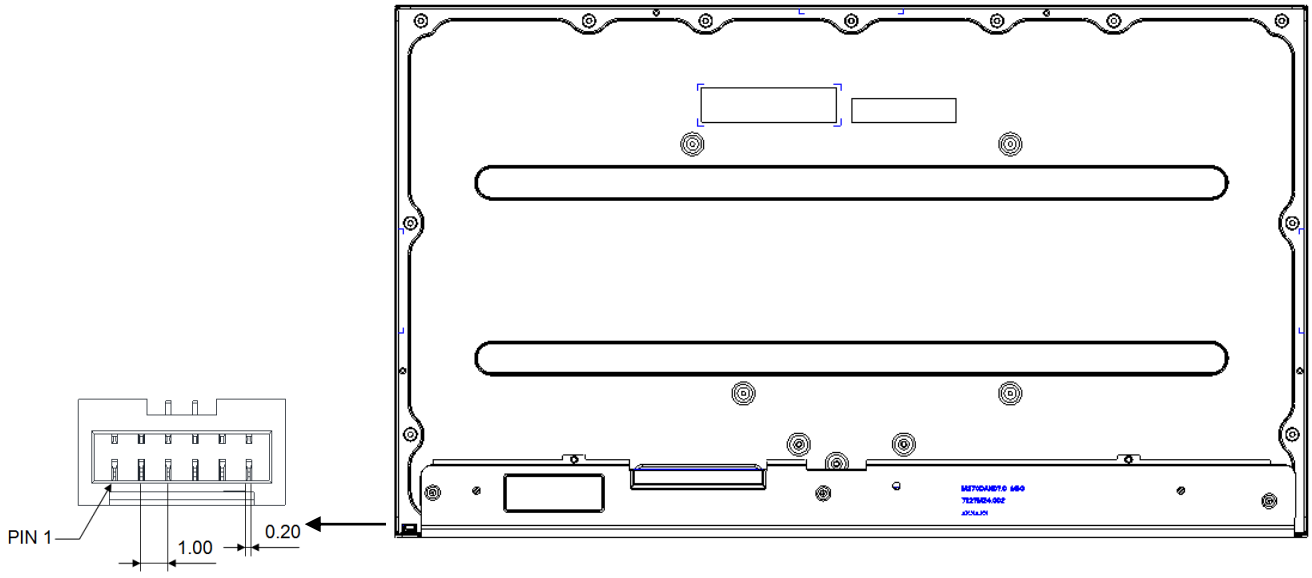
Mating Connector dimension:


3.80 ± 0.25
4.00 ± 0.25
7.00 ± 0.25
2.30± 0.25
3.42± 0.13


(3.8)
(4.3)
(7.3)

4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25℃)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio

4.3.2 Recommended Operating Condition

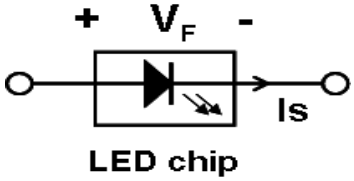
(Ta=25℃)

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current		60	66	[mA]	100% duty ratio of LED chip, ***Note 4-6***
Vs	LED String Voltage	45	49.5	59.4	[Volt]	Is=60mA @ 100% duty ratio; ***Note 4-1, Note 4-5, Note 4-7***
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3.6	[Volt]	Is=60mA @ 100% duty ratio; ***Note 4-2***
P_{BLU}	LED Light Bar Power Consumption	-	11.9	14.3	[Watt]	***Note 4-3***
LT_{LED}	LED Life Time	30,000	-	-	[Hour]	***Note 4-4***
OVP	Over Voltage Protection in system board	110% Vsmax	-	-	[Volt]	***Note 4-5***

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)=2.5, V_F(Typ.)=2.75, V_F(Max.)=3.3

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);

a. ΔV_F: LED chip forward voltage deviation; (0.2 V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4 ; (4 is total String No. of LED Light bar)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4 ;

Note 4-4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

b. Test condition: Is = 60mA and 25℃ (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.

Note 4-7: Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	*Note 5-1*
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	*Note 5-2*
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.

ESD discharged points should avoid display area and periphery front bezel of display area. Suggest points were 4 side parallel edge of display area surface.

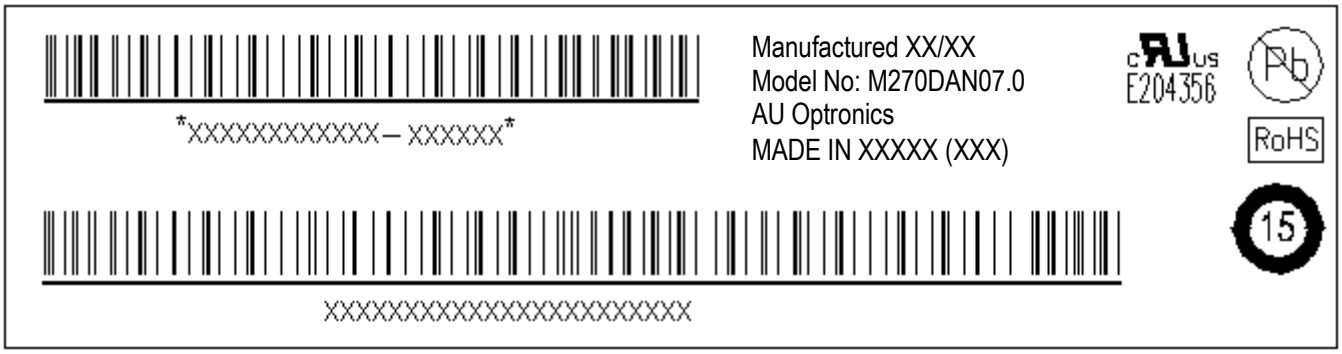
Metal front bezel must cover half area of BM (black matrix), and metal front bezel must connect with metal back bezel to protect source IC of panel by ESD damaged.

Note 5-3 : Result Evaluation Criteria:

TFT-LCD panels test should take place after gradually cooling enough at room temperature In the normal application, there should be no particular problems that may affect the display function.

6 Shipping Label

The label is on the panel as shown below:



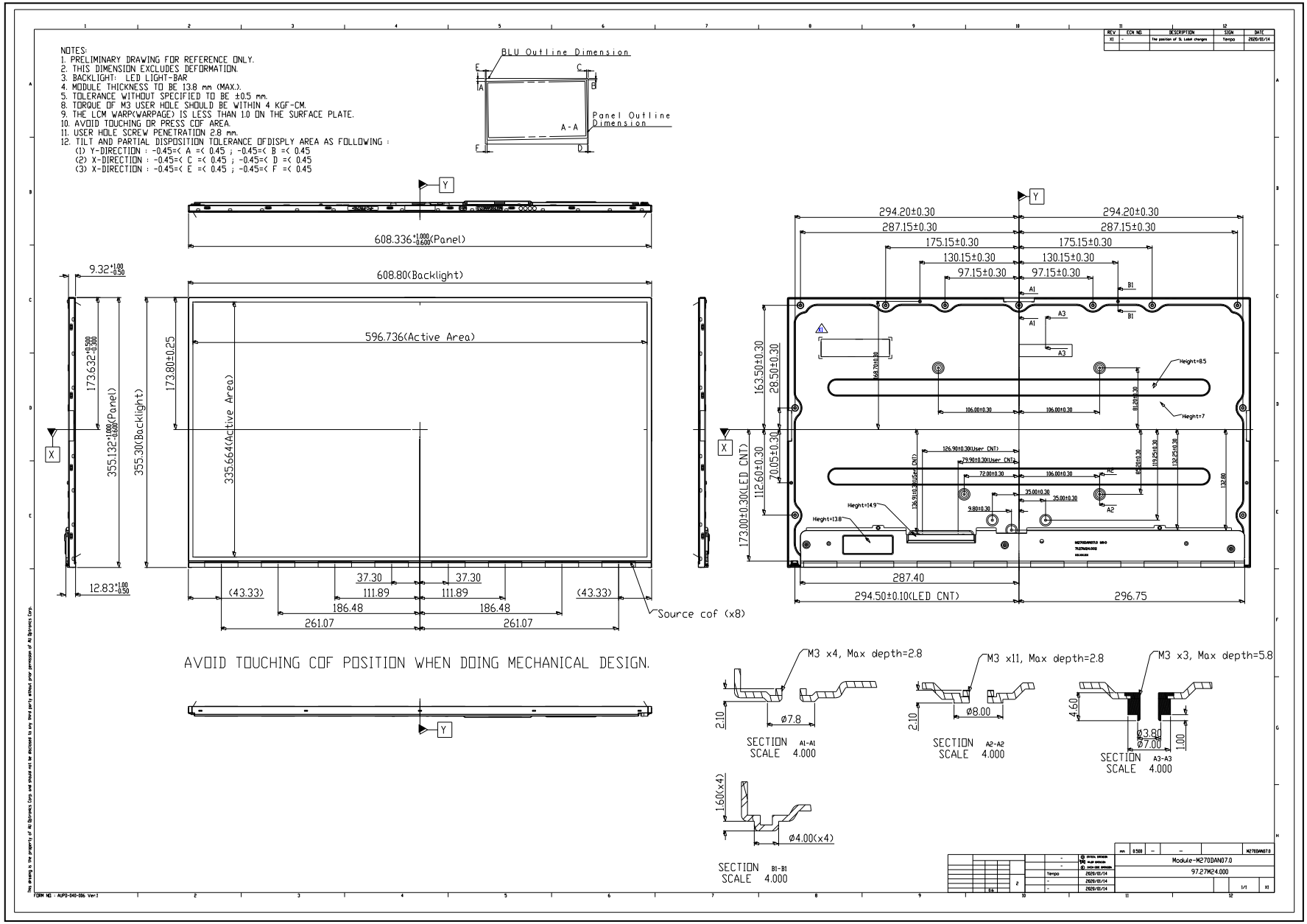
Note 6-1: For Pb Free products, AUO will add for identification.

Note 6-2: For RoHS compatible products, AUO will add for identification.

Note 6-3: For China RoHS compatible products, AUO will add for identification.

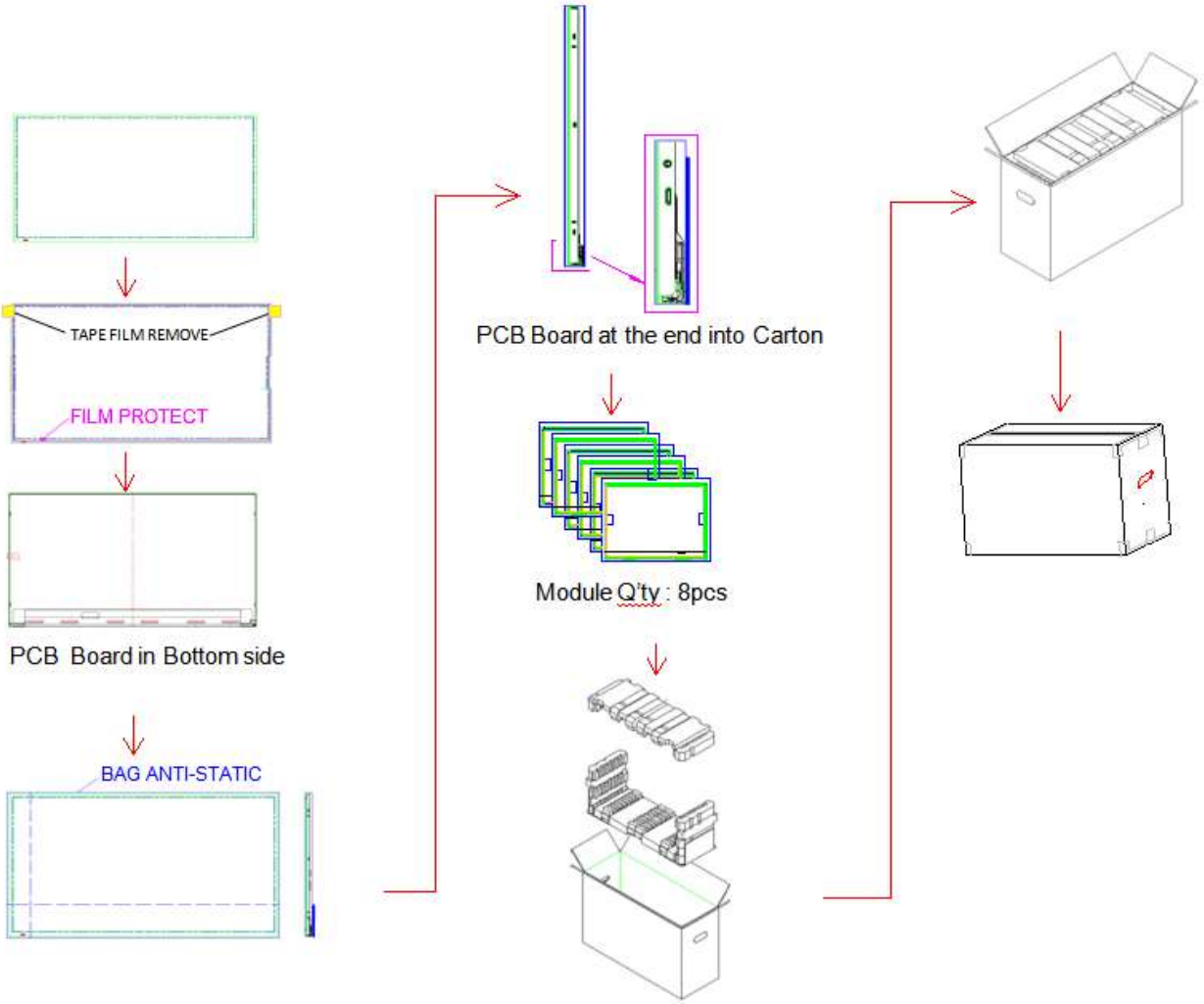
Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

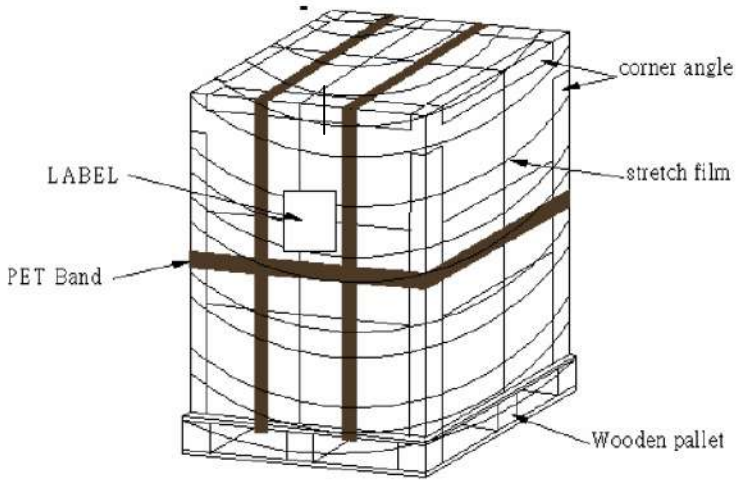
7 Mechanical Characteristics



8 Packing Specification

8.1 Packing Flow





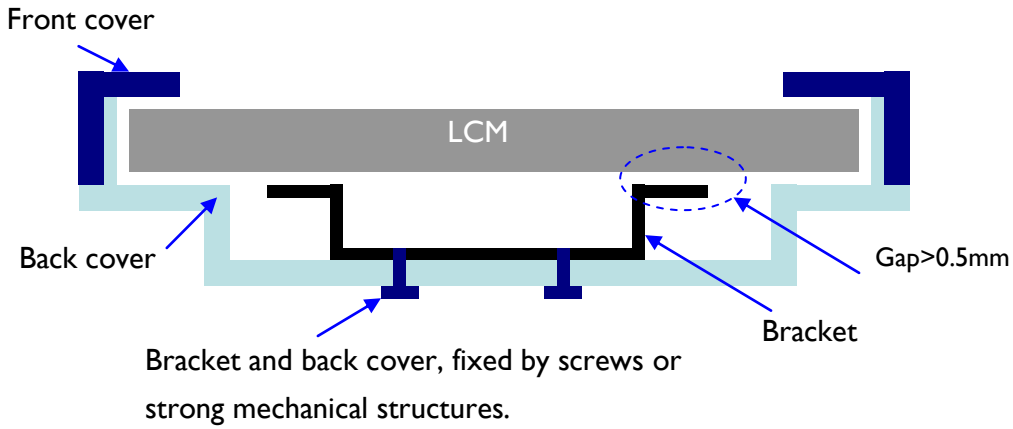
8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	608.8(H)mm × 354.8(V)mm × 11.645(D)mm	3.25	
Cushion	1	-	1.7	
Box	1	702(L)mm x 264(W)mm x 456(H)mm	1.2	without Panel & cushion
Packing Box	8 pcs/Box	702(L)mm x 264(W)mm x 456(H)mm	28.9	with panel & cushion & Box
Pallet	1	1070(L)mm x 740(W)mm x 132(H)mm	14.80	
Pallet after Packing	8 boxes/pallet	1070(L)mm x 740(W)mm x 1086(H)mm	246.0	

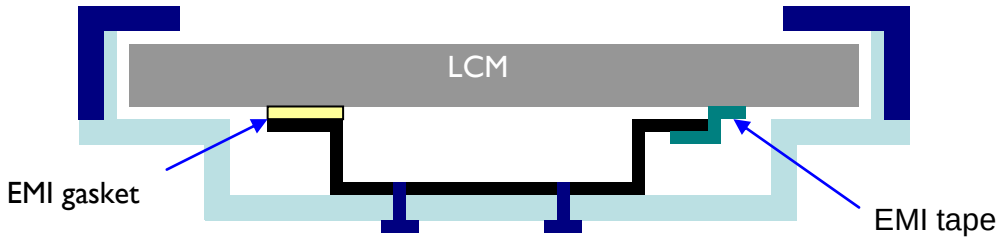
9 Design Guide for System

9.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

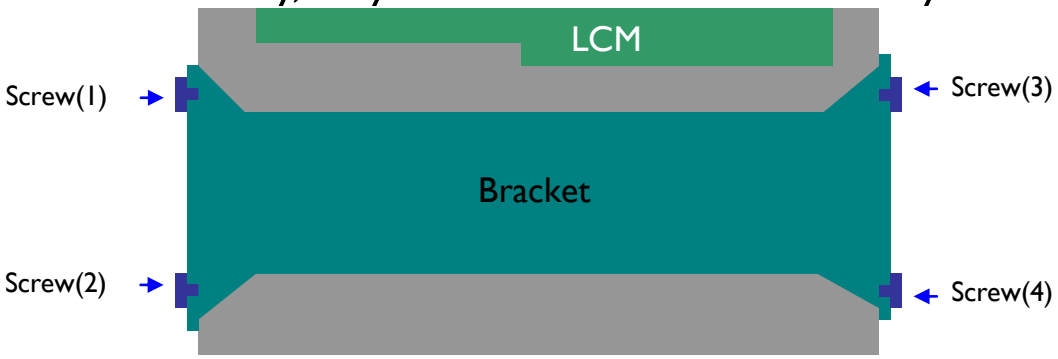
9.2 The system bracket should be fixed on back cover firmly.



9.3 The EMI gasket should be uniform and not push panel strongly.



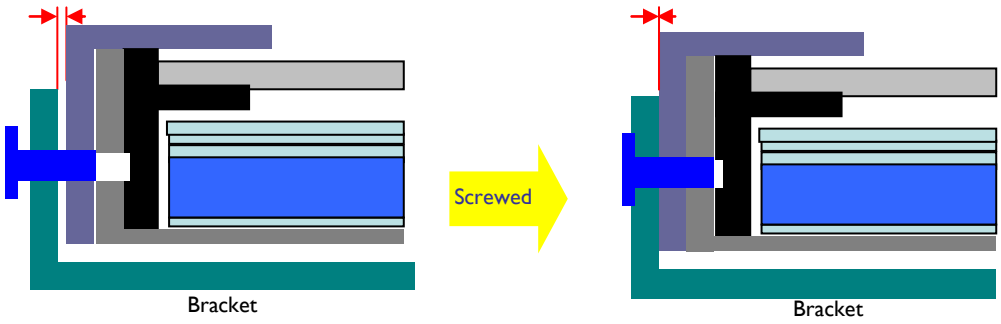
9.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.5 The system bracket and panel should be in parallel with having no gap after inserting screws.

Proper and Parallel gap

0 gap and no mechanical damage



9.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.