PSRAM 8-Mbit (512K x 16) Pseudo Static RAM

Features

- Advanced low-power architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.6V
- Typical active current: 2 mA @ f = 1 MHz
- Typical active current: 11 mA @ f = f_{MAX}
- Low standby power
- Automatic power-down when deselected

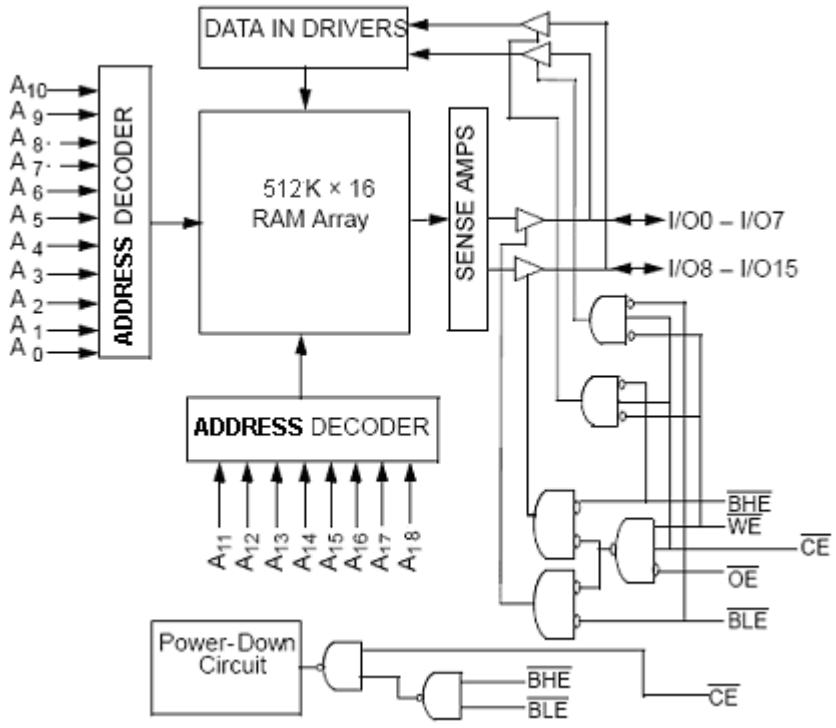
Functional Description

The M24L816512SA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 512K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O0through I/O_{15}) are placed in a high-impedance state when : deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable($\overline{CE}$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins(A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 toI/O_{15}. Refer to the truth table for a complete description of read and write modes.

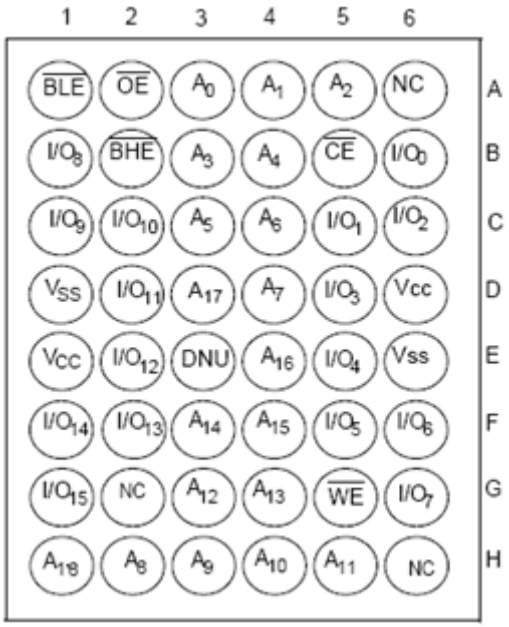
Logic Block Diagram



Pin Configuration[2, 3, 4]

48-ball VFBGA

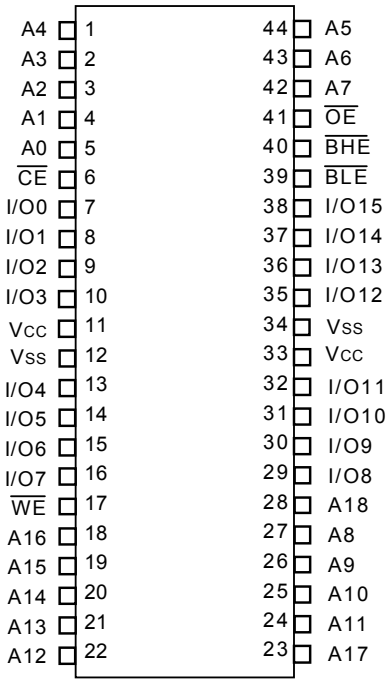
Top View



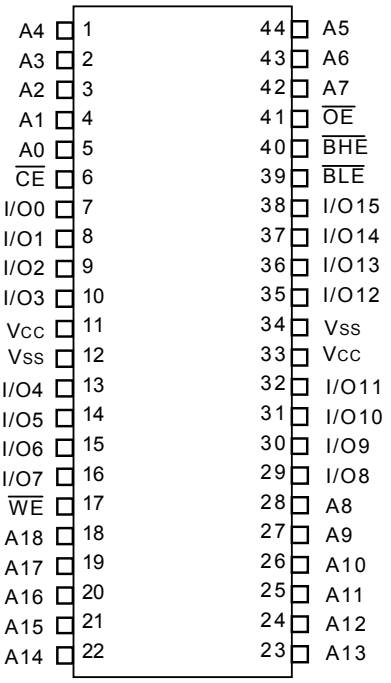
44-Pin TSOPII(Note*)

Top View

(Default)



(TypeA)



Note* :
The default pin arrangement of TSOPII package of the device is as ”Default” figure.
User also can control pin 18~28 to turn into pin arrangement of “Type A” with software.
(The difference in pin arrangement between ”Default” and “Type A” is pin 18~28)

Product Portfolio Product

Product	V_{CC} Range (V)			Speed(ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby, I_{SB2}(μA)	
					f = 1MHz		f = f_{MAX}			
	Min.	Typ.	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ. [5]	Max.
M24L816512SA	2.7	3.0	3.6	55	2	5	11	22	55	100
				70				17		110(for Vcc > 3.3V)

Notes:
2.DNU pins are to be left floating or tied to VSS.
3.Ball G2, H6 are the address expansion pins for the 16-Mbit and 32-Mbit densities respectively.
4.NC “no connect”—not connected internally to the die.
5.Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC\ (typ)}$ and T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)
Storage Temperature .....–65°C to +150°C
Ambient Temperature with
Power Applied .....–55°C to +125°C
Supply Voltage to Ground Potential .....−0.4V to 4.6V
DC Voltage Applied to Outputs
in High-Z State[6, 7, 8] .....−0.4V to 3.7V
DC Input Voltage[6, 7, 8] .....−0.4V to 3.7V
Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage ..... > 2001V
(per MIL-STD-883, Method 3015)
Latch-up Current .....> 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Extended	−25°C to +85°C	2.7V to 3.6V
Industrial	−40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics (Over the Operating Range) [5, 6, 7, 8]

Parameter	Description	Test Conditions		-55			-70			Unit
				Min.	Typ .[5]	Max.	Min.	Typ. [5]	Max.	
V_{CC}	Supply Voltage			2.7	3.0	3.6	2.7	3.0	3.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = −0.1 mA		V_{CC}-0.4			V_{CC}-0.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			0.8* V_{CC}		V_{CC}+ 0.4V	0.8* V_{CC}		V_{CC}+0 .4V	V
V_{IL}	Input LOW Voltage	f = 0		-0.4		0.4	-0.4		0.4	V
I_{IX}	Input Leakage Current	GND ≤V_{IN} < V_{CC}		-1		+1	-1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		-1		+1	-1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = 3.6V I_{OUT} = 0mA CMOS level		11	22		11	17	mA
		f = 1 MHz			2	5		2	5	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE}$ ≥V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, V_{IN} ≤ 0.2V, f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$)			100	400		100	400	µA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE}$ ≥ V_{CC}−0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	V_{CC} = 3.3V		55	100		55	100	µA
			V_{CC} = 3.6V			110			110	

Capacitance[9]

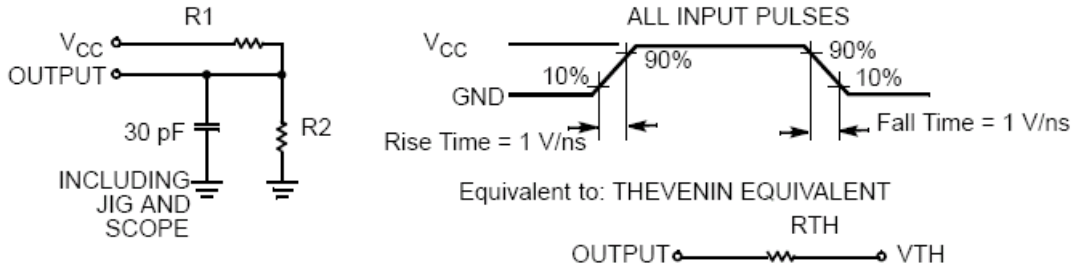
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{CC} = $V_{CC(typ)}$	8	pF

Thermal Resistance[9]

Parameter	Description	Test Conditions	BGA	Unit
ΘJA	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
ΘJC	Thermal Resistance (Junction to Case)		17	°C/W

Notes:
6.$V_{IH(MAX)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
7.$V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
8.Overshoot and undershoot specifications are characterized and are not 100% tested.
9.Tested initially and after design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V V_{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R_{TH}	11000	Ω
V_{TH}	1.50	V

Switching Characteristics Over the Operating Range[10, 11, 12, 13, 14]

Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55[14]		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11, 12]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		25		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11, 12]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 12]		25		25	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[11, 12]	5		5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z[11, 12]		10		25	ns
t_{SK}[14]	Address Skew		0		10	ns

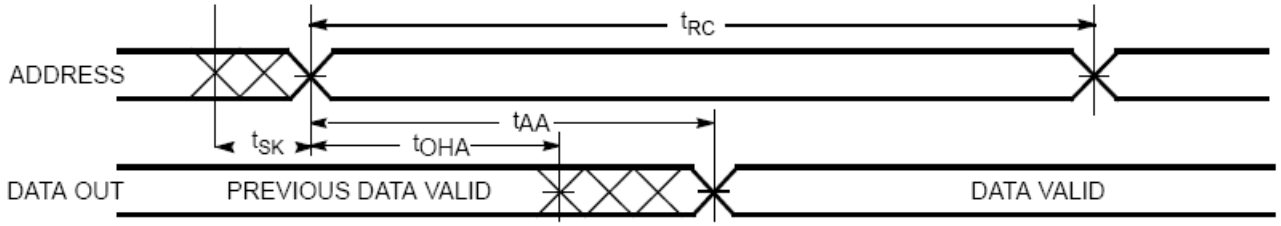
Notes:
10. Test conditions assume signal transition time of 1V/ns or higher, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE}transitions are measured when the outputs enter a high-impedance state.
12. High-Z and Low-Z parameters are characterized and are not 100% tested.
13. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
14. To achieve 55-ns performance, the read access should be $\overline{CE}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics (Over the Operating Range) (continued)[10, 11, 12, 13, 14]

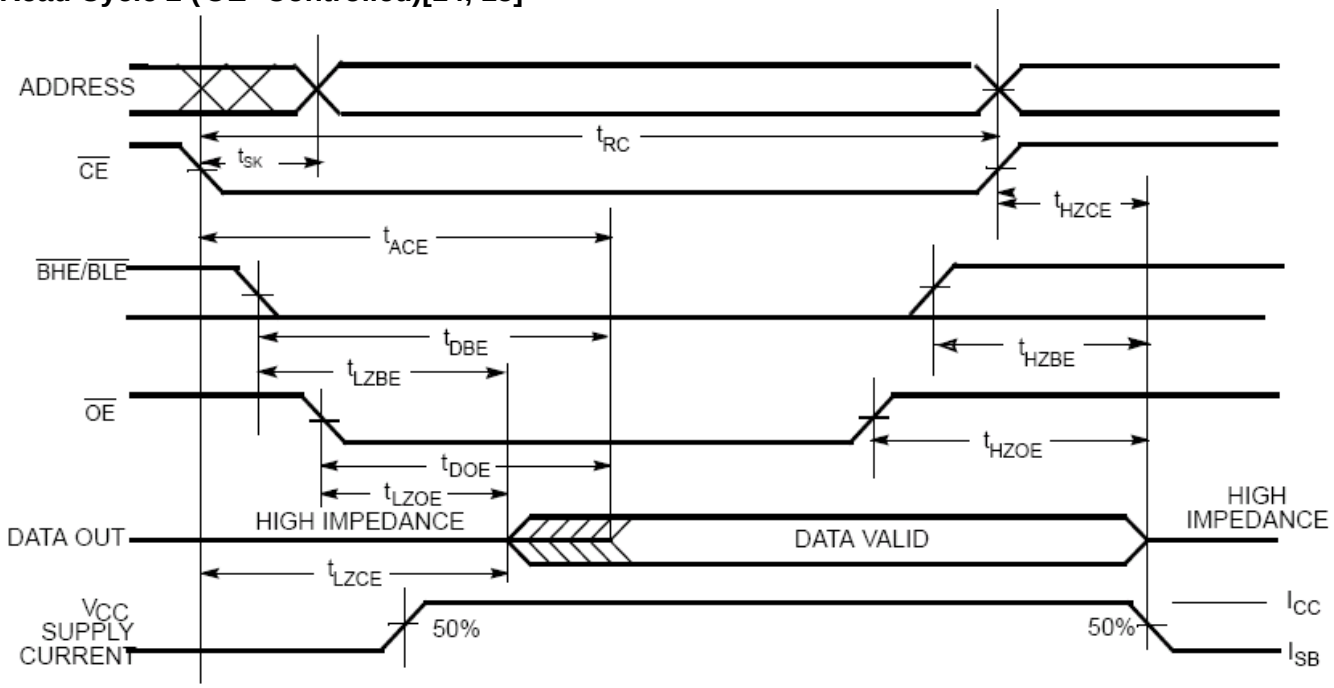
Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
Write Cycle[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		55		ns
t_{AW}	Address Set-up to Write End	45		55		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		55		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	50		55		ns
t_{SD}	Data Set-up to Write End	42		42		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11, 12]	5		5		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[14, 15, 16]



Read Cycle 2 ($\overline{OE}$ Controlled)[14, 15]

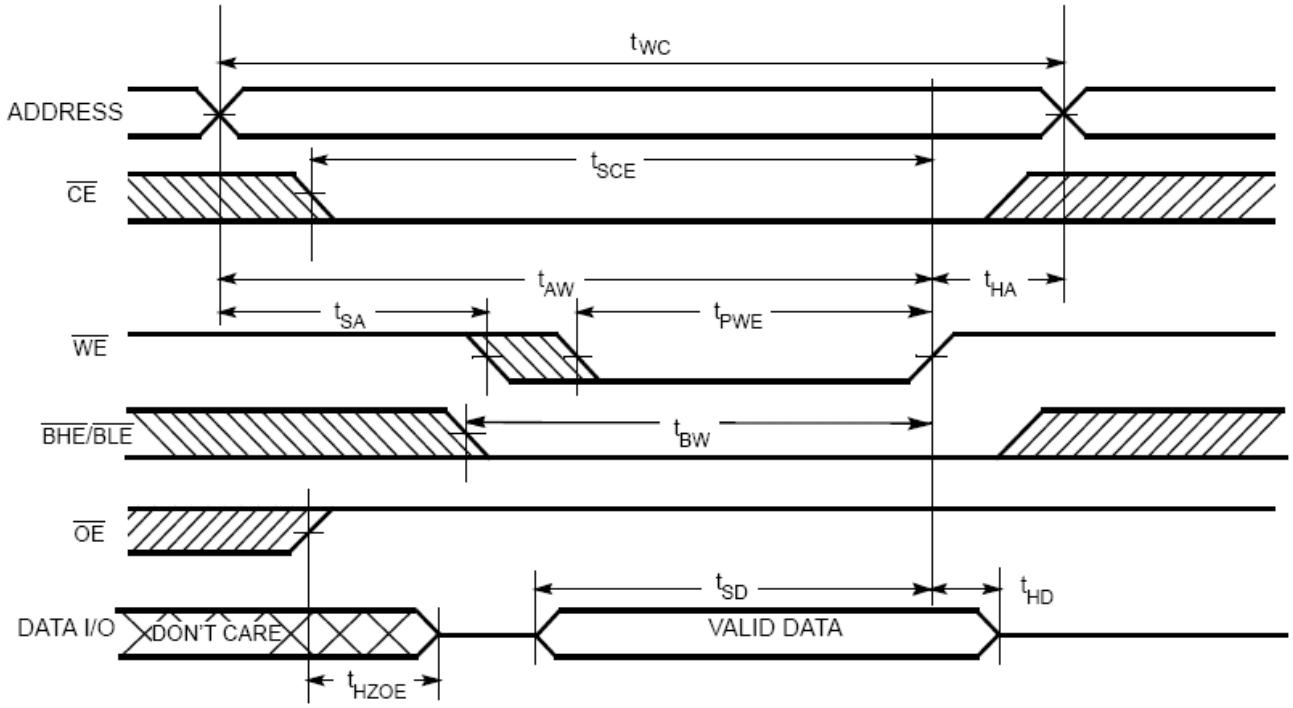


Notes:

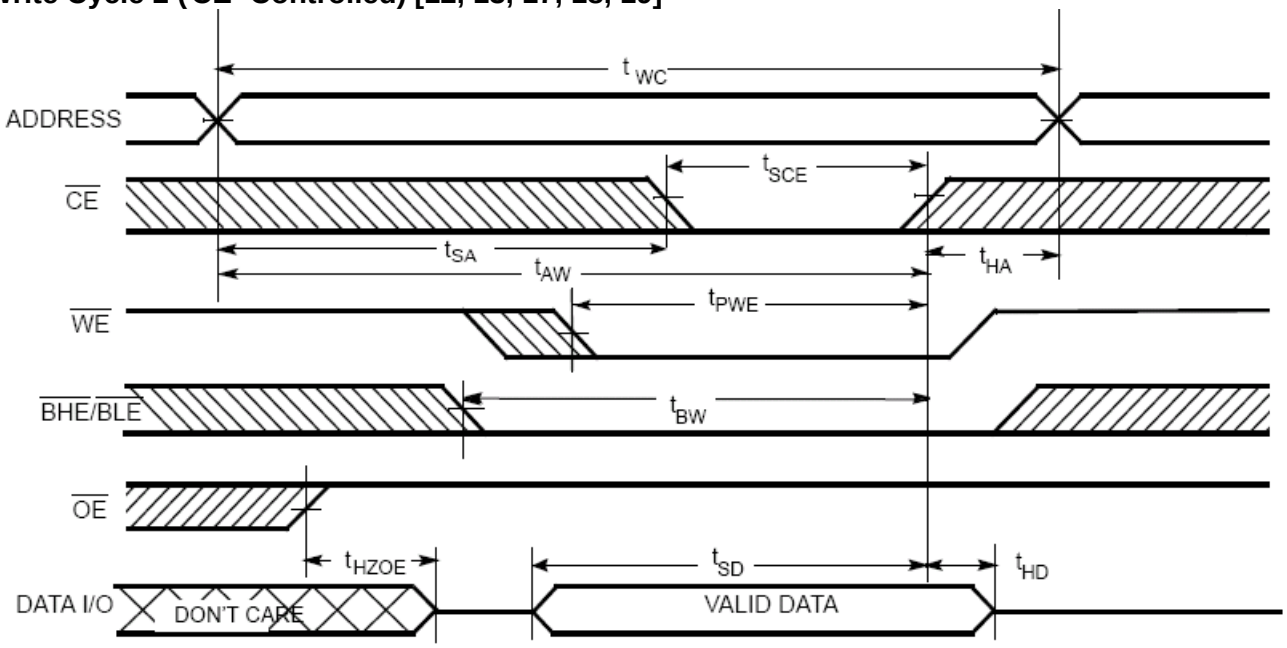
15. $\overline{WE}$ is HIGH for Read Cycle.
16. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled) [12, 13, 17, 18, 19]



Write Cycle 2 ($\overline{CE}$ Controlled) [12, 13, 17, 18, 19]



Notes:

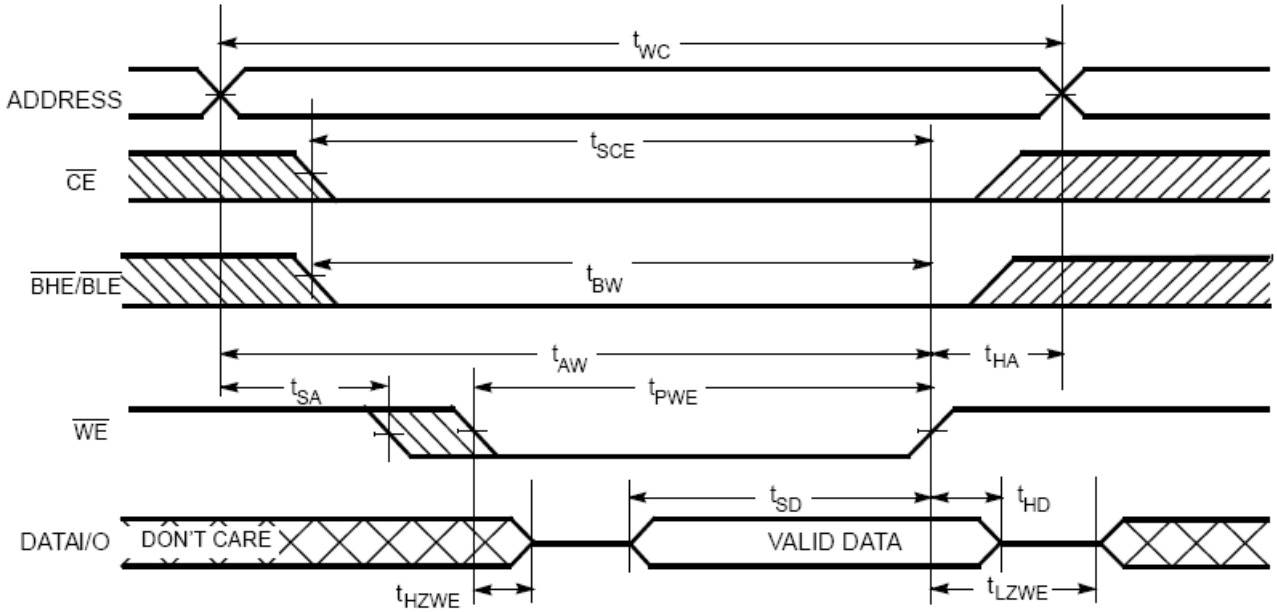
17.Data I/O is high impedance if $\overline{OE}$ ≥ V_{IH}.

18.If Chip Enable goes INACTIVE simultaneously with $\overline{WE}$ = HIGH, the output remains in a high-impedance state.

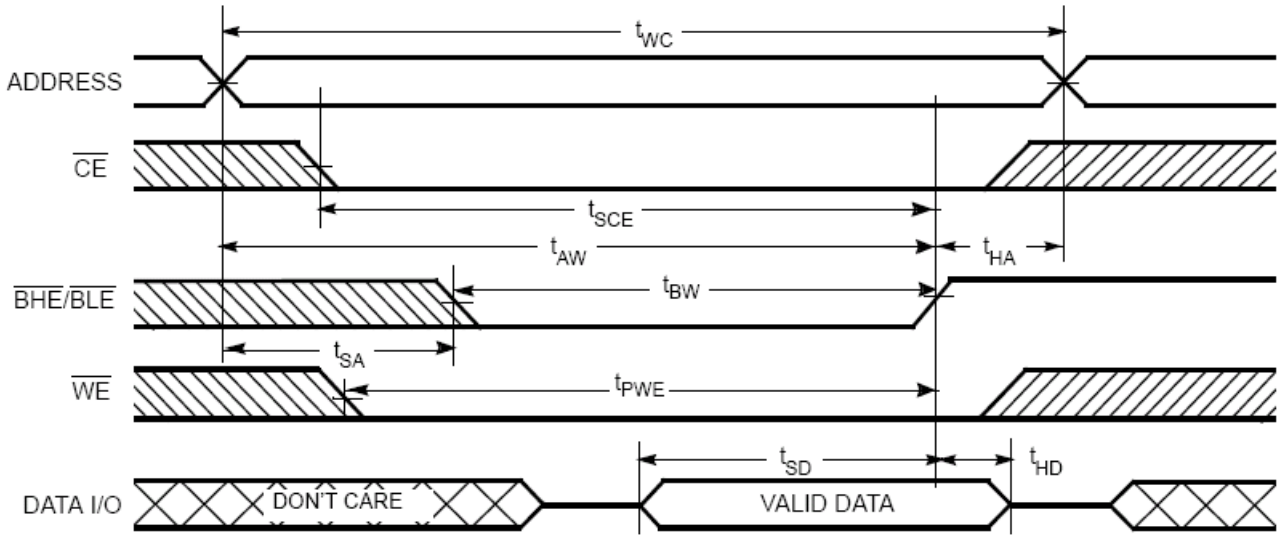
19.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[18, 19]



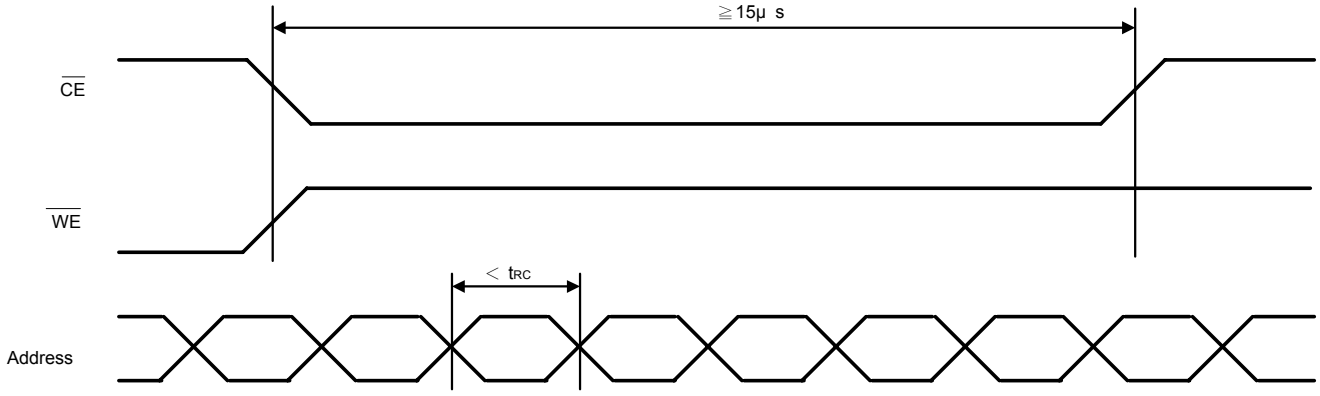
Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[18, 19]



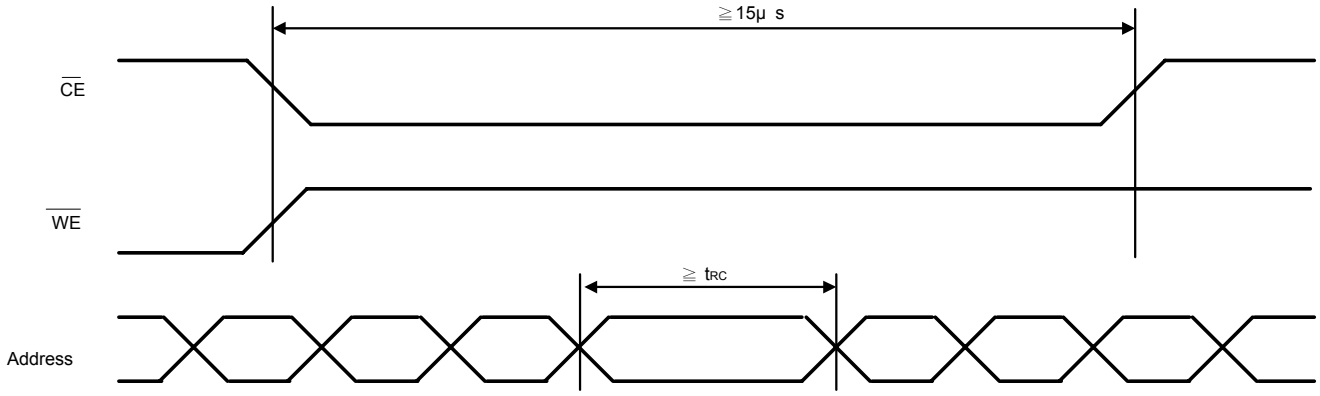
Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than t_{RC} during over 15μs at read operation shown as in Abnormal Timing, it requires a normal read timing at leat during 15μs shown as in Avoidable timing 1 or toggle $\overline{CE}$ to high ($\geqq t_{RC}$) one time at least shown as in Avoidable Timing 2.

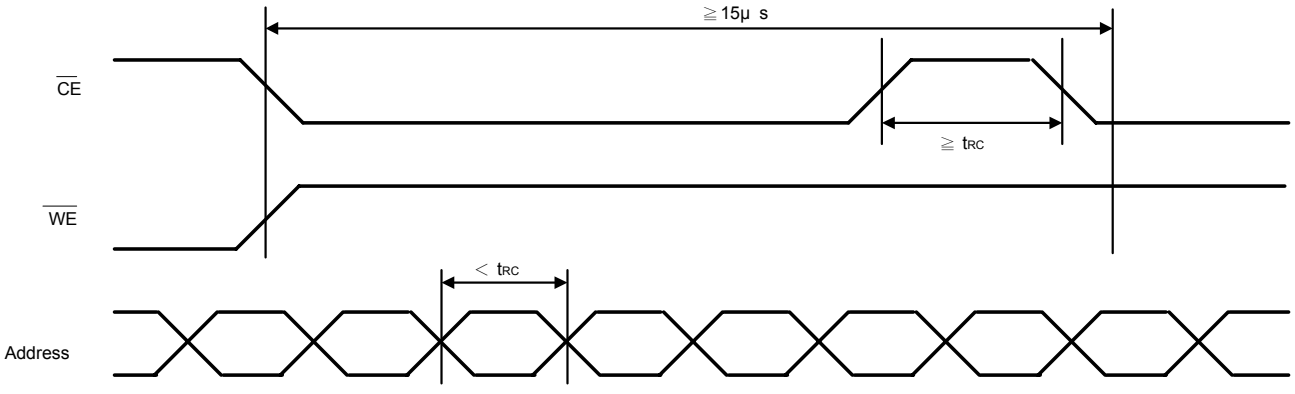
Abnormal Timing



Avoidable Timing 1



Avoidable Timing 2



Truth Table[20]

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); (I/O_8–I/O_{15}) in High Z	Read (Lower Byte only)	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); (I/O_0–I/O_7) in High Z	Read (Upper Byte only)	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write (Upper Byte and Lower Byte)	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); (I/O_8–I/O_{15}) in High Z	Write (Lower Byte Only)	Active (I_{CC})
L	L	X	L	H	Data Out (I/O_8–I/O_{15}); (I/O_0–I/O_7) in High Z	Write (Upper Byte Only)	Active (I_{CC})

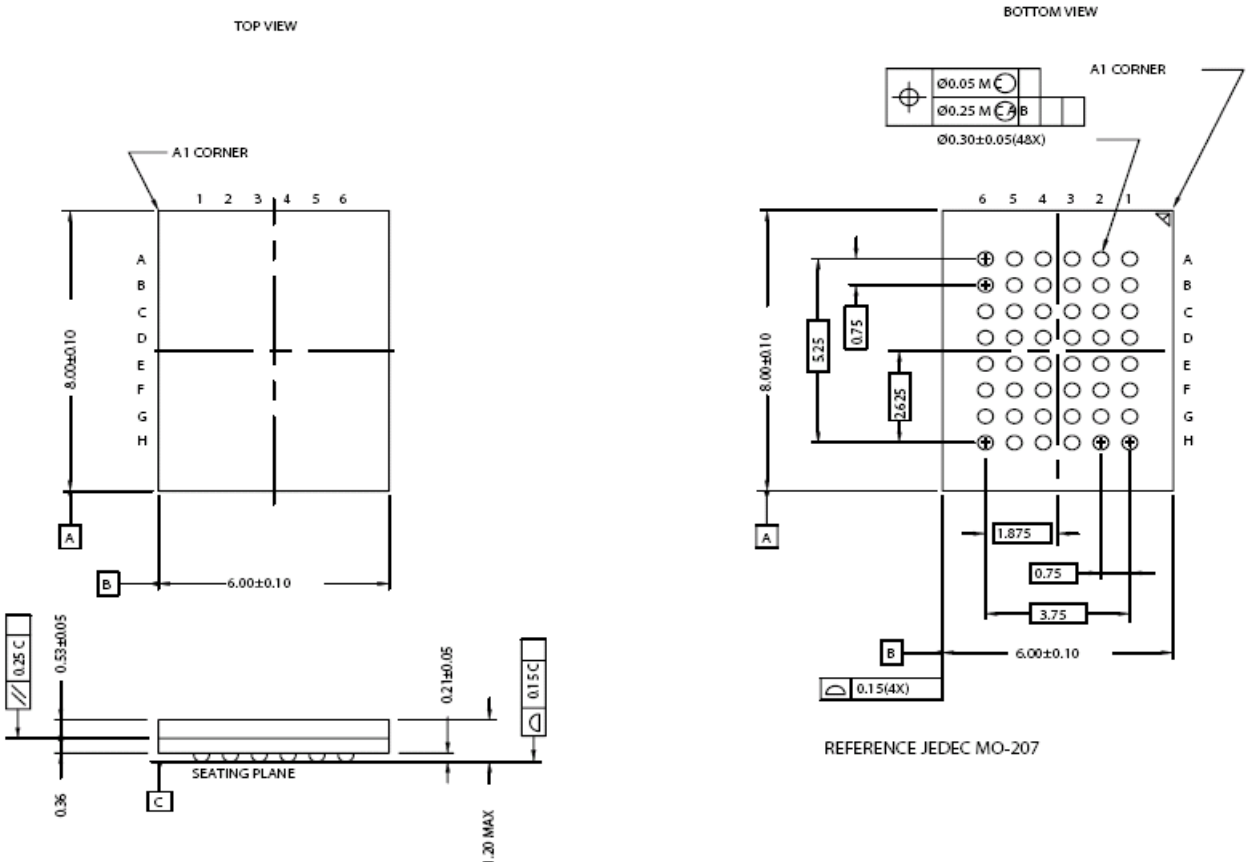
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L816512SA-55BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Extended
70	M24L816512SA -70BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Extended
55	M24L816512SA-55TEG	44-pin TSOPII (Pb-Free)	Extended
70	M24L816512SA-70TEG	44-pin TSOPII (Pb-Free)	Extended
55	M24L816512SA-55BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial
70	M24L816512SA-70BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial
55	M24L816512SA-55TIG	44-pin TSOPII (Pb-Free)	Industrial
70	M24L816512SA-70TIG	44-pin TSOPII (Pb-Free)	Industrial

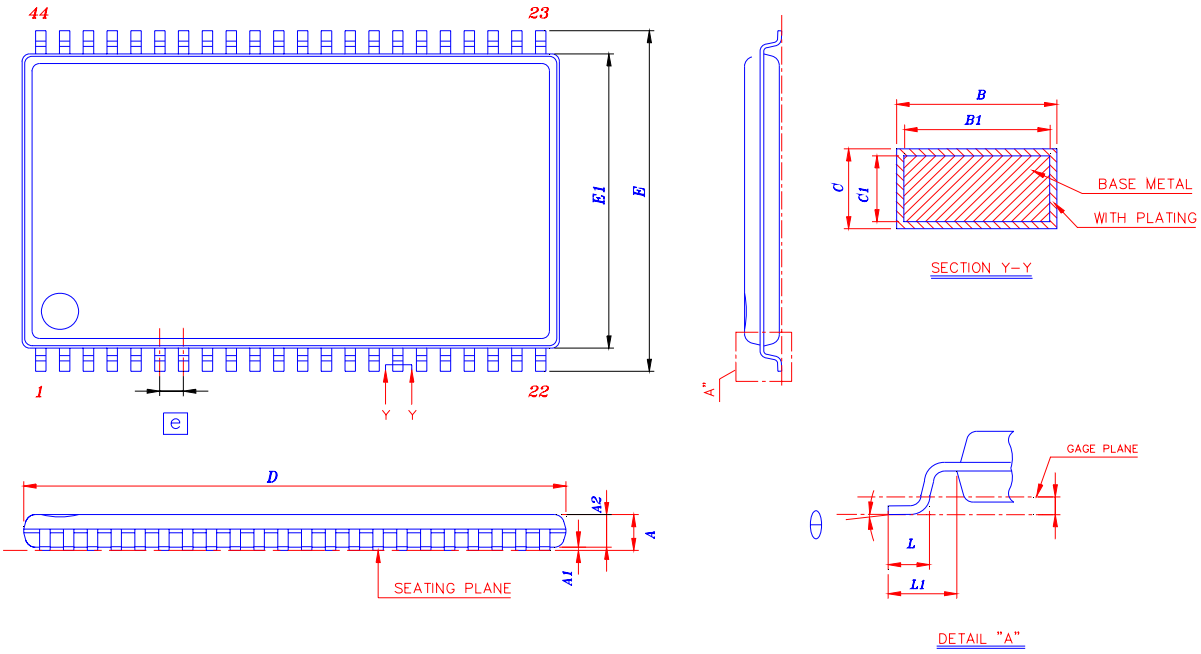
Note:
20.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Package Diagrams

48-Ball (6 mm x 8mm x 1.2 mm) FBGA



44-LEAD TSOP(II) PSRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.20	——	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
B	0.30	——	0.45	0.012	——	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	——	0.21	0.005	——	0.008
C1	0.10	——	0.16	0.004	——	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0°	——	8°	0°	——	8°

Revision History

Revision	Date	Description
1.0	2008.02.27	Original
1.1	2008.03.24	Add I-grade for TSOPII package
1.2	2008.06.23	1. Move Revision History to the last 2. Modify voltage range from 2.7V~3.3V to 2.7V~3.6V
1.3	2008.07.04	Add Industrial grade for BGA package
1.4	2009.02.20	1.Correct Logic Block Diagram 2.Correct the ball name of H1 in BGA configuration
1.5	2009.06.22	Correct the ball name of D3 in BGA configuration

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