PSRAM 4-Mbit (512K x 8) Pseudo Static RAM

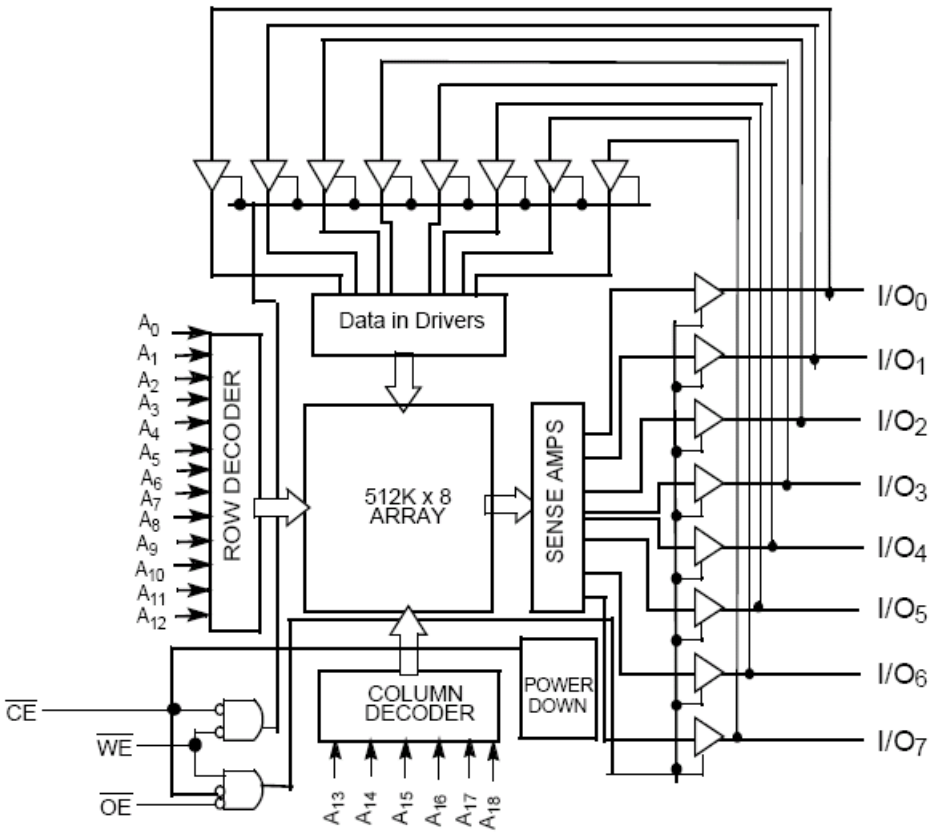
Features

- Advanced low power architecture
- High speed: 55 ns, 60 ns and 70 ns
- Wide voltage range: 2.7V to 3.6V
- Typical active current: 1mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

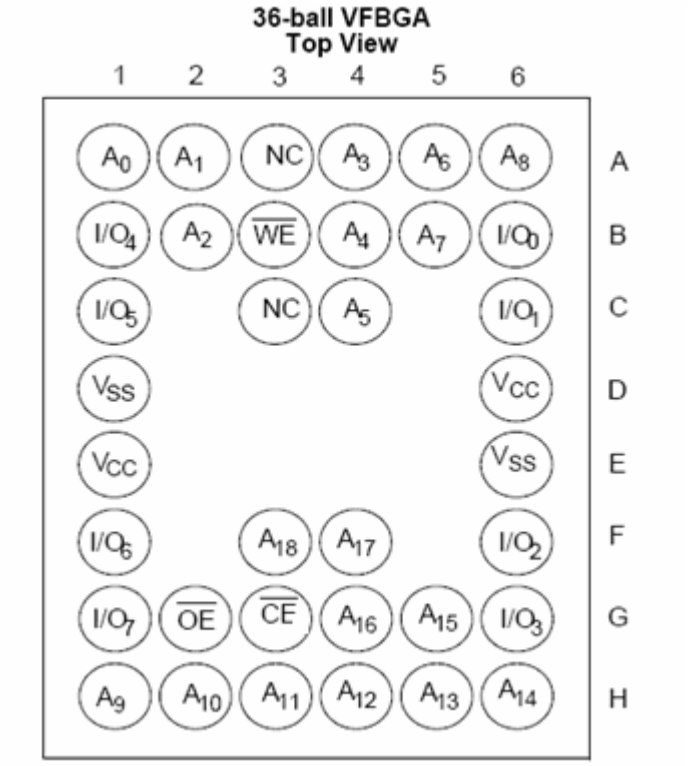
Functional Description

The M24L48512SA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$).This device has an automatic power-down feature that reduces power consumption dramatically when deselected. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).Reading from the device is accomplished by asserting the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) inputs LOW while forcing Write Enable ($\overline{WE}$) HIGH . Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW). See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



Pin Configuration[2]



Product Portfolio

Product	V_{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, I_{CC} (mA)				Standby, I_{SB2} (μA)	
					f = 1 MHz		f = f_{MAX}			
	Min.	Typ.	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
M24L48512SA	2.7	3.0	3.6	55	1	5	14	22	17	40
				60						
				70			8	15		

Notes:
2. NC "no connect"—not connected internally to the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC\ (typ)}$ and T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)
Storage Temperature .....–65°C to +150°C
Ambient Temperature with
Power Applied .....–55°C to +125°C
Supply Voltage to Ground Potential .....−0.4V to 4.6V
DC Voltage Applied to Outputs
in High-Z State[4, 5, 6] .....−0.4V to 3.7V
DC Input Voltage[4, 5, 6] .....−0.4V to 3.7V
Output Current into Outputs (LOW) .....20 mA
Static Discharge Voltage ..... > 2001V
(per MIL-STD-883, Method 3015)
Latch-up Current .....> 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Extended	−25°C to +85°C	2.7V to 3.6V
Industrial	−40°C to +85°C	2.7V to 3.6V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		-55, 60, 70			Unit
				Min.	Typ.[3]	Max.	
V_{CC}	Supply Voltage			2.7	3.0	3.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = −0.1 mA		V_{CC} – 0.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA				0.4	V
V_{IH}	Input HIGH Voltage			0.8 * V_{CC}		V_{CC} + 0.4	V
V_{IL}	Input LOW Voltage			-0.4		0.4	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ Vcc		-1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ Vcc, Output Disabled		-1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = 3.6V, I_{OUT} = 0 mA, CMOS level		14 for 55ns speed 14 for 60 ns speed 8 for 70 ns speed	22 for 55 ns speed 22 for 60 ns speed 15 for 70 ns speed	mA
		f = 1 MHz			1 for all speed	5 for all speeds	
I_{SB1}	Automatic $\overline{CE}$ Power-down Current —CMOS Inputs	$\overline{CE}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, V_{IN} ≤ 0.2V, f = f_{MAX}(Address and Data Only), f = 0, V_{CC} = 3.6V			150	250	µA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current —CMOS Inputs	$\overline{CE}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.6V			17	40	µA

Capacitance[7]

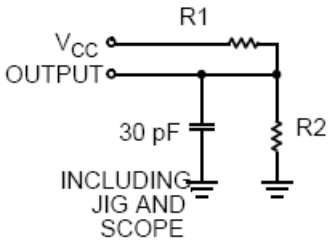
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

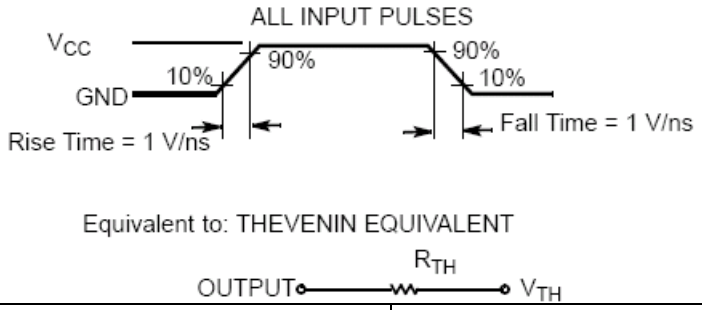
Notes:
4.$V_{IH(MAX)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
5.$V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
6.Overshoot and undershoot specifications are characterized and are not 100% tested.
7.Tested initially and after design or process changes that may affect these parameters.

Thermal Resistance[7]

Parameter	Description	Test Conditions	VFBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	55	˚C/W
θ_{JC}	Thermal Resistance (Junction to Case)		17	˚C/W

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT

Parameters	3.0V V_{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R_{TH}	11000	Ω
V_{TH}	1.50	V

Switching Characteristics (Over the Operating Range)[8]

Parameter	Description	–55		–60		–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	55[12]		60		70		ns
t_{AA}	Address to Data Valid		55		60		70	ns
t_{OHA}	Data Hold from Address Change	5		8		10		ns
t_{ACE}	$\overline{CE}$ LOW		55		60		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9, 10]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		25		25		25	ns
t_{LZCE}	$\overline{CE}$ LOW	2		2		5		ns
t_{HZCE}	$\overline{CE}$ HIGH		25		25		25	ns
t_{SK} [12]	Address Skew		0		0		10	ns
Write Cycle[11]								
t_{WC}	Write Cycle Time	55		60		70		ns
t_{SCE}	$\overline{CE}$ LOW	45		45		60		ns
t_{AW}	Address Set-up to Write End	45		45		55		ns
t_{HA}	Address Hold from Write End	0		0		0		ns

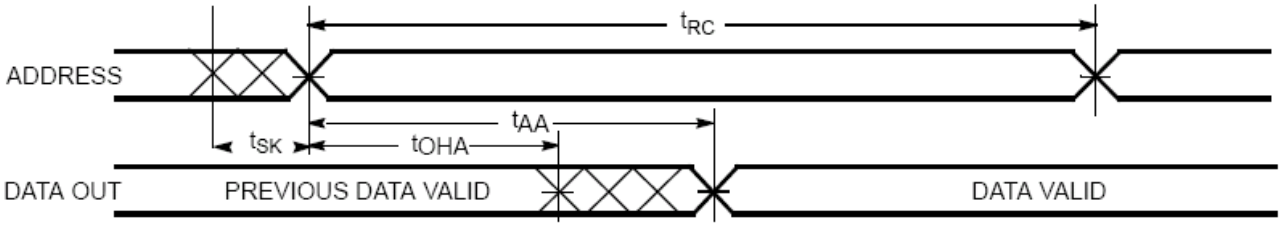
Notes:
8. Test conditions assume signal transition time of 1 V/ns or higher, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
10. High-Z and Low-Z parameters are characterized and are not 100% tested.
11. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
12. To achieve 55-ns performance, the read access should be $\overline{CE}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics (Over the Operating Range)[8] (continued)

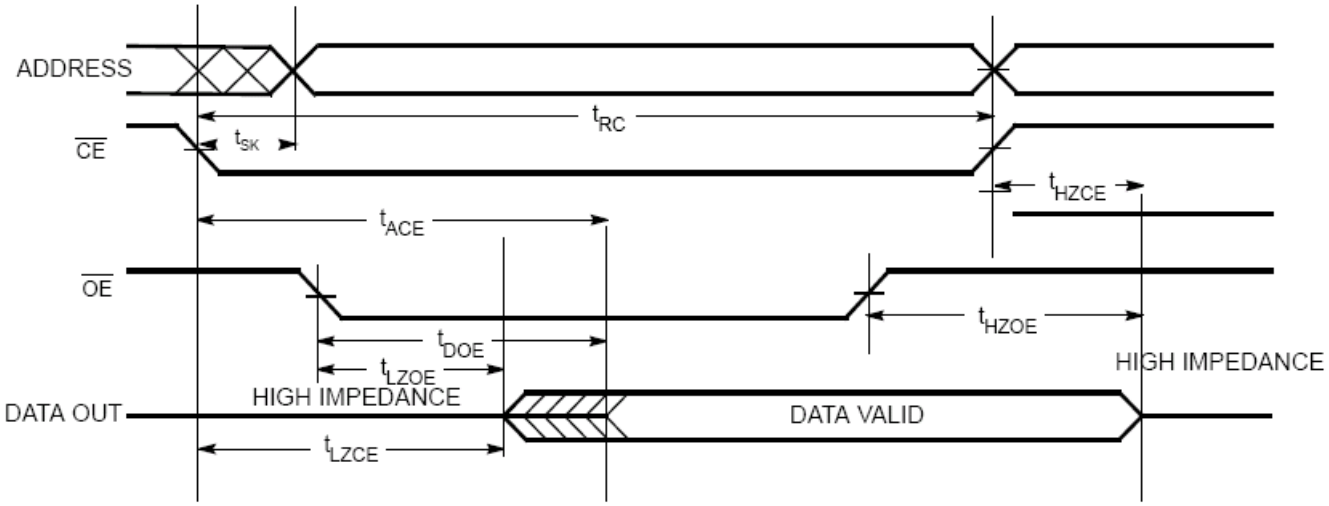
Parameter	Description	–55		–60		–70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		40		45		ns
t_{SD}	Data Set-up to Write End	25		25		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		25		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9, 10]	5		5		5		ns

Switching Waveforms

Read Cycle 1 (Address Transition Controlled) [12, 13, 14]



Read Cycle 2 ($\overline{OE}$ Controlled) [12, 14]



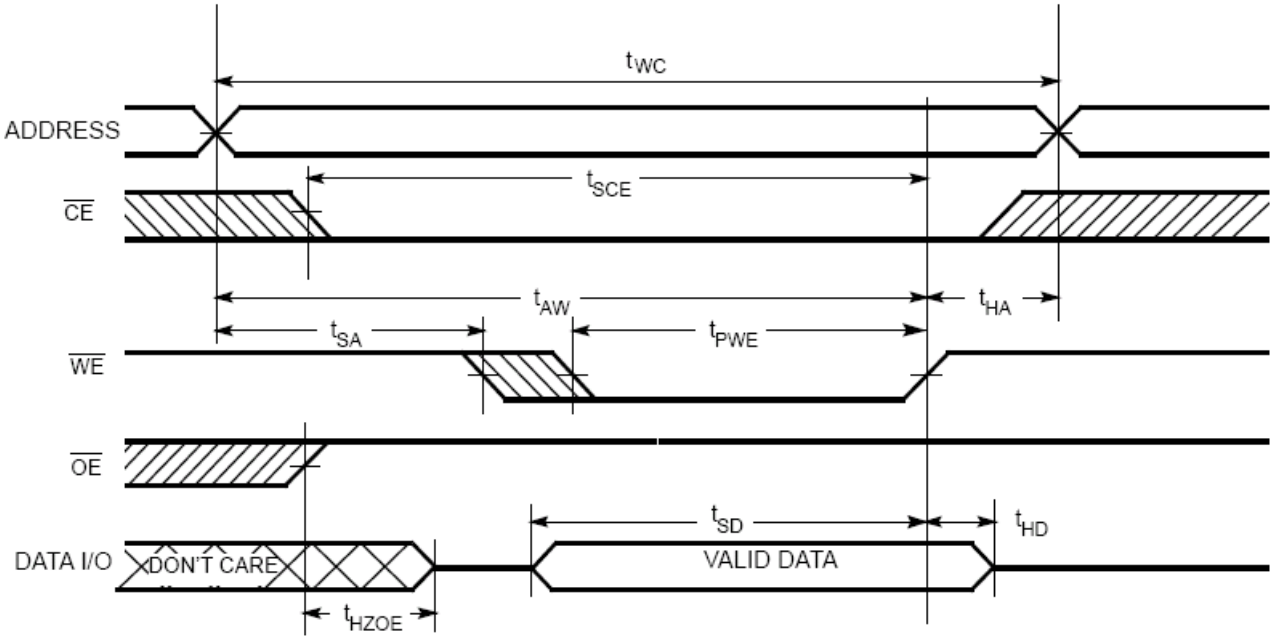
Notes:

13.Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.

14. $\overline{WE}$ is HIGH for Read Cycle.

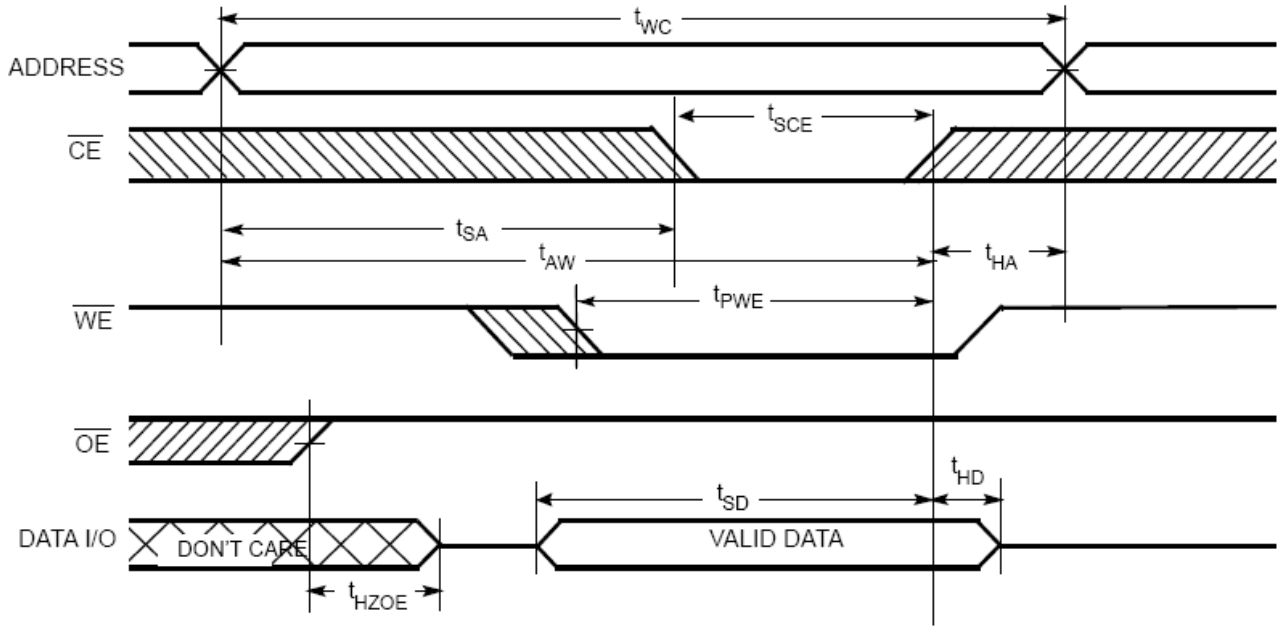
Switching Waveforms (continued)

Write Cycle No. 1($\overline{WE}$ Controlled) [10, 11, 15, 16, 17]



Switching Waveforms (continued)

Write Cycle 2 ($\overline{CE}$ Controlled) [10, 11, 15, 16, 17]



Notes:

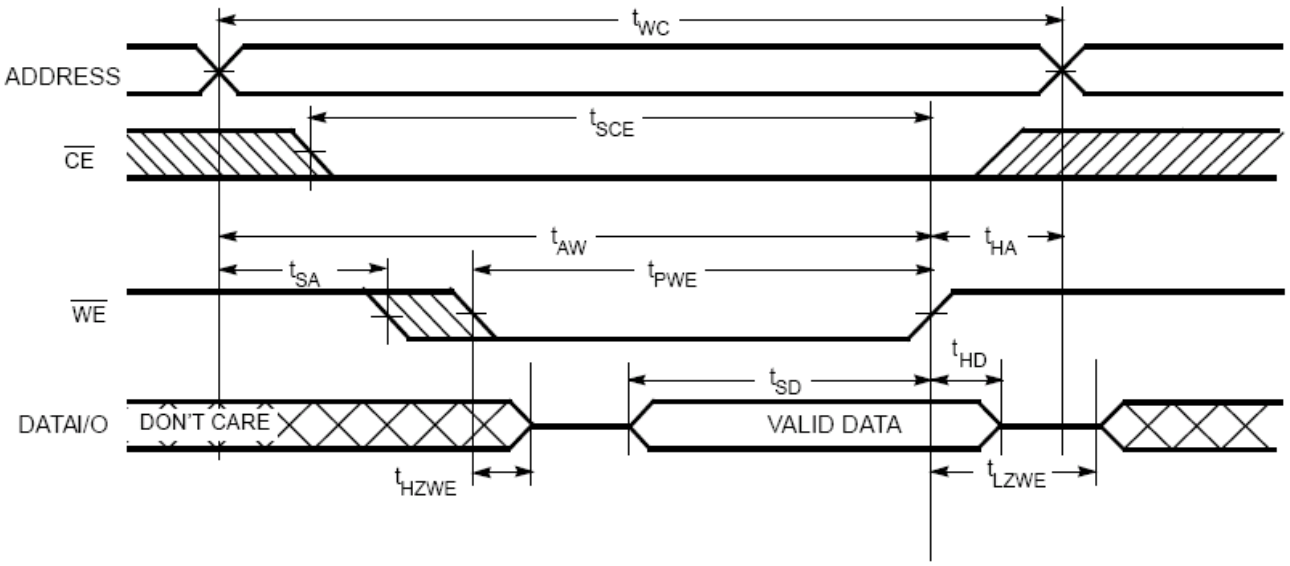
15.Data I/O is high impedance if $\overline{OE}$ ≥ V_{IH}.

16.If Chip Enable goes INACTIVE simultaneously with $\overline{WE}$ =HIGH, the output remains in a high-impedance state.

17.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

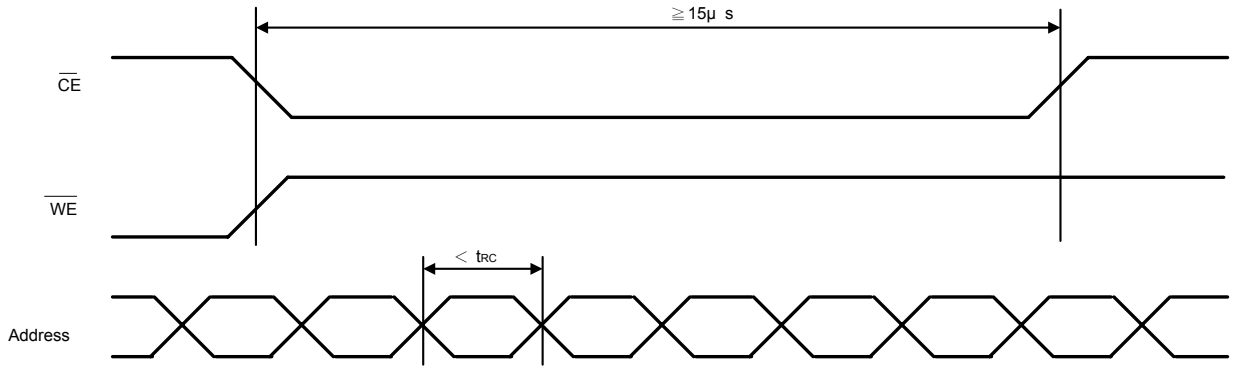
Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16, 17]



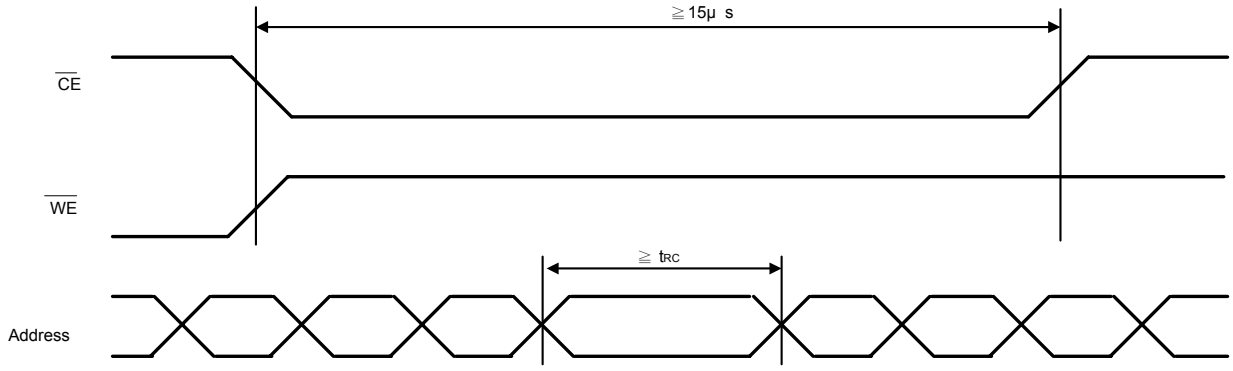
Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than tRC during over 15μs at read operation shown as in Abnormal Timing, it requires a normal read timing at leat during 15μs shown as in Avoidable timing 1 or toggle $\overline{CE}$ to high ($\geqq t_{RC}$) one time at least shown as in Avoidable Timing 2.

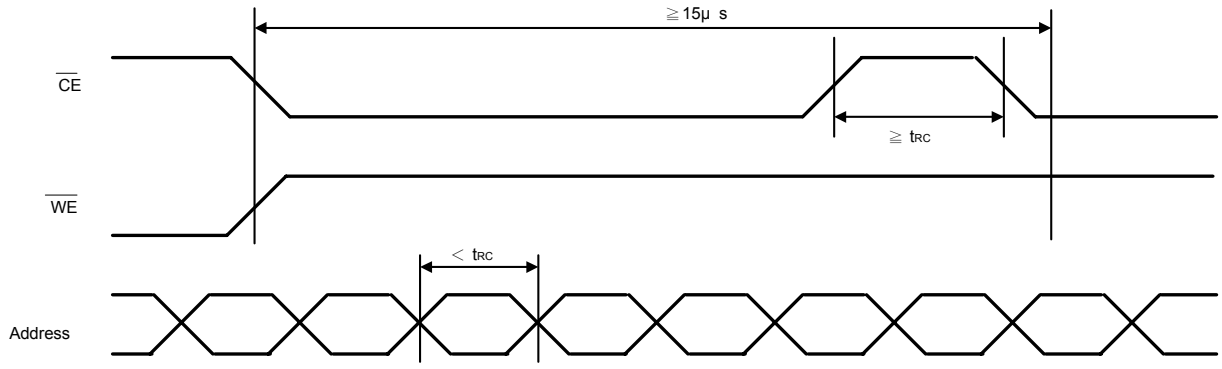
Abnormal Timing



Avoidable Timing 1



Avoidable Timing 2



Truth Table[18]

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB})
X	X	X	High Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

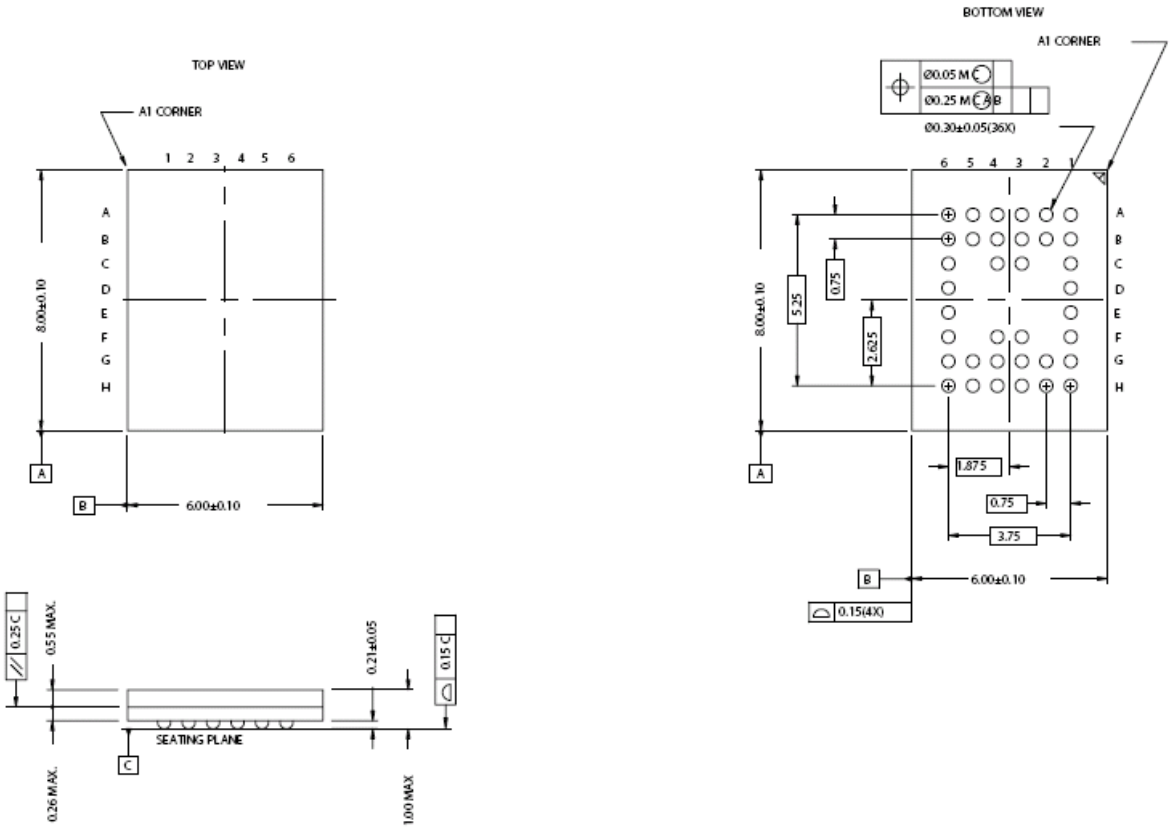
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L48512SA-55BEG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Extended
60	M24L48512SA -60BEG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Extended
70	M24L48512SA -70BEG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Extended
55	M24L48512SA-55BIG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Industrial
60	M24L48512SA-60BIG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Industrial
70	M24L48512SA-70BIG	36-Lead VFBGA (6 x 8 x 1 mm) (pb-free)	Industrial

Note:
18.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Package Diagram

36-Lead VFBGA (6 x 8 x 1 mm)



Revision History

Revision	Date	Description
1.0	2007.07.19	Original
1.1	2008.07.04	1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade 4. Add Avoid timing

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