



Lyontek Inc.

LY62L10248

Rev. 0.6

1024K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 0.1	Initial Issue	Jan.8.2007
Rev. 0.2	Revised I _{SB1} , I _{CC1} , I _{DR} , V _{DR} Delete -45ns Spec.	Nov.1.2007
Rev. 0.3	Added I _{SB} Spec.	Feb.1.2008
Rev. 0.4	Added SL Spec.	Jul.2.2008
Rev. 0.5	Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available	May.20.2009
	Added packing type in ORDERING INFORMATION Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS	
Rev. 0.6	Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised I _{DR} Spec.	Oct.29.2009



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FEATURES

- Fast access time : 55/70ns
- Low power consumption:
Operating current : 30/20mA (TYP.)
Standby current : 5 μ A (TYP.) LL-version
1.5 μ A (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62L10248 is a 8,388,608-bit low power CMOS static random access memory organized as 1,048,576 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

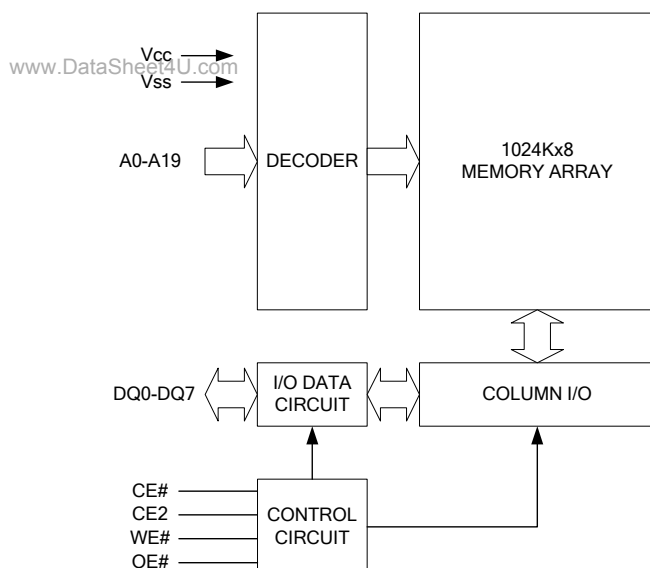
The LY62L10248 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L10248 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62L10248	0 ~ 70°C	2.7 ~ 3.6V	55/70ns	5 μ A(LL)/1.5 μ A(SL)	30/20mA
LY62L10248(E)	-20 ~ 80°C	2.7 ~ 3.6V	55/70ns	5 μ A(LL)/1.5 μ A(SL)	30/20mA
LY62L10248(I)	-40 ~ 85°C	2.7 ~ 3.6V	55/70ns	5 μ A(LL)/1.5 μ A(SL)	30/20mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

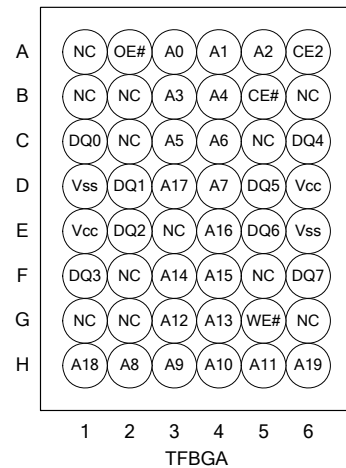
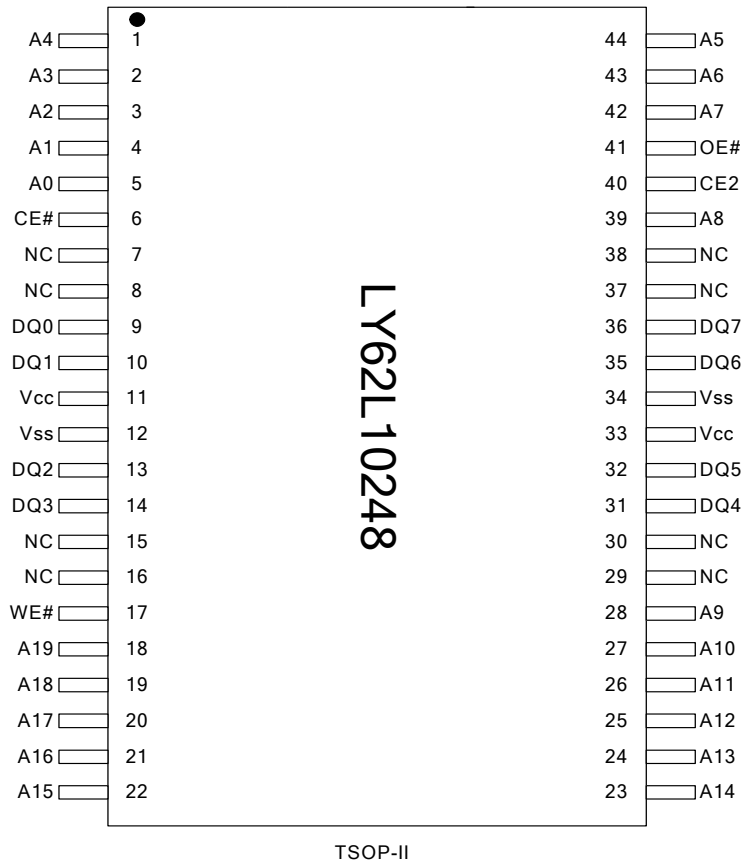


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PIN CONFIGURATION



**LY62L10248**

Rev. 0.6

1024K X 8 BIT LOW POWER CMOS SRAM**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB} , I _{SB1}
	X	L	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



LY62L10248

Rev. 0.6

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}			2.7	3.0	3.6	V	
Input High Voltage	V _{IH} ^{*1}			2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ^{*2}			- 0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled		- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA		2.2	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	- 55	-	30	40	mA	
			- 70	-	20	30	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	4	8	mA		
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}		-	0.15	1	mA	
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	5	30	μA	
			LLE	-	5	40	μA	
			LLI	-	5	50	μA	
			SL ^{*5} SLE ^{*5} SLI ^{*5}	25°C	-	1.5	5	μA
			SL ^{*5} SLE ^{*5} SLI ^{*5}	40°C	-	1.5	5	μA
			SL	-	1.5	15	μA	
			SLE	-	1.5	15	μA	
			SLI	-	1.5	20	μA	

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

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**LY62L10248**

Rev. 0.6

1024K X 8 BIT LOW POWER CMOS SRAM**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	LY62L10248-55		LY62L10248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	LY62L10248-55		LY62L10248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

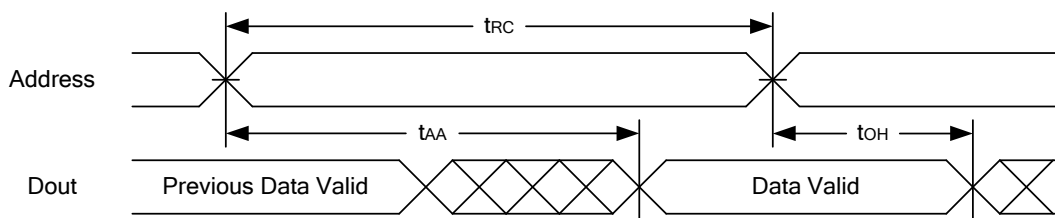
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Rev. 0.6

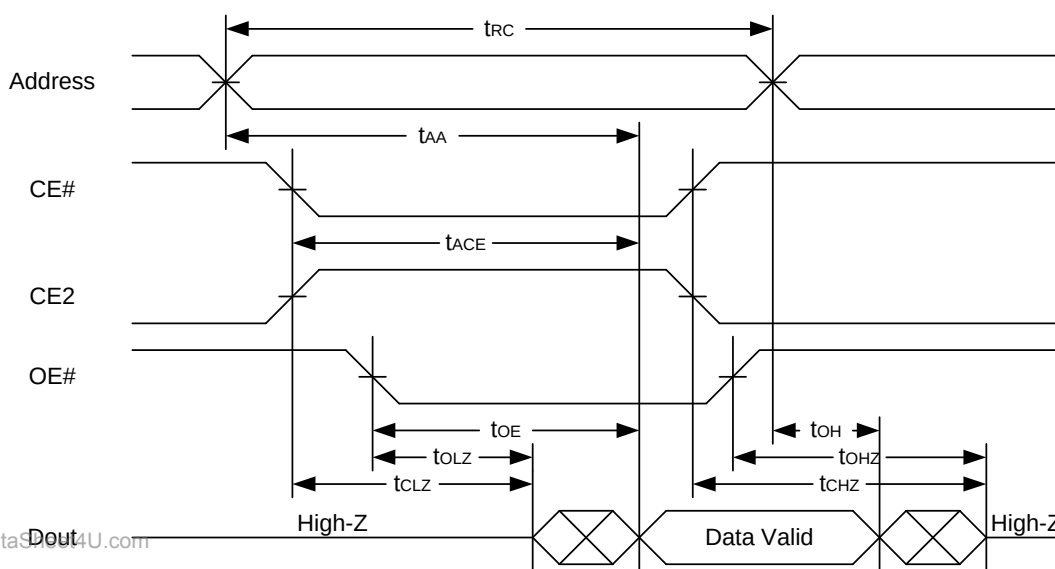
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TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



LY62L10248

Rev. 0.6

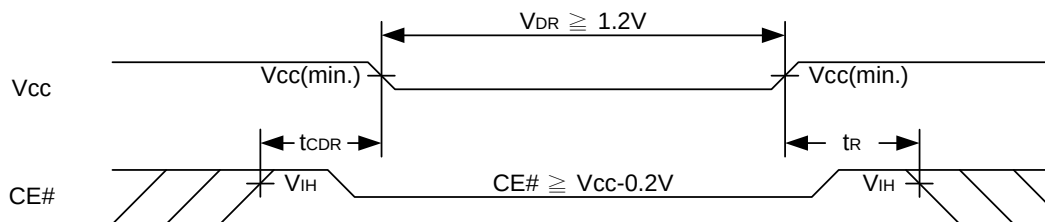
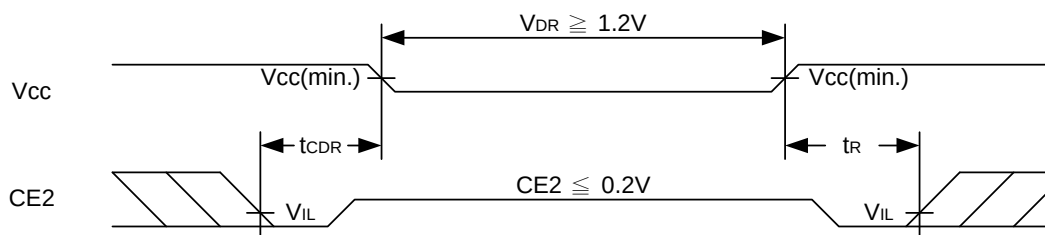
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DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V	1.2	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.2V CE# $\geq$ V _{CC} -0.2V or CE2 $\leq$ 0.2V other pins at 0.2V or V _{CC} -0.2V	LL	-	2	25 μ A
			LLE	-	2	30 μ A
			LLI	-	2	40 μ A
			SL	25°C	1	3 μ A
			SLE	40°C	1	3 μ A
			SLI			
			SL/SLE	-	1	15 μ A
			SLI	-	1	20 μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

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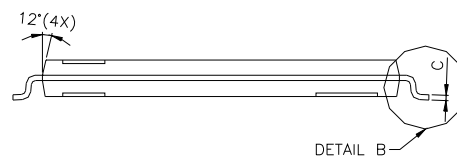
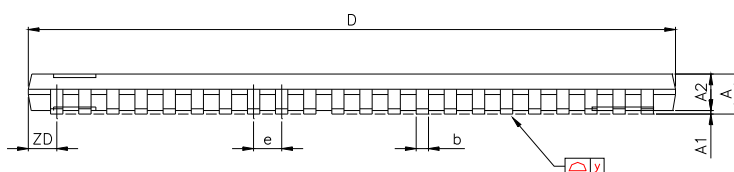
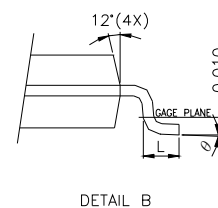
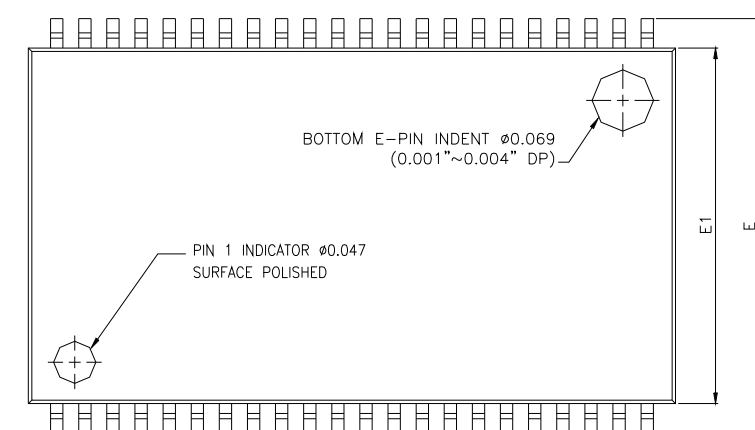
LY62L10248

Rev. 0.6

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PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension



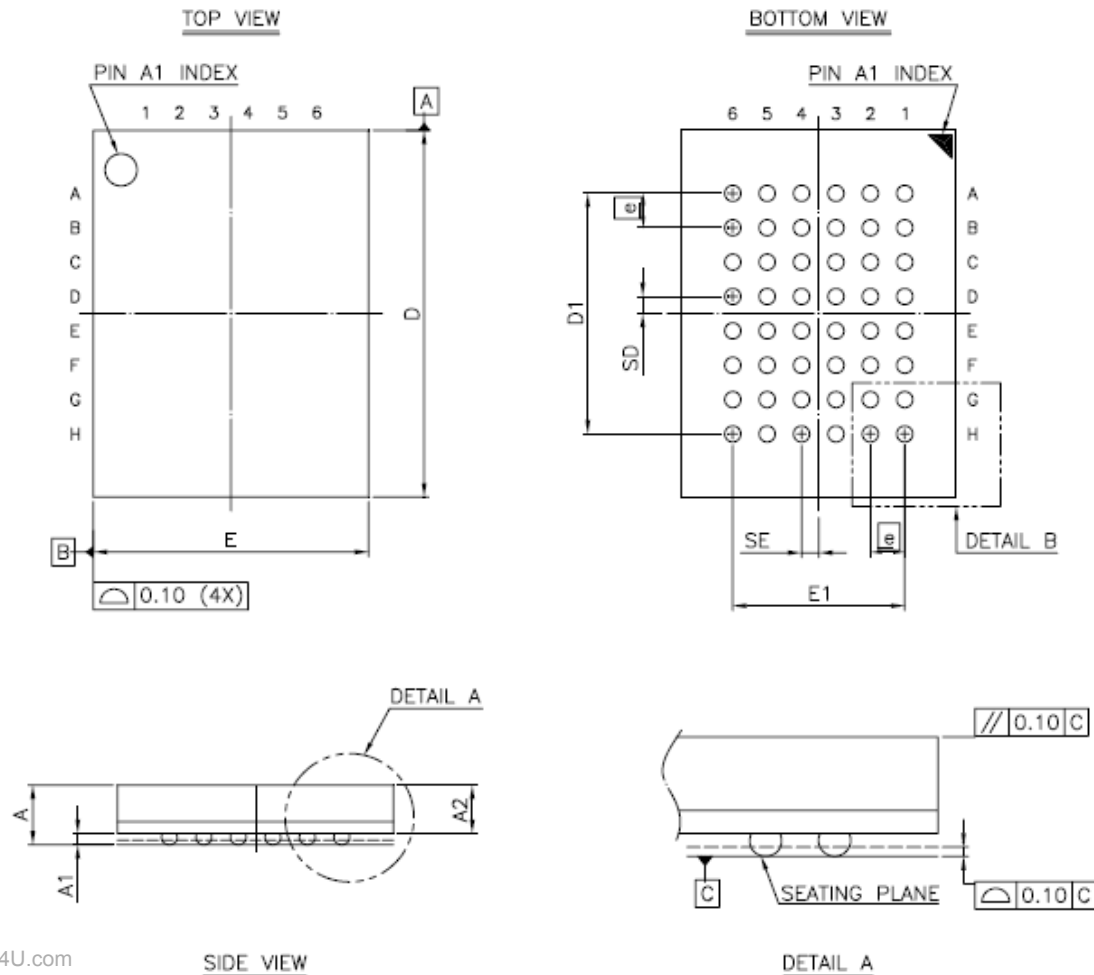
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

LY62L10248

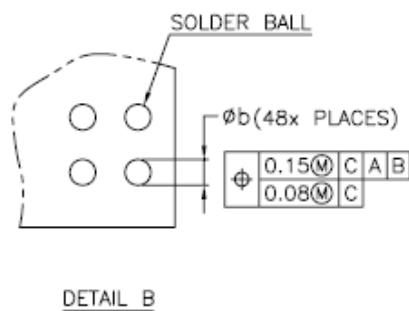
Rev. 0.6

1024K X 8 BIT LOW POWER CMOS SRAM

48-ball 6mm × 8mm TFBGA Package Outline Dimension



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SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
Ⓢ	0.75 BSC			0.030 BSC		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



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ORDERING INFORMATION

LY62L10248 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray

T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C

E : (Extended) -20°C ~ +80°C

I : (Industrial) -40°C ~ +85°C

XX : Power Type

LL : Ultra Low Power

SL : Special Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

M : 44-pin 400 mil TSOP-II

G : 48-ball 6 mm x 8 mm TFBGA



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