LX7714

Quad 46V, 2.5A/1.25A RLCL Power Switches for Space

Description

The LX7714 is a quad power switch with line protection that is radiation-hardened-by-design and is used for spacecraft power distribution. It provides a means to turn on and off four independent DC loads with continuous currents up to 2.5A.

The LX7714 comprises 4 independent protected power switch sections, each capable of driving a load up to 1.25A or 2.5A, depending on the version.

The internal PMOS power switches use slew limiting when turned on and off to control power switching to capacitive loads, and to manage the switching off of inductive loads. A power switch automatically opens the circuit in the event of an overload condition. The overload condition is a function of fault current over time; more severe fault conditions cause the switch to open faster.

Each power switch has an individual differential ON/OFF control input pair which directly interfaces to single-ended logic or an RS-422 type bus. Power switches default to the ON state with open-circuit control inputs.

A tripped power switch enters hiccup mode, that allows a die cool-down period for 10s with the load disconnected before retrying. Up to 4,096 cool-down/retry cycles are attempted before the power switch latches OFF.

Each channel includes complementary Power Good and In Reset logic status outputs for telemetry purposes. Power Good is asserted when the device is supplying nominal power to the load. In Reset status is asserted when the device is in hiccup fault recovery mode.

Each power switch has thermal shutdown for secondary protection in the unlikelihood of a malfunction with the primary overload protection function.

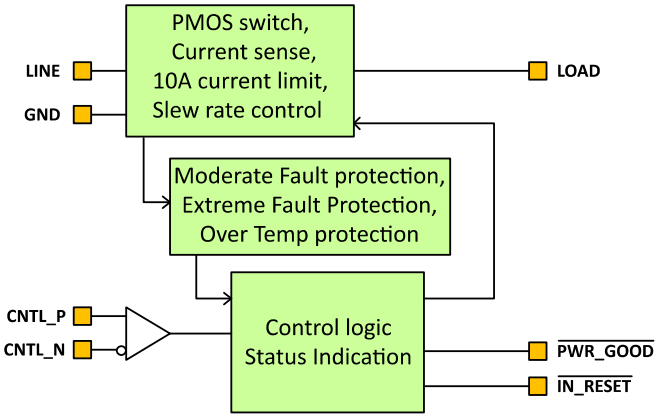
The LX7714 is packaged in a 28-pin hermetic ceramic flatpack (CFP) package. It operates over a -55°C to 125°C temperature range and is radiation tolerant to a minimum of 100krad(Si) TID and a minimum of 50krad(Si) ELDRS, as well as single event effects.

Features

- Four internal 2.5A or 1.25A rated power switches
- Power switches can be paralleled up to 10A
- Switches voltages to 46V
- Built-in fuse-like I^2t current limiting
- Safe management of soft overload faults
- Automatic hiccup retry timer to clear faults
- Power Good and Fault status outputs
- Differential ON and OFF control inputs
- Low power switch voltage drop
- Over temperature shutdown
- Load current slew rate control
- Small hermetic 28 lead ceramic flatpack package
- Radiation tolerant: 100krad(Si) TID, 50krad(Si) ELDRS, SEL immune up to 60 MeV.cm²/mg and 125°C (fluence of 10^7 particles/cm²)

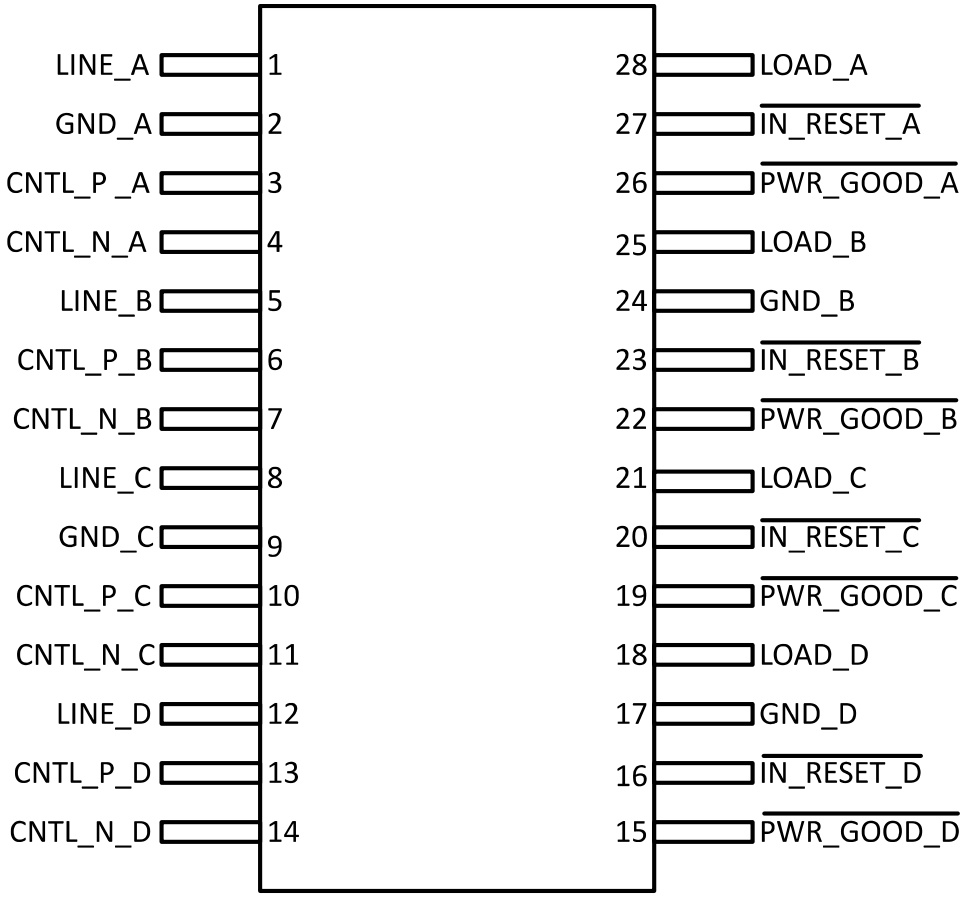
Applications

- Spacecraft power control and distribution



One of Four Independent Power Switches

1 CFP-28 Pin Configuration and Pinout



Notes

1. The LX7714 comprises 4 independent die bonded within a common package
2. The metal package top is electrically isolated from the body of the package, and should either remain isolated or be connected to GND if the four power switch ground pins share a common GND connection
3. Use the base of the package as the surface for conducting heat from the package. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so is inferior to the base of the package for heat removal. The leads can be formed to mount the package upside down on the PCB if convenient

2 Ordering Information

Operating Temperature	Package Type	Package	Part Number	Current Rating	SMD Number	Flow	Shipping Type
-55°C to 125°C	Hermetic Ceramic	CFP-28L	LX7714-25MFB-EV	2.5A	TBD	MIL-PRF-38535 Class V	Tray
			LX7714-25MFB-EQ		TBD	MIL-PRF-38535 Class Q	
	Ceramic		LX7714-25MFB-ES		-	Engineering Sample	
	Hermetic Ceramic		LX7714-12MFB-EV	1.2A	TBD	MIL-PRF-38535 Class V	
			LX7714-12MFB-EQ		TBD	MIL-PRF-38535 Class Q	
	Ceramic		LX7714-12MFB-ES		-	Engineering Sample	
			MECH-SAMPLE-CSOIC28	-	-	Empty Package Sample	

3 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	LINE_A	Power	Power switch A input supply	Connect to the power supply to be switched by power switch A. This is also the supply to the switch's control section. Bypass with a ≥47nF capacitor to GND_A
2	GND_A	Power	Power switch A GND	Ground for power switch A
3	CNTL_P_A	Logic Input	Power switch A active high ON/OFF control	Active high enable input for power switch A. CNTL_P_A is half of the differential enable input comprising active high CNTL_P_A and active low CNTL_P_A. Turn power switch A on by either setting {CNTL_P_A = high, CNTL_N_A = low) or leaving both CNTL_P_A and CNTL_N_A open
4	CNTL_N_A	Logic Input	Power switch A active low ON/OFF control	Active low enable input for power switch A. CNTL_N_A is half of the differential enable input comprising active low CNTL_P_A and active high CNTL_P_A. Turn power switch A on by either setting {CNTL_P_A = high, CNTL_N_A = low) or leaving both CNTL_P_A and CNTL_N_A open
5	LINE_B	Power	Power switch B input supply	Connect to the power supply to be switched by power switch B. This is also the supply to the switch's control section. Bypass with a ≥47nF capacitor to GND_B
6	CNTL_P_B	Logic Input	Power switch B Active high ON/OFF control	Active high enable input for power switch B. CNTL_P_B is half of the differential enable input comprising active high CNTL_P_B and active low CNTL_P_B. Turn power switch B on by either setting {CNTL_P_B = high, CNTL_N_B = low) or leaving both CNTL_P_B and CNTL_N_B open
7	CNTL_N_B	Logic Input	Power switch B Active low ON/OFF control	Active low enable input for power switch B. CNTL_N_B is half of the differential enable input comprising active low CNTL_P_B and active high CNTL_P_B. Turn power switch B on by either setting {CNTL_P_B = high, CNTL_N_B = low) or leaving both CNTL_P_B and CNTL_N_B open
8	LINE_C	Power	Power switch C input supply	Connect to the power supply to be switched by power switch C. This is also the supply to the switch's control section. Bypass with a ≥47nF capacitor to GND_C
9	GND_C	Power	Power switch C GND	Ground for power switch C
10	CNTL_P_C	Logic Input	Power switch C Active high ON/OFF control	Active high enable input for power switch C. CNTL_P_C is half of the differential enable input comprising active high CNTL_P_C and active low CNTL_P_C. Turn power switch C on by either setting {CNTL_P_C = high, CNTL_N_C = low) or leaving both CNTL_P_C and CNTL_N_C open
11	CNTL_N_C	Logic Input	Power switch C Active low ON/OFF control	Active low enable input for power switch C. CNTL_N_C is half of the differential enable input comprising active low CNTL_P_C and active high CNTL_P_C. Turn power switch C on by either setting {CNTL_P_C = high, CNTL_N_C = low) or leaving both CNTL_P_C and CNTL_N_C open
12	LINE_D	Power	Power switch D input supply	Connect to the power supply to be switched by power switch D. This is also the supply to the switch's control section. Bypass with a ≥47nF capacitor to GND_D
13	CNTL_P_D	Logic Input	Power switch D Active high ON/OFF control	Active high enable input for power switch D. CNTL_P_D is half of the differential enable input comprising active high CNTL_P_D and active low CNTL_P_D. Turn power switch D on by either setting {CNTL_P_D = high, CNTL_N_D = low) or leaving both CNTL_P_D and CNTL_N_D open
14	CNTL_N_D	Logic Input	Power switch D Active low ON/OFF control	Active low enable input for power switch D. CNTL_N_D is half of the differential enable input comprising active low CNTL_P_D and active high CNTL_P_D. Turn power switch D on by either setting {CNTL_P_D = high, CNTL_N_D = low) or leaving both CNTL_P_D and CNTL_N_D open
15	$\overline{\text{PWR\_GOOD\_D}}$	Logic Output	Power switch D status-good indicator	Active low open drain status output indicating that power switch D is enabled and is operating normally
16	$\overline{\text{IN\_RESET\_D}}$	Logic Output	High side rail power source	Active low open drain status output indicating that power switch D is in fault recovery (hiccup) mode
17	GND_D	Power	Power switch D GND	Ground for power switch D
18	LOAD_D	Power	Power switch D load	Connect to the load to be switched by power switch D
19	$\overline{\text{PWR\_GOOD\_C}}$	Logic Output	Power switch C status-good indicator	Active low open drain status output indicating that power switch C is enabled and is operating normally
20	$\overline{\text{IN\_RESET\_C}}$	Logic Output	High side rail power source	Active low open drain status output indicating that power switch C is in fault recovery (hiccup) mode
21	LOAD_C	Power	Power switch C load	Connect to the load to be switched by power switch C
22	$\overline{\text{PWR\_GOOD\_B}}$	Logic Output	Power switch B status-good indicator	Active low open drain status output indicating that power switch B is enabled and is operating normally
23	$\overline{\text{IN\_RESET\_B}}$	Logic Output	High side rail power source	Active low open drain status output indicating that power switch B is in fault recovery (hiccup) mode
24	GND_B	Power	Power switch B GND	Ground for power switch B
25	LOAD_B	Power	Power switch B load	Connect to the load to be switched by power switch B
26	$\overline{\text{PWR\_GOOD\_A}}$	Logic Output	Power switch A status-good indicator	Active low open drain status output indicating that power switch A is enabled and is operating normally
27	$\overline{\text{IN\_RESET\_A}}$	Logic Output	High side rail power source	Active low open drain status indicating that power switch A is in fault recovery (hiccup) mode
28	LOAD_A	Power	Power switch A load	Connect to the load to be switched by power switch A

4 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Line voltage (V_{LINE_x}) relative to GND_x	-0.7	58	V
Load voltage relative to line voltage (V_{LOAD_x} - V_{LINE_x})	-58	0.7	V
Ground voltage (GND_x) of any section relative to GND_x of any other section	-TBD	TBD	V
Logic input voltage ($V_{CNTL\_P\_x}$, $V_{CNTL\_N\_x}$) relative to GND_x	-7	12	V
Logic output voltage ($V_{\overline{IN\_RESET\_x}}$, $V_{\overline{PWR\_GOOD\_x}}$) relative to GND_x	-0.7	13	V
Output current ($I_{\overline{IN\_RESET\_x}}$, $I_{\overline{PWR\_GOOD\_x}}$) for digital outputs		5	mA
Load current (I_{LOAD}) for LX7714-25MFB. Positive current is internally limited	-0.1	12.5	A
Load current (I_{LOAD}) for LX7714-12MFB. Positive current is internally limited	-0.1	6.2	A
Operating junction temperature	-55	150	ºC
Storage junction temperature	-65	160	ºC
Peak lead solder temperature (10 seconds)		275	ºC

5 Electrostatic Discharge Ratings

JEDEC JEP155 states that 500V HBM allows safe manufacturing with a standard ESD controlled process.
JEDEC JEP157 states that 250V CDM allows safe manufacturing with a standard ESD controlled process.
ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±2kV
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±TBDV

6 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Line voltage (V_{LINE_x}) and load voltage (V_{LOAD_x}) relative to GND_x	14	46	V
Continuous load current (I_{LOAD}) for LX7714-25MFB (single channel)	-0.1	2.5	A
Continuous load current (I_{LOAD}) for LX7714-25MFB (two channels paralleled)	-0.2	TBD	A
Continuous load current (I_{LOAD}) for LX7714-25MFB (three channels paralleled)	-0.3	TBD	A
Continuous load current (I_{LOAD}) for LX7714-25MFB (four channels paralleled)	-0.4	TBD	A
Continuous load current (I_{LOAD}) for LX7714-12MFB (single channel)	-0.1	1.25	A
Logic input voltage ($V_{CNTL\_P\_x}$, $V_{CNTL\_N\_x}$) relative to GND_x	TBD	TBD	V
Logic output voltage ($V_{\overline{IN\_RESET\_x}}$, $V_{\overline{PWR\_GOOD\_x}}$) relative to GND_x	-0.3	12	V
Output current ($I_{\overline{IN\_RESET\_x}}$, $I_{\overline{PWR\_GOOD\_x}}$) for digital outputs		TBD	mA

7 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: V_{LINE_x} = 28V, $V_{CNTL\_P\_x}$ = 5V; $V_{CNTL\_N\_x}$ = 0V; external 10kΩ pullup resistor to 5V on $\overline{IN\_RESET\_x}$ and $\overline{PWR\_GOOD\_x}$ outputs. Typical parameters refer to T_J = 25°C. Positive currents flow into pins.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating Current (for one channel only)						
I_{GND}	Normal current		-10	-5		mA
	Standby current	$V_{CNTL\_P\_x}$ = 0V; $V_{CNTL\_N\_x}$ = 5V	-0.5	-0.25		mA
	Standby current at 125°C		TBD		TBD	mA
POR Detection						
V_{LINE_POR}	LINE power on reset threshold	Voltage rising relative to GND	8	10	12	V
$V_{LINE\_POR\_HYST}$	LINE power on reset hysteresis	$V_{LINE\_POR\_HYST}$ = $V_{LINE\_POR(rising)}$ - $V_{LINE\_POR(falling)}$	TBD	1	TBD	
T_{POR}	Power on reset delay	Step V_{LINE_x} to V_{LOAD_x} = 5% of V_{LINE}	50	150	300	µs
Switch Characteristics						
$V_{LINE-LOAD}$	Power switch voltage drop LX7714-25MFB	V_{LINE_x} - V_{LOAD_x}; I_{LOAD_x} = -1A			250	mV
	Power switch voltage drop LX7714-12MFB				500	mV
$R_{LINE-LOAD}$	Power switch resistance LX7714-25MFB	Between LINE_x and LOAD_x; I_{LOAD_x} = -1A			250	mΩ
	Power switch resistance LX7714-12MFB				500	mΩ
I_{LOAD}	Power switch off leakage	$V_{CNTL\_P\_x}$ - $V_{CNTL\_N\_x}$ < -1.2V; V_{LOAD_x} = GND			10	µA
t_{DELAY}	Turn off delay	From CNTL_x_x to V_{LOAD_x} = 23V, I_{LOAD_x} = 1A	7	50	150	µs
	Turn on delay	From CNTL_x_x to V_{LOAD_x} = 5V, I_{LOAD_x} = 1A	5	30	100	µs
dV/dt_{LOAD}	Rising load slew rate	Off to On transition (20% to 80%)	1.0	2.5	4.0	V/ µs
	Falling load slew rate	On to Off transition (80% to 20%)	-4.0	-2.5	-1.0	
I_{LOAD}	Load current limit LX7714-25MFB	Momentary output fault	7.5	10	12.5	A
	Load current limit LX7714-12MFB	Momentary output fault	3.7	5	6.2	A
I_{TRIP}	Trip current LX7714-25MFB	Continuous load current to guarantee trip	>2.5		3.5	A
	Trip current LX7714-12MFB	Continuous load current to guarantee trip	>1.25		1.75	A
Logic						
V_{CNTL_DIFF}	Positive Differential Input Logic Threshold	$V_{CNTL\_P\_x}$ - $V_{CNTL\_N\_x}$; ON state	2			V
	Inverted Differential Input Logic Threshold	$V_{CNTL\_P\_x}$ - $V_{CNTL\_N\_x}$; OFF state			0.8	
V_{CNTL_OPEN}	Open circuit voltage	$V_{CNTL\_P\_x}$ - $V_{CNTL\_N\_x}$; less than ±100nA		TBD		V
V_{CNTL_CM}	Common Mode Range	($V_{CNTL\_P\_x}$ + $V_{CNTL\_N\_x}$)/2; V_{CNTL_DIFF} = 2V	-6		9	V
$I_{CNTL\_P\_x}$	Input Current	$V_{CNTL\_P\_x}$ = 0V	-27	-8	-1	µA
$I_{CNTL\_N\_x}$	Input Current	$V_{CNTL\_N\_x}$ = 5V	-27	-8	-1	µA
$I_{CNTL\_P\_x}$, $I_{CNTL\_N\_x}$	Cold spare current	V_{LINE} = 0V; 0V < $V_{CNTL\_P\_x}$ or $V_{CNTL\_N\_x}$ < 5V	-12		12	µA
$V_{\overline{IN\_RESET}}$, $V_{\overline{PWR\_GOOD}}$	Logic Output Levels	High level; 10kΩ external pullup resistor to 5V	4.7	TBD	5	V
		Low output voltage; $I_{\overline{IN\_RESET\_x}}$ = 1mA and/or $I_{\overline{PWR\_GOOD\_x}}$ = 1mA	0	TBD	0.3	
$I_{\overline{IN\_RESET}}$, $I_{\overline{PWR\_GOOD}}$	Cold spare current	V_{LINE} = 0V; 0V < V_{IN_RESET} and/or V_{PWR_GOOD} < 5V	-1		1	µA

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Timing						
$t_{SETTLING}$	Turn on indicator	CNTL_x_x to $\overline{PWR\_GOOD\_x}$ (with no fault)	0	10	100	µs
		From fault removal to $\overline{PWR\_GOOD\_x}$. Depends on when the fault is removed with respect to hiccup timing	0		15	s
t_{FAULT}	Fault indicator	From application of short circuit fault to $\overline{PWR\_GOOD\_x}$ and $\overline{IN\_RESET\_x}$	0	0.1	1	ms
T_{OVLD_INT25}	Overload interrupt time at 250%	From application of 250% rated current to current falling below 10% or rated current LX7714-25MFB	0.37	0.73	1.34	s
		From application of 250% rated current to current falling below 10% or rated current LX7714-12MFB	TBD	TBD	TBD	
T_{OVLD_INT40}	Overload interrupt time at 400%	From application of 400% rated current to current falling below 10% or rated current LX7714-25MFB	23	54	122	ms
		From application of 400% rated current to current falling below 10% or rated current LX7714-12MFB	TBD	TBD	TBD	
T_{OVLD_INT60}	Overload interrupt time at 600%	From application of 600% rated current to current falling below 10% or rated current LX7714-01	6	12	24	ms
		From application of 600% rated current to current falling below 10% or rated current LX7714-02	TBD	TBD	TBD	
t_{COOL}	Hiccup cool down	From LOAD_x fault to LOAD_x recovery	5	10	15	s
$\#_{HICCUP}$	Maximum hiccup cycles	Continuous cycles prior to shutdown		4096		count
Over Temperature Detect						
$TEMP_{OT}$	Over temperature threshold	Shutdown (die temperature rising)	150		175	°C
$TEMP_{OT}$	Over temperature hysteresis	Reset (die temperature falling)		TBD		°C
t_{TEMP}	Reaction time	Delay from die temperature threshold event to OT fault detection		TBD		ms

8 Thermal Properties

Thermal resistance, θ_{JB}, is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
CFP-28	θ_{JB}	1.2	°C/W

9 Heatsink Recommendations

The LX7714 dissipates up to about 3W: ({250mV per output} x 2.5A x {4 circuits}) for the four switches at full load, plus (46V x 10mA) operating power and so thermal considerations are usually necessary. The base of the ceramic package should be used as the heat conducting surface for all but light duty applications. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. It is recommended to apply a thermal interface material between the base of the package and the heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element.

10 Functional Block Diagram

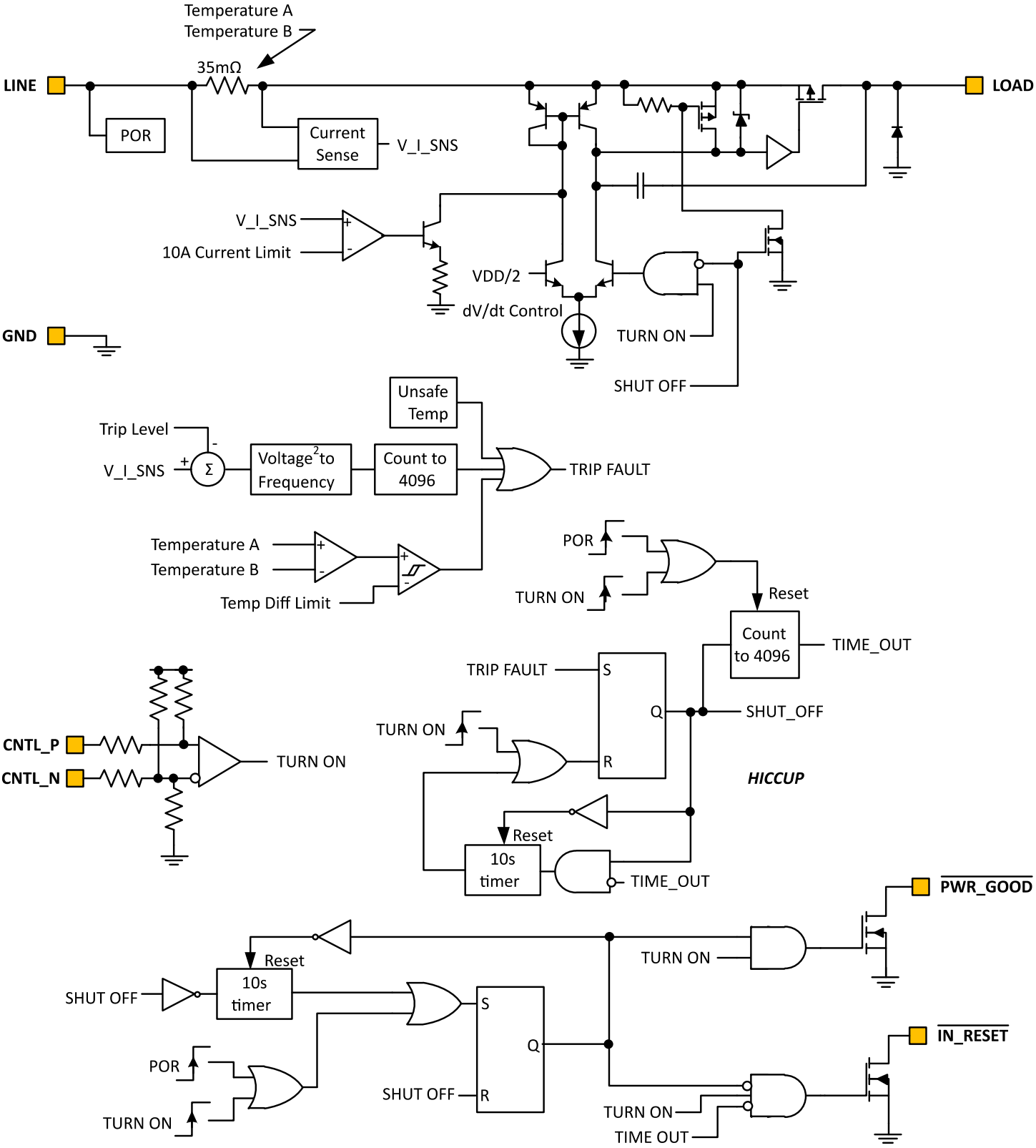


Figure 1. Functional Block Diagram (One of four independent circuits)

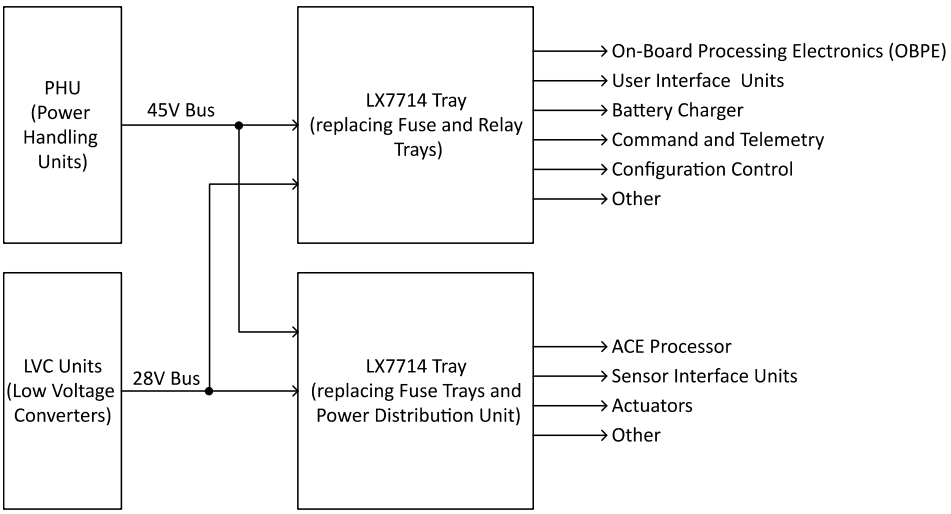


Figure 2. Typical System Application

11 LX7714 Operation

11.1 General Design Architecture

The LX7714 comprises 4 identical die mounted on electrically isolated pads within a common package. Each die contains a protected power switch section capable of driving a load up to 1.25A (LX7714-12MFB) or 2.5A (LX7714-25MFB).

The functional block architecture is shown in Figure 1 on page 7. The major functional blocks are:

- PMOS power switch with rise time control and maximum current limit
- On and off controls (CTRL_P_x and CTRL_N_x)
- Fault detection
- Fault management, status outputs, and hiccup mode timing

11.2 PMOS Power Switch

The power switch consists of a P channel MOSFET in series with a current sense resistor connecting LINE_x to LOAD_x pins. An internal current limit circuit limits the load current when the voltage drop across the sense resistor exceeds 350mV. The slew rate of the PMOS power switch turning on and off is controlled to ±1V/µs, whether the power switch is enabled on application of LINE_x power or controlled after power-up by the CTRL_P_x and CTRL_N_x logic inputs.

The four power switch sections may be paralleled in any permutation to increase load current carrying capability. The CTRL_P_x and CTRL_N_x logic inputs for paralleled power sections must be paralleled also, to ensure that paralleled power switches turn on and off together. For example, one LX7714-25MFB package can be configured to provide a single 10A switch, two 5A switches, or a 7.5A switch plus a 2.5A switch. The intrinsic positive temperature coefficient of the PMOS power switch aids current sharing, presuming that the package base is evenly attached to a heat dissipater.

11.3 On and Off Controls

The differential CTRL_P_x and CTRL_N_x logic inputs turn the respective power switch on and off. A positive differential control signal (CTRL_P_x = high, CTRL_N_x = low) turns the power switch on. An inverted differential control signal (CTRL_P_x = low, CTRL_N_x = high) turns the power switch off. The TTL 0.8V/2V input voltage levels are compatible with both 3.3V and 5V signal levels

Each control input includes an internal weak pullup (1 to 27µA) to an internal nominal 10V rail. Each power switch defaults to the ON state when both its CTRL_P_x and CTRL_N_x inputs are open circuit, achieved by internal biasing.

11.3.1 Differential Signaling

The -7V to +12V input voltage range is compatible with standard EIA-485 and EIA-422A differential signaling. Switching logic with a differential signal connection is shown in Table 1 below.

Fitting a 100kΩ (or as appropriate) pulldown resistor from CTRL_N_x to GND improves noise immunity for the power switch defaulting to the ON state, when both CTRL_P_x and CTRL_N_x inputs are open circuit.

Fitting a 100kΩ (or lower) pulldown resistor from CTRL_P_x to GND causes the power switch to default to the OFF state when both CTRL_P_x and CTRL_N_x inputs are open circuit. The resistor pulls the open circuit CTRL_P_x down towards GND (sinking 1 to 27µA), while the open circuit CTRL_N_x input is internally pulled up to about 10V.

CNTL_P_x and CNTL_N_x Inputs		Power Switch Condition
Specification	Example Operation	
$V_{CNTL\_P\_x} - V_{CNTL\_N\_x} \le 0.8V$	$V_{CNTL\_P\_x}$ = GND, $V_{CNTL\_N\_x}$ = 3.3V or 5V	OFF
$V_{CNTL\_P\_x} - V_{CNTL\_N\_x} \ge 2V$	$V_{CNTL\_P\_x}$ = 3.3V or 5V, $V_{CNTL\_N\_x}$ = GND	ON

Table 1. CTRL_P_x and CTRL_N_x Logic Inputs Truth Table (Differential Signaling)

11.3.2 Single-Ended Signaling

Connect CTRL_N_x to GND to use a single logic output connected to CTRL_P_x as the active-high control signal. (Table 2 below). A power switch will default to the ON state when the CTRL_P_x input is open circuit since the open circuit CTRL_P_x input will be internally pulled up to about 10V while the CTRL_N_x input is grounded.

CNTL_P_x	CNTL_N_x	Power Switch Condition	Default with CNTL_P_x = Hi-Z
Logic high: $V_{CNTL\_P\_x} \ge 2V$	GND	ON	Power switch ON
Logic low: $V_{CNTL\_P\_x} \le 0.8V$		OFF	

Table 2. CTRL_P_x and CTRL_N_x Logic Inputs Truth Table (Control by Single Active High Logic Level)

Table 3 below shows the truth table to use a single logic output connected to CTRL_N_x for an active-low control signal. Bias CTRL_P_x to 3V with a potential divider to an appropriate supply. A power switch will default to the OFF state when the CTRL_N_x input is open circuit, since the open circuit CTRL_N_x input will be internally pulled up to about 10V while the CTRL_P_x input is connected to 3V or lower, depending on the condition of the bias supply.

CNTL_P_x	CNTL_N_x (3.3V or 5V logic)	Power Switch Condition	Default with CNTL_N_x = Hi-Z
Bias to V_B = 3V	$V_{CNTL\_N\_x}$ = low. $V_B - V_{CNTL\_N\_x} \ge 2V$	ON	Power switch OFF
	$V_{CNTL\_N\_x}$ = high. $V_B - V_{CNTL\_N\_x} \le 0.8V$	OFF	

Table 3. CTRL_P_x and CTRL_N_x Logic Inputs Truth Table (Control by Single Active Low Logic Level)

11.4 Fault Detection

The circuit breaker can be tripped in one of three ways depending on the type of fault:

- If the LX7714 becomes detached from the heat sink and overheats, it will trigger an internal over-temperature shutdown somewhere between 150°C and 175°C
- A hard overload will cause the LX7714 to current limit, increasing dissipation in the power switch. A differential temperature sensor with a $k_H = i^2t$ profile detects the fault before the die overheats
- A soft overload current is processed with a $k_L = i^2t$ profile to provide a trip time inversely proportional to the square of the current in excess of the rated current

11.5 Fault Management, Status Outputs, and Hiccup Mode Timing

Two active low, open drain logic outputs $\overline{\text{PWR\_GOOD\_x}}$ and $\overline{\text{IN\_RESET\_x}}$ indicate the state of the power switch:

- When the power switch is off, both $\overline{\text{PWR\_GOOD\_x}}$ and $\overline{\text{IN\_RESET\_x}}$ are high-Z
- When the power switch is on, and operating normally, $\overline{\text{PWR\_GOOD\_x}}$ is active low and $\overline{\text{IN\_RESET\_x}}$ is high-Z
  - $\overline{\text{PWR\_GOOD\_x}}$ and $\overline{\text{IN\_RESET\_x}}$ may be indeterminate during turn-on into a heavy load as the current limits
- When a fault occurs $\overline{\text{PWR\_GOOD\_x}}$ is high-Z, and $\overline{\text{IN\_RESET\_x}}$ is active low during automatic fault recovery

When a fault occurs, the LX7714 enters hiccup mode. Hiccup mode begins by turning off the power switch, followed by a 10 second cool off period. Then the power switch will attempt to ramp up the output voltage. If the fault is still present, it will be sensed and the hiccup cycle will repeat. Hiccup cycles repeat for up to 4096 attempts, after which the power switch remains latched off. The power switch can be reset back to normal operation by either toggling the power input LINE_x, or by toggling the CTRL_P_x and CTRL_N_x control signals to off and then back to on again.

Hiccup mode on fault can be prevented by monitoring the LX7714's $\overline{\text{IN\_RESET\_x}}$ output to detect a falling edge indicating a fault, and then toggling the CTRL_P_x and CTRL_N_x control signals to turn the power switch off some time during the first 10 second cool off period.

Alternatively, an LX7714 $\overline{\text{IN\_RESET\_x}}$ output's falling edge can be detected and used to latch the power switch off without external intervention. The first circuit in Figure 3 uses the single-ended logic shown in Table 2 with the CTRL_N_x input grounded. The second circuit in Figure 3 uses the single-ended logic shown in Table 3 with the CTRL_P_x input biased to the midpoint of the 5V logic supply used for the NAND gates. The $\overline{\text{IN\_RESET\_x}}$ output is pulled up to the same logic supply. The single-ended ON/$\overline{\text{OFF}}$ control from the host system is now the ON input. The new FAULT output provides fault status to the host.

The NAND latch comprising N1 and N2 asserts the active high FAULT status output on the falling edge of $\overline{\text{IN\_RESET}}$, and turns off the power switch by taking the CNTL_P control input low (first circuit) or the CNTL_N control input high (second circuit). The $\overline{\text{IN\_RESET}}$ output will now return high, but the FAULT status will remain latched until the ON input is taken low. Taking ON high again will restart the power switch.

On power-up:

- If the ON control is low (for the power switch to initialize in the off state), then the NAND latch will stabilize in the correct state even if the $\overline{\text{IN\_RESET}}$ output pulses low during the power supply ramp up. The 47kΩ pulldown resistor ensures that the ON control is low if disconnected
- If the ON control is high during power-up, the NAND latch may store a false FAULT status alert if the $\overline{\text{IN\_RESET}}$ output pulses low during the power supply ramp up, and so the power switch may not initialize in the on state. The FAULT status will be cleared when the ON control is first taken low

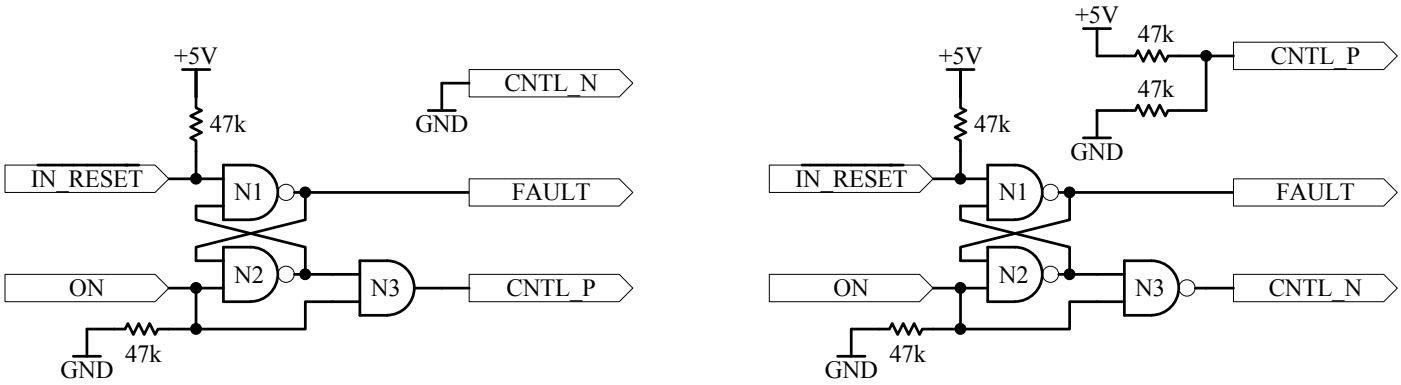


Figure 3. Single Power Switch Auto Latch-off On Fault Detection

The latch concept is easily extended to provide interlocks between switches. Figure 4 illustrates two power switches with independent on/off controls, but a fault on either power switch will cause both power switches to latch off. Also, one power switch cannot be turned on while the other has an uncleared fault. The FAULT_A and FAULT_B status outputs identify which power switch (or both) detected a fault. As before, a fault is cleared when the affected ON_x control is taken low. Note that since a non-faulty power switch may only be being held off by the other fault latch, be sure to set the non-faulty power switch to off (ON_x = 0) before setting ON_x =0 for the faulty power switch. If both power switches have faulted out, then the order doesn't matter.

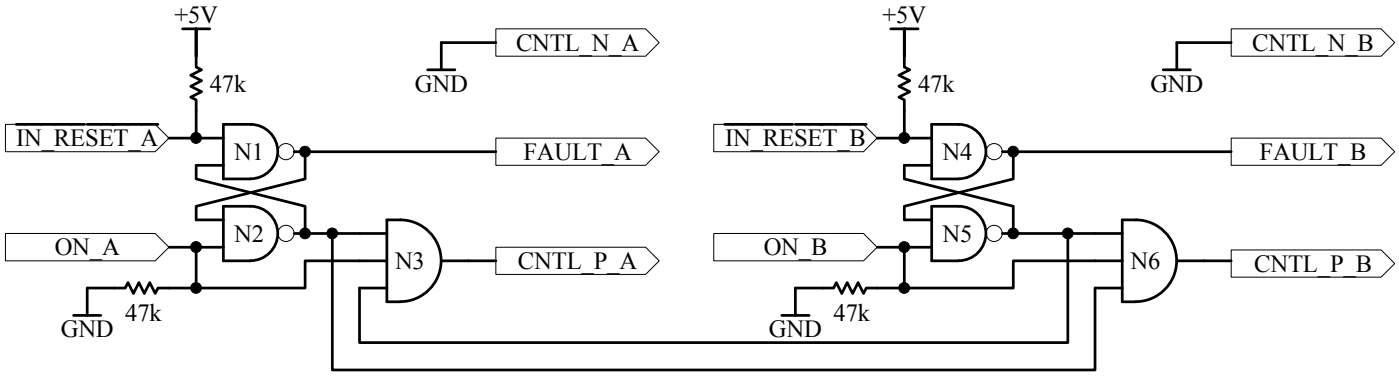


Figure 4. Dual Power Switches Both Auto Latch-off On Fault Detection on Either Switch

12 CFP-28 (Ceramic Flat Pack) Dimensions

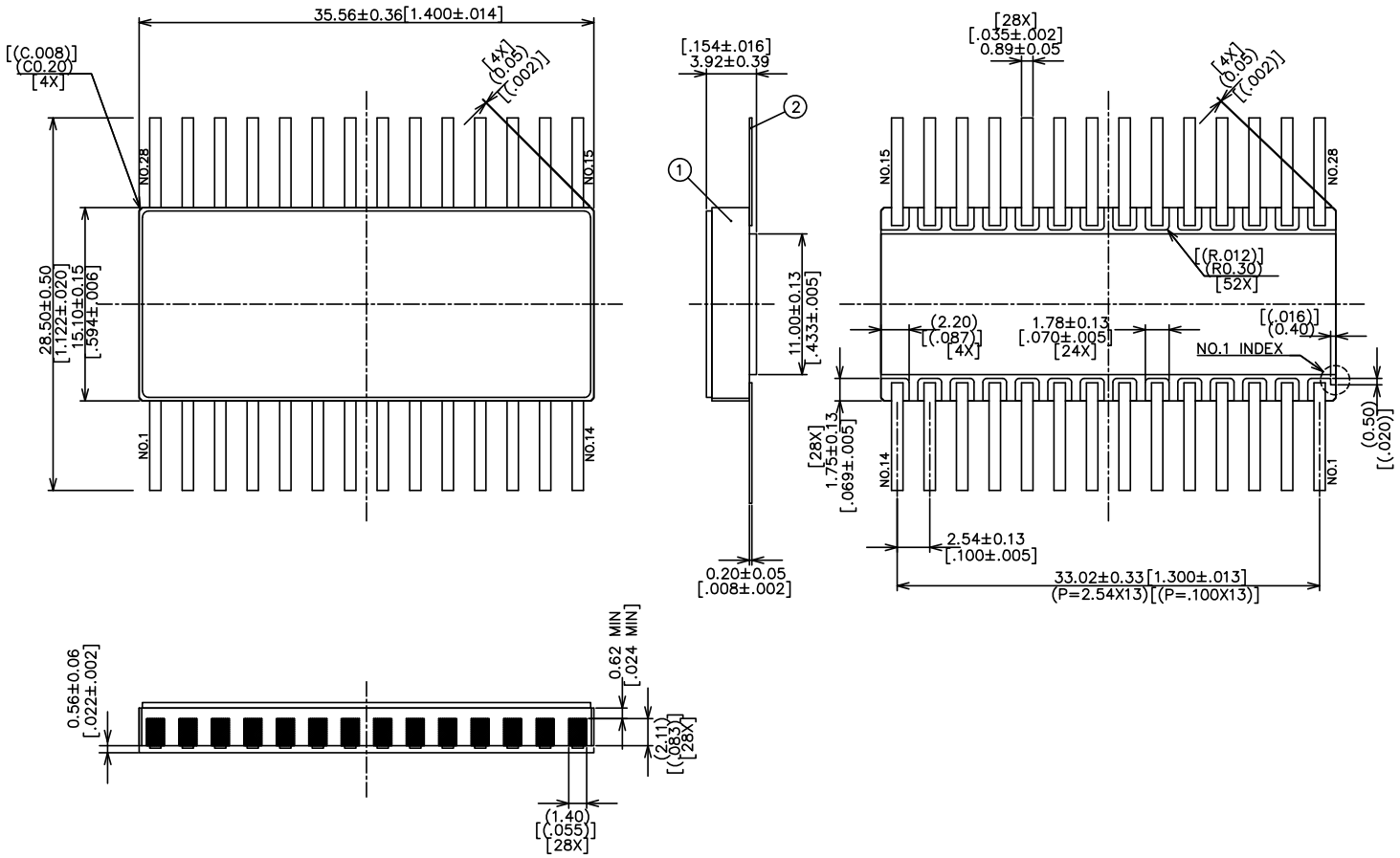


Figure 5. CFP-28 Package Dimensions

Note:
1. Controlling dimensions are in mm. Imperial (inch) equivalents are shown for general information
2. Parts are shipped with unformed leads
3. Package mass is 6.5g typical with un-cropped leads
4. Ceramic package body is NTK BA-914 HTCC Alumina (Al_2O_3)
5. Lead and lid material are Kovar with NiAu plating (nickel under-plate followed by gold plating)
6. Lid is electrically isolated from the leads, and is bonded hermetically to the ceramic body using AuSn solder
7. Use the base of the package as the surface for conducting heat from the package. The lid is attached to the package body at the top of relatively thin cavity walls, and so is inferior to the base of the package for heat removal. The leads can be formed to mount the package upside down on the PCB if convenient
8. Pin 1 is identifiable from underneath by a notch in the pad metallization

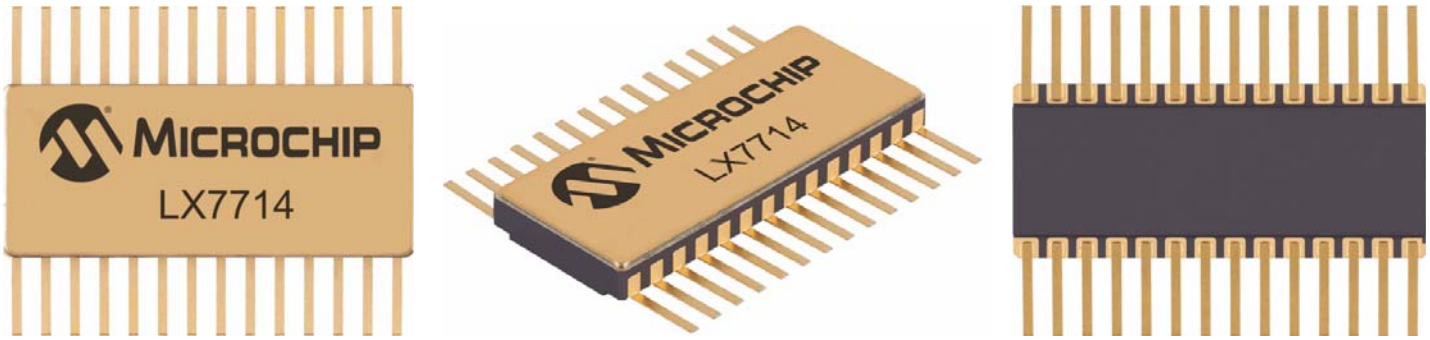


Figure 6. Package Top, Side and Bottom Views

13 Revision History

13.1 Revision 0.8 - May 2023

Pre-release. Changes not logged.

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