LX7220

2.7V to 5.5V, 6A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C

Features

- Constant Frequency Hysteretic Control
- Extremely Fast Line/Load Transient Response
- I²C for Output Adjustment (3.4 Mbps)
- 1.2 MHz Switching Frequency
- Extremely Low-R_{DSON} MOSFETs
- Input Voltage Rail 2.7V to 5.5V
- Greater than 6A Output Current
- Default Power Save Mode for Light-Load Efficiency
- UVLO, OVP, OCP
- -40°C to +85°C Ambient Temperature
- Available in VQFN 2 mm x 3 mm 14-Lead Package
- RoHS Compliant

Applications

- High Performance HDD
- Solid-State Drive
- Data Center Applications
- Raid/Host Bus Adaptors
- Optical Transceivers

General Description

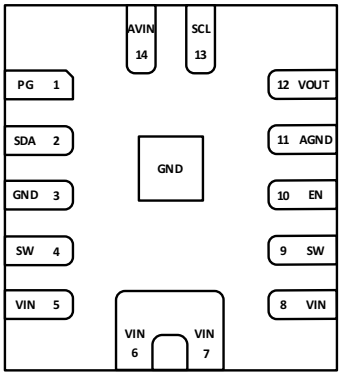
LX7220 is a digitally-controlled step-down regulator IC with an integrated 22 mΩ high-side P-channel MOSFET and a 13 mΩ low-side N-channel MOSFET. It features Microchip proprietary constant frequency hysteretic control engine for near-instantaneous correction to line/load transients. It does not require high-ESR output capacitors and incorporates energy-saving PSM (Power Save or Pulse Skip Mode) at light loads, to extend battery life in mobile applications.

LX7220 has an I²C serial interface port for output voltage margining and monitoring if required (it can also operate in default mode). In addition, it includes robust fault monitoring functions.

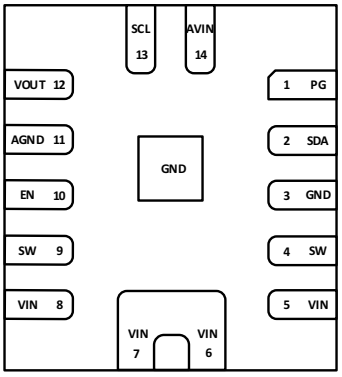
LX7220 will operate from 2.7V to 5.5V and is available in 0.95V or 0.9V output voltages (no voltage divider is necessary). The output voltage can also be adjusted with an input voltage of 5V and external voltage divider up to 3.3V.

Package Types

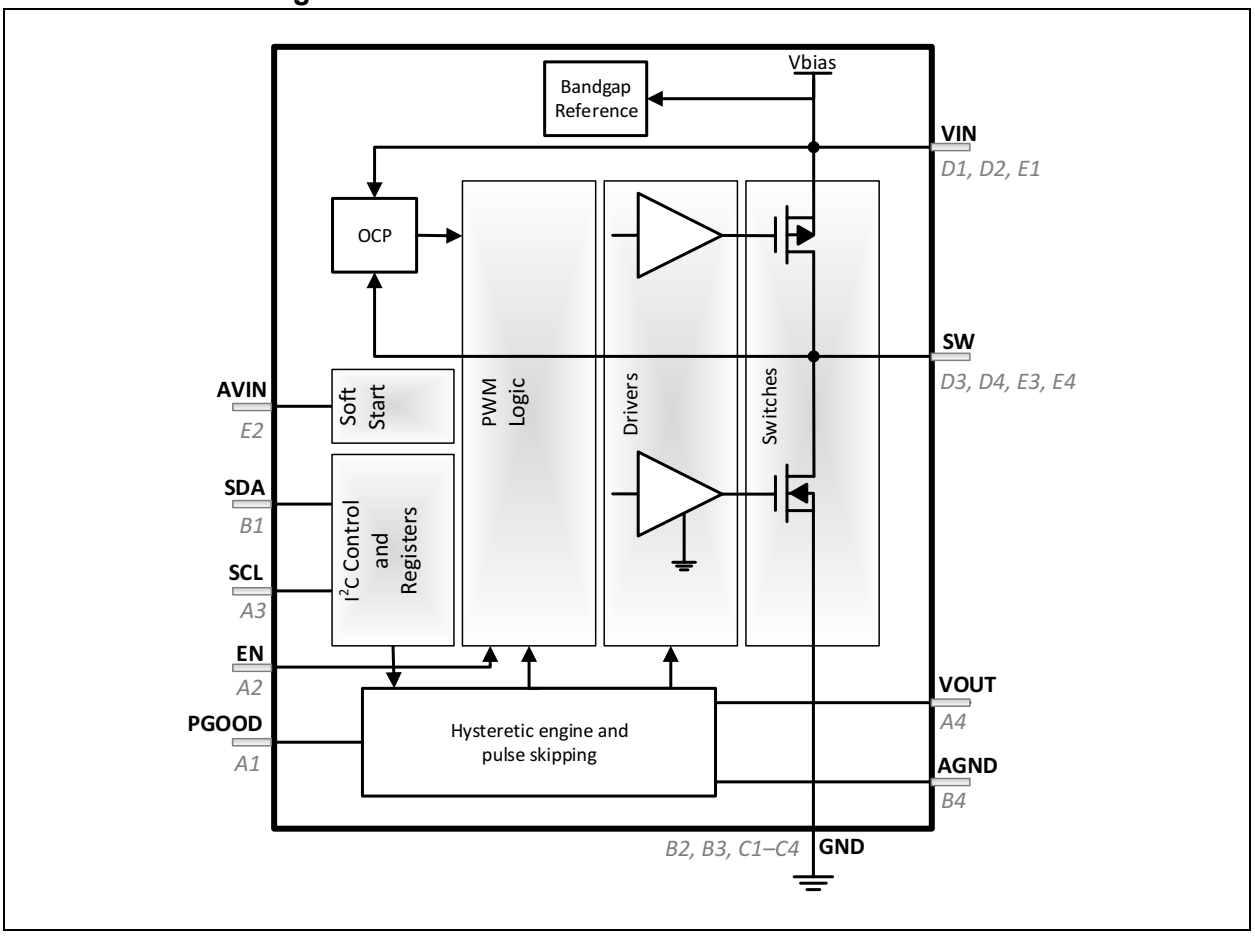
LX7220
Top View
14-Lead, VQFN, 2 mm x 3 mm



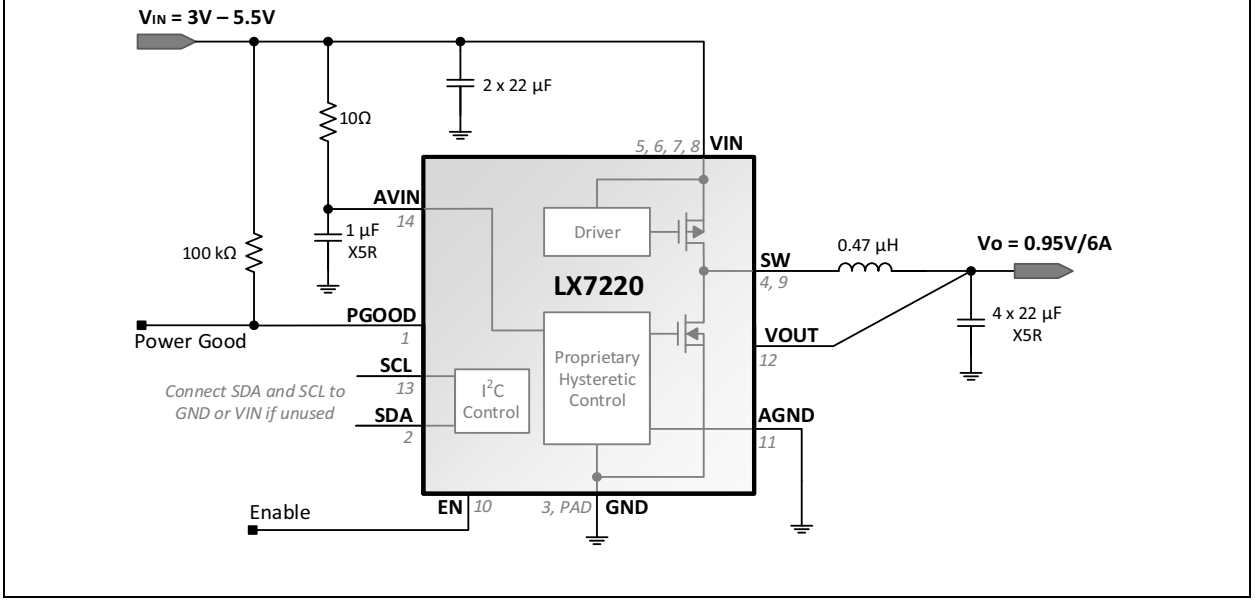
LX7220
Bottom View
14-Lead, VQFN, 2 mm x 3 mm



Functional Block Diagram



Typical Application Circuit



Applications Specifics

Efficiency	I_{OUT} = 2.0A, V_{IN} = 5V, V_{OUT} = 3.3V	95%
	I_{OUT} = 4.0A, V_{IN} = 5V, V_{OUT} = 0.8V, Inductor (IHLP-2020CZ-01)	>84%
	I_{OUT} = 4.0A, V_{IN} = 5V, V_{OUT} = 0.9V, Inductor (SPM5015)	>83%
V_{OUT} Max Transient	100 mA⇔ 4A, 1A/2 µs, C_{LOAD} = 4 × 22 µF ceramic caps, 0.47 µH inductor. Step Duration 1 µs-50 µs.	Peak to peak < 80 mV
Typical Load Inductance	IHLP2020CZ (DCR = 6.7 mΩ, I_{DC} = 12.2A, I_{SAT} = 16A) SPM5015 (DCR = 16.3 mΩ, I_{DC} = 7A, I_{SAT} = 13.8A)	0.47 µF
Typical Load Capacitance	6.3V, X5R	4×22 µF
V_{IN}, V_{OUT} Ripple Noise Measurement (EMI)	I_{OUT} = 5A, V_{IN} = 5V, V_{OUT} = 1V, Inductor (SPM5015)	<200 mV_{PP} <50 mV_{PP}
Start-Up V_{IN} inrush current with V_{OUT} pre-bias	V_{IN} = 5V, R_{LOAD} = 50Ω, C_{LOAD} = 200 µF ceramic caps, Enable f = 500 Hz, 90% duty cycle	<175 mA_{PEAK}

Ordering Information

Temperature	Package Type	Part Marking	Part Number	y-Output Voltage	x-Client Address A1A0 (Note 4)	Packaging Type
–40°C to 85°C	VQFN, 2 mm x 3 mm 14-Lead, RoHS compliant, Pb-free	MSCN 7220	LX7220-03ILQ-TR	3 = 0.95V	0 = E0h	Tape and Reel
		MSCP 7220	LX7220-13ILQ-TR		1 = E2h	
		MSCR 7220	LX7220-23ILQ-TR		2 = E4h	
		MSCS 7220	LX7220-33ILQ-TR		3 = E6h	
		MSCJ 7220	LX7220-02ILQ-TR	2 = 0.9V	0 = E0h	
		MSCK 7220	LX7220-12ILQ-TR		1 = E2h	
		MSCL 7220	LX7220-22ILQ-TR		2 = E4h	
		MSCM 7220	LX7220-32ILQ-TR		3 = E6h	

Note 1: Consult factory for other I^2C client address and set output voltage options. (LX7220-xyILQ-TR).

2: "x" is the 2 LSB bits of the binary I^2C client address (0 to 3).

3: "y" is the set output voltage (3 is 0.95V, 2 is 0.9V, 1 is 0.8, 0 is 0.85).

4: Refer to Table 4-1.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

VIN, SW to GND ..... -0.3V to +7V
AVIN, VOUT, SDA, SCL, EN, PGOOD to GND ..... -0.3V to +7V
SW to GND (Shorter than 50 ns) ..... -2V to +7V
Maximum Junction Temperature ..... +150°C
Lead Soldering Temperature (30s, reflow) ..... +260 (+0, -5)°C
Storage Temperature ..... -65°C to +150°C

Operating Ratings ‡

VIN ..... +2.7V to +5.5V
Ambient Temperature ..... -40°C to +85°C
Output Current ..... 0A to 6A

† **Notice**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{IN} = V_{EN} = 5V, SDA = SCL = 5V, default register settings. **Bold** specifications apply over the T_A range of -40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Voltage						
Input Current	I_Q	**200**	440	**600**	µA	I_{LOAD} = 0, PSM enabled
Input Current at Shut Down	I_{IN}	—	0.1	14	µA	EN = GND, T_A = 25°C
Input Current I^2C Shut Down	$I_{IN\_I^2C}$	—	100	**120**	µA	VSEL(7) = low, EN = high
Undervoltage Rising Threshold	UVLO	—	2.6	**2.89**	V	V_{IN} rising
UVLO Hysteresis	$UVLO_{HYST}$	—	0.26	—	V	
Overvoltage Rising Threshold	OVP_R	**6.05**	—	**6.40**	V	
Overvoltage Falling Hysteresis	OVP_F	—	0.2	—	V	
Reference Voltage						
V_{REF} Slew Rate	T_{SS}	—	0.8	—	mV/µs	SLEW: Ctrl2(2:1) = 01
Hiccup Time	T_{HICCUP}	—	9.8	—	ms	V_{OUT} = 0.2V
Output Voltage						
Default V_{OUT}	V_{OUT}	**0.94**	0.95	**0.959**	V	V_{OUT} = 0.95V (V_{IN} = 2.7V – 5V) VSEL = 40h
V_{OUT} I^2C VSEL		**0.743**	0.75	**0.758**	V	V_{OUT} = 0.75V (V_{IN} = 2.7V – 5V), VSEL = 20h
		0.741	0.75	0.759	V	V_{OUT} = 0.75V (V_{IN} = 2.7V – 5V), VSEL = 20h, –10°C ≤ T_A ≤ +85°C
		1.185	1.197	**1.209**	V	V_{OUT} = 1.197V (V_{IN} = 2.7V – 5V), VSEL = 7Fh
Line Regulation	—	—	0.1	—	%	V_{IN} from 3V to 5.5V, I_{LOAD} = 1A **Note 1**

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{IN} = V_{EN} = 5V, SDA = SCL = 5V, default register settings. **Bold** specifications apply over the T_A range of -40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Load Regulation	—	—	–0.23	—	%/A	I_{LOAD} = 0A to 5A. **Note 1**
V_{OUT} Input Current	—	—	0	**1**	µA	
V_{OUT} Undervoltage Threshold	V_{OUV}	**77**	82	**85**	%V_{REF}	V_{OUT} below this threshold will initiate a hiccup sequence
SW						
High Side on Resistance	R_{DSON_H}	—	22	—	mΩ	V_{IN} = 5V
Low Side on Resistance	R_{DSON_L}	—	13	—	mΩ	V_{IN} = 5V
Current Limit	OCP	7.5	8.5	10	A	**Note 1**
Thermal Shut Down Threshold	T_{SH}	—	150	—	°C	**Note 1**
Hysteresis	T_H	—	20	—	°C	**Note 1**
PWM Switching Frequency	F_{SW}	**1**	1.2	**1.4**	MHz	
SW Discharge Resistance	R_{SWDISC}	**80**	200	**1400**	Ω	EN = low, Discharge: Ctrl2(4) = 1
EN, SDA (as input), SCL						
Input High	V_{IH}	**1.1**	—	—	V	
Input Low	V_{IL}	—	—	**0.4**	V	
Hysteresis	V_H	**0.05**	0.15	—	V	
Input Current	I_{II}	—	0	**1.1**	µA	
Low Level Output Voltage	V_{OL}	0	—	0.2 × VDD	V	Logic0 output voltage, Isink = 2 mA (**Note 1**)
Low Level Output Current	I_{OL}	3	—	—	mA	V_{OL} = 0.4V (**Note 1**)
PGOOD						
PGOOD V_{OUT} Lower Threshold	V_{PG90}	**82**	85	**88**	%V_{REF}	V_{OUT} rising, percentage of V_{REF}
PGOOD V_{OUT} Upper Threshold	V_{PG110}	**105**	110	**115**	%V_{REF}	V_{OUT} falling, percentage of V_{REF}
Hysteresis	V_{PGHY}	—	5	—	%V_{REF}	Percentage of V_{REF}
PGOOD Pull Down Resistance	PG_{RDSON}	—	13	**20**	Ω	
PGOOD Leakage Current	—	—	0	**1**	µA	
PGOOD Delay	—	**27**	45	**69**	ms	PGOOD rising edge delay
7 Bit DAC						
Differential Linearity	—	—	—	0.8	LSB	Monotonicity assured by design

Note 1: Guaranteed by design.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Package Thermal Resistance						
Thermal Resistance, VQFN	θ_{JA}	—	50	—	°C/W	

Note 1: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

TABLE 1-1: I^2C TIMING SPECIFICATIONS

Parameter	Sym.	C_b = 100 pF (max) (Note 2)		C_b = 400 pF		Units	Conditions
		Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCHL}	0	3.4	0	0.4	MHz	
Set-up time for a repeated START condition	$t_{SU;STA}$	160	—	600	—	ns	
Hold time (repeated) START condition	$t_{HD;STA}$	160	—	600	—	ns	
LOW period of the SCL clock	t_{LOW}	160	—	1300	—	ns	
HIGH period of the SCL clock	t_{HIGH}	60	—	600	—	ns	
Data set-up time	$t_{SU;DAT}$	10	—	100	—	ns	
Data hold time	$t_{HD;DAT}$	0	70	0	—	ns	
Rise time of SCL signal	t_{rCL}	10	40	$20 \times 0.1C_b$	300	ns	
Rise time of SCL signal after a repeated START condition and after an acknowledge bit	t_{rCL1}	10	80	$20 \times 0.1C_b$	300	ns	
Fall time of SCL signal	t_{fCL}	10	40	$20 \times 0.1C_b$	300	ns	
Rise time of SDA signal	t_{rDA}	10	80	$20 \times 0.1C_b$	300	ns	
Fall time of SDA signal	t_{fDA}	10	80	$20 \times 0.01C_b$	300	ns	
Set-up time for STOP condition	$t_{SU;STO}$	160	—	600	—	ns	
Bus free time between a STOP and START condition	t_{BUF}	160	—	1300	—	ns	
Data valid time	$t_{VD;DAT}$	—	160	—	900	ns	
Data valid acknowledge time	$t_{VD;ACK}$	—	160	—	900	ns	
Capacitive load for each bus line	C_b	—	100	—	400	pF	SDA and SCL lines

Note 1: All values referred to V_{IH}(min) and V_{IL}(max) levels of I/O stages table.

2: Loads in excess of 100 pF will restrict bus operation speed below 3.4 MHz.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PINOUT DESCRIPTION

Pin Number	Pin Name	Description
1	PGOOD	Open Drain status output, requires external pull up resistor. This pin will go low when VOUT is outside the defined power good range, when the die is hotter than the thermal shutdown threshold, when PVIN is above the overvoltage threshold, or when PVIN is below the undervoltage threshold. PGOOD will go high after the last of these fault conditions clear.
2	SDA	Serial data bus (bidirectional) for I^2C. Connect directly to GND if unused.
3, PAD	GND	Ground. Connect to ground plane.
4, 9	SW	Switching Node. Drives the external L-C low pass filter.
5, 6, 7, 8	VIN	Input of IC and buck stage. Connect to input rail VIN (between 2.7V and 5.5V). A minimum input capacitance of one 1 µF and one 22 µF of X5R or better multilayer ceramic, should be placed very close to IC between this node and GND.
10	EN	Enable for switching regulator. Force high to enable, force low to disable the IC.
11	AGND	Analog Ground. Connect to ground plane.
12	VOUT	Output voltage sense. Connect directly to output rail or resistive voltage divider output.
13	SCL	Serial clock input for I^2C. Connect directly to GND if unused.
14	AVIN	Analog input voltage pin.

3.0 OPERATION THEORY

3.1 Basic Operation

The LX7220 compares V_{OUT} voltage to an internal reference, V_{REF}. When V_{OUT} is lower than V_{REF}, the upper switch turns on and the lower switch turns off. When V_{OUT} is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp helps to keep the switching frequency constant over a wide range of output capacitor values and parasitic components (i.e. ESR, ESL). In addition, a frequency control loop keeps the switching frequency constant during continuous conduction mode.

At light loads, if enabled, the converter automatically reduces the switching frequency and enters discontinuous conduction mode to optimize efficiency while ensuring low V_{OUT} ripple voltage.

An integrated I^2C bus interface, operating up to 3.4 Mbps, adds the following use programmability to the converter:

1. On-the-fly programming of the output voltage in 4.7 mV increments
2. Enable/Disable the regulator
3. Allow PSM or limit operation to PWM only mode
4. Set the V_{REF} slew rate
5. Switch node slew rate control.

3.2 Setting the Output Voltage

The output voltage is set with the reference voltage and how the VOUT pin (12) is connected to the output. With a direct connection (see Typical Application Circuit), the reference voltage equals the output voltage. When the VOUT pin (12) is connected to a resistor divider, this also determines the output voltage. At start-up, the reference voltage is determined by the parts number "y" parameter (i.e. LX7220-xyILQ); "y" sets the output voltage (3 is 0.95V, 2 is 0.9V). After start-up, the reference voltage can be programmed with the I^2C bus VSEL register value.

$$V_{REF} = 0.6V + N_{SEL} \times 0.0046875V \quad (2)$$

Where:

N_{SEL} is the decimal value of the 7 VSEL bits.

The output voltage is determined as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right) \quad (3)$$

Where:

R_{TOP} is the resistor connected from VOUT pin to output.

R_{BOTTOM} is the resistor connected from VOUT pin to GND.

3.3 Start-Up

If the LX7220 is enabled, when V_{IN} rises above the UVLO threshold, the regulator will initiate a start-up sequence. The serial port registers are initialized to their default values and all internal bias voltages and currents are allowed to stabilize. V_{REF} then ramps up from 0V to the default voltage, at the default slew rate. At the end of the ramp time, PGOOD is allowed to go high after V_{OUT} has reached the PGOOD rising threshold. During the ramp time, the LX7220 switches to PSM to allow discontinuous operation. This switchover is independent of the MODE bit setting.

3.4 Overcurrent Protection

LX7220 protects against all types of short circuit conditions. Cycle-by-cycle overcurrent protection turns off the upper switch when the current exceeds the OCP threshold. When this occurs, the upper switch is held off for at least 350 ns before being allowed to turn on again. After start-up, if V_{OUT} drops below the V_{OUT} undervoltage threshold, a hiccup sequence will be initiated where both output switches are shut off for 6.5 ms before initiating another soft start cycle. This protects against a crowbar short circuit. The V_{OUT} undervoltage detection is not active during start-up.

3.5 Positive Voltage Transitions

After the initial start-up sequence, the output voltage can be programmed to a new value by programming the VSEL register bits and then asserting the GO bit. V_{REF} will transition to the new value at the programmed slew rate. The PGOK monitor bit is deasserted during the V_{REF} ramp time, or when V_{OUT} is outside the error envelope.

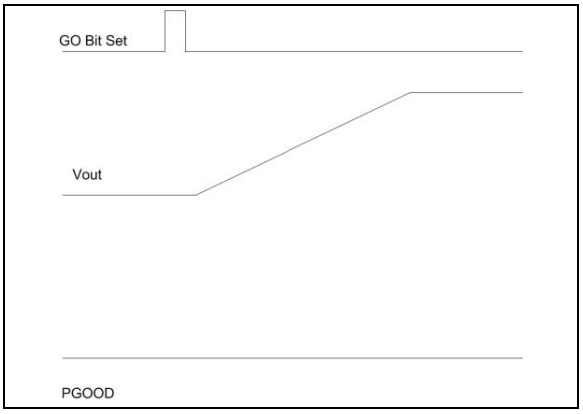


FIGURE 3-1: *Positive Voltage Transition.*

3.6 Negative Voltage Transitions

A negative voltage transition occurs when a lower output voltage is programmed into the VSEL register, and initiated by asserting the GO bit. In PSM, the LX7220 will not discharge the output filter capacitor.

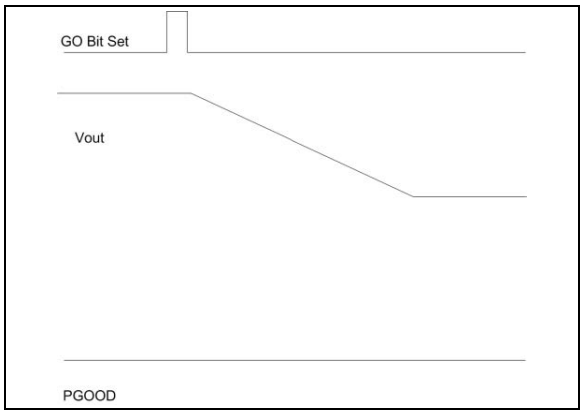


FIGURE 3-2: *Negative Voltage Transition.*

3.7 Enabling Regulator from I^2C Bus

In addition to the EN pin, the regulator can be enabled and disabled via the I^2C bus by programming the control register. During disable, the regulator and most of the support circuitry is turned off. However, the I^2C bus circuitry is still active and may be programmed.

3.8 Switch Node Rise Rate Adjustment

The LX7220 can be programmed to operate in a lower emissions mode by slowing down the switch node rise rate. In this mode, the switch node rise rate will slow down 25%, reducing the switching frequency harmonic content.

4.0 I²C INTERFACE

I²C Port Functional Description

- Simple two wire, bidirectional, serial communication port.
- Multiple devices on same bus speeds from 400 kbps (FS-Mode) to 3.4 Mbps (HS-Mode).
- SOC Host controls bus.
- Device listens for the unique address that precedes data.

4.1 General I²C Port Description

LX7220 includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage when they are not being controlled by a device on the bus. The LX7220 interface acts as an I²C client that is clocked by the incoming SCL clock. The LX7220 I²C port will support both the Fast mode (400 kHz max) and typically the High Speed mode (3.4 MHz max). The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

4.2 Register Map

LX7220 has five 8-bit user-accessible registers. See Control Register Bit Definition.

4.3 Client Address

In the table below, the A1 and A0 are the binary value of the address given in the ordering information for the “x” value shown in Ordering Information.

TABLE 4-1: I²C CLIENT ADDRESS

7	6	5	4	3	2	1	0
1	1	1	0	0	A1	A0	R/W

4.4 START and STOP Commands

When the bus is idle, both SCL and SDA must be high except in the power up case where they may be held high or low during the system power up sequence.

The STX SOC (bus host) signals START and STOP bits signify the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The STX SOC acts as the I²C host and always generates the START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transfer, STX SOC host can generate repeated START conditions. The START and the repeated START conditions are functionally equivalent.

4.5 Data Transfers

Data is transferred in 8-bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the host. The acknowledge occurs when the transmitter host releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver client during the 9th clock pulse to signify acknowledgment. A receiver client which has been addressed must generate an acknowledgement (“ACK”) after each byte has been received.

After the START condition, the STX SOC (I²C) host sends a chip address. The standard I²C address is seven bits long. Making the eighth bit a data direction bit (R/W). For the eighth bit (LSB), a “0” indicates a WRITE and a “1” indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a receiver client does not acknowledge the client address, the data line must be left HIGH by the client. The host can then generate a STOP command to abort the transfer. If a client receiver does acknowledge the client address but, sometime later in the transfer cannot receive any more data bytes, the host must again abort the transfer.
This is indicated by the client generating the not acknowledge on the first byte to follow.

The client leaves the data line HIGH and the host generates the STOP command. The data line is also left high by the client and host after a client has transmitted a byte of data to the host in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

4.6 Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid STOP command has been performed.

4.7 I²C Electrical Characteristics

The minimum HIGH and LOW periods of the SCL clock specified the I²C Timing Specification table determine the maximum bit transfer rates of, 400 kbits/s for Fast-mode devices, and 3.4 Mbits/s for HS-mode Plus. Devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the I²C clock synchronization procedure, which will force the host into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Figure 4-3 and Figure 4-4 show all timing parameters for the HS & FS-mode timing. The 'normal' START condition S does not exist in HS-mode. Timing parameters for Address bits, R/W bit, Acknowledge bit and DATA bits are all the same. Only the rising edge of the first SCL clock signal after an acknowledge bit has a larger value because the external Rp has to pull-up SCL without the help of the internal current-source.

The HS & FS-mode timing parameters for the bus lines are specified in the Table 1-1. The minimum HIGH and LOW periods and the maximum rise and fall times of the SCL clock signal determine the highest bit rate.

With an internally generated SCL signal with LOW and HIGH level periods of 200 ns and 100 ns respectively, an HS-mode host fulfills the timing requirements for the external SCL clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4 Mbit/s. So a basic frequency of 10 MHz, or a multiple of 10 MHz, can be used by an HS-mode host to generate the SCL signal. There are no limits for maximum HIGH and LOW periods of the SCL clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load up to 100 pF for each bus line allowing the maximum possible bit rate of 3.4 Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400 pF are specified in Table 1-1, allowing a maximum bit rate of 1.7 Mbit/s. For capacitive bus loads between 100 pF and 400 pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDA and SCL to prevent reflections of the open ends.

1	7	1	1	8	1	8	1	1
Start	xxxxxxx Device Address	0 Write	Ack	xxxxxxxx Register Address	Ack	xxxxxxxx Data	Ack	Stop

FIGURE 4-1: *Write Protocol.*

1	7	1	1	8	1	1	7	1	1	8	1	1
Start	xxxxxxx Device Address	0 Write	Ack	xxxxxxxx Register Address	Ack	Repeated Start	xxxxxxx Device Address	1 Read	Ack	xxxxxxxx Data	Host Ack	Stop

FIGURE 4-2: *Read Protocol.*

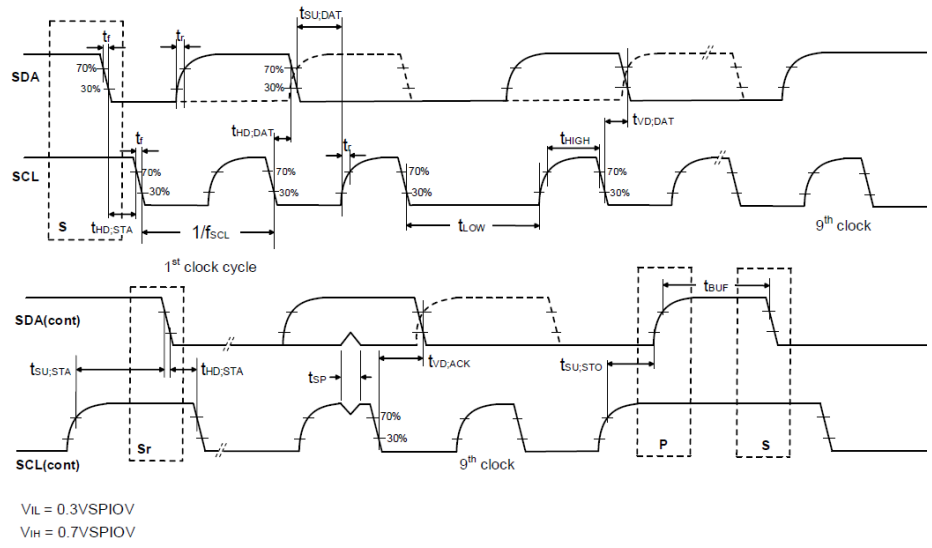


FIGURE 4-3: *Definition for FS-Mode Devices on the I²C Port.*

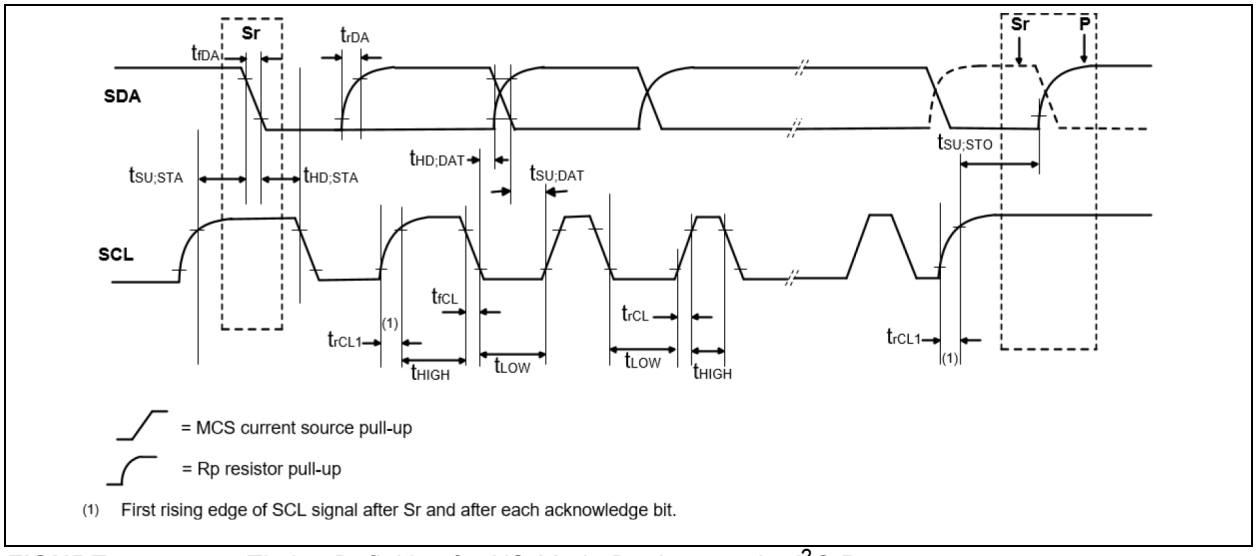


FIGURE 4-4: *Timing Definition for HS-Mode Devices on the I²C Port.*

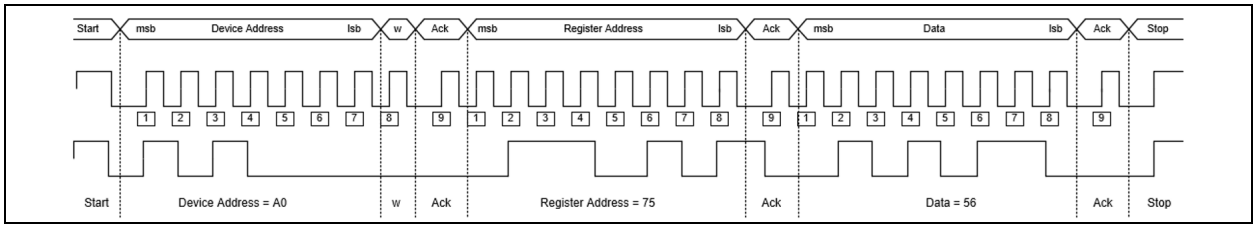


FIGURE 4-5: *Write Cycle Diagram.*

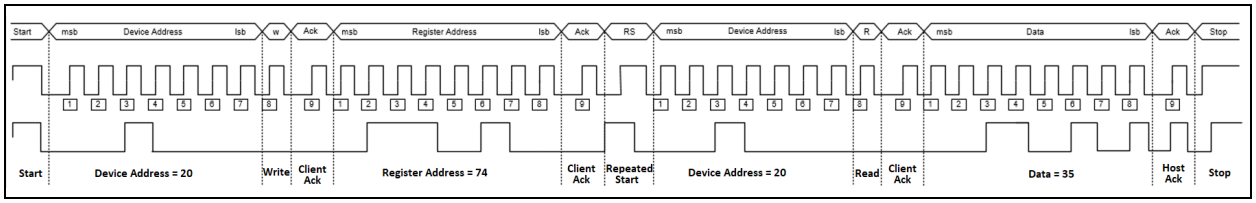


FIGURE 4-6: *Read Cycle Diagram.*

CONTROL REGISTER BIT DEFINITION

Bit	Name	Value	Description
Status, Address 00h			
7:3	Reserved	—	—
2	OCP	—	Latched to 1 if the overcurrent limit is reached. Write a “1” to reset the status flag.
1	OTP	—	Latched to 1 if an overtemperature event occurs. Write a “1” to reset the status flag.
0	FB_UVLO	—	Latched to 1 if a FB_UVLO event occurs. Write a “1” to reset the status flag.
Vsel, Address 01h, (aka dac)			
7	EN	1-d	Device enabled.
		0	Device disabled.
6:0	VSEL[6:0]	—	7-bit DAC value to set V_{REF}. The default value is determined by the part ordering code.
Ctrl1, Address 02h, (aka reg2)			
7:6	Reserved	00-d	—

CONTROL REGISTER BIT DEFINITION (CONTINUED)

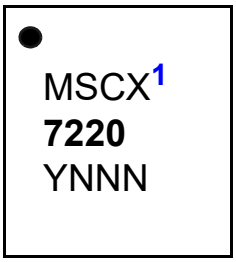
Bit	Name	Value	Description
5	ctrl1	1-d	TBD
4	DLY_DIS	1	45 ms delay on PGOOD is enabled.
		0-d	Disable 45 ms delay on PGOOD.
3	Reserved	1-d	—
		0	—
2	Reserved	1-d	—
		0	—
1	Reserved	1-d	—
		0	—
0	MODE	0	PWM mode only – NO PSM.
		1-d	Power Saving Mode – allows discontinuous conduction.
Vendor ID, Address 03h (Read Only)			
7:4	VID[3:0]	0010	Microchip Vendor ID.
3:2	A1A0	00	Designates the client address version. These bits will correspond to the two LSB bits.
1:0	VOUT	11	The default output voltage is 0.95V.
Ctrl2, Address 04h, (aka reg4)			
7:6	Reserved	—	—
5	GO	1	Writing to this bit starts a V_{OUT} transition regardless of its initial value.
		0-d	The V_{OUT} is ramped to the default VSEL Value.
4	Discharge	1	When the regulator is disabled, the output voltage is discharged through the SW pin.
		0-d	When the regulator is disabled, the output voltage is not discharged.
3	PGOK (read only)	1	Is high when output is in regulation and V_{REF} has stabilized.
		0	Is low during an output voltage transition or when the output is not in regulation.
2:1	SLEW	—	—
		—	—
		01-d	V_{REF} slews at 0.8 mV/µs.
		—	—
		10	V_{REF} slews at 2.2 mV/µs.
		—	—
		11	V_{REF} slews at 8.4 mV/µs.
		—	—
0	Reserved	—	—

Note: -d is the default value at start-up.

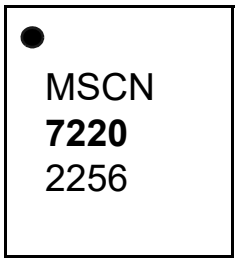
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

14-Lead VQFN



Example:



Note 1: For detailed information, please refer to Section Ordering Information.

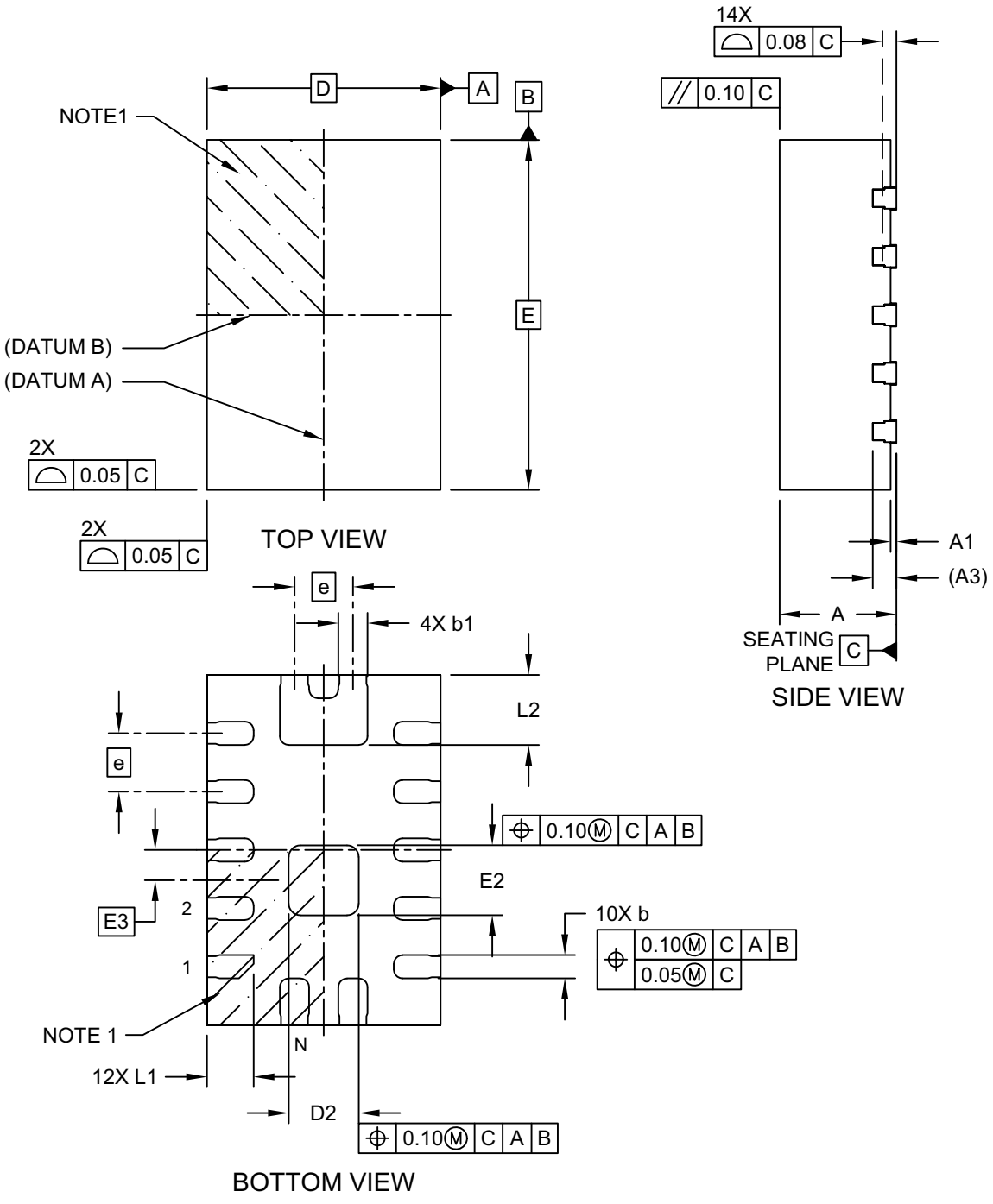
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

14-Lead Very Thin Quad Flat, No Lead Package (NVC) - 2x3x1.0 mm Body [VQFN] With 0.6 mm Exposed Pad; Microsemi Legacy Package

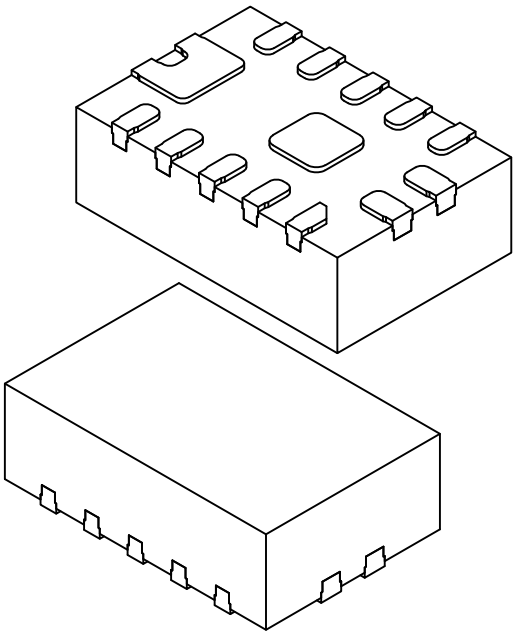
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25488 Rev A Sheet 1 of 2

14-Lead Very Thin Quad Flat, No Lead Package (NVC) - 2x3x1.0 mm Body [VQFN] With 0.6 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	0.55	0.60	0.65
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	0.55	0.60	0.65
Exposed Pad Offset	E3		0.26 BSC	
Terminal Width	b1	0.20	0.25	0.30
Terminal Width	b2	0.15	0.20	0.25
Terminal Length	L1	0.35	0.40	0.45
Terminal Length	L2	0.55	0.60	0.65

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

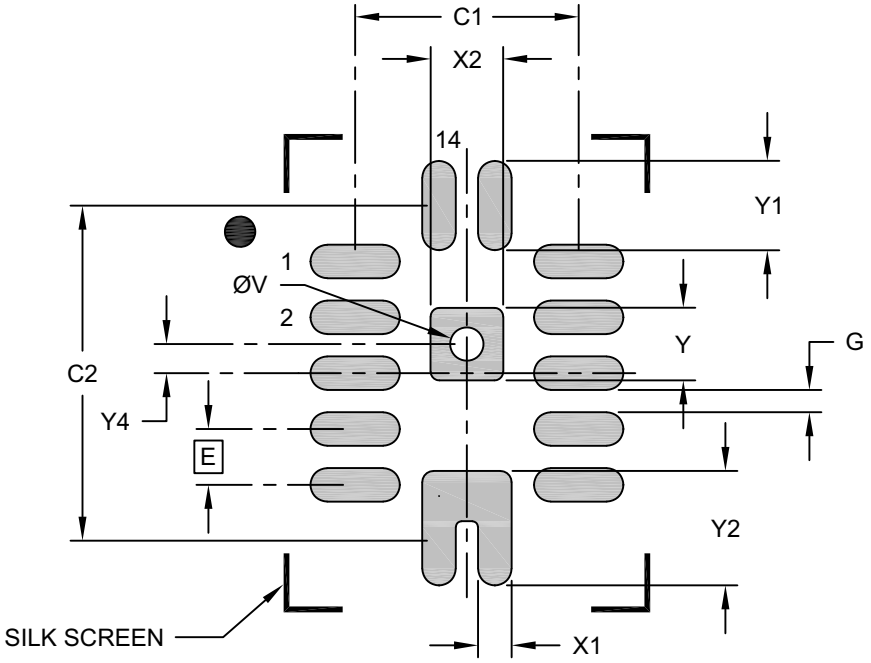
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25488 Rev A Sheet 2 of 2

14-Lead Very Thin Quad Flat, No Lead Package (NVC) - 2x3x1.0 mm Body [VQFN] With 0.6 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		X.XX BSC	
Center Pad Width	X2			0.65
Center Pad Length	Y3			0.65
Center Pad Offset	Y4			0.26
Contact Pad Spacing	C1		2.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad Length (Xnn)	Y2			1.03
Contact Pad to Contact Pad (Xnn)	G	0.20		
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27488 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Microsemi document "*LX7220 - 2.7V to 5.5V, 6A Constant Frequency Hysteretic Synchronous Buck Regulator with I^2C Production Data Spec*" to Microchip data sheet DS20006704A.
- Updated Package Types.
- Updated Typical Application Circuit.
- Updated Functional Block Diagram.
- Updated Electrical Characteristics.
- Minor text and format changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X (Note 1)	X	X	XX	-XX (Note 2)
Device	Client Address A1A0	Output Voltage	Temperature Range	Package	Tape and Reel

Device:	LX7220:		Synchronous Buck Regulator with I^2C Interface
Client Address A1A0:	0 1 2 3	= = = =	E0h E2h E4h E6h
Output Voltage:	3 2	= =	0.95V 0.9
Temperature Range:	I	=	-40°C to +85°C (Industrial)
Package:	LQ	=	14-Lead VQFN, 2 mm x 3 mm, RoHS compliant, Pb-free
Tape and Reel Option:	TR	= Tape and Reel (Note 2)	

Examples:

a) LX7220-03ILQ-TR: LX7220, Client Address E0h, 0.95V Output Voltage, Industrial Temperature, 14-Lead VQFN, 2 mm x 3 mm, RoHS compliant, Pb-free, Tape and Reel

Note 1: Refer to Table 4-1.

2: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Trademarks

ISBN: 978-1-6683-1175-2

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820