LightWise Camera Series

High Performance

Line Scan Module

FireWire™ / 1394a

Smart Digital Imaging Module

Featuring High Quality Linear 1K Sensor

and On-Camera Image Buffer

LW-ELIS-1024A-1394

User's Guide

Version 2.2

Important Note Regarding Grounding and ESD Protection:

We have observed some inconsistencies in 3rd party 1394 interface cards grounding strategy. Some 1394 cards do not ground the 1394 shield to chassis ground on the host computer, and some cards exhibit a "partial" ground. Some professional vision cards assume that the camera ground will be provided by the vision system or apparatus the camera is mounted to.

The ISG 1394 cameras require proper grounding and assume the 1394 cable shield provides a path to ground for the camera chassis. If this connection is faulty, the camera may exhibit an increased susceptibility to electro-static discharge. Please insure that the card you are using provides a ground path via the 1394 cable shield, or add a ground wire or other means to properly ground the camera.

Table of Contents:

1 LW-ELIS-1024 Introduction and Specification Overview
- 1.1 Product Description
- 1.2 Key Specifications
- 1.3 Panavision SVI ELIS Series Image Sensor
- 1.4 Programming and User Configuration Options
- 1.5 Automatic Gain and Offset Correction
- 1.6 Modes of Operation
- 1.7 Simplified Block Diagram

2 External Signals and Connectors
- 2.1 External Connectors
- 2.2 Internal Connectors
- 2.3 Connector Pin Assignments

3 Programming Guide
- 3.1 Interface
- 3.2 Memory Map and Register Definitions

4 Mechanical Information
- 4.1 Lens Mount
- 4.2 Tripod Connection
- 4.3 Imager Module Dimensions
- 4.4 Evaluation Platform Dimensions
- 4.5 Module Components

5 ISG Firmware + FPGA Upgrade Process

Section 1: LW-ELIS-1024 Introduction and Specification Overview

1.1 Product Description

The ISG Line Scan Imager Module provides a High performance Line Imager with high quality high-speed video with excellent response characteristics. The low cost and ease of integration into existing systems make it an excellent solution for a wide variety of applications. The interfaces to the Imager are industry standard to provide ease of integration into target systems. Applications include:

Automated Inspection Systems
Bar Code Reading
Machine Vision Systems
Encoding and Positioning
Parcel Scanning
Programmable Smart Camera Applications

1.2 Key Specifications

- Linear Resolution: 1024 Pixels
- Data Rate: Up to 10 Mpixels / second
- Data Resolution: On-Board 14 bit A to D
- High Sensitivity and Wide Dynamic Range
- On-Board FPN Correction
- Standard FireWire™ (1394a) Interface (see TM note, page 23)
  Fully compliant to IEEE-1394a IIDC DCAM Specification Version 1.3
- Single 12V Supply
- Compact Form Factor
- User Programmable: *Integration Time, Multiple Gain Adjustments, Offset, Bit Depth, and Data Rate*
- Built-In Test Pattern
- External Trigger Option
- On-Board Image Buffer (16MB)
- On-Board FPGA for User-Configurability

1.3 Panavision SVI ELIS Series CMOS Image Sensor

The module utilizes the ELIS family of image sensors (see ELIS data sheets for detailed sensor information), which consists of an array of high performance, low dark current photo-diode pixels. The sensor features sample and hold capability, selectable resolution and advanced power management. Internal logic automatically reduces power consumption when lower resolution settings are selected. A low power standby mode is also available to reduce system power consumption when the imager is not in use.

1.4 Programming and User Configuration Options

The LW-ELIS-1024 offers several levels of programmability and user configurability. These include:

- Full Parameter Control, Set-Up and Operation Control via the **ISG Graphical User Interface Software**. This software is included with each unit.

- Parameter Control, Set-Up and Operation Control using software packages which support the **IIDC 1394-based Digital Camera Specification Version 1.30**. This includes vision packages by National Instruments, Matrox, Unibrain and many others.

- Full Parameter Control, Set-Up and Operation Control via **direct access of the module's register set**. Section 3 is the programmers' reference for this mode of operation.

-

  -Customization of on-board FPGA. The on-board FPGA can be customized to include smart camera functionality, such as specialized image processing, data feature extraction, custom dynamic range mapping, etc. This method can also be used to configure the external I/O signals for custom functionality.
  Imaging Solutions Group is available for consulting with customers to enable custom configurations via the on-board FPGA. Contact sales@isgchips.com for information.

1.5 Automatic Gain and Offset Correction

The LW-ELIS-1024 provides on-board FPN correction through gain and offset compensation. The FPGA algorithms in conjunction with an on-board dual 8-bit DAC perform automatic offset correction and semiautomatic gain corrections. These functions can be selected and activated by the provided ISG Graphical User Interface (GUI) software, or can be accessed directly via register programming.

1.6 On-Board Image Buffer

The camera provides on-board image buffering for up to three frames color or nine frames monochrome 16MB of image data. Combined with the module's flexible trigger modes, this image buffer enables capturing a sequence of frames at the maximum frame rate of the sensor, then transferring the frames at any available 1394 bandwidth.

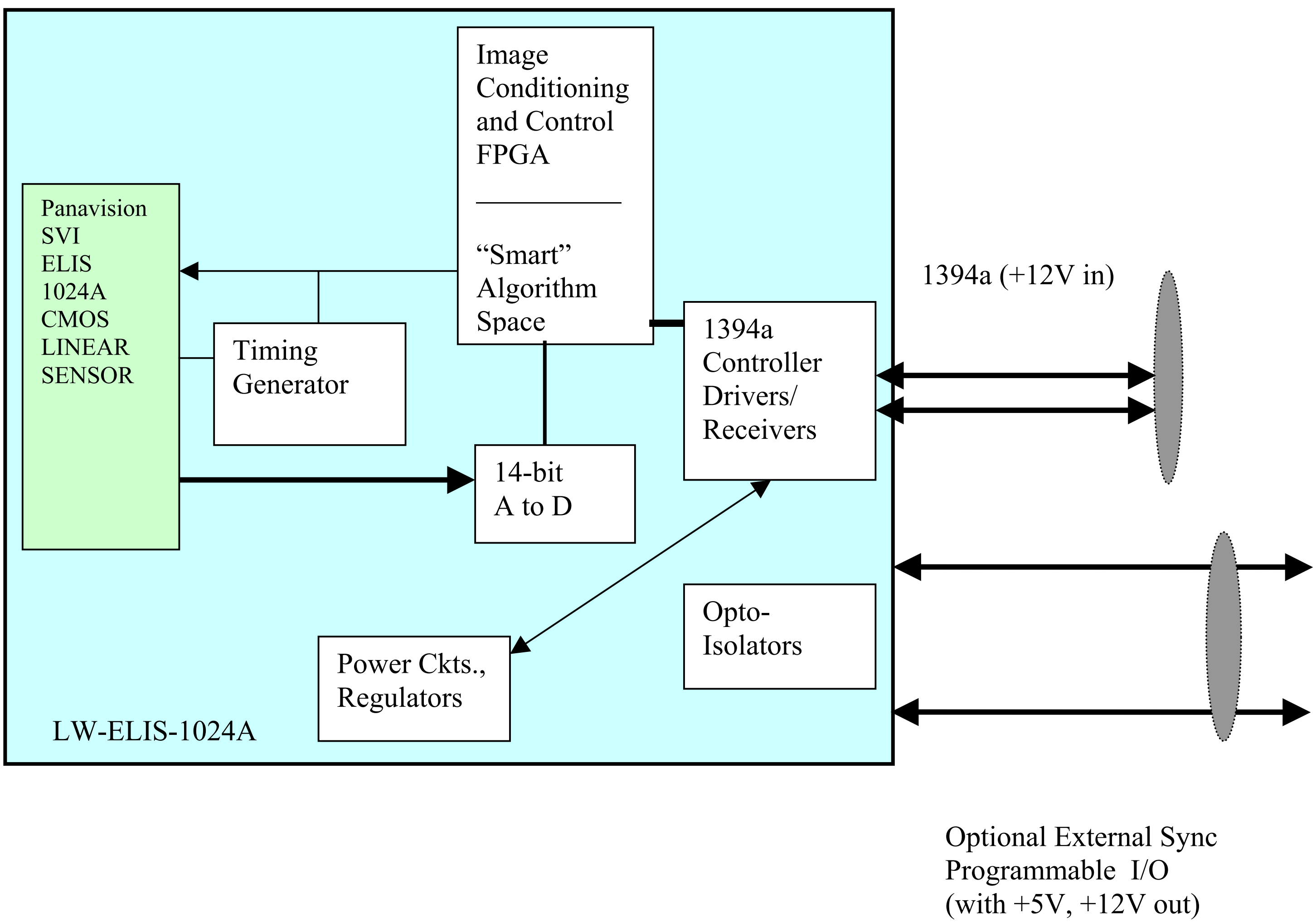
1.7 Modes of Operation

The LW-ELIS-1024A can be programmed to run in two different modes depending on the application.

Standard Mode (Default Operation) - In this mode the sensor integration time is controlled by the amount of time the electronic shutter is active. The integration time is followed by readout, and then the process is repeated. This allows for very precise control of integration time, while trading off some sensitivity. A characteristic to note in this mode is that the dark current profile of each pixel will be different because the pixels near the end of the array will be read out later in time relative to when the pixel integration ended. Most applications will not be sensitive to this effect.

Dynamic Pixel Reset (DPR Mode) – In this mode each pixel is reset after read out and starts integrating immediately. An advantage to this mode is that every pixel is integrating for the entire line time (minus the one clock cycle for reset). A disadvantage is that the minimum integration time is driven by the readout time of the sensor (no electronic shutter). The integration time can be extended by adding a delay between line readouts (DPR Delay Register). DPR mode is available by setting ISG-defined registers via the 1394 interface. See table in Section 3.1.2.

1.8 Simplified Block Diagram



Section 2: Connectors and Trigger Modes

The ISG linear cameras can be triggered in frame or line rate modes or a combination of the two. The frame rate trigger (described in section 2.1) controls when the lines that make up a frame begin to be acquired. The line rate trigger (described in section 2.2) controls the interval between each line read out of the imager. It is possible to use both types of triggers simultaneously as long as the opto-isolate trigger input is used for the frame trigger and the differential trigger input is used for the line rate trigger. When not using line rate triggering either the differential or opto-isolated input can be used for frame triggering.

Section 2.1: Frame Trigger Description

Register Description:

Trigger Delay – A 16 bit value used to delay the start of image acquisition from the active edge of the input trigger. This value can be programmed in steps of 20.83us to a maximum value of 1.37s.

Strobe Advance – This 8 bit register is used to apply the strobe signal a programmed amount of time before the start of image acquisition to allow for illumination turn on time. This value can be programmed in steps of 5.21us to a maximum value of 1.33ms. Note: The trigger delay must be greater then the strobe advance.

Strobe Delay – This 18 bit register is used to delay the strobe signal a programmed amount of time after the start of image acquisition. This delay is intended for use with flash illumination devices. This value can be programmed in steps of .65us to a maximum value of 170 ms. Note: The strobe delay must not exceed the image acquisition time. If a value is programmed for Strobe Advance the Strobe Delay value will be ignored.

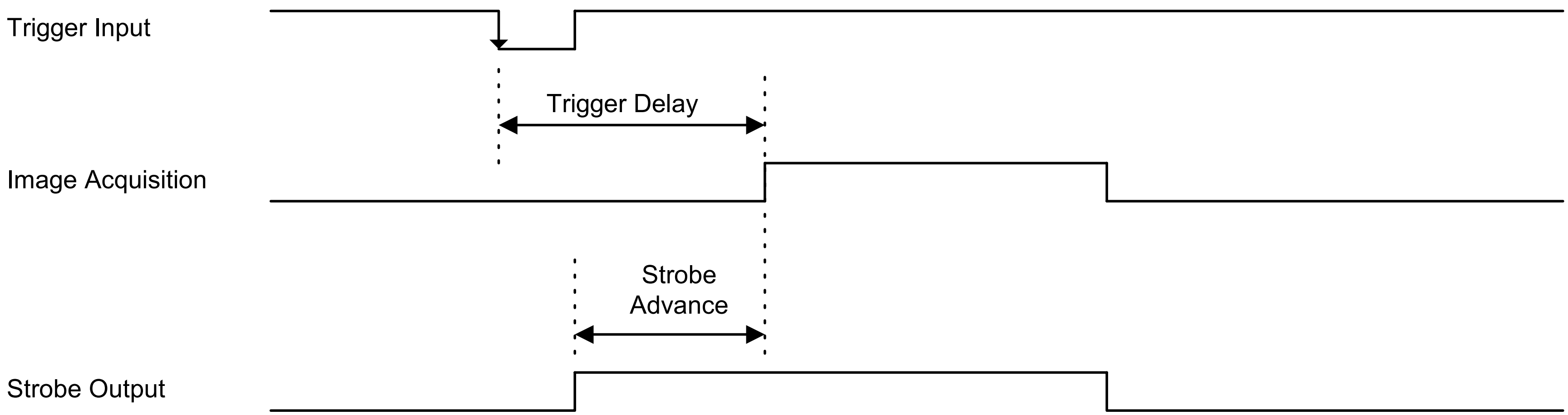
Retrigger Delay – The 16 bit value in this register is used to program the time between image acquisition intervals when in Retrigger Mode. This value can be programmed in steps of 5.2us to a maximum value of 341ms.

Strobe Duration - This register is used to program the duration of the strobe pulse when strobe duration mode is enabled. This value can be programmed in steps of 5.2us to a maximum value of 341ms. Note: The strobe output will go inactive at the end of image acquisition no mater what the strobe duration is set to.

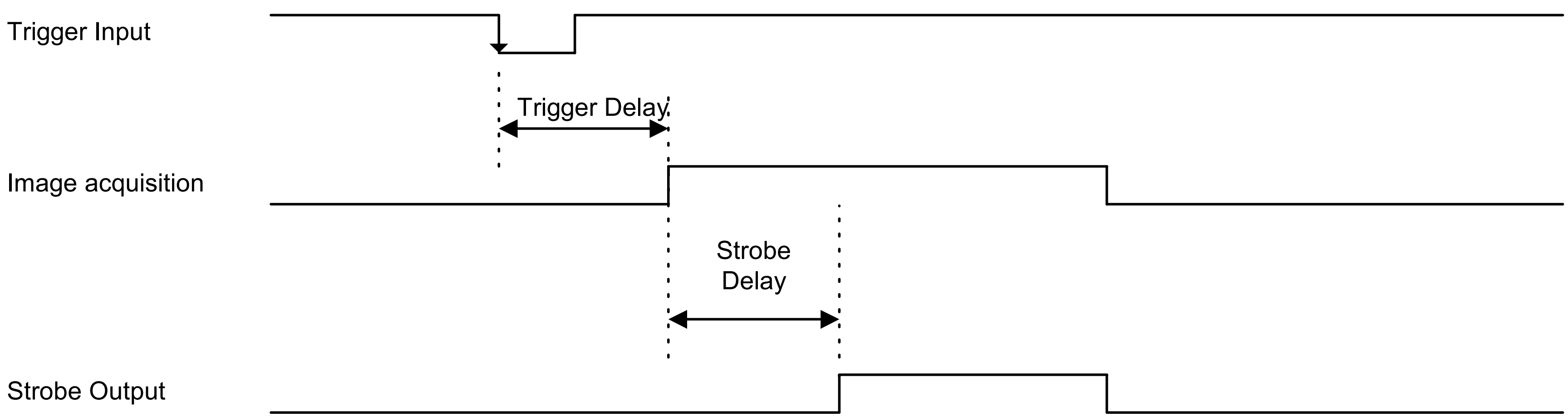
Trigger and Strobe Description:

The input trigger sense can be active low or high. A software trigger is also available to the programming interface (Host Mode) as well as a trigger status bit. The strobe output is intended to control an illumination system and can be selected to be active low or high as well as always high or always low. The diagrams on the following pages show the trigger as active low and the strobe as active high.

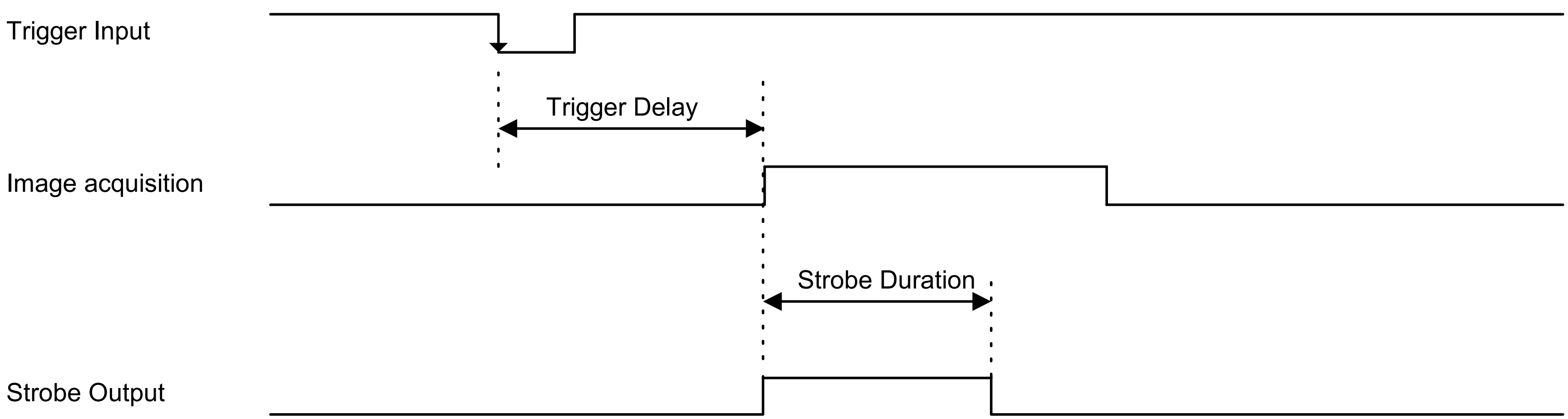
Trigger Mode A = IIDC Trigger Mode 0
Strobe Advance Shown



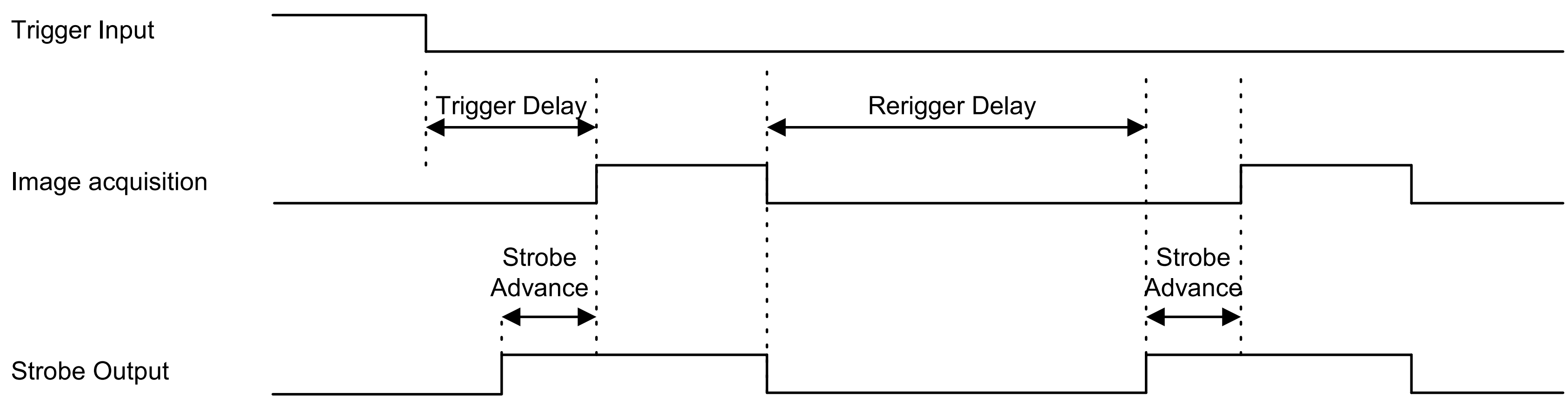
Trigger Mode A = IIDC Trigger Mode 0
Strobe Delay Shown



Trigger Mode A = IIDC Trigger Mode 0
Strobe Duration Shown



Trigger Mode C



Version 2.2 Subject to change without notice.

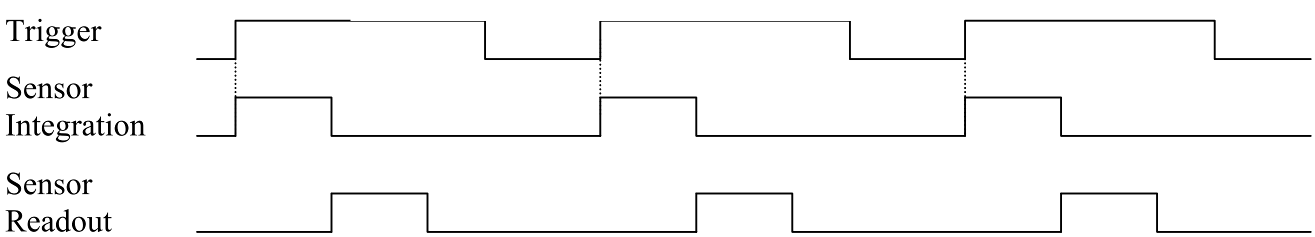
Section 2.2: Line Rate Trigger Description

The line rate trigger is offered for applications such as web inspection where synchronization between the imaged target and the sensor line rate are required to maintain proper image aspect ratio. This is accomplished by feeding a differential signal from the tach to the differential trigger input. Two line scan modes are provided and can be enabled with bits 11 and 10 of the LISCR (0x424).

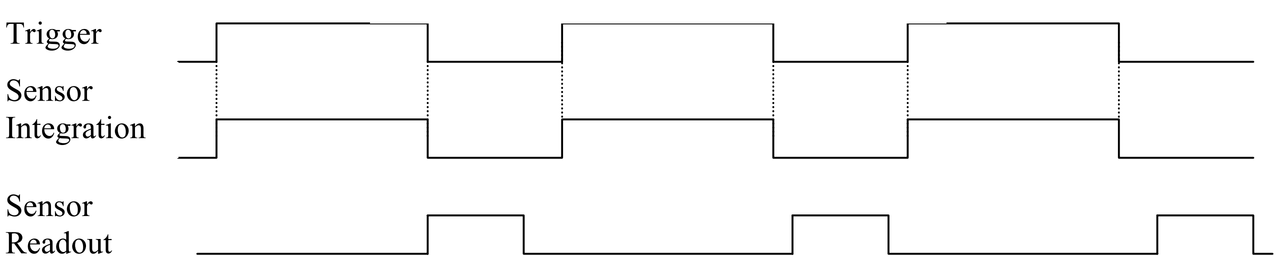
LISCR[11:10] 00 = Line rate trigger disabled.
LISCR[11:10] 01 = Line rate trigger enabled in edge mode.
LISCR[11:10] 10 = Line rate trigger enabled in level mode.

When using edge mode, the integration time is controlled with the shutter register as it is when not using line rate triggering. When using level mode, the line integration is controlled by the trigger active time. In other words the pulse width of the trigger input will control sensor integration time. Both modes are illustrated below.

Line Rate Trigger Edge Mode



Line Rate Trigger Level Mode



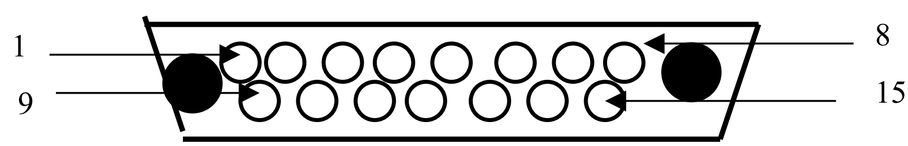
2.2 External Connectors

2.2.1 Firewire™ Connector: This interface is based on the industry standard 1394a specification. Two connectors are provided to allow camera daisy chaining.

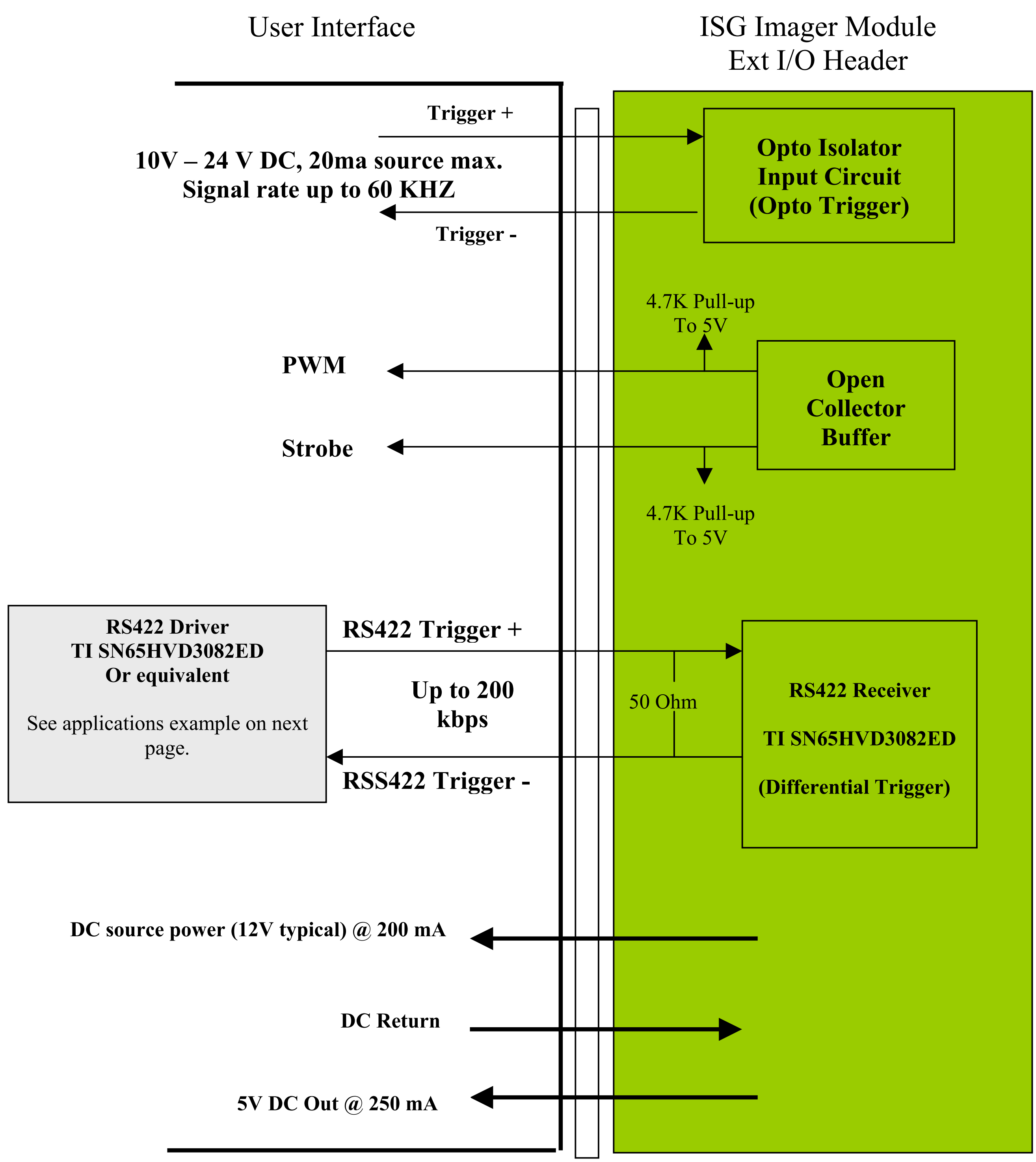
2.2.2 15-position D-SUB I/O Connector:

- Connector part number: Molex part number 83612-9020
- Thumb Screw part number: Molex MDSM – 9PE-Z10-VR25
- Recommended Cable: Molex CA 83422-9014

Pin	Function	Input/Output Type
1	Trigger +	Optoisolated Input
2	Trigger -	Optoisolated Input
3	GND	
4	DC Input (Optional)	Power Input
5	Strobe	Open Collector Output
6	Programmable PWM	Open Collector Output
7	GND	
8	DC Input (Optional)	Power Input
9	RS422 Trigger +	Diff. TTL Input
10	RS422 Trigger -	Diff. TTL Input
11	DC +5V Output	Power Output
12	Programmable Output +	Optoisolated Output
13	Programmable Output -	Optoisolated Output
14	Reserved	
15	GND	



15-pin Micro-D **EXT IO Connector, Front View**



External Input Output Interface connection

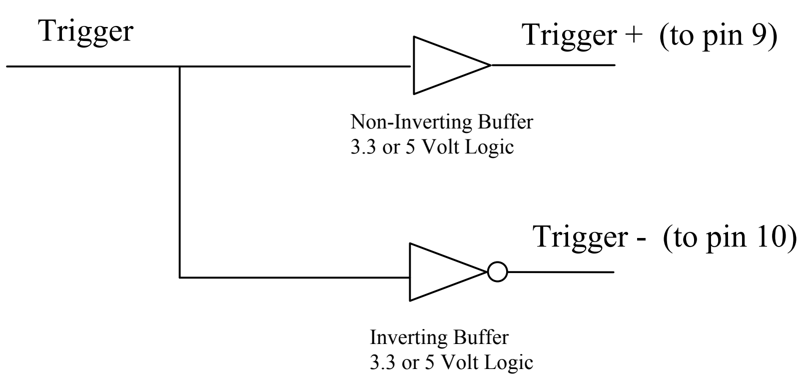
Applications Example: Using The RS422 Trigger Input

1) Preferred Method – RS422 Driver

The optimal way to utilize this input to trigger the camera is to drive the RS422 Receiver in the camera with the corresponding driver device. The recommended driver is TI part number SN65HVD3082ED. This method provides a balanced, robust differential input.

2) Alternate Method - Driving the RS422 Trigger Input with Standard 3.3 or 5 Volt CMOS/TTL Logic

Standard digital logic can be used to simulate a differential signal and trigger the camera using the RS422 input. This can be accomplished by generating a 3.3 or 5 Volt logic signal for RS422 Trigger +, and providing a logically inverted output of this signal for RS422 Trigger -. The following diagram illustrates this approach:



Section 3: Programming Guide

3.1 Top Level Memory Map: All addresses are offset from address 0x7000

Sensor Map	0x000 - 0x3ff	B12

Sensor Interface

SICR	0x400	B15	Sensor Interface Control (Control Register1)
SISTAT	0x404		Sensor Interface Status
TRGDLY	0x408	U16	Trigger Delay
STRBDLY	0x40C	U16	Strobe Delay
RTGDLY	0x410	U16	Retrigger Delay
PWM	0x414	U8	PWM Duty Cycle
STRADV	0x418	U8	Strobe Advance
STRDUR	0x41C	U16	Strobe Duration
ILISCR	0x424	B10	Linear Control Register (Control Reegister2)
SHUTTER	0x428	U16	Shutter Value (LGINT on SLIS)
NUM_ROWS	0x42C	U16	Number of rows in a frame
VV_STRT	0x430	U12	Start of line ROI
VV_END	0x434	U12	End of line ROI
INT_COUNT_VAL	0x43C	U11	Short Integration for SLIS
NDRO_COUNT	0x440	U8	NDRO Line count (ELIS Only)
DPR_DLY	0x444	U16	DPR delay (ELIS Only)
CLKCR	0x448	U5	Clock Divider/Control
PWM_SF	0x44C	U8	PWM Scale Factor
LRT_MULT	0x450	U9	Line Rate Multiplier

Image Path Control

IPCR	0x800	B14	Image Path Control
IPSTAT	0x804	B2	Image Path Status
HISTCOLSTRT	0x808	U12	Histogram Window Column Start
HISTCOLWIDTH	0x80C	U12	Histogram Window Column Width
HISTROWSTRT	0x810	U11	Histogram Window Row Start
HISTROWDEPTH	0x814	U11	Histogram Window Row Depth
HISTCR	0x818	B4	Histogram Control
HISTADDR	0x81C	U5	Histogram Address
HISTDATA	0x820	U26	Histogram Data
DGAIN	0x824	U4.4	Digital Gain
LUTADDR	0x8B4	U10	Look Up Table Address
LUTDATA	0x8B8	U10	Look Up Table Data
DOFF	0x918	U14	Digital Offset

3.2 Register Detail

Please contact ISG for register programming details.

Section 4: Mechanical Information

4.1 Lens Mount

A Case-Mount **CS** type (1.0” diameters with 12.5 mm spacing between the surface of the sensor and top of the lens-mount) lens mount is provided for both system configurations.

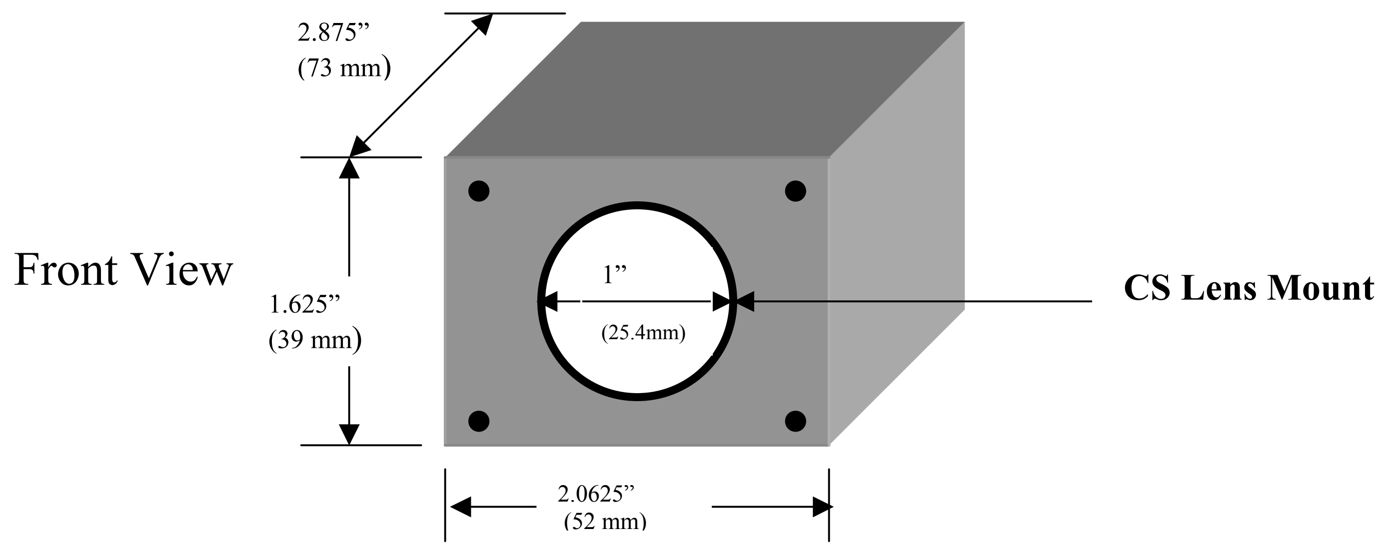
C-Type Lenses: A five mm extender will change the CS to C-Type lens mount with 17.5 mm Back Focal Length.

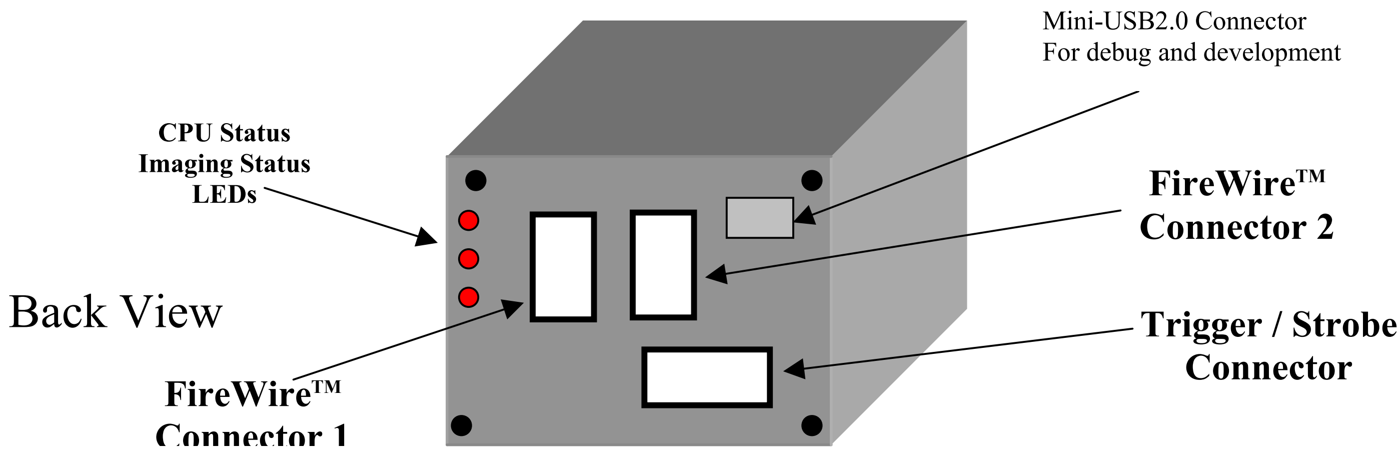
F-Type Lenses: Using the Cannon 50mm F-type FD series + the Cannon "C-type to F-type" adapter will covert the camera to F-type with 39.9 mm Back Focal Length.

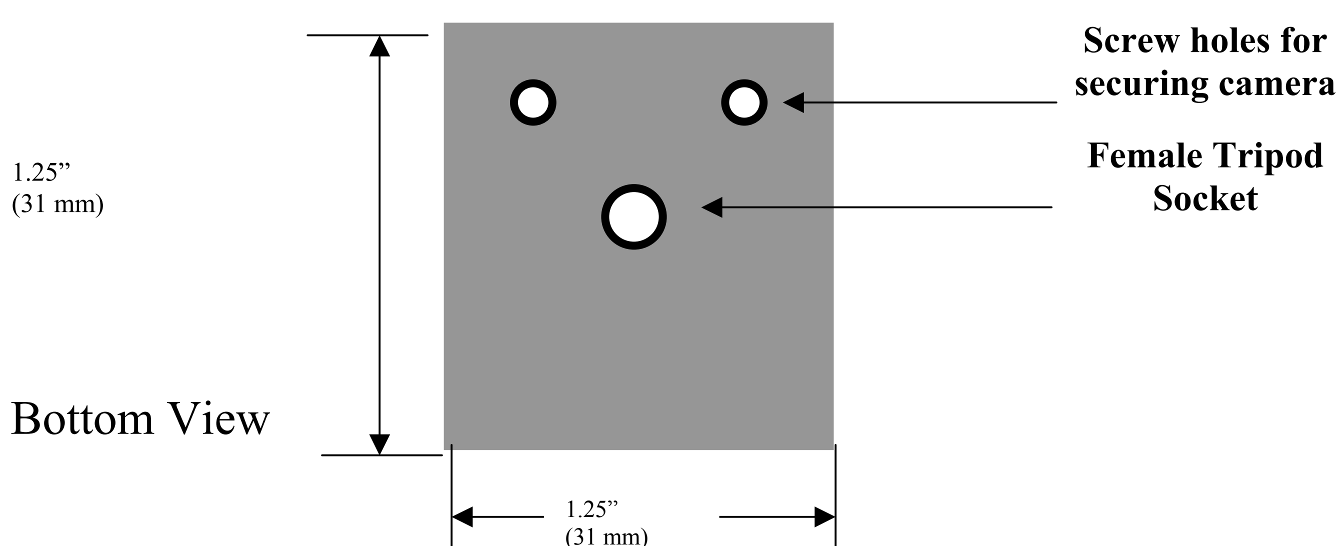
4.2 Tripod Connection

A standard female tripod connection is provided at the bottom of the Imager module and the Evaluation platform

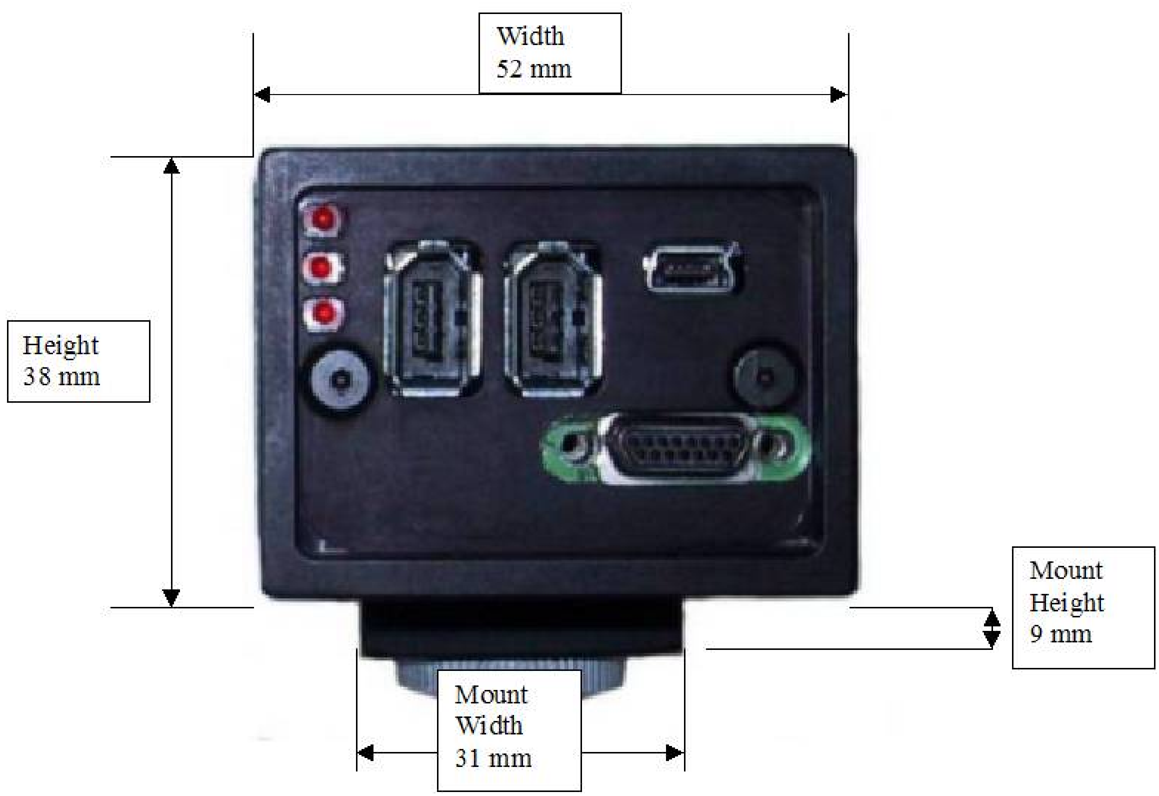
4.3 LW-ELIS-1024A-1394 Line Scan Module Dimensions







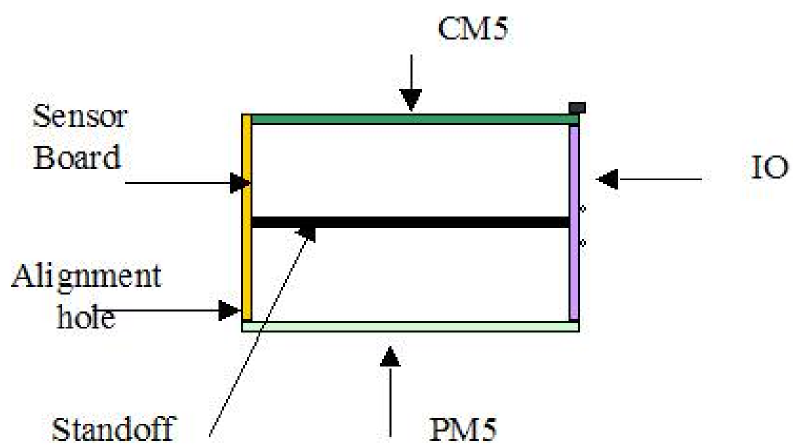

C Adapter
Width 5 mm
Length
C-mount 78 mm
CS-mount 73 mm
Note: CS + C
adapter = C-mount
All Mounting Holes are on 19.9644 mm centers. Mounting holes are on top & bottom. Front plate also has mounting holes on sides. Top & Bottom holes are 15.48mm from edges. Side holes are 9mm from edge.


Width
52 mm
Height
38 mm
Mount
Height
9 mm
Mount
Width
31 mm

4.4 Module Components:

The ISG LW-ELIS-1024A-1394 Line Scan Module hardware design is partitioned into four separate boards: 1) Sensor, 2) Controller 3) I/O board and 4) Power Management boards. These boards are SMT type 2 (double sides) and are connected to each others as shown below:

The module electronics consists of 4 boards: Sensor, Controller (CM5), Power Management Board (PM5) and the IO board.



4.5 Operating Conditions

Measured Average Power Consumption via 1394 cable:
12V, 250 ma rms / 3.0W

Ambient Operating Temperature Range:
-10 to 45 C

FCC and CE Qualification: In progress.
Test results available upon request.

Vibration and Shock Testing: In progress.
Target specification: 7G rms (10Hz to 2000Hz) Random, Shock 70G. Test results available upon request.

5.0 ISG Firmware + FPGA Upgrade Process

This process will use the ISG Camera Control GUI application software on the host PC, to update firmware and/or FPGA code on the ISG 1394 camera. The camera's firmware/FPGA code is loaded through the 1394 interface using the ISG GUI.

A customer wishing to do a firmware or FPGA upgrade should perform the following steps:

1) Extract, and copy the firmware/FPGA binary data files to a directory on your host PC. The files are named isgcpu_ccxx_xxxx.bin for updating the camera firmware, and isgfpga_ccxx_xxxx.bin for updating the camera hardware (i.e. FPGA device code). The ccxx field represents the camera type, and the xxxx field will hold the version number.

2) To upgrade the firmware on the camera, start by running the ISG Lightwise GUI. Note that the ISG supplied driver for the camera must be installed in order to use the ISG GUI. It is recommended that the camera viewer window be closed before continuing.

3) Click on the “Camera Control Dialog” button on the ISG GUI.

4) Select the “Camera Setup” tab from the Camera Control Dialog page. The Camera Setup page can be used to update either the firmware or the FPGA code of the camera, or both.

5) Use the browse button (labeled “…”) to search for and select either the isgcpu or isgfpga binary file defined in step 1 above, depending on which part of the camera you are updating.

6) To begin the actual download procedure, click on the “Download to CPU” or “Download to HW” button as appropriate. A popup box will ask if you are sure that you want to continue the process.

7) Confirm that you are sure you want to proceed with the upgrade by answering, "yes" within the confirmation popup dialog. Once confirmed, insure that this process is not interrupted (i.e. maintain 1394 cable connection). The progress bar will show the status of the update. Note that an FPGA update will take a few minutes to complete. The process is completed once the dialog states "Done" on the download button. At this point, the camera is upgraded with new firmware/FPGA code.

8) Exit the GUI. Power cycle the camera by disconnecting and reconnecting the 1394 cable to allow the new code to be executed.

9). After the camera is connected, you can right click in the top toolbar of the GUI and select “about isg camera system” to read the new version numbers.

Trade Mark Note:

FireWire™ is a registered trademark of Apple Inc